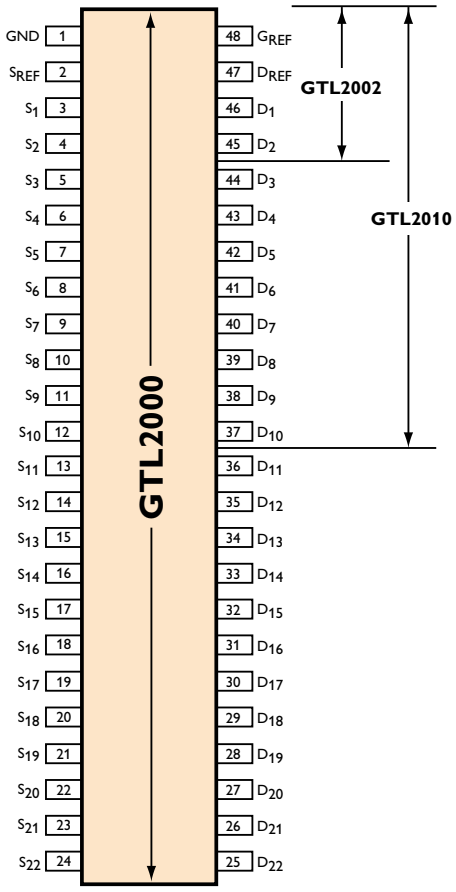
GTL2000/GTL2002/ GTL2010

Bi-directional low voltage translators



Semiconductors

Description

The Philips family of Gunning Transceiver Logic (GTL) Bi-Directional Low Voltage Translators are used for high-speed translation between different voltage levels with low ON-state resistance and minimal propagation delay. Unlike level shifting bus switches, which are limited to translation between two fixed voltages (e.g. 5 V and 3.3 V), the 22-bit GTL2000, 2-bit GTL2002, and 10-bit GTL2010 can translate any voltage between 1 V and 5 V to any other voltage between 1 V and 5 V.

The devices provide NMOS pass transistors (Sn and Dn pins) with a common gate (G_{REF} pin) and a reference transistor (S_{REF} and D_{REF} pins). When one of the Sn or Dn ports are low, the clamp is in the ON-state and the Sn and Dn ports are connected through a low ON-resistance connection. Assuming the higher voltage is applied on the Dn port:

- when the Dn port is high, the voltage on the Sn port is limited to the voltage set by S_{REF}
- when the Sn port is high, the Dn port is pulled to a higher voltage by a pull up resistor

This functionality allows a seamless translation between higher and lower voltages selected by the user, without the need for directional control signals. All transistors have the same electrical characteristics and deviation from one output to another in voltage or propagation delay is minimal. This is a benefit over discrete transistor voltage translation. The translator's transistors also provide excellent ESD protection to lower voltage devices and protects less ESD resistant devices.

Features

- No directional control required for bi-directional voltage translations
- Low 6.5 Ω R_{ON} resistance between input and output pins (Sn/Dn)
- 1.5 ns typical propagation delay
- 7.5 pF channel off-state capacitance
- Very low 5 µA stand-by current
- No power supply required – Will not latch up

Applications

- Any application that requires bi-directional or unidirectional voltage level translation from any voltage between 1.0 V & 5.0 V to any voltage between 1.0 V & 5.0 V
- The open drain construction with no directional control is ideal for bi-directional low voltage (e.g., 1.0 V, 1.2 V, 1.5 V, or 1.8 V) processor I^2C port voltage level translation to legacy 3.3 V and/or 5.0 V I^2C bus signal levels at speeds up to 3.4 MHz.
- Shifting processor sideband I/O signals from GTL / GTL+ voltage levels to LVTTL / TTL signal levels.

Ordering information

Package	Container	GTL2000	GTL2002	GTL2010
SO	Tube	NA	GTL2002D	NA
	T & R	NA	GTL2002D-T	NA
SSOP	Tube	GTL2000DL	NA	NA
	T & R	GTL2000DL-T	NA	NA
TSSOP	Tube	GTL2000DGG	NA	GTL2010PW
	T & R	GTL2000DGG-T	GTL2002DP-T	GTL2010PW-T
HVQFN	T & R	NA	NA	GTL2010BS-T

In Europe and Asia, add ", 112" for tube orders and substitute ", 118" for "-T" for tape and reel orders (e.g., GTL2010PW, 112 and GTL2010PW, 118).

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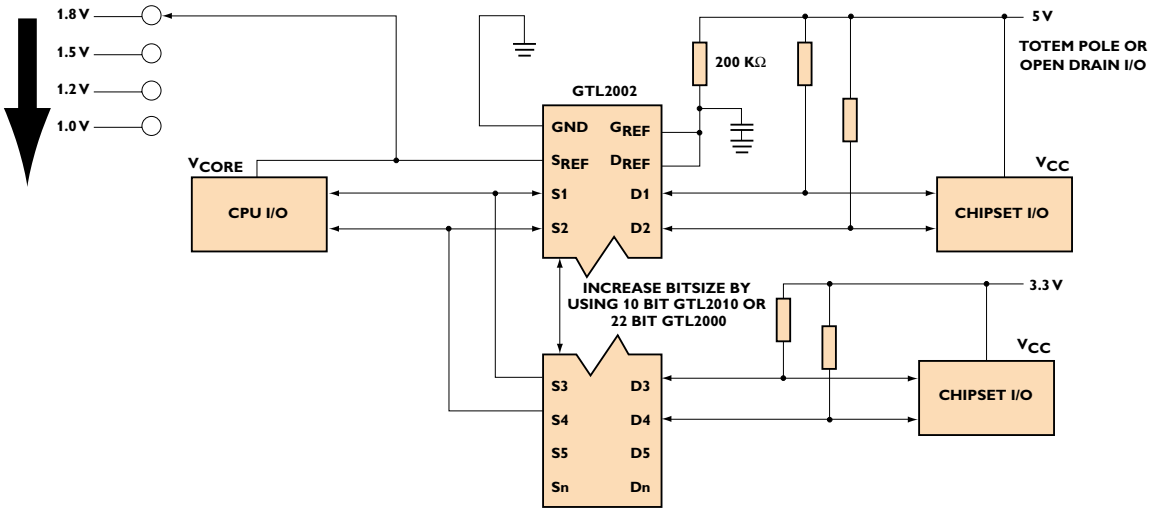
GTL2000/GTL2002/GTL2010

Bi-directional low voltage translators

Typical bi-directional voltage translation



Bi-directional voltage translation

For the bi-directional clamping configuration, the G_{REF} input must be connected to D_{REF} and both pins must be pulled to high side V_{CC} through a pull-up resistor (typically 200 kΩ). A filter capacitor on D_{REF} is recommended. The CPU output can be totem pole or open drain (pull up resistors may be required) and the chipset output can be totem pole or open drain (pull up resistors are required to pull the Dn outputs to V_{CC}). However, if either output is totem pole, data must be uni-directional or the outputs must be 3-stateable and the outputs must be controlled by some direction control mechanism to prevent high to low contentions in either direction. If both outputs are open drain, no direction control is needed. The opposite side of the reference transistor (S_{REF}) is connected to the CPU power supply voltage. When D_{REF} is connected through a 200 kΩ resistor to V_{CC} and S_{REF} is set between 1.0 V to V_{CC} – 1.5 V, the output of each Sn has a maximum output voltage equal to S_{REF} and the output of each Dn has a maximum output voltage equal to the pull up resistor voltage (e.g., 3.3 V and/or 5 V).

Additional technical information can be found in Application Note AN10145 Bi-Directional Voltage Translators at:
www.semiconductors.philips.com/logic/support/appnotes/specialty

Down voltage translation only

The reference transistor is connected the same as for the bi-directional translation. Pull up resistors are required if the chipset I/O are open drain.

Up voltage translation only

The reference transistor is connected the same way as for the bi-directional translation. A pull-up resistor is required on the higher voltage side (Dn) to get the full high level, since the translator will only pass the reference source voltage (S_{REF}) as a high when doing an up translation. The driver on the lower voltage side only needs pull-up resistors if it is open drain.

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