Amphion Semiconductor, Ltd.

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Features

- Support Virtex™-II, Virtex-E, and Virtex devices.
- Supports, G.721, G.723, G.726, G.726a, G.727, and G.727a ITU standards
- 512 channel simplex/256 channel duplex encoding and decoding
- Online configurable for different compression rates, µ-law and A-law for each encoding or decoding channel
- Coding (encode or decode) for one data sample in 1 clock cycle
- Can work in both burst and continuous modes
- Conforms fully to ITU test vectors

AllianceCORE™ Facts	
Core Specifics	
See Table 1	
Provided with Core	
Documentation	User Guide, Design Guide
Design File Formats	EDIF netlist, VHDL RTL available extra
Constraints File	ADPCM512.ncf
Verification	Testbench, Test Vectors
Instantiation Templates	VHDL, Verilog
Reference Designs & Application Notes	None
Additional Items	None
Simulation Tool Used	
ModelSim v5.3c	
Support	
Support provided by Amphion	

Applications

- Digital Enhanced Cordless Telecommunications (DECT)
- Video conferencing
- Telecommunications
- Voicemail systems
- Satellite communications
- VoIP

Table 1: Core Implementation Table

Supported Family	Device Tested	CLB Slices[1]	Clock IOBs[2]	IOBs[2]	Performance (Minimum Functional Clock)	Xilinx Tools	Special Features
Virtex-II	2V500-5	2423[2]	1	70	xx MHz[2]	3.2i	9 block RAMs
Virtex-E	V400E-8	2369	1	70	6 MHz	3.2i	35 Block RAMs

Notes:
1. Assuming all core I/Os are routed off-chip.
2. Preliminary data; subject to change. Check with Amphion Semiconductor for latest data.

General Description

The Amphion family of adaptive differential pulse code modulators (ADPCMs) is designed to provide high performance solutions for a broad range of applications requiring speech compression and decompression. These application specific virtual components (ASVCs) support up to 1024 simplex channels on Xilinx FPGA. Each channel is independently selectable for encoding or decoding, and are fully compliant with ITU G.726, G.726a, G.727 and G.727a standards.

The core supports 256 duplex/512 simplex channels. The core is online configurable in terms of compression rates. It has been tested and verified to be fully compliant using the ITU standard test vectors.

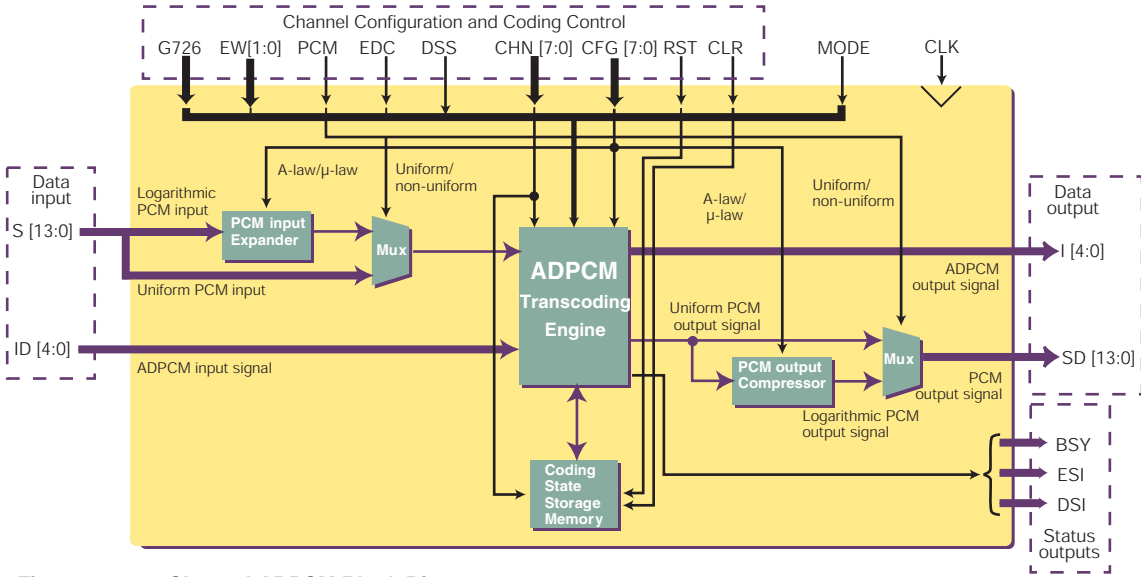

Figure 1: 512-Channel ADPCM Block Diagram

Functional Description

The Amphion ADPCM core consists of 5 primary sections: a PCM Input Expander, an ADPCM Transcoding Engine, a PCM Output Compressor, a Coding State Storage Memory, and a Channel Configuration and Coding Control, as illustrated in Figure 1. The core operates on one input sample at a time, using 1 clock cycle to complete the encoding or decoding. Multichannel coding is implemented on time-multiplexing basis. The input/output channel multiplexing and serial to/from parallel conversion circuitry may be added to suit the target system as required.

The core can encode data from three types of PCM format, as specified by ITU standard G.711, to 2, 3, 4 or 5-bit ADPCM format. These are 8-bit µ-law or A-law logarithmic PCM, 14-bit µ-law uniform PCM or 13-bit A-law uniform

PCM. The core can also decode data from the 2, 3, 4 or 5-bit ADPCM format to the three types of PCM format.

The cores are on-line configurable in terms of compression rate and PCM law and allow on-the-fly selection of PCM/uniform PCM input/output. Each member of Amphion's ADPCM family has been tested and verified to be fully compliant using the ITU standard test vectors.

PCM Input Expander (Logarithmic PCM to Uniform PCM)

This block converts the input PCM signal from 8-bit A or µ-law logarithmic PCM format to a 13-bit A-law or 14-bit µ-law uniform PCM signal. This decoding is performed according to the G.711 standard.Convert to Uniform PCM

ADPCM Transcoding Engine

The primary encoding and decoding operations of the Amphion ASVC take place within the ADPCM transcoding engine.

When encoding, the difference between the uniform PCM input signal with a prediction of this signal is calculated. The difference signal is then passed to an adaptive quantizer where 5, 4, 3 or 2 binary digits are assigned as its value, following the quantization methods stipulated by the G.726 or G.727 standards. The result is the ADPCM signal for transmission.

The current ADPCM signal is then used to predict the next signal estimate. It is fed to an inverse adaptive quantizer and the output is added to the current input signal estimate to determine the reconstructed version of the input signal. This signal and the output of the adaptive quantizer are then used by the adaptive predictor to determine the estimate of the next input signal, which is then fed back to determine the next difference signal.

When decoding, the reverse procedure is performed. First, the ADPCM signal is inversely quantized; then the resulting signal is added to a prediction of this signal, forming a reconstructed signal. The inversely quantized signal and the reconstructed signal are used by the adaptive predictor to determine the signal estimate for the next iteration.

This reconstructed signal is converted to a PCM signal before passing through an additional block needed for synchronous coding adjustment. This block prevents cumulative distortion occurring on synchronous tandem codings. This is when the signal is converted from PCM to ADPCM to PCM and back to ADPCM. The idea is that when the PCM signal is converted the resulting ADPCM signal is the same at every stage. The output PCM signal from this block is the resulting decoded output of the codec.

PCM Output Compressor (Logarithmic PCM to Uniform PCM)

This block converts the output PCM signal from either 13-bit A-law or 14-bit μ-law uniform PCM format to an 8-bit A- or μ-law logarithmic PCM signal. This encoding is performed according to the G.711 standard.

Coding State Storage Memory

The 512 channel ADPCM algorithm requires 279 bit states for each encoding or decoding channel (i.e., 558 bits per duplex channel). These states are stored in the memory of the ADPCM core.

The total memory required by the core is N x 279 where N is the number of simplex channels available.

Channel Configuration and Coding Control

The IW, EW, EBI and LAW input configuration control signals determine the compression rate and law for each channel. The function of each signal is listed in Table 2.

The input signal G726 is used to specify whether the G.726 or G.727 is in use; when high the core operates per the G.726 standard, low indicates G.727.

It should be noted that:

- Input data S and ID are also latched on the clock rising edge when INSTROB is HIGH.
- The output data is registered.
- Encoding and decoding can be performed in any order.

Encoding/Decoding Operation

Encoding or decoding of one data sample is performed by asserting the data strobe signal (INSTROB). The input select signal INEDC defines whether the core performs an encoding or a decoding operation. When INEDC is HIGH, the core performs encoding and the input S is taken. When INEDC is LOW the core will decode and the input ID is taken. Input signal PCM specifies the type of encoding input data and decoding output data, and input INCHN specifies the channel the data belongs to, as described in the previous sections.

The ADPCM core requires 1 clock cycle to complete an encoding or decoding operation for one data sample and has a fixed latency of 2 clock cycles.

Channel Selection

The INCHN input specifies the channel with which the input data is associated when the core is performing a coding operation.

Global Reset and Configuration

RST is an asynchronous global reset signal. INIT initializes a channel to the ITU specified initial state.

When INSTROB is high, all channel configuration and data input signals are taken.

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Table 2: Configuration Control Signals

Signal	Description	Control Choice			
	Control Values	**0**		**1**	
LAW	Selects either A-law or μ-law for encoding and decoding	μ-law		A-law	
EBI	Control whether even bit inversion is performed for A-law/μ-law encoding/decoding operations	No bit inversion		Even bit inversion performed for A-law All bit inversion performed for μ-law	
	Control Values	**00**	**01**	**10**	**11**
IW[1:0]	Controls the number of bits in the ADPCM output word when encoding, or the number of bits in the input word when decoding, using the G.726 standard	2 bits	3 bits	4 bits	5 bits
	Controls the number of core bits in the ADPCM output word when encoding or the number of bits in the ADPCM input word when decoding, using the G.727 standard.	2 bits	3 bits	4 bits	not valid
EW[1:0]	Input	Specifies the number of G.727 enhancement bits "00": = 0 bits "01" = 1 bit "10" = 2 bits "11" = 3 bits			

Core Modifications

The Amphion ADPCM core can be modified to meet specific design needs. Modifications include:

- Number of channels
- Compression ratios supported
- Coding laws supported (A-law or μ-law)
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Pinout

Pinout of the ADPCM core has not been fixed to specific FPGA I/O, allowing flexibility with a user's application. Table 3 gives the descriptions of the input and output ports (shown graphically in Figure 2) of the 512 ADPCM codecs. Unless otherwise stated, all signals are active high and bit (0) is the least significant bit.

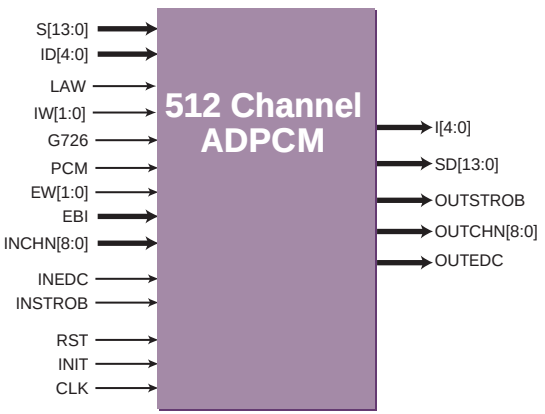

Figure 2: 512-Channel ADPCM Core Pinouts

Table 3: Pinout Table

Signal	Signal Direction	Description
CLK	Input	Clock input-rising edge active
RST	Input	Global reset input, active high
INIT	Input	Initialisation signal, active high
INSTROB	Input	Input data strobe signal, active high, encoding/decoding is performed when asserted
INEDC	Input	Selects encode or decode operation: High = encode Low = decode
PCM	Input	Logarithmic PCM or uniform PCM selection control signal High = logarithmic PCM Low = uniform PCM
S[13:0]	Input	Logarithmic or uniform PCM input word for encoding S[13:0] = µ-law uniform PCM input S[13:1] = A-law uniform PCM input S[7:0] = Logarithmic PCM input
ID [4:0]	Input	ADPCM input word for decoding ID[4:3] = 2 bit ADPCM word, 16 Kbits/sec data rate ID[4:2] = 3 bit ADPCM word, 24 Kbits/sec data rate ID[4:1] = 4 bit ADPCM word, 32 Kbits/sec data rate ID[4:0] = 5 bit ADPCM word, 40 Kbits/sec data rate
G726	Input	Specifies G.726 or G.727 operation High: G.726 standard Low: G.727 standard
INCHN[8:0]	Input	Specifies channel with which the input data is associated when the core is performing coding operation or performing channel reset.
IW[1:0] EBI LAW EW[1:0]	Input	Compression configuration, even bit inversion, law control and enhancement bits - See Table 2
I[4:0]	Output	ADPCM input word for decoding ID[4:3] = 2 bit ADPCM word, 16 Kbits/sec data rate ID[4:2] = 3 bit ADPCM word, 24 Kbits/sec data rate ID[4:1] = 4 bit ADPCM word, 32 Kbits/sec data rate ID[4:0] = 5 bit ADPCM word, 40 Kbits/sec data rate
SD[13:0]	Output	Logarithmic or uniform PCM output word from decoding SD[13:0] = µ-law uniform PCM output SD[13:1] = A-law uniform PCM output SD[7:0] = Logarithmic PCM output
OUTSTROB	Output	Output data strobe
OUTEDC	Output	Encoded or decoded result - HIGH encoding, LOW decoding result.
OUTCHN 8:0]	Output	Channel relating to resulting signal

Verification Methods

Complete functional and timing simulation has been performed using Model Technology ModelSim.

Recommended Design Experience

Users should be familiar with HDL design methodology and Xilinx design flows including VHDL/Verilog language and syntax, component instantiation, synthesis, and simulation.

Ordering Information

For information on the 512 channel ADPCM core, please contact Amphion directly from the address available on the first page of this datasheet.

Related Information

European Telecommunications Standards Institute

For information on European digital broadcasting systems standards contact:

European Telecommunications Standards Institute
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Xilinx Programmable Logic

For information on Xilinx programmable logic or development system software, contact your local Xilinx sales office, or:

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