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SRK2000

Synchronous rectifier smart driver for LLC resonant converter

Preliminary data

Features

- Secondary-side synchronous rectifier controller optimized for LLC resonant converter
- Safe management of load transient, light load and start-up condition
- Intelligent automatic sleep mode at light load
- Dual gate driver for n-channel MOSFETs with 1 A source and 3.5 A sink drive current
- Operating voltage range 4.5 to 32 V
- Programmable UVLO with hysteresis
- 250 µA quiescent consumption
- Operating frequency up to 500 kHz
- SO8 package

Applications

- All-in-one PC
- High-power AC-DC adapters
- 80+/85+ compliant ATX SMPS
- 90+/92+ compliant server SMPS
- Industrial SMPS

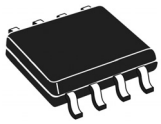
Description

The SRK2000 smart driver implements a control scheme specific for secondary-side synchronous rectification in LLC resonant converters that use a transformer with center-tap secondary winding for full-wave rectification.

It provides two high-current gate-drive outputs, each capable of driving one or more N-channel Power MOSFETS. Each gate driver is controlled separately and an interlock logic circuit prevents the two synchronous rectifier MOSFETS from conducting simultaneously.

The control scheme in this IC provides for each synchronous rectifier being switched on as the corresponding half-winding starts conducting and switched off as its current goes to zero. A unique feature of this IC is its intelligent automatic sleep mode. It allows the detection of a low-power operating condition for the converter and puts the IC in a low consumption sleep-mode where gate driving is stopped and quiescent consumption is reduced. In this way, converter's efficiency improves at light load, where synchronous rectification is no more beneficial. The IC automatically exits from sleep-mode and restarts switching as it recognizes that the load for the converter has increased.

A noticeable feature is the very low external component count required.



SO-8

Figure 1. Internal block diagram

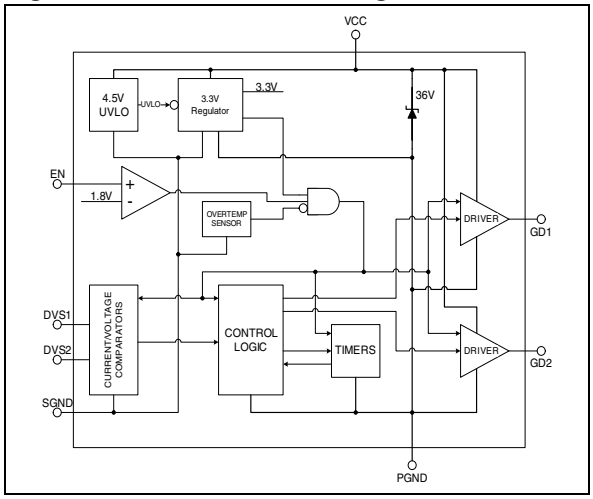


Table 1. Device summary

Order code	Package	Packing
SRK2000D	SO-8	Tube
SRK2000DTR		Tape and reel

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Figure 2. Pin configuration

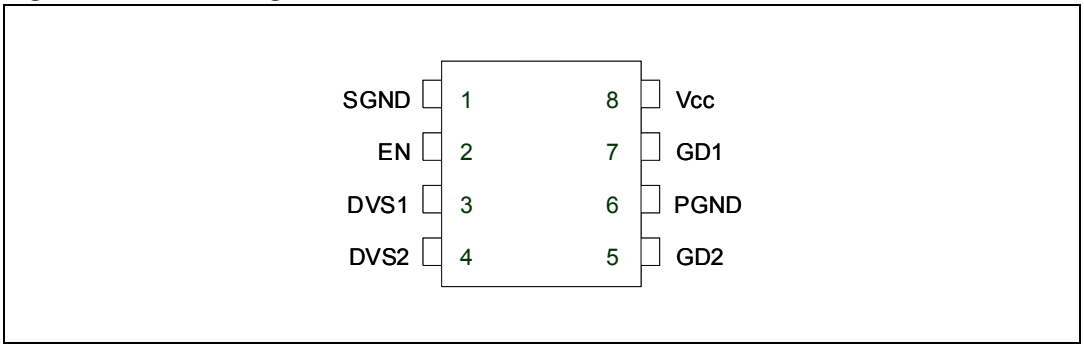

Table 2. Pin description

n.	Name	Function
1	SGND	Signal Ground. Return of the bias current of the device and 0 volt reference for drain-to-source voltage monitors of both sections. Route directly this pin to PGND.
2	EN	Drain voltage threshold setting for synchronous rectifier MOSFET turn-off. UVLO threshold programming. This pin will typically be biased by either a pull-up resistor connected to Vcc or by a resistor divider sensing Vcc. Pulling the pin to ground will disable the gate driver outputs GD1 and GD2, thus it can be used as Enable input as well.
3 4	DVS1 DVS2	Drain voltage sensing for sections 1 and 2. These pins are to be connected to the respective drain terminals of the corresponding synchronous rectifier MOSFET via limiting resistors. When the voltage on either pin goes negative, the corresponding synchronous rectifier MOSFET is switched on; as its (negative) voltage exceeds a threshold defined by the EN pin, the MOSFET is switched off. An internal logic rejects switching noise, however extreme care in a proper routing of the drain connection is recommended.
5 7	GD2 GD1	Gate driver output for sections 2 and 1. Each totem pole output stage is able to drive power MOSFETs with a peak current of 1 A source and 3.5 A sink. The high-level voltage of these pins is clamped at about 12V to avoid excessive gate voltages in case the device is supplied with a high Vcc.
6	PGND	Power ground. Return for gate drive currents. Route this pin to the common point where the source terminals of both synchronous rectifier MOSFETs are connected.
8	Vcc	Supply Voltage of the device. A small bypass capacitor (0.1 µF typ.) to SGND, located as close to IC's pins as possible, might be useful to get a clean supply voltage for the internal control circuitry. A similar bypass capacitor to PGND, again located as close to IC's pins as possible, might be an effective energy buffer for the pulsed gate-drive currents.

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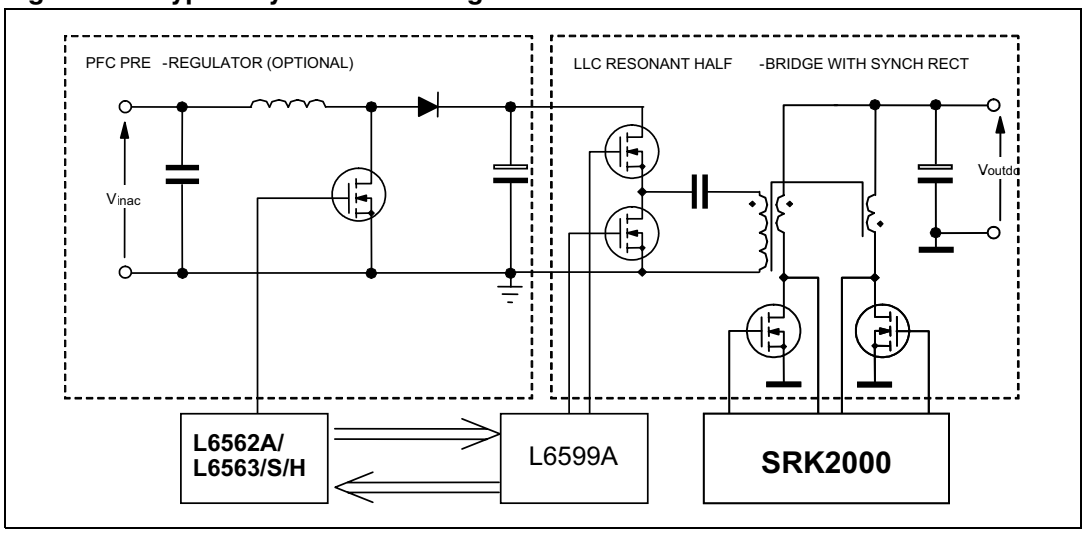
Figure 3. Typical system block diagram



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2 Maximum ratings

Table 3. Absolute maximum ratings

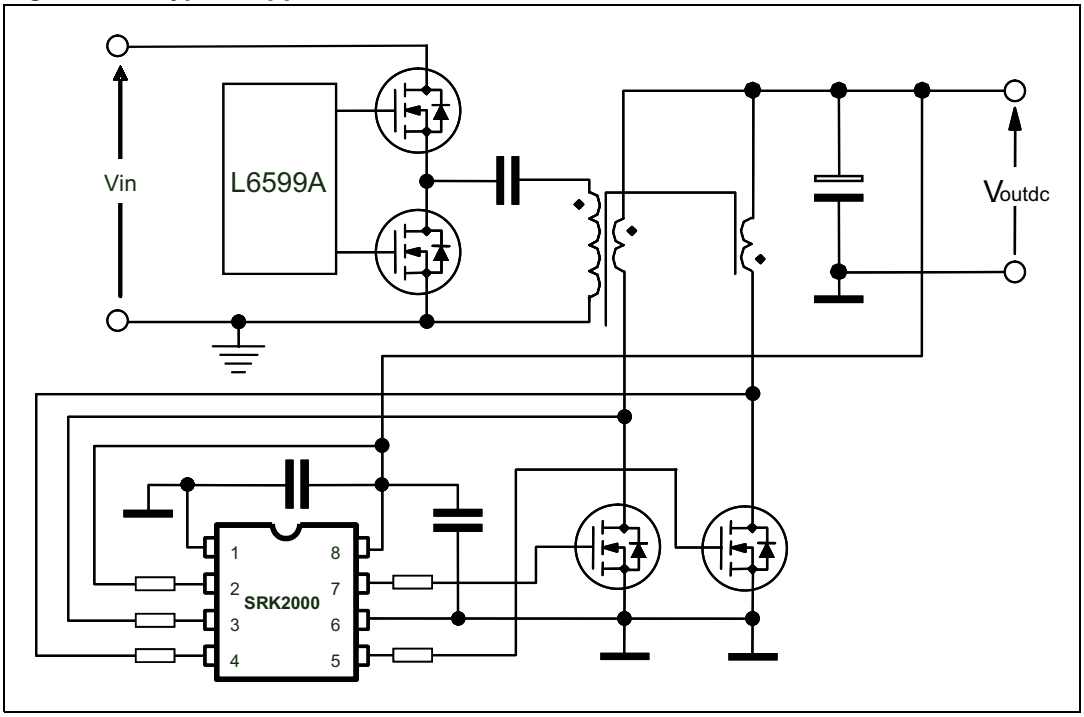
Symbol	Pin	Parameter	Value	Unit
Vcc	8	Dc supply voltage	-0.3 to Vcc_Z	V
Icc_Z	8	Internal Zener maximum current	25	mA
---	2, 3, 4	Analog inputs voltage rating	-0.3 to Vcc_Z	V
$I_{DVS1,2\_sk}$	3, 4	Analog inputs max. sink current (single pin)	25	mA
$I_{DVS1,2\_sr}$	3, 4	Analog inputs max. source current (single pin)	-5	mA

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Max. thermal resistance, junction-to-ambient	150	°C/W
Ptot	Power dissipation @T_A = 50 °C	0.65	W
T_J	Junction temperature operating range	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

3 Typical application schematic

Figure 4. Typical application schematic



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4 Electrical characteristics

T_J = -25 to 125 °C, V_{CC} = 12 V, C_{GD1} = C_{GD2} = 4.7 nF, EN = V_{CC}; unless otherwise specified; typical values refer to T_J = 25 °C

Table 5. Electrical characteristics

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
Supply voltage						
V_{CC}	Operating range	After turn-on	4.5		32	V
V_{CCOn}	Turn-on threshold	(1)	4.25	4.5	4.75	V
V_{CCOff}	Turn-off threshold	(1)	4	4.25	4.5	V
Hys	Hysteresis			0.25		V
Vcc_Z	Zener voltage	Icc_Z = 20 mA	33	36	39	V
Supply current						
$I_{start-up}$	Start-up current	Before turn-on, Vcc = 4 V		45	70	µA
Iq	Quiescent current	After turn-on		250	500	µA
I_{CC}	Operating supply current	@ 300 kHz		35		mA
Iq	Quiescent current	EN = SGND		150	250	µA
Drain sensing inputs and synch functions						
$V_{DVS1,2\_H}$	Upper clamp voltage	$I_{DVS1,2}$ = 20 mA		Vcc_Z		V
$I_{DVS1,2\_b}$	Input bias current	$V_{DVS1,2}$ = 0 to Vcc (2)	-1		1	µA
$V_{DVS1,2\_A}$	Arming voltage (positive-going edge)			1.4		V
$V_{DVS1,2\_PT}$	Pre-triggering voltage (negative-going edge)			0.7		V
$V_{DVS1,2\_TH}$	Turn-on threshold		-250	-200	-180	
$I_{DVS1,2\_On}$	Turn-on source current	$V_{DVS1,2}$ = -250 mV		-50		µA
$V_{DVS1,2\_Off}$	Turn-off threshold (positive-going edge)	R = 680 kΩ from EN to Vcc	-18	-25	-32	mV
		R = 270 kΩ from EN to Vcc	-9	-12.5	-16	
T_{PD_On}	Turn-on debounce delay	After sourcing $I_{DS1,2\_On}$		250		ns
T_{PD_Off}	Turn-off propagation delay	After crossing $V_{DS1,2\_Off}$			60	ns
T_{ON_min}	Minimum ON-time			150		ns
D_{OFF}	Min. operating duty-cycle			40		%
D_{ON}	Restart duty-cycle			60		%
Gate-drive enable function						
V_{EN_On}	Enable threshold	Positive going edge (1)	1.7	1.8	1.9	V
Hyst	Hysteresis	Below V_{EN_On}		45		mV

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Table 5. Electrical characteristics (continued)

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
I_{EN}	Bias current	$V_{EN} = V_{EN\_On}$			1	µA
Turn-off threshold selection						
V_{EN-Th}	Selection threshold	$V_{CC} = V_{CCOn}$	0.32	0.36	0.40	V
I_{EN}	Pull-down current	$V_{EN} = V_{EN\_Th}$, $V_{CC} = V_{CCOn}$	7	10	13	µA
Gate drivers						
V_{GDH}	Output high voltage	$I_{GDsource}$= 5 mA	11.75	11.9		V
		$I_{GDsource}$= 5 mA, Vcc = 5 V	4.75	4.9		
V_{GDL}	Output low voltage	I_{GDsink} = 200 mA		0.2		V
		I_{GDsink} = 200 mA, Vcc = 5 V		0.2		
$I_{sourcepk}$	Output source peak current			-1		A
I_{sinkpk}	Output sink peak current			3.5		A
t_f	Fall time			18		ns
t_r	Rise time			40		ns
$V_{GDclamp}$	Output clamp voltage	$I_{GDsource}$ = 5 mA; Vcc = 20 V	12	13	15	V
V_{GDL_UVLO}	UVLO saturation	Vcc = 0 to V_{CCon} Isink = 5 mA		1	1.3	V

1. Parameters tracking each other
2. For Vcc>30 V $I_{DVS1,2\_b}$ could be greater than 1 µA because of the possible current contribution of the internal clamp zener (few tens of µA)

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5 Application information

5.1 EN pin: pin function and usage

The pin may perform three different functions: it sets the threshold $V_{DVS1,2\_Off}$ for the drain-to-source voltage of either Synchronous Rectifier (SR) power MOSFET to determine their turn-off in each conduction cycle; it allows the user to program the UVLO thresholds of the gate drivers and can be used as Enable (remote on/off control).

5.1.1 Pull-up resistor configuration

At start-up, an internal 10 µA current sink (I_{EN}) is active as long as the device supply voltage Vcc is below the start-up threshold V_{CCOn}. The moment Vcc equals V_{CCOn}, (4.5 V typical) the voltage V_{EN} on the EN pin determines the turn-off threshold $V_{DVS1,2\_Off}$ for the drain voltage of both synchronous rectifiers during their cycle-by-cycle operation: if $V_{EN} < V_{EN\_Th}$ (= 0.36 V) the threshold will be set at -25 mV, otherwise at -12 mV. Once the decision is made, the setting will be frozen as long as Vcc is greater than the turn-off level V_{CCOff} (4.25 V typical).

A simple pull-up resistor R_1 to Vcc can be used to set $V_{DVS1,2\_Off}$ turn-off threshold. The voltage on the EN pin as the device turns on is given by:

$$V_{EN} = V_{CCOn} - I_{EN} R1$$

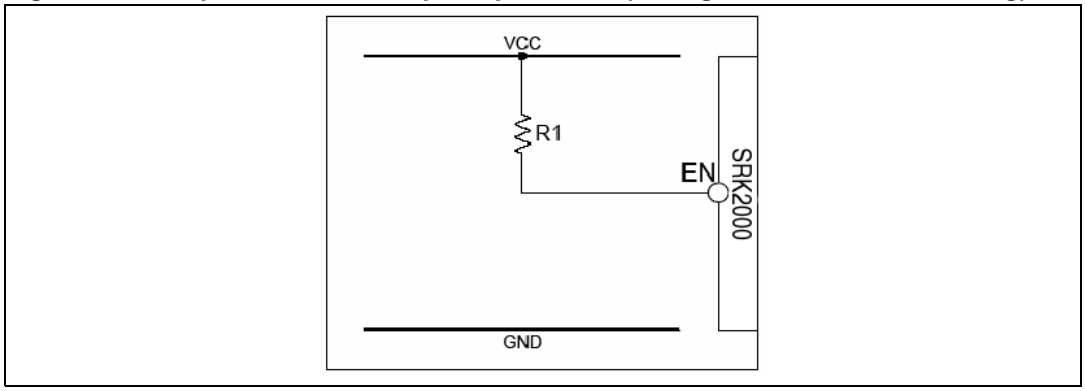
Then, considering worst-case scenarios, we have:

$$R1 > 633\ k\Omega \rightarrow V_{DVS1,2\_Off} = -25\ mV$$

$$R1 < 296\ k\Omega \rightarrow V_{DVS1,2\_Off} = -12\ mV$$

Some additional margin (equal to resistor's tolerance) needs to be considered; assuming 5% tolerance, it is possible to suggest the use of the standard values R_1 = 680 kΩ in the first case and R_1 = 270 kΩ in the second case.

Figure 5. EN pin biased with a pull-up resistor (for logic-level MOSFET driving)



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As Vcc exceeds V_{CCOn} the internal current sink I_{EN} is switched off and the enable function is activated. The voltage on the pin is then compared to an internal reference V_{EN_On} set at 1.8 V: if this threshold is exceeded the gate drivers GD1 and GD2 will be enabled and the SR MOSFETs will be operated; otherwise, the device will stay in an idle condition and the SR MOSFETs in the off state.

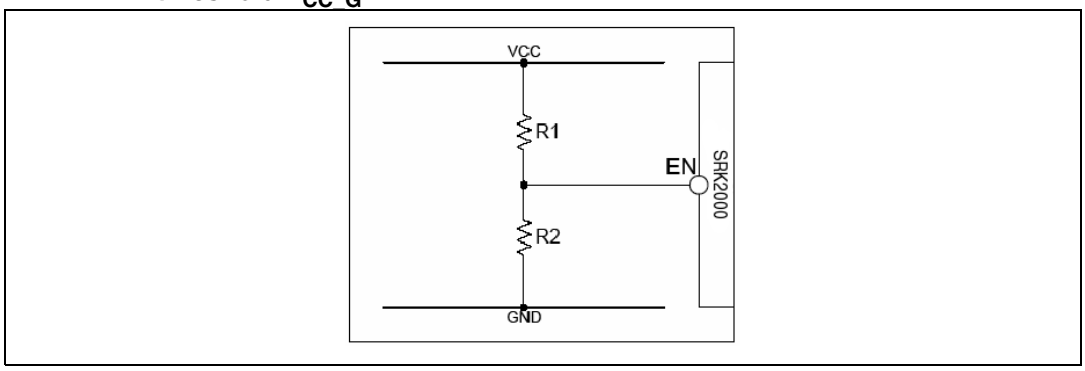
Using the pull-up resistor R_P the voltage on the EN pin will rise as I_{EN} is switched off and tend to Vcc, thus exceeding V_{EN_On} and enabling the operation of both SR MOSFETs. Essentially, this results in enabling gate driving as Vcc exceeds V_{CCOn} and disabling it as Vcc falls below V_{CCOn}. This configuration is thereby suggested when SR MOSFETs are logic-level type.

5.1.2 Resistor divider configuration

To enable gate-driving with a Vcc voltage higher than a predefined value V_{CC_G}, to properly drive standard SR MOSFET, the EN pin will be biased by a resistor divider (R1 upper resistor, R2 lower resistor) whose values will be chosen so as to exceed V_{EN_On} when Vcc = V_{CC_G} and set the desired $V_{DVS1,2\_Off}$ level as well. Note that, with a falling Vcc, gate-driving will be disabled at a Vcc level about 2.5% lower than V_{CC_G}, because of the 45 mV hysteresis of the comparator.

The equations that describe the circuit in the two crucial conditions Vcc = V_{CCOn} (when the decision of the $V_{DVS1,2\_Off}$ level is made) and Vcc = V_{CC_G} (when gate driving is to be enabled) are respectively:

Figure 6. EN pin biased with a resistor divider to program the gate-drive UVLO threshold V_{CC_G}



Equation 1

$$\begin{cases} \dfrac{V_{CCOn} - V_{EN}}{R1} = I_{EN} + \dfrac{V_{EN}}{R2} \\ V_{CC\_G}\dfrac{R2}{R1+R2} = V_{EN\_On} \end{cases}$$

Solving these equations for R_1 and R_2 we get:

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Equation 2

$$\begin{cases} R1 = \dfrac{V_{CCOn} - V_{EN}\dfrac{V_{CC\_G}}{V_{EN\_On}}}{I_{EN}} \\ R2 = R1\dfrac{V_{EN\_On}}{V_{CC\_G} - V_{EN\_On}} \end{cases}$$

If V_{CC_G} is not too low (<8÷9 V) its tolerance is not critical because related only to that of V_{EN_On} (±5.6%) and of the external resistors R1, R2 (±1% each is recommended). Then, some care needs to be used only as far as the selection of the -12/-25 mV threshold is concerned: in fact, the large spread of I_{EN} will considerably affect the voltage on the EN pin as the device turns on, value that can be found by solving the first of (1) for V_{EN}:

Equation 3

$$V_{EN} = \frac{V_{CCOn} - I_{EN}R1}{1 + \dfrac{R1}{R2}}$$

A couple of examples will clarify the suggested calculation methodology.

Example 1 V_{CC_G} = 10 V, $V_{DVS1,2\_Off}$ = - 25 mV.

In this case V_{EN} must be definitely lower than the minimum value of V_{EN_Th} (= 0.32 V). From the second of (2), the nominal ratio of R1 to R2 will be (10 – 1.8) / 1.8 = 4.555. Substituting the appropriate extreme values in (3) it must be (4.75 - $7 \cdot 10^{-6} \cdot$R1) / (1 + 4.555) < 0.32; solving for R1 yields R1 > 425 kΩ; let us consider an additional 4% margin to take both the tolerance and the granularity of the R1 and R2 values into account, so that: R1 > 425·1.04 = 442 kΩ. Choose R1 = 442 kΩ (E48 standard value) and, from the second of (2), R2 = 442/4.555 = 97 kΩ; use 97.6 kΩ (E48 standard value).

Example 2 V_{CC_G} = 10 V, $V_{DVS1,2\_Off}$ = - 12 mV.

In this case V_{EN} must be definitely higher than the maximum value of V_{EN_Th} (= 0.40 V). from the second of (2), the nominal ratio of R1 to R2 will be (10 – 1.8) / 1.8 = 4.555. Substituting the appropriate extreme values in (3) it must be (4.25 - $13 \cdot 10^{-6} \cdot$R1) / (1 + 4.555) > 0.4; solving for R1 yields R1 < 156 kΩ; with 4% additional margin R1 < 156/1.04 = 150 kΩ. Choose R1 = 147 kΩ (E48 standard value) and, from the second of (2), R2 = 147/4.555 = 32.3 kΩ; use 32.4 kΩ (E48 standard value).

Note: In both examples the gate drivers will be disabled as Vcc falls below 9.75 V (nominal value), as the voltage on the EN pin falls 45 mV below V_{EN_On}.

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5.1.3 Remote on/off control

Whichever configuration is used, since a voltage on the EN pin 45 mV below V_{EN_On} disables the gate drivers, any small-signal transistor can be used to pull down the EN pin and force the gate drivers in an off state.

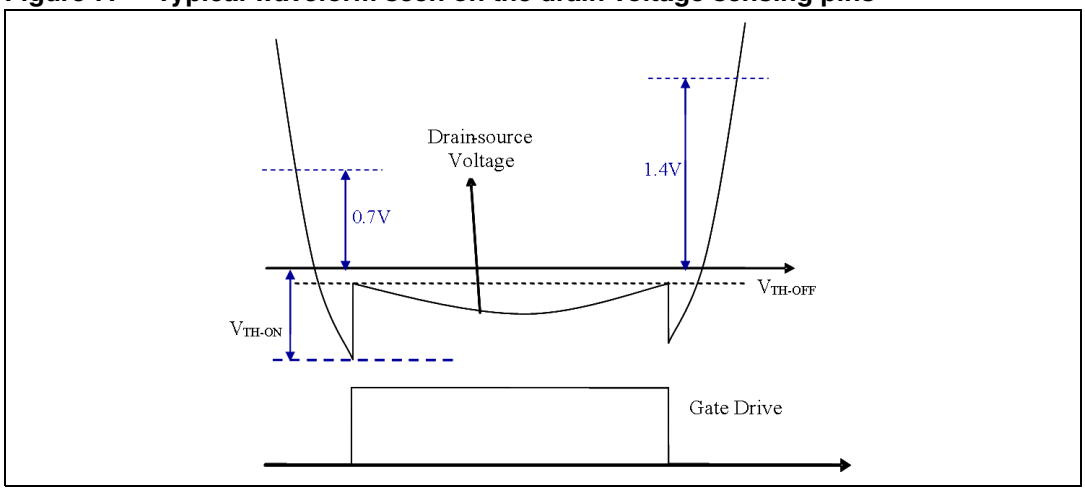
Finally, it should be noted that during power-up, power-down and under overload or short circuit conditions the gate drivers will be shut down if the Vcc voltage is insufficient: < V_{CCOff} in case of pull-up resistor configuration, < 0.975·V_{CC_G} in case of resistor divider configuration (the coefficient 0.975 depends on the hysteresis on the enable pin threshold).

5.2 Drain voltage sensing

In the following explanations, it is assumed that the reader is familiar with the LLC resonant half-bridge topology and its waveforms, especially those on the secondary side with a center-tap transformer winding for full-wave rectification.

To understand the polarity and the level of the current flowing in the SR MOSFETs (or their body diodes, or diodes in parallel to the MOSFETs) the IC is provided with two pins, DVS1-2, able to sense the voltage level of the MOSFET's drain.

Figure 7. Typical waveform seen on the drain voltage sensing pins



The logic that controls the driving of the two SR MOSFETs is based on two gate-driver state machines working in parallel in an interlocked way to avoid switching on both gate drivers at the same time.

There are four significant drain voltage thresholds: the first one, $V_{DVS1,2\_A}$ (= 1.4 V), sensitive to positive-going edges, arms the opposite gate driver (interlock function); the second one $V_{DVS1,2\_PT}$ (=0.7 V), sensitive to negative-going edges provides a pre-trigger of the gate driver; the third one is the (negative) threshold $V_{TH\text{-}ON}$ that triggers the gate driver as the body diode of the SR MOSFET starts conducting; the fourth one is the internal (negative) threshold $V_{DVS1,2\_Off}$ where the SR MOSFET is switched off (selectable between -12 mV or -25 mV by properly biasing the EN pin.

The value of the on threshold $V_{TH\text{-}ON}$ is affected by the external resistor in series to each pin DVS1-2 needed essentially to limit the current that might be injected into the pins when one SR MOSFET is off and the other SR MOSFET is conducting. In fact, on the one hand, when one MOSFET is off (and the other one is conducting) its drain-to-source voltage is slightly

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higher than twice the output voltage; if this exceeds the voltage rating of the internal clamp (Vcc_Z = 36 V typ.) a series resistor R_D has to limit the injected current below an appropriate value, lower than the maximum rating (25 mA) and taking the related power dissipation into account. On the other hand, when current starts flowing into the body diode of one MOSFET (or in the diode in parallel with the MOSFET), the drain-to-source voltage is negative (≅-0.7 V); when the voltage on pins VDS1-2 reaches the threshold $V_{DVS1,2\_TH}$ (-0.2V typ.) an internal current source $I_{DVS1,2\_On}$ is activated; as this current exceeds 50 µA, the gate of the MOSFET is turned on. Therefore, the actual triggering threshold can be determined by the following formula:

$$V_{TH-ON} = R_D \cdot I_{DVS1,2On} + V_{DVS1,2\_TH}$$

For instance, with R_D = 2 kΩ, the triggering threshold will be located at -(2 kΩ · 50 µA) - 0.2 V = -0.3 V.

To avoid false triggering of the gate driver, a debounce delay T_{PD_On} (= 250 ns) is used after sourcing $I_{DS1,2\_On}$ (i.e. the current sourced by the pin must exceed 50 µA for more than 250 ns before the gate driver is turned on). This delay is not critical for the converter's efficiency because the initial current is close to zero or anyway much lower than the peak value.

Once the SR MOSFET has been switched on, its drain-to-source voltage drops to a value given by the flowing current times the MOSFET $R_{DS(on)}$. Again, since the initial current is low, the voltage drop across the $R_{DS(on)}$ might exceed the turn-off threshold $V_{DVS1,2\_Off}$, and determine an improper turn-off. To prevent this, the state machine enables the turn-off comparator referenced to $V_{DVS1,2\_Off}$ only in the second half of the conduction cycle, based on the information of the duration of the previous cycle. In the first half of the conduction cycle only an additional comparator, referenced to zero, is active to prevent the current of the SR MOSFET from reversing, which would impair the operation of the LLC converter.

Once the threshold $V_{DVS1,2\_Off}$ is crossed (in the second half of the conduction cycle) and the GATE is turned off, the current will again flow through the body diode causing the drain-to-source voltage to have a negative jump, going again below V_{TH-ON}. The interlock logic, however, prevents a false turn-on.

It is worth pointing out that, due to the fact that each MOSFET is turned on after its body diode starts conducting, the ON transition happens with the drain-source voltage equal to the body diode forward drop; therefore there is neither Miller effect nor switching losses at MOSFET turn-on. Also at turn-off the switching losses are not present, in fact the current is always flowing from source to drain and, when the MOSFET is switched off, it goes on flowing through the body diode (or the external diode in parallel to the MOSFET).

Unlike at turn-on, the turn-off speed is critical to avoid current reversal on the secondary side, especially when the converter operates above the resonance frequency, where the current flowing through the MOSFET exhibits a very steep edge while decreasing down to zero: the turn-off propagation T_{PD_Off} delay has a maximum value of 60 ns.

The interlock logic, in addition to checking for consistent secondary voltage waveforms (one MOSFET can be turned on only if the other one has a positive drain-to-source voltage > $V_{DVS1,2\_A}$) to prevent simultaneous conduction, allows only one switching per cycle: after one gate driver has been turned off, it cannot be turned on again before the other gate drive has had its own on/off cycle.

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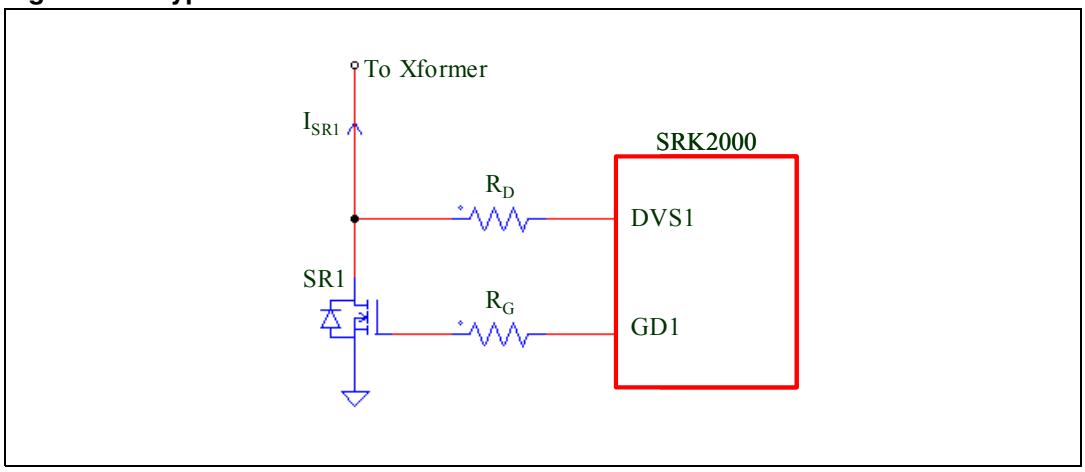
Figure 8. Typical connection of the SRK2000 to the SR MOSFET



5.3 Gate driving

The IC is provided with two high-current gate-drive outputs (1A source and 3.5 A sink), each capable of driving one or more N-channel Power MOSFETs. Thanks to the programmable gate-drive UVLO, it is possible to drive both standard MOSFETs and logic level MOSFETs.

The high-level voltage provided by the driver is clamped at $V_{GDclamp}$ (=12 V) to avoid excessive voltage levels on the gate in case the device is supplied with a high Vcc.

The two gate drivers have a pull down capability that ensures the SR MOSFETs cannot be spuriously turned on even at low Vcc: in fact the drivers have a 1V (typical) UVLO saturation level at Vcc below the turn-on threshold.

5.4 Intelligent automatic sleep-mode

A unique feature of this IC is its intelligent automatic sleep-mode. The logic circuitry is able to detect a light load condition for the converter and stop gate driving, reducing also IC's quiescent consumption. This improves converter's efficiency at light load, where the power losses on the rectification body diodes (or external diodes in parallel to the MOSFETs) become lower than the power losses in the MOSFETs and those related to their driving.

The IC is also able to detect an increase of the converter's load and automatically restart gate driving.

The algorithm used by the intelligent automatic sleep-mode is based on a dual time measurement system. The duration of a switching cycle of an SR MOSFET (that is one half of the resonant converter switching period) is measured using a combination of the negative-going edge of the drain-to-source voltage falling below $V_{DVS1,2\_PT}$ and the positive-going edge exceeding $V_{DVS1,2\_A}$.; the duration of the SR MOSFET conduction is measured from the moment its body diode starts conducting (drain-to source voltage falling below V_{TH-ON}) to the moment the gate drive is turned off (in case the device is operating) or to the moment the body diode ceases to conduct (drain-to source voltage going over V_{TH-ON}). While at full load the SR MOSFET conduction time occupies almost 100% of the switching cycle, as the load is reduced, the conduction time is reduced and as it falls below 40% (D_{OFF}) of the SR MOSFET switching cycle the device enter sleep-mode. To prevent wrong decisions, the sleep mode condition must be confirmed for 16 consecutive switching

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cycles of the resonant converter (i.e. 16 consecutive cycles for each SR MOSFET of the center-tap).

Once in sleep mode, SR MOSFET gate driving is re-enabled when the conduction time of the body diode (or the external diodes in parallel to the MOSFET) exceed 60% (D_{ON}) of the switching cycles. Also in this case the decision is made considering the measurement on 8 consecutive switching cycles (i.e. 8 consecutive cycles for each SR MOSFET of the center-tap). Furthermore, after each sleep mode entering/exiting transition, the timing is ignored for a certain number of cycles, to let the resulting transient in the output current fade out; then the time check is enabled. The number of ignored resonant converter switching cycles switching cycles is 128 after entering sleep mode and 256 after exiting the sleep mode.

5.5 Layout guidelines

The IC is designed with two grounds, SGND and PGND.

SGND is used as the ground reference for all the internal high precision analog blocks. PGND, instead, is the ground reference for all the noisy digital blocks, as well as the current return for the gate drivers. Additionally, it is also the ground for the ESD protection circuits. SGND is protected by ESD events versus PGND through two anti-parallel diodes.

When laying out the PCB, care must be taken in keeping the source terminals of both SR MOSFETS as close to one another as possible and routing the trace that goes to PGND separately from the load current return path. This trace should be as short as possible and be as close to the physical source terminals as possible. Doing the layout as more geometrically symmetrical as possible will help make the circuit operation as much electrically symmetrical as possible. SGND should be directly connected to PGND using a path as short as possible (under the device body).

Also drain voltage sensing should be done as physically close to the drain terminals as possible: any stray inductance involved by the load current that is in the drain-to-source voltage sensing circuit may significantly alter the current reading, leading to a premature turn-off of the SR MOSFET. It is worth mentioning that, especially in higher power applications or at higher operating frequencies, even the stray inductance of the internal wire bonding can be detrimental. In this case a cautious selection of the SR MOSFET package is required.

The usage of bypass capacitors between Vcc and both SGND and PGND is recommended. They should be low-ESR, low-ESL type and located as close to the IC pins as possible. Sometimes, a series resistor (in the ten) between the converter's output voltage and the Vcc pin, forming an RC filter along with the bypass capacitor, is useful to get a cleaner Vcc voltage.

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6 Package mechanical data

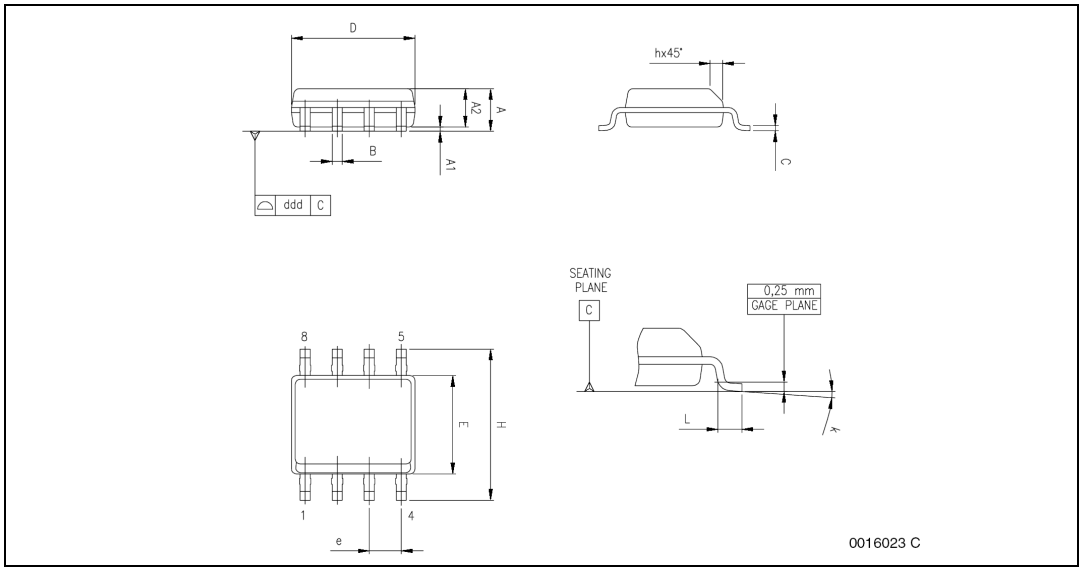
In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

Table 1. SO-8 mechanical data

Dim.	mm.			inch		
	Min	Typ	Max	Min	Typ	Max
A	1.35		1.75	0.053		0.069
A1	0.10		0.25	0.004		0.010
A2	1.10		1.65	0.043		0.065
B	0.33		0.51	0.013		0.020
C	0.19		0.25	0.007		0.010
D (1)	4.80		5.00	0.189		0.197
E	3.80		4.00	0.15		0.157
e		1.27			0.050	
H	5.80		6.20	0.228		0.244
h	0.25		0.50	0.010		0.020
L	0.40		1.27	0.016		0.050
k	0° (min.), 8° (max.)					
ddd			0.10			0.004

1. Dimensions D does not include mold flash, protrusions or gate burrs. Mold flash, potrusions or gate burrs shall not exceed 0.15mm (.006inch) in total (both side).

Figure 9. Package dimensions



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7 Revision history

Table 6. Document revision history

Date	Revision	Changes
10-Aug-2010	1	Initial release.

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