SIEMENS

ISDN PC Adapter Circuit
IPAC

PSB/F 2115 Version 1.2

Addendum/Corrections 02.99 to Data Sheet 11.97

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1 Back to Back Frames

The back to back frame transmission as described in chapter 3.4.1 on pages 177 and 178 is not supported by the chip.

2 Length of FSC Pulse in NT and LT-S Modes

In NT and LT-S mode the S/T-interface superframe with 5 ms period can be synchronized to a master device by modulation of the pulse width of FSC.

The IPAC samples the FSC input with the second falling edge of DCL in the very first bit of the frame and resets the S/T-interface transmit frame, including multiframe, if the sample bit is zero. The remaining FSC clocks must be of **at least two DCL periods** duration.

Please note, that in a NT application the superframe marker of IEC-Q must be disabled due to different multiframe periods of U- and S-interface.

3 Microprocessor Interface Timing

The timing value t_{RWD} is specified as tbd in the Data Sheet 11.97 (page 288). The actual value can be seen from the table below.

Parameter	Symbol	Limit Values		Unit
		min.	max.	
R/$\overline{W}$ hold from $\overline{CS}$ x $\overline{DS}$ inactive	t_{RWD}	5		ns

Revision History: Previous Version: none
Major Changes:

4 Pin Definitions and Functions

One function of the pins AUX3-5 is not described on page 22.

If the PCM interface is disabled (in LT-S and LT-T modes) AUX3-5 can be used as general purpose I/O pins, i.e. same functions as in TE mode.