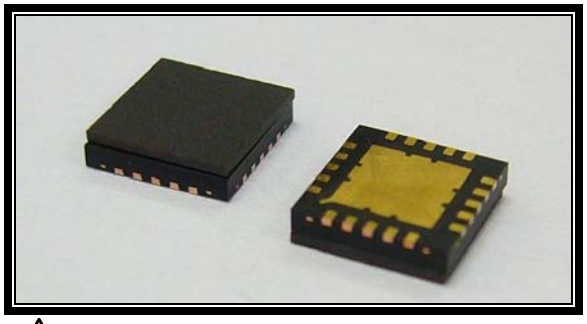
EMP114-Q5

UPDATED: 04/24/2008

7.0 – 9.0 GHz Surface-Mounted PA



FEATURES

- **7.0 – 9.0 GHz Operating Frequency Range**
- **30.0dBm Output Power at 1dB Compression**
- **17.0 dB Typical Small Signal Gain**
- **-40dBc OIMD3 @Each Tone Pout 20dBm**

APPLICATIONS

- **Point-to-point and point-to-multipoint radio**
- **Military Radar Systems**

Caution! ESD sensitive device.

ELECTRICAL CHARACTERISTICS (T_a = 25 °C, 50 ohm, VDD=7V, IDQ=800mA)

SYMBOL	PARAMETER/TEST CONDITIONS	MIN	TYP	MAX	UNITS
F	Operating Frequency Range	7.0		9.0	GHz
P1dB	Output Power at 1dB Gain Compression	28.5	30.0		dBm
Gss	Small Signal Gain	15.0	17.0		dB
OIMD3	Output 3rd Order Intermodulation Distortion @Δf=10MHz, Each Tone Pout 20dBm		-40	-37	dBc
Input RL	Input Return Loss		-12		dB
Output RL	Output Return Loss		-5		dB
Idss	Saturate Drain Current V_{DS} =3V, V_{GS} =0V	990	1230	1400	mA
V_{DD}	Power Supply Voltage		7	8	V
Rth	Thermal Resistance[1]		10		°C/W
Tb	Operating Base Plate Temperature	-35		+85	ºC

ABSOLUTE MAXIMUM RATINGS FOR CONTINUOUS OPERATION[2,3]

SYMBOL	CHARACTERISTIC	CONTINUOUS
V_{DS}	Drain to Source Voltage	8 V
V_{GS}	Gate to Source Voltage	-4 V
I_{DD}	Drain Current	Idss
I_{GSF}	Forward Gate Current	18mA
P_{IN}	Input Power	@ 3dB compression
T_{CH}	Channel Temperature	150°C
T_{STG}	Storage Temperature	-65/150°C
P_T	Total Power Dissipation	12.0W

1. R_{th} is mounting dependent. Measured result when used with Excelics recommended evaluation board.
2. Operating the device beyond any of the above rating may result in permanent damage.
3. Bias conditions must also satisfy the following equation V_{DS}*I_{DS} < (T_{CH} –T_{HS})/R_{TH}; where T_{HS} = ambient temperature

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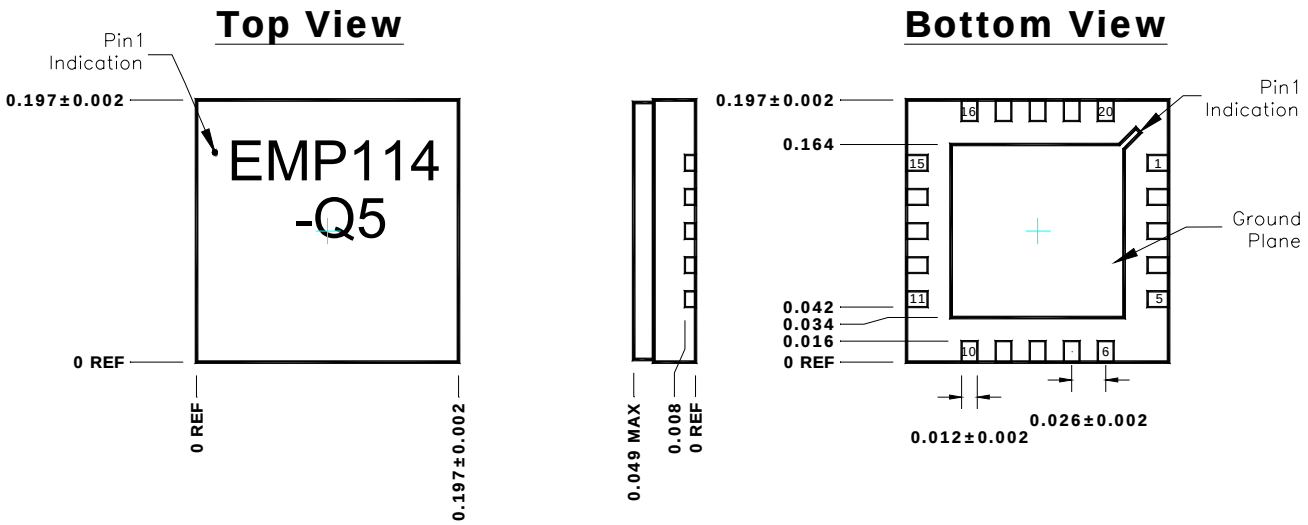
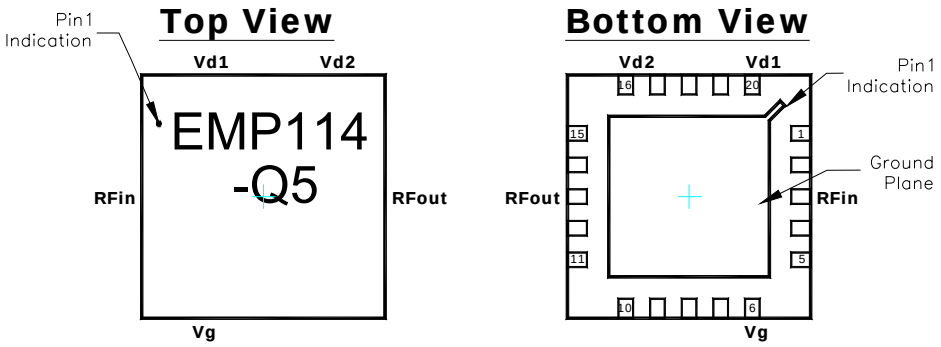
CHIP OUTLINE AND PIN ASSIGNMENT



Additional Notes:

1) Ground Plane must be soldered to PCB RF ground
2) All dimensions are in inches
3) Refer to Excelics application notes on QFNs for further guidelines
4) Pin Assignment:



Pin	Assignment
1, 2, 4, 5	NC
3	RF_{in}
6	V_g
7, 8, 9, 10, 11, 12, 14, 15	NC
13	RF_{out}
16	V_{d2}
17, 18, 19	NC
20	V_{d1}

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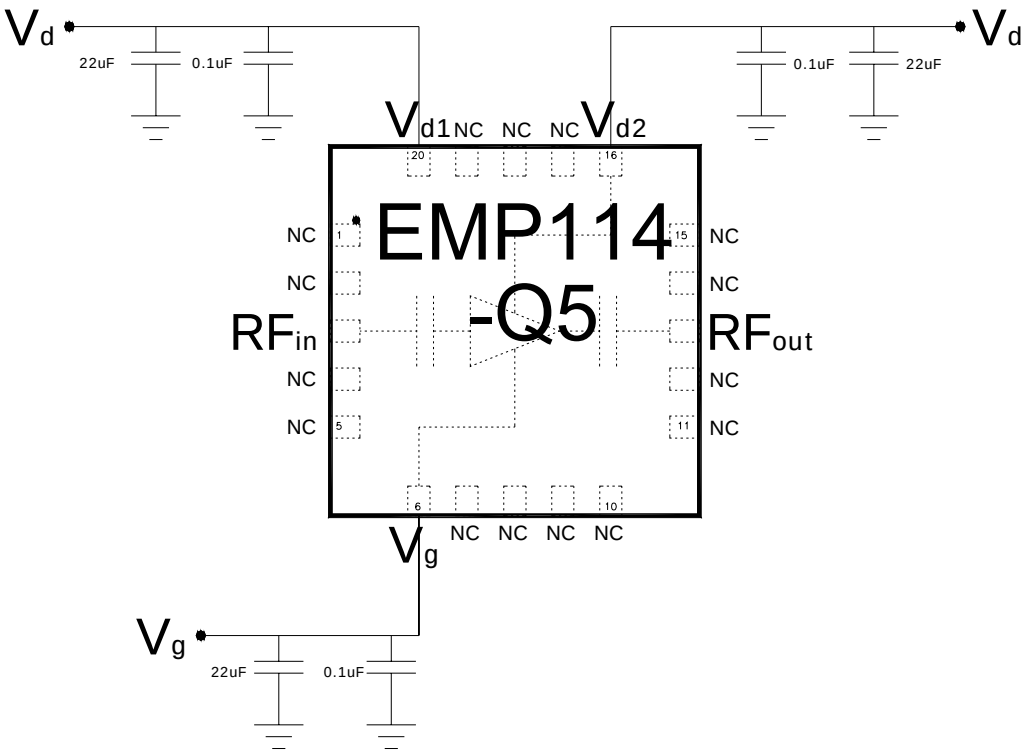
Recommended Circuit Schematic:



Notes:

1) External bypass capacitors should be placed as close to the package as possible.
2) Dual biasing sequence required:
   a. Turn-on Sequence: Apply V_g = -2.5V, followed by V_d = 7V, lastly increase V_g until required I_{dq}
   b. Turn-off Sequence: Turn off V_d, followed by V_g
3) Demonstration board available upon request.