

NTMD6601NR2G

Power MOSFET

80 V, 2.2 A, Dual N-Channel, SO-8

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- Dual SO-8 Surface Mount Package Saves Board Space
- This is a Pb-Free Device

Applications

- LCD Displays

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DSS}	80	V
Gate-to-Source Voltage - Continuous	V_{GS}	± 15	V
Continuous Drain Current $R_{\theta JA}$ (Note 1)	I_D	$T_A = 25^\circ\text{C}$	1.4
		$T_A = 70^\circ\text{C}$	1.2
Power Dissipation $R_{\theta JA}$ (Note 1)	P_D	$T_A = 25^\circ\text{C}$	1.0
		$T_A = 70^\circ\text{C}$	0.6
Continuous Drain Current $R_{\theta JA}$ (Note 2)	I_D	$T_A = 25^\circ\text{C}$	1.1
		$T_A = 70^\circ\text{C}$	0.9
Power Dissipation $R_{\theta JA}$ (Note 2)	P_D	$T_A = 25^\circ\text{C}$	0.6
		$T_A = 70^\circ\text{C}$	0.6
Continuous Drain Current $R_{\theta JA} t < 5$ s (Note 1)	I_D	$T_A = 25^\circ\text{C}$	2.2
		$T_A = 70^\circ\text{C}$	1.7
Pulsed Drain Current	I_{DM}	9.0	A
	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$		
Operating Junction and Storage Temperature	T_J, T_{STG}	-55 to +150	$^\circ\text{C}$
Source Current (Body Diode)	I_S	1.3	A
Single Pulse Drain-to-Source Avalanche Energy $T_J = 25^\circ\text{C}, V_{DD} = 50$ V, $V_{GS} = 10$ V, $I_L = 7.0$ A _{pk} , $L = 1.0$ mH, $R_G = 25 \Omega$	EAS	2.5	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

THERMAL RESISTANCE RATINGS

Rating	Symbol	Max	Unit
Junction-to-Ambient - Steady State (Note 1)	$R_{\theta JA}$	120	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - $t \leq 5$ s (Note 1)	$R_{\theta JA}$	48	
Junction-to-FOOT (Drain)	$R_{\theta JF}$	40	
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	200	

1. Surface-mounted on 2 inch sq FR4 board using 1 inch sq pad size, 1 oz Cu.
2. Surface-mounted on FR4 board using the minimum recommended pad size.

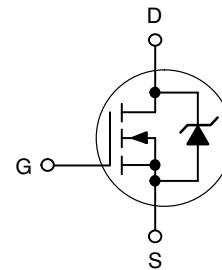


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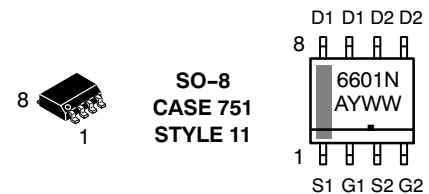
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ Max	I_D Max
80 V	215 m Ω @ 10 V	2.2 A
	245 m Ω @ 4.5 V	

N-Channel



MARKING DIAGRAM & PIN ASSIGNMENT



- 6601N = Device Code
- A = Assembly Location
- Y = Year
- WW = Work Week
- = Pb-Free Package

ORDERING INFORMATION

Device	Package	Shipping†
NTMD6601NR2G	SO-8 (Pb-Free)	2500/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NTMD6601NR2G

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = 250 μA	80			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			99.8		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = 80 V	T _J = 25°C		1.0	μA
			T _J = 125°C		25	
Gate-to-Source Leakage Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±15 V			±100	nA

ON CHARACTERISTICS (Note 3)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = 250 μA	1.0	1.9	3.0	V
Negative Threshold Temperature Coefficient	V _{GS(TH)} /T _J			4.6		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = 10 V	I _D = 2.2 A	190	215	mΩ
		V _{GS} = 5.0 V	I _D = 1.0 A	215	245	

CHARGES, CAPACITANCES AND GATE RESISTANCE

Input Capacitance	C _{ISS}	V _{GS} = 0 V, f = 1.0 MHz, V _{DS} = 25 V		220	400	pF
Output Capacitance	C _{OSS}			55	100	
Reverse Transfer Capacitance	C _{RSS}			16	30	
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 5.0 V, V _{DS} = 40 V, I _D = 1.0 A		5.0	9.0	nC
Threshold Gate Charge	Q _{G(TH)}			0.4		
Gate-to-Source Charge	Q _{GS}			1.0		
Gate-to-Drain Charge	Q _{GD}			2.75		
Total Gate Charge	Q _{G(TOT)}	V _{GS} = 10 V, V _{DS} = 40 V, I _D = 1.0 A		9.0	15	nC

SWITCHING CHARACTERISTICS (Note 4)

Turn-On Delay Time	t _{d(ON)}	V _{GS} = 4.5 V, V _{DD} = 40 V, I _D = 1.0 A, R _G = 27 Ω		21	35	ns
Rise Time	t _r			62	105	
Turn-Off Delay Time	t _{d(OFF)}			52	85	
Fall Time	t _f			50	85	
Turn-On Delay Time	t _{d(ON)}	V _{GS} = 10 V, V _{DD} = 40 V, I _D = 2.5 A, R _G = 47 Ω		15		ns
Rise Time	t _r			95		
Turn-Off Delay Time	t _{d(OFF)}			50		
Fall Time	t _f			105		

BODY - DRAIN DIODE RATINGS (Note 3)

Forward Diode Voltage	V _{SD}	V _{GS} = 0 V I _D = 1.0 A	T _J = 25°C	0.8	1.0	V
			T _J = 150°C	0.6		
Reverse Recovery Time	t _{RR}	V _{GS} = 0 V, dI _S /dI _T = 100 A/μs, I _S = 1.0 A		44		ns
Charge Time	T _a			21		
Discharge Time	T _b			23		
Reverse Recovery Time	Q _{RR}			43	86	

3. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%.
4. Switching characteristics are independent of operating junction temperatures.

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TYPICAL ELECTRICAL CHARACTERISTICS

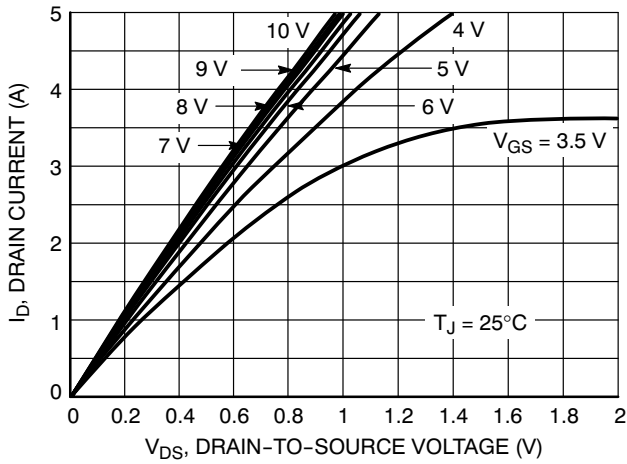


Figure 1. On-Region Characteristics

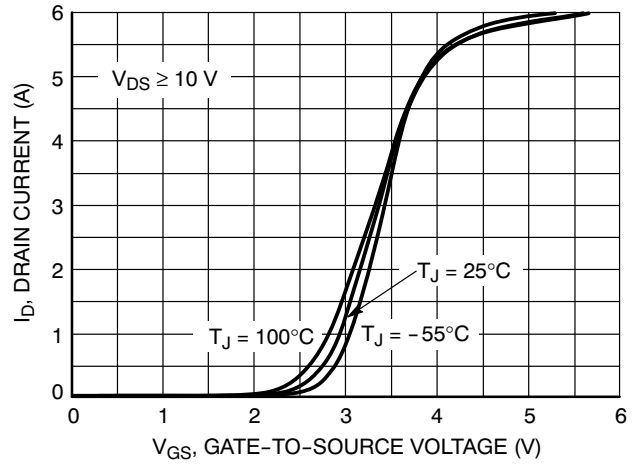


Figure 2. Transfer Characteristics

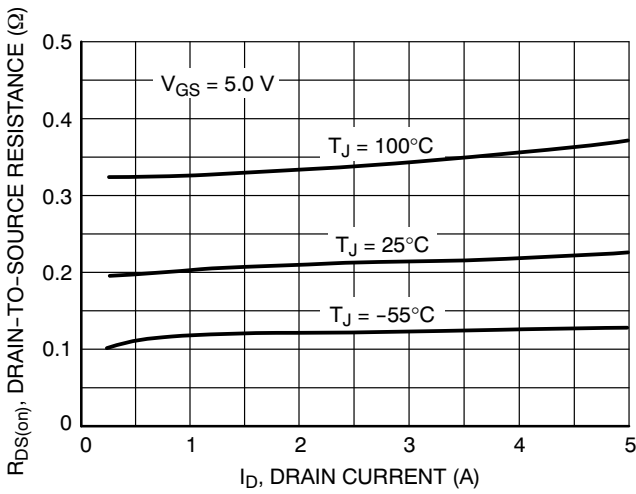


Figure 3. On-Resistance versus Drain Current and Temperature

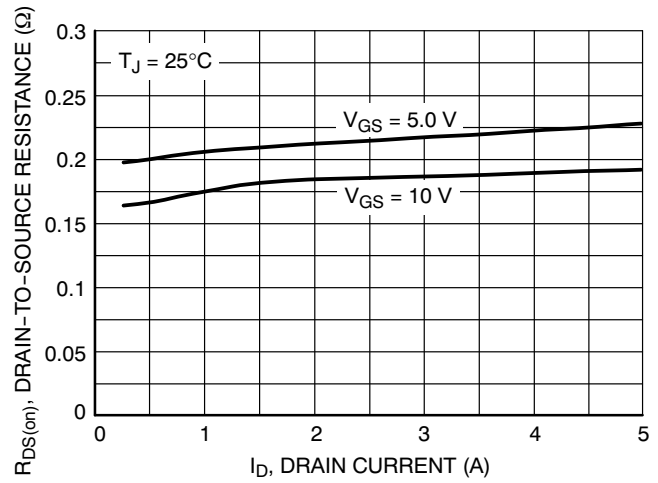


Figure 4. On-Resistance versus Drain Current and Gate Voltage

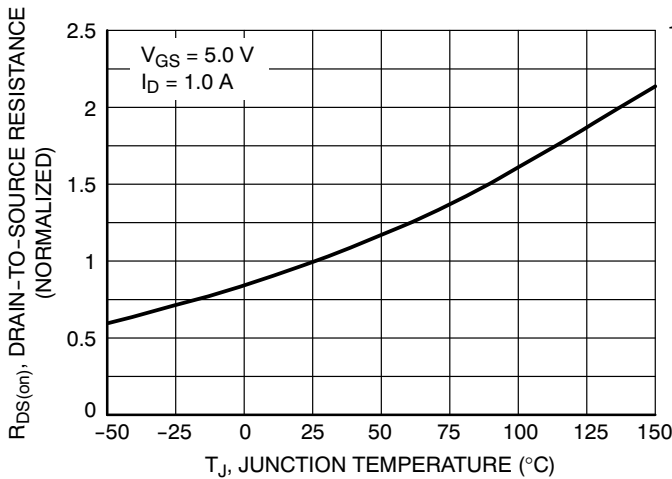


Figure 5. On-Resistance Variation with Temperature

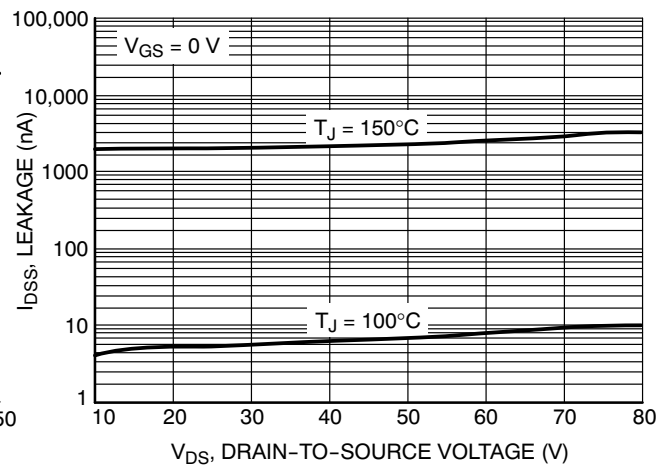


Figure 6. Drain-To-Source Leakage Current versus Voltage

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TYPICAL ELECTRICAL CHARACTERISTICS

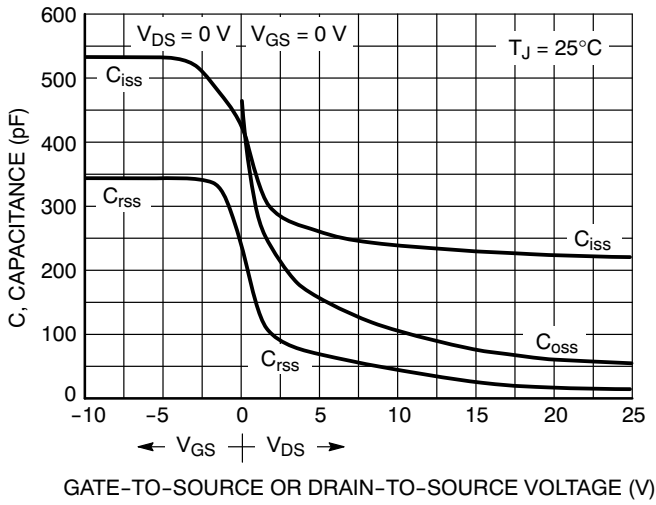


Figure 7. Capacitance Variation

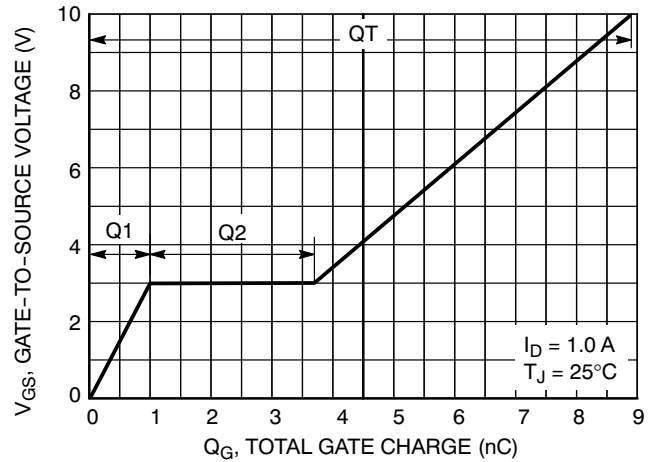


Figure 8. Gate-To-Source and Drain-To-Source Voltage versus Total Charge

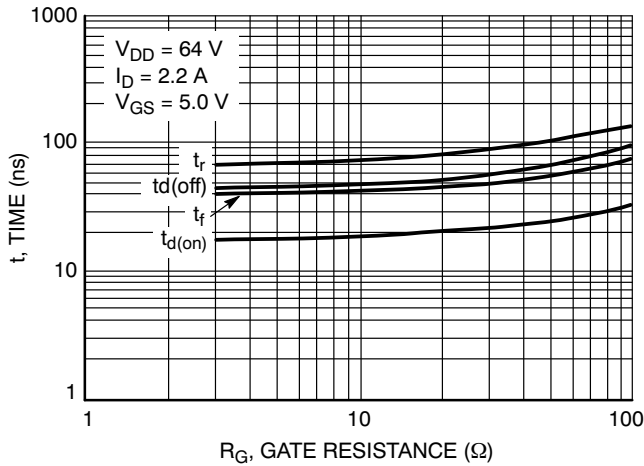


Figure 9. Resistive Switching Time Variation versus Gate Resistance

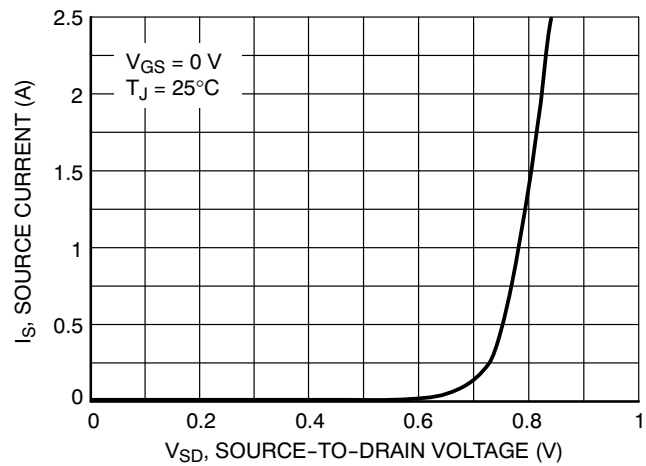


Figure 10. Diode Forward Voltage versus Current

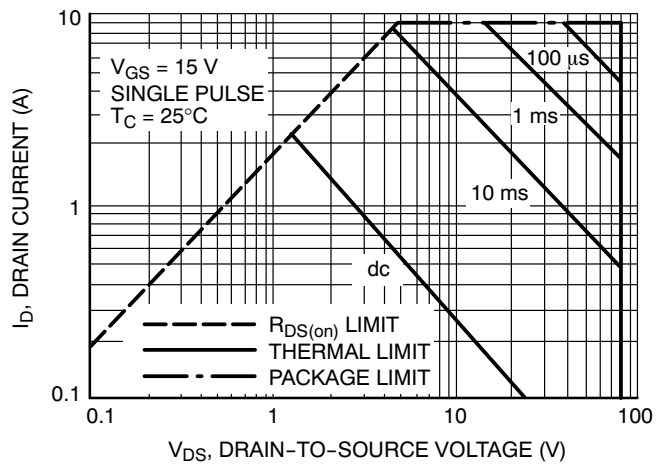


Figure 11. Maximum Rated Forward Biased Safe Operating Area

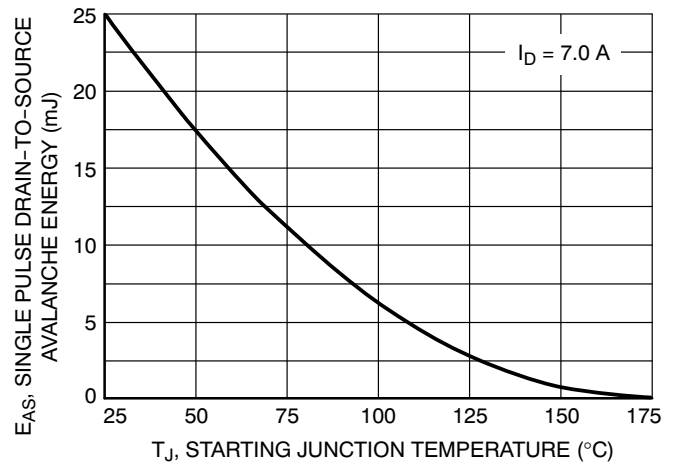


Figure 12. Maximum Avalanche Energy versus Starting Junction Temperature

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TYPICAL ELECTRICAL CHARACTERISTICS

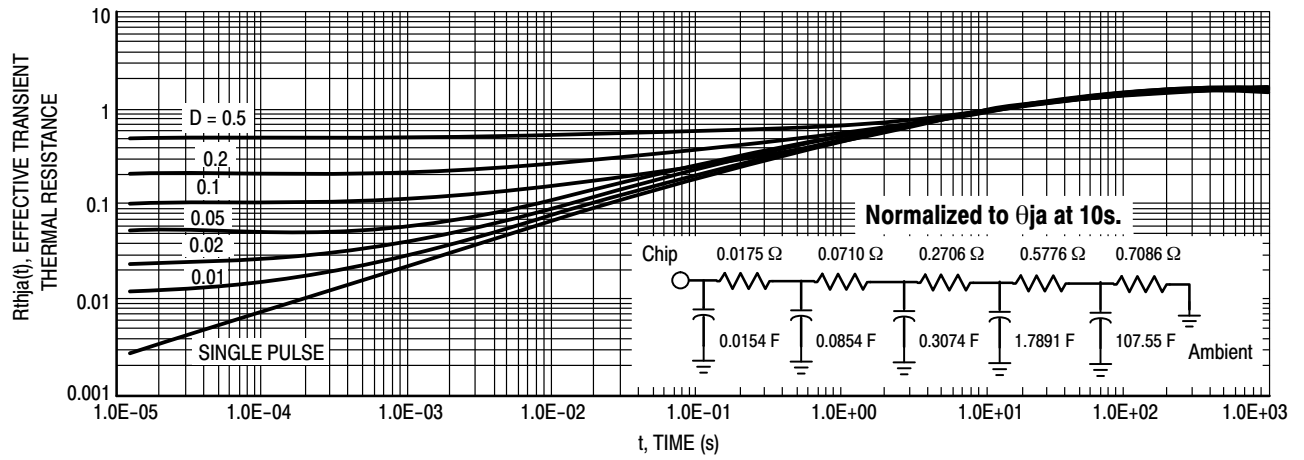


Figure 13. Thermal Response

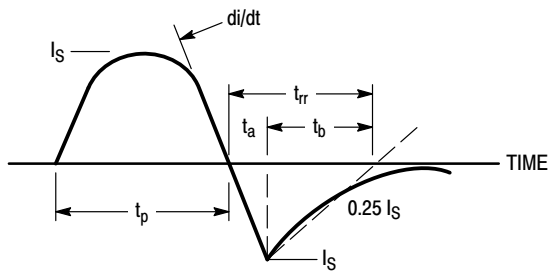
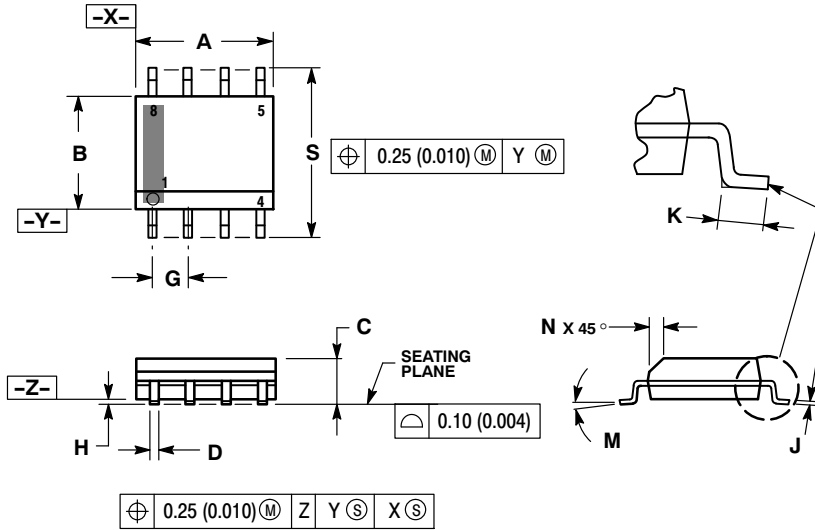


Figure 14. Diode Reverse Recovery Waveform

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PACKAGE DIMENSIONS

SO-8 NB
CASE 751-07
ISSUE AJ

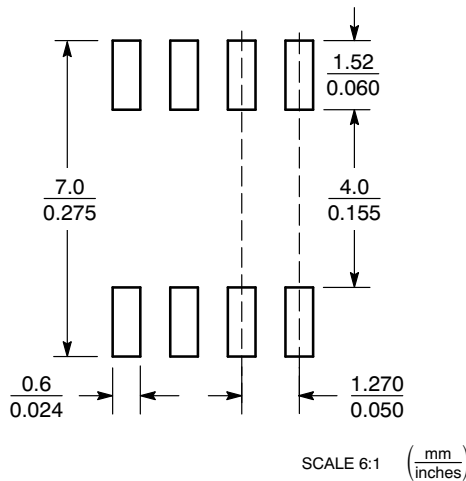


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

STYLE 11:

1. SOURCE 1
2. GATE 1
3. SOURCE 2
4. GATE 2
5. DRAIN 2
6. DRAIN 2
7. DRAIN 1
8. DRAIN 1

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