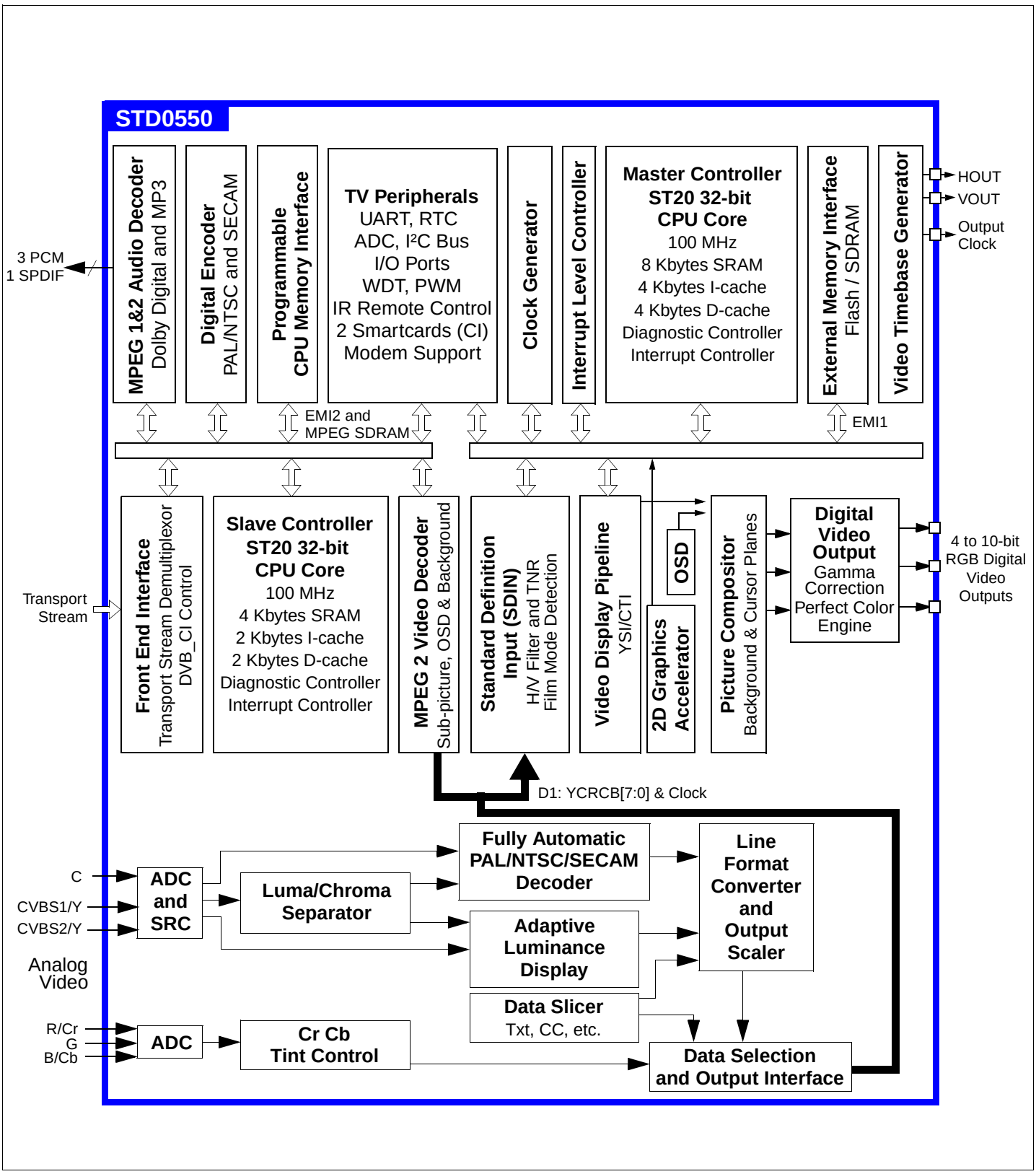
STD0550

Matrix Display Digital TV Processor

PRELIMINARY SPECIFICATION

- **Fully-programmable Digital Video Output Stage for direct RGB interface to Flat Display Panel with 4- to 10-bit color resolution and pixel resolution from VGA (640 x 480) to WXGA (1366 x 768) including HDV2.**
- **Versatile Integrated Up-Converter**
  - 50/60-Hz Progressive output with Line-Interpolation (A + A*), Field-Merging (A + B) or with Motion-adaptive De-interlacing based on median f(A, B)
  - Advanced Still Picture modes: AA*AA* and ABAB interlaced or AAAA non-interlaced
  - Automatic Movie mode detection and scanning
- **2 Embedded 32-bit ST20 CPU Cores**
  - Master CPU: 32-bit, 100 MHz, 4 Kbyte Instruction Cache, 4 Kbyte Data Cache and 8 Kbyte SRAM
  - Slave CPU: 32-bit, 100 MHz, 2 Kbyte Instruction Cache, 2 Kbyte Data Cache and 4 Kbyte SRAM
- **Programmable CPU Memory Interfaces for SDRAM, ROM or other peripherals**
- **MPEG SDRAM Memory Interface**
  - 2 x 16 Mbit or 1 x 64 Mbit or 1 x 128 Mbit SDRAM
  - Up to 133 MHz SDRAM
- **Hardware Transport Stream Demultiplexor**
  - Parallel/Serial Input
  - DVB Descramblers
  - 32 PID support
  - Support for 2-slot DVB_CI Interface
- **Digital Audio Decoder**
  - MPEG-1 and MPEG-2 Multi-channel Decoding
  - MP3 Decoding
  - Dolby Digital® (2.0 and 5.1)
  - 3 x 2-channel PCM Outputs (I2S)
  - IEC60958/IEC61937 Digital Output (S/PDIF)
- **Digital Video Decoder**
  - Supports MPEG-2 MP@ML
  - Fully-programmable Zoom-in and Zoom-out
- **Multi-Standard Video Encoder for Digital Sources**
  - CVBS, Y/C, RGB and YUV outputs with 10-bit DACs running at 27 MHz
  - PAL/NTSC/SECAM Encoding
  - Programmable Luma and Chroma bandwidths
  - Macrovision® 7.1
- **Analog-to-Digital Video Multistandard Decoder**
  - Automatic NTSC/PAL/SECAM Digital Chroma Decoder
  - VBI Data Slicer for Teletext, Closed Caption, WSS and other systems
  - NTSC/PAL Adaptive 4H/2D Comb Filter
  - Analog RGB/Fast Blanking Capture and Insertion in YCrCb Output Flow (SCART legacy)
  - Analog YCrCb inputs with Tint Control
  - Automatic Flesh Control on 117° or 123° Color Axis References
  - NTSC Hue Control
  - Line-locked ITU-R BT. 656/601 YCrCb Outputs (Data and Clock)
  - Orthogonal Correction on Output Pixels
  - ITU-R BT.601 Resolution for all Standards
  - Copy-Protection System compatible
- **Video Processing and Display**
  - 3D Temporal Noise Reduction with Comet-effect Correction
  - Scene-change Detector and histogram for Contrast Enhancer
  - Letterbox Format Detection
  - Letterbox and 4:3 to 16:9 format conversion with programmable 5-segment Panoramic mode
  - Picture Structure Improvement including Color Transition Improvement, Luma Peaking/Coring and Luma Contrast Enhancer
  - H/V format conversion with Zoom In/Out (4x to 1/8x) with H/V decimation
  - Very flexible Sync Generator for Master and Slave modes by Vsync and Hsync signals with Line-locked Pixel Clock
  - Mosaic mode with up to 16 pictures displayed
  - Freeze mode
- **High-Performance 8-bit Bitmap OSD Generator**
  - Pixel-based resolution with 10-bit RGB outputs
  - Programmable Resolution up to 1920x1024, all standard displays are supported:
    - Teletext 1.5 (480x520) and 2.5 (672x520)
    - Double-page Teletext (960x520) with Picture-and-Text
    - TeleWeb (640x480)
  - 4 graphic planes with full alpha-blending capabilities:
    - 24-bit Background Plane
    - 10-bit RGB Video Plane
    - Bitmap OSD Plane with Color Map
    - Up to 128 x 128 pixel Cursor Plane
  - 5th still picture plane available in MPEG video decoder OSD, used for MHP or MHEG-5 applications.
  - 2D Graphics Accelerator
- **Peripherals and I/Os for TV Chassis Control:**
  - 74 fully-programmable I/Os and 4 external interrupts
  - 8-bit programmable PWM with 4 inputs/outputs
  - Infrared Digital Preprocessor
  - Real Time Clock and Watchdog Timer
  - 4 16-bit standard timers
  - 10-bit ADC with 6 inputs and wake-up capability
  - 2 Master/Slave I²C Bus Interfaces and UART
  - 2 Smartcard interfaces and Clock Generators
  - Modem support
- **Teletext 1.5 and 2.5, Closed-Caption, VPS and WSS VBI Data Decoding, TeleWeb Compliant**
- **MHP Enhanced Profile and MHEG-5 compliant**
- **Embedded Emulation Resources with In-Situ Flash Programming Capabilities**
- **Professional Toolset Support**
  - Visual Debugger
  - ANSI C Compiler and Libraries
- **1.8V and 3.3V Power supplies**
- **Eco Standby and Low Power modes**
- **27-MHz Crystal Oscillator and VCXO for MPEG decoder**
- **Typical Power Consumption: 2.9 Watts**
- **35x35, 532+36 balls PBGA Package**


STD0550
MPEG 1&2 Audio Decoder
Dolby Digital and MP3
Digital Encoder
PAL/NTSC and SECAM
Programmable CPU Memory Interface
TV Peripherals
UART, RTC
ADC, I²C Bus
I/O Ports
WDT, PWM
IR Remote Control
2 Smartcards (CI)
Modem Support
Clock Generator
Interrupt Level Controller
Master Controller
ST20 32-bit
CPU Core
100 MHz
8 Kbytes SRAM
4 Kbytes I-cache
4 Kbytes D-cache
Diagnostic Controller
Interrupt Controller
External Memory Interface
Flash / SDRAM
Video Timebase Generator
HOUT
VOUT
Output Clock
3 PCM
1 SPDIF
EMI2 and MPEG SDRAM
EMI1
Front End Interface
Transport Stream Demultiplexor
DVB_CI Control
Slave Controller
ST20 32-bit
CPU Core
100 MHz
4 Kbytes SRAM
2 Kbytes I-cache
2 Kbytes D-cache
Diagnostic Controller
Interrupt Controller
MPEG 2 Video Decoder
Sub-picture, OSD & Background
Standard Definition Input (SDIN)
H/V Filter and TNR
Film Mode Detection
Video Display Pipeline
YSI/CTI
OSD
2D Graphics Accelerator
Picture Compositor
Background & Cursor Planes
Digital Video Output
Gamma Correction
Perfect Color Engine
4 to 10-bit RGB Digital Video Outputs
Transport Stream
D1: YCRCB[7:0] & Clock
C
CVBS1/Y
CVBS2/Y
Analog Video
ADC and SRC
Luma/Chroma Separator
Fully Automatic PAL/NTSC/SECAM Decoder
Adaptive Luminance Display
Data Slicer
Txt, CC, etc.
Line Format Converter and Output Scaler
R/Cr
G
B/Cb
ADC
Cr Cb Tint Control
Data Selection and Output Interface

1 General Description

1.1 Introduction

The STD0550 is dedicated to iDTV, LCD and Matrix Display. Combined with an external audio processor STV82x7, it provides cost effective high performance solution for LCD-iDTV applications with resolution from VGA (640 x 480) up to WXGA (1366 x 768).

It includes an MPEG decoder system, with its slave controller. The Transport stream is demultiplexed and demodulated. The front end interface supports a 2 slot DVB-CI interface.

The MPEG slave controller is a ST20, 32 bit CPU, it can access memory via the programmable CPU interface (or EMI) or the shared memory interface (SMI or MPEG SDRAM interface) which is shared with the video, audio and MPEG graphics.

PAL/SECAM/NTSC Analog video is demodulated and converted into digital video (4:2:2 YCrCb).

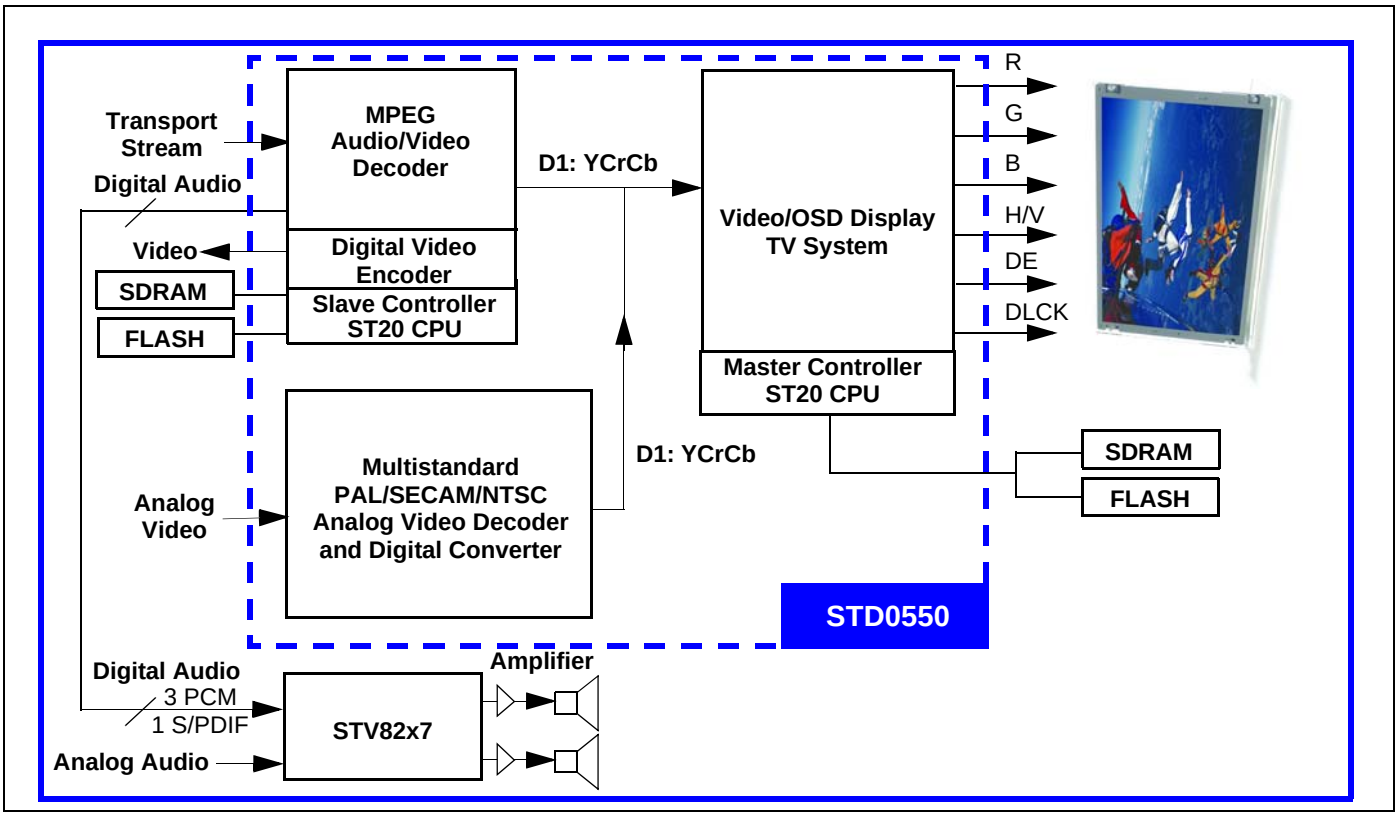
Digital video (from a digital or analog source) is sent to the Video display/TV system. Digital audio is sent to the external Audio processor.

The video display/TV system is controlled by a Master 32 bit ST20 CPU. The video display system includes field or line-up converter to support progressive display and all peripherals required for controlling the TV chassis. Teletext data is extracted from the incoming stream and decoded by the master CPU. An embedded On-Screen Display (OSD) generator delivers text and graphics. A video display pipeline performs feature box image processing such as picture improvement, horizontal and vertical rescaling and Temporal Noise Reduction.

The Master CPU system operates with an external SDRAM that is used for the field-rate up-conversion, text and graphic generation.The external SDRAM can be configured as a single bank of 16/64/128 Mb (16-bit configuration) or a dual bank of 16 to 256 Mb (32-bit configuration).

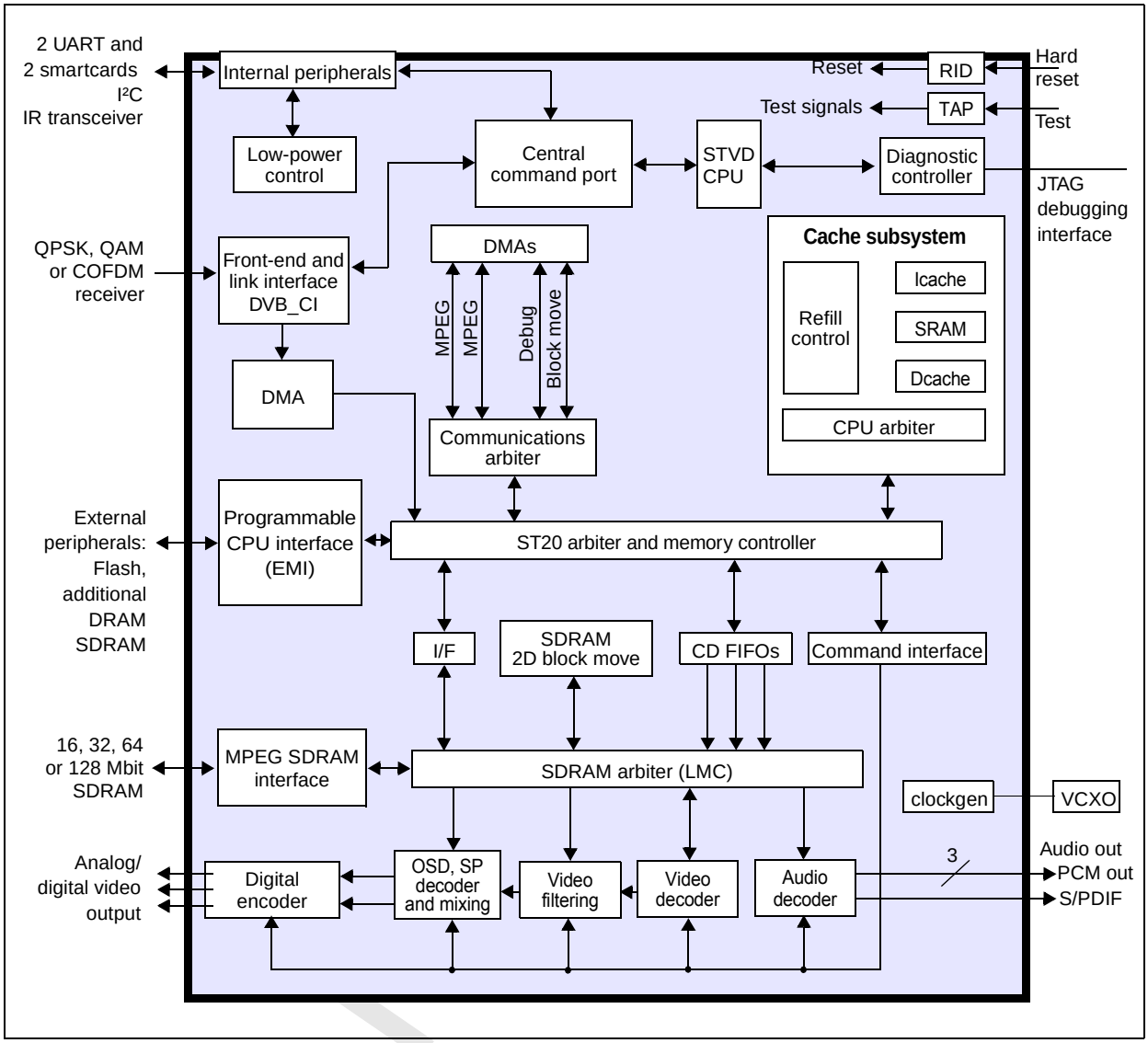
Application program codes are stored in an external Flash Memory and executed from the SDRAM.

Figure 1: STD0550 Block Diagram



1.2 MPEG Video/Audio Decoder System

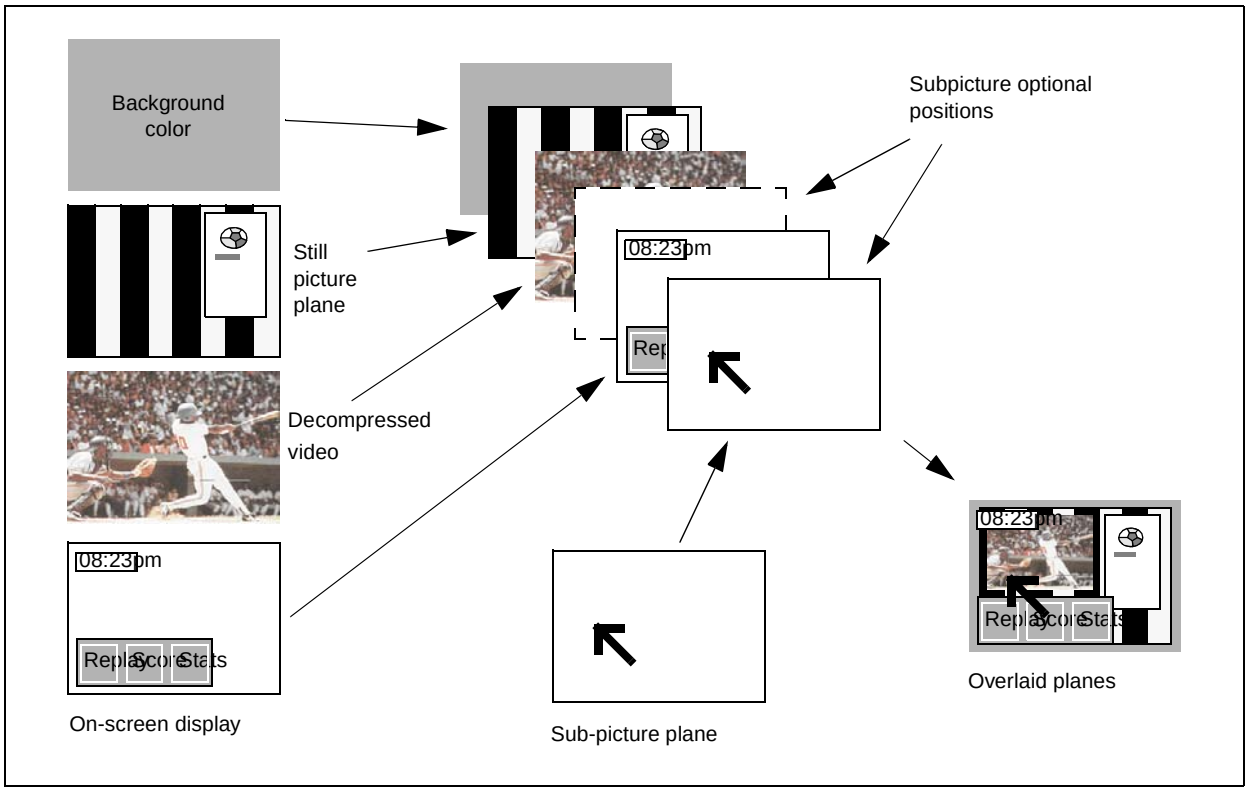
Figure 2: Functional block diagram



1.2.1 MPEG Video Decoder

This is a real-time video compression processor supporting the MPEG-1 and MPEG-2 standards at video rates up to 720 x 480 x 60 Hz and 720 x 576 x 50 Hz. Picture format conversion for display is performed by vertical and horizontal filters. The MPEG video decoder includes a display unit with five display planes as shown in the figure below. The display planes are normally overlaid in the order illustrated, with the background color at the back and the sub-picture at the front (used as a cursor plane). The sub-picture plane can alternatively be positioned between the OSD and MPEG video planes where it can be used as a second on-screen display plane. The MPEG display unit is used for MHP or MHEG-5 applications.

Figure 3: MPEG display planes



1.2.2 Digital Audio Decoder

The audio decoder supports the decoding of the following formats: Dolby Digital, MPEG-1 layers I, II and III (MP3), MPEG-2 layer II 6 channels, PCMmultichannel linear PCM (LPCM).

S/PDIF input data (IEC-60958 or IEC-61937 standards) is accepted if an external circuitry extracts the PCM clock from the stream.

Skip frame, repeat blocks and soft mute frame features can be used to synchronize audio and video data. PTS audio extraction is also supported.

The device outputs up to 6 channels of PCM data and appropriate clocks for external digital-to-analog converters.

Programmable downmix enables 1, 2 or 3 channel outputs. Data can be output in either I²S format or Sony format. The decoder can format output data according to IEC-60958 standard (for non compressed data: L/R channels, 16, 18, 20 and 24-bits) or IEC-61937 standard (for compressed data), for F_S = 48 kHz, 44.1 kHz or 32 kHz.

Sampling frequencies of 48 kHz, 44.1 kHz, 32 kHz and half sampling frequencies are supported. A downsampling filter (48 kHz) is available.

The decoder supports dual mode for MPEG and Dolby Digital.

In global mute mode, the incoming bit-stream is decoded normally but the PCM and S/PDIF outputs are soft-muted. This mode is used to prepare a period of the decoding mode, in order to synchronize audio and video data without hearing the audio.

Analog Audio Sources are demodulated using external IC STV82x7. Demodulated digital audio is sent to STV82x7 which also includes Audio processing: virtualizers (SRS TruSurround XT which is Virtual Dolby Digital and Virtual Dolby Surround compliant) and sound enhancements (spatial effects, bass enhancements, dialog enhancement).

1.2.3 Modem analog front-end interface

The modem analog front-end interface is used to transfer transmit and receive DAC and ADC samples between the memory and an external modem analog front-end (MAFE), using a synchronous serial protocol. DMA is used to transfer the sample data between memory buffers and the MAFE interface module, with separate transmit and receive buffers and double buffering of the buffer pointers. FIFOs are used to take into account the access latency to memory, in a worst case system and to allow the use of bursts for memory bandwidth efficiency improvement.

V22bis is supported by software.

1.2.4 Slave CPU Memory subsystem

On-chip

The on-chip memory includes 2 Kbytes of instruction cache, 2 Kbytes of data cache and 4 Kbytes of SRAM. The subsystem provides 240 Mbytes of internal bandwidth, supporting pipelined 2-cycle internal memory access.

The instruction and data caches are direct-mapped, with a write-back system for the data-cache. The caches support burst accesses to the external memories for refill and write-back.

Off-chip

There are two off-chip memory interfaces:

- MPEG memory interface controls the movement of data between the STD0550 and 16, 32, 64 or 128 Mbits of SDRAM. This external SDRAM stores the display data generated by the MPEG decoder and the slave CPU working data.
- The external memory interface (EMI2) accessed by the slave CPU is used for the transfer of data and programs between the STD0550 and external peripherals, flash and additional SDRAM.

The EMI uses minimal external support logic for the memory subsystems. It accesses a 32-Mbyte physical address space (greater if SDRAM is used) in four general purpose memory banks of 8 or 16 bits wide, 21 or 22 address lines, and byte select. For applications requiring extra memory, the EMI supports this extra memory with zero external support logic, even for 16-bit SDRAM devices. The EMI can be configured for a wide variety of timing and decode functions by the configuration registers. The timing of each of the four memory banks can be set separately, with different device types being placed in each bank with no need for external hardware.

1.2.5 Serial communication

Asynchronous serial controllers

The asynchronous serial controller (ASC), also referred to as the UART interface, provides serial communication between the STD0550 and other microcontrollers, microprocessors or external peripherals. The STD0550 has three ASCs available for applications. An additional UART interface is used for the communication between the master CPU and the slave CPU.

Eight or nine bit data transfer, parity generation, and the number of stop bits are programmable. Parity, framing, and overrun error detection increase data transfer reliability. Transmission and reception of data can be double-buffered, or 16-deep FIFOs can be used. A mechanism to distinguish the address from the data bytes is included for multiprocessor communication. Testing is supported by a loop-back option. A 16-bit baud-rate generator provides the ASC with a separate serial clock signal.

Two ASCs support full-duplex and 2 half-duplex asynchronous communication, where both the transmitter and the receiver use the same data frame format and the same baud rate. Each ASC can be set to operate in smartcard mode for use when interfacing to a smartcard.

Synchronous serial control

The two synchronous serial controllers (SSCs) provide high-speed interface to a wide variety of serial memories, remote control receivers and other microcontrollers. They support some features of the serial peripheral interface bus (SPI) and the I^2C bus. The SSCs can be programmed to interface to other serial bus standards. They share pins with the parallel input/output (PIO) ports, and support half-duplex synchronous communication. One SSC supports full-duplex synchronous communication.

1.2.6 Hardware transport stream demultiplexer interface

The STD0550 can be connected to a front-end through the following interfaces:

- transport stream serial interface,
- transport stream parallel interface.

The PIO pins can be tri-stated under software control to support low cost DVB-CI implementations and similar module interfaces.

1.2.7 On-chip PLL

There are three on-chip frequency synthesizers and one PLL, accepting 27 or 54 MHz input, which generate all the internal high-frequency clocks needed for the slave CPU, MPEG and audio subsystems.

1.2.8 Diagnostic controller (DCU)

The ST20 diagnostic controller unit (DCU) is used to boot the CPU and to control and monitor the chip systems via the standard IEEE 1194.1 test access port. The DCU includes on-chip hardware with ICE (in-circuit emulation) and LSA (logic state analyzer) features to facilitate verification and debugging of software running on the on-chip CPU in real time. It is an independent hardware module with a private link from the host to support real-time diagnostics. The slave CPU and master CPU each have their own DCU.

1.2.9 Interrupt subsystem, Slave CPU

The interrupt system allows an on-chip module or external interrupt pin to interrupt an active process so that an interrupt handling process can be run. An interrupt can be signalled by one of the following: a signal on an external interrupt pin, a signal from an internal peripheral or subsystem, software asserting an interrupt in the pending register.

Interrupts are implemented by an on-chip interrupt controller and an on-chip interrupt-level controller. The interrupt controller supports eight prioritized interrupts as inputs and manages the pending interrupts. This allows the nesting of preemptive interrupts for real-time system design. Each interrupt can be programmed to be at a lower or higher priority than the high priority process queue.

1.2.10 PAL/NTSC/SECAM encoder

The integrated digital encoder converts a multiplexed 4:2:2 or 4:4:4 YCbCr stream into a standard analog baseband PAL/NTSC or SECAM signal and into RGB, YUV, YC and CVBS components. The encoder can perform closed-caption, CGMS encoding, and allows Macrovision^{TM} 7.1 copy protection (option).

The digital encoder is able to encode Teletext according to the ***CCIR/ITU-R Broadcast Teletext System B*** specification, also known as World System Teletext.

In DVB applications, Teletext data is embedded within DVB streams as MPEG data packets. It is the responsibility of the software to handle incoming data packets and in particular to store Teletext packets in a buffer, which then passes them to the digital encoder on request.

The digital encoder also provides enhanced possibilities through programmable luma and chroma bandwidth.

1.2.11 Smartcard interfaces

Two smartcard interfaces support smartcards compliant with ISO7816-3. Each interface has a UART (ASC), a dedicated programmable clock generator, and eight bits of parallel IO port.

1.3 PAL/SECAM/NTSC Analog Video Decoder

The STD0550 includes a high-quality video front-end for processing all analog standards into a digitalized 4:2:2 YCrCb video format. It processes NTSC/PAL/SECAM CVBS signals, as well as conventional analog RGB or YCrCb signals.

The analog video decoder outputs demodulated chrominance, in-phased luminance and sliced data for the most common services such as Teletext, Closed Caption, WSS, etc.

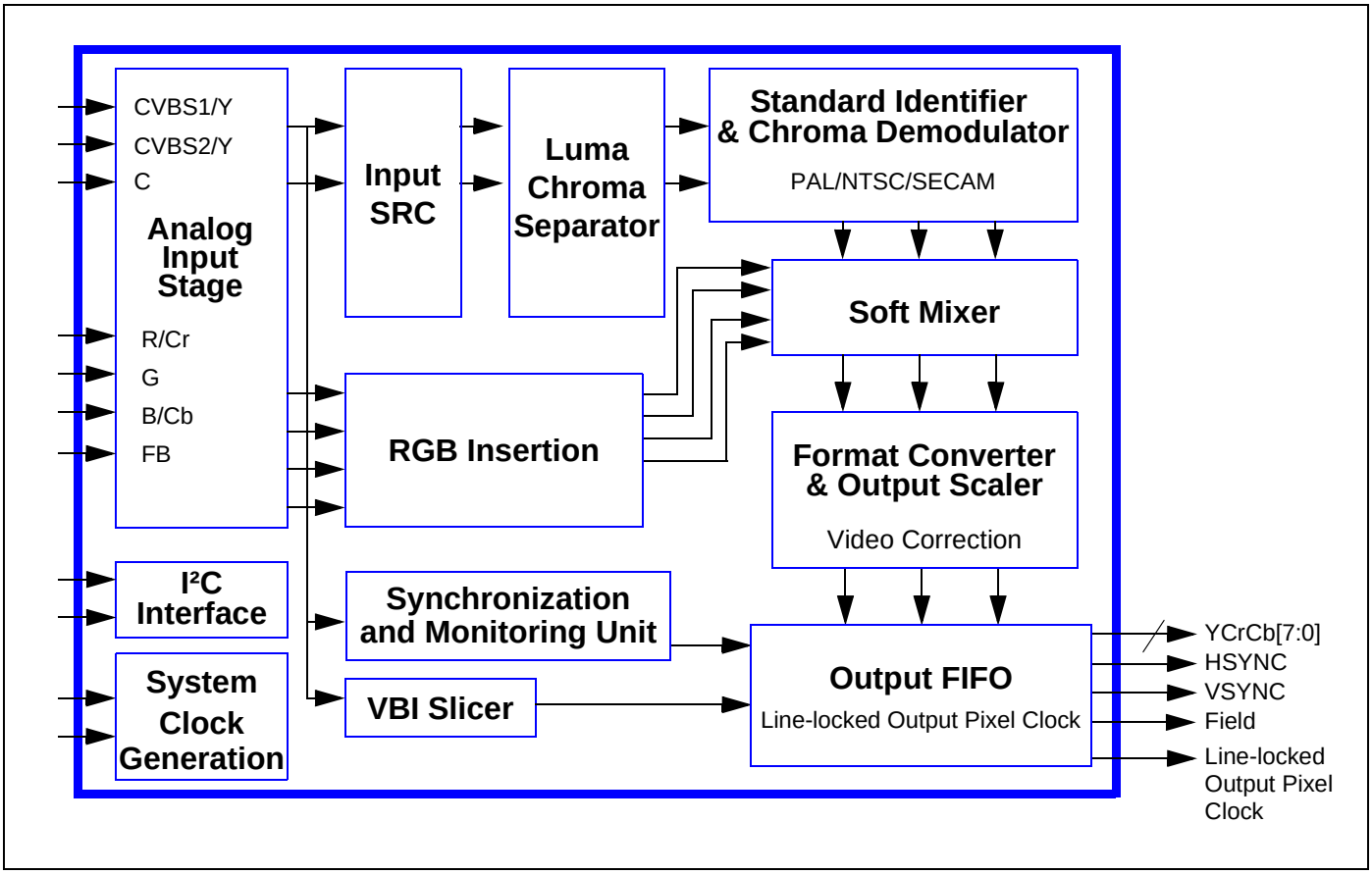
The analog video decoder does not need an external synchronization system. It extracts all necessary synchronization signals from CVBS or Y signals, and delivers the horizontal, vertical and frame signals either on dedicated pins or embedded into the digital bit stream.

It features automatic standard recognition and automatic selection of the optimal Y/C separation algorithm according to the standard and has extensive output scaling capabilities. The analog video decoder chip includes an analog RGB capture feature and programmable automatic mixing with the main picture digital output.

8-bit ITU-R BT.601/656 output standard is supported.

All sub-level blocks operate at the frequency used as a sampling frequency (f_S) for the five embedded A/D converters. This free-running clock is called the system clock (f_S) and is provided by an external clock generator from a video display/TV system.

Figure 4: Architectural Block Diagram



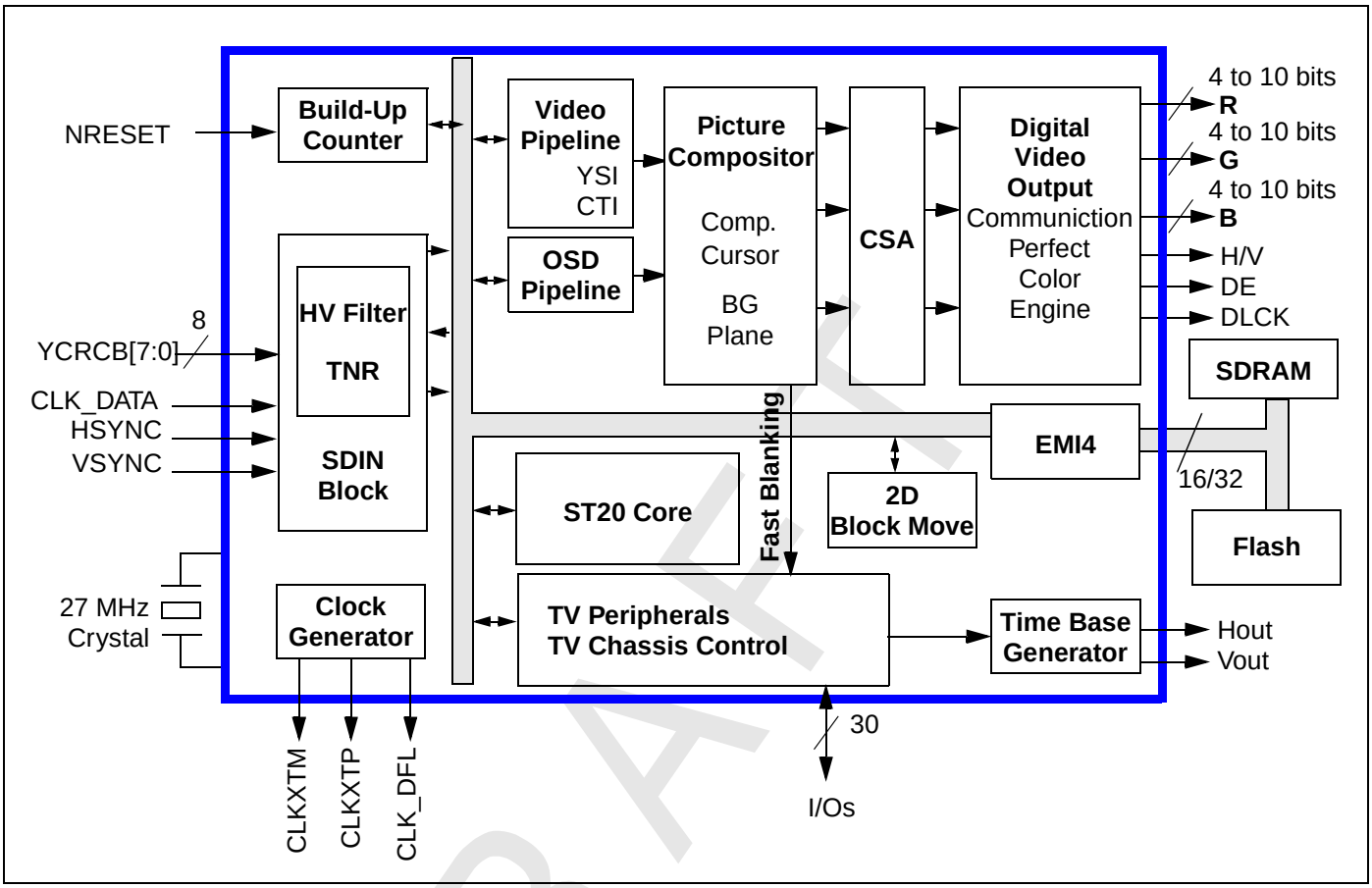
1.4 Video Display/TV System, Master CPU Controller

1.4.1 General Description

The STD0550 includes a 32-bit ST20 CPU core with all peripherals required for controlling the TV chassis. Teletext data is extracted from the incoming stream and decoded by the CPU. An embedded On-Screen Display (OSD) generator delivers the text and graphics. The Video Display Pipeline performs feature box image processing such as picture improvement, horizontal and vertical rescaling and Temporal Noise Reduction.

The video display/TV system operates with a single external SDRAM that is used for the field-rate up-conversion, text and graphic generations.The external SDRAM can be configured as a single bank of 16/64/128 Mb (16-bit configuration) or a dual bank of 16 to 256 Mb (32-bit configuration). Application program codes are stored in an external Flash memory and executed from the SDRAM.

Figure 5: Architectural Block Diagram



1.4.2 Deinterlacing Modes and Progressive Scan Output

The de-interlacing can be done in the following modes:

- Spatial line interpolation, using the high resolution vertical polyphase filter
- Motion adaptive spatial-temporal interpolation, using the median filter
- Field merging for film sources

The following table shows typical de-interlacing modes, according to the input format:

Table 1: De-interlacing and Scaling Modes

		INPUT						
	Panels & Output modes	**50 Hz interlaced Video**	**50 Hz interlaced movie**	**50 Hz n-interlaced game**	**60 Hz interlaced Video**	**60 Hz interlaced movie (3:2)**	**60 Hz interlaced movie (2:2)**	**60 Hz n-interlaced game**
OUTPUT	**VGA**	A+A*B*+B Or A+Med (A,B) Z out H 720>640 Z out V 576>480	A+B Z out H 720>640 Z out V 576>480	A+A*B*+B Or A+Med (A,B) Z out H 720>640 Z out V 576>480	A+A*B*+B Or A+Med (A,B) Z out H 720>640 Z out V 576>480	3:2pd Z out H 720>640 Z out V 576>480	A+B Z out H 720>640 Z out V 576>480	A+A*B*+B Or A+Med (A,B) Z out H 720>640 Z out V 576>480
	XGA	A+A*B*+B Or A+Med (A,B) Z in H 720>1024 Z in V 576>768	A+B Z in H 720>1024 Z in V 576>768	A+A*B*+B Or A+Med (A,B) Zin H 720>1024 Z in V 576>768	A+A*B*+B Or A+Med (A,B) Zin H 720>1024 Z in V 576>768	3:2pd Zin H 720>1024 Z in V 576>768	A+B Zin H 720>1024 Z in V 576>768	A+A*B*+B Or A+Med (A,B) Zin H720>1024 Z in V 576>768

Note: 720 pixels/line refers to ITU-R BT 601/656 video input standard resolution.

1.4.3 Regulation Modes

The regulation modes of the input and output dataflows are based on the configurations of several blocks such as the SDIN, VTG, Display, and also depends on the selected synchronization modes.

These regulation modes are then managed by a software layer that controls the various registers and includes algorithms to maintain the balance between the input and output dataflows. This service software layer allows various regulation modes as described below, selectable at the application level.

When the VTG block is set in Slave mode, the PLL that line-locks the clock pixel to the Hsync signal is used to regulate the input and output dataflows.

When the VTG block is set in Master mode, the following regulation modes are possible:

1. Frame Skip & Repeat Mode (used for Proscan mode)

   In this mode, depending on the speed variations between the input flow and the output flow, a frame is repeated or skipped from time to time (1 to 2 per second).

2. Field Skip & Repeat Mode (used for field rate up-conversion as 100 Hz)

   In this mode, depending on the speed variations between the input flow and the output flow, a field is repeated or skipped from time to time (1 to 2 per second).

3. Line Skip & Repeat Mode

   In this mode, certain lines are repeated or skipped during the VBI, depending on the delay between the input and output Vsync signals.

4. Pixel Skip & Repeat Mode

   In this mode; pixel periods are repeated or skipped during the horizontal or vertical blanking interval, depending on the delay between each Vsync signal.

5. Clock Modulation Mode

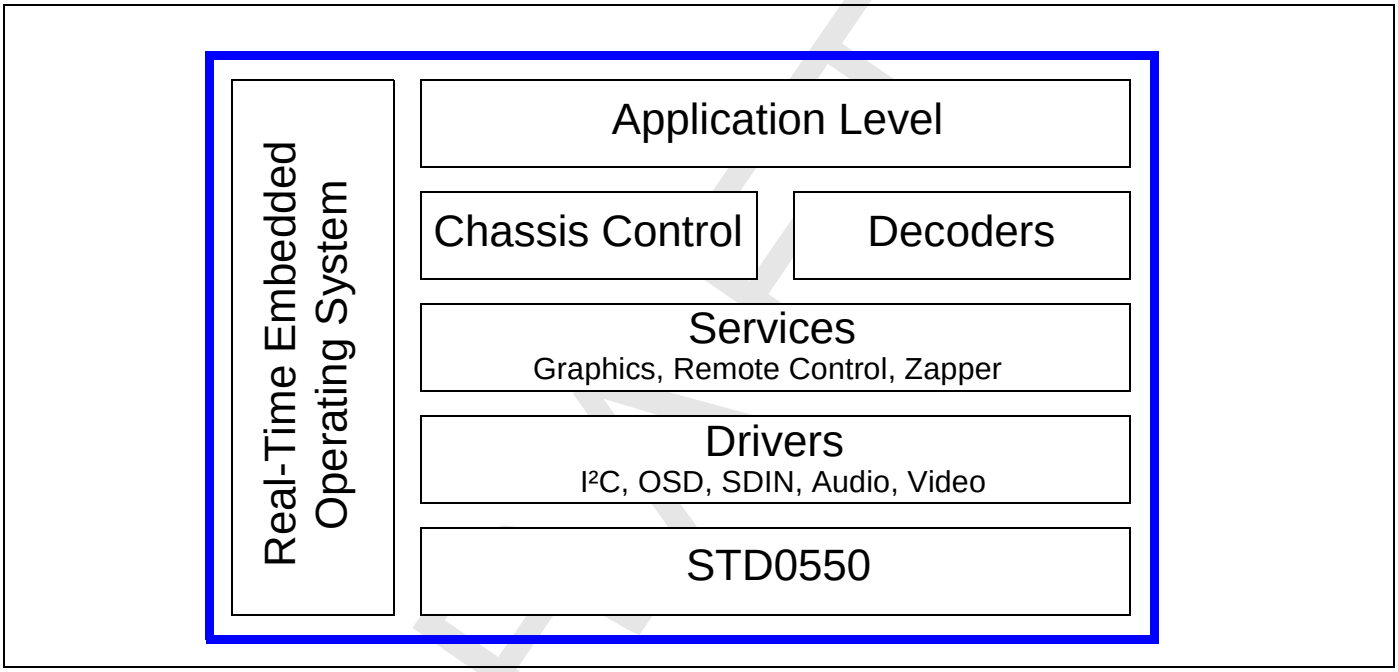
In this mode, the output pixel clock free-running frequency is fine-tuned, depending on the delay between the input and output Vsync signals. The PLL filtering is performed by software.

1.5 Software

The layering model adopted for the Software Stack is based on certain non-functional requirements:

- Re-usable
- Portable
- Modular
- Reliable and robust
- Readable and maintainable

Figure 6: Global Software Architecture

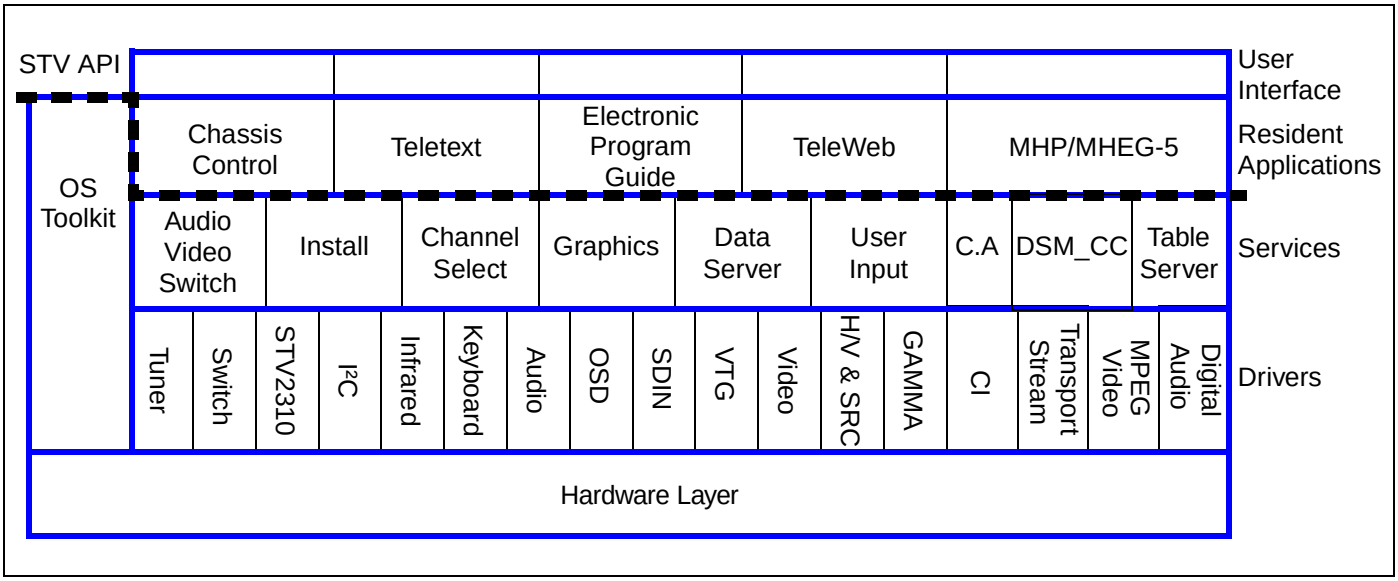


The application software consists of 4 main layers based on these non-functional requirements:

- System Layer provides certain general-purpose components such as Handle or Link List Managers. This layer also contains the Operating System Abstraction Layer (OSAL) components which enable other layers to be OS-independent.
- Driver Layer provides a hardware abstraction to the upper layers making them hardware-independent.
- Service Layer contains the components that provide the Application layer with high level interfaces in order to manage the TV set. The set of Service components included in the demonstration application are very useful for developing applications.

- Application Layer which contains the software that defines the “Look & Feel” of the TV set. This layer, for instance, contains the components that are responsible for the following features: interpretation of user inputs, display and navigation functions and Teletext applications.

Figure 7: Software Architecture Example



2 Ball Connections

Alternate functions printed in ***Italic*** show a suggested use of the PIO; alternate functions not printed in ***Italic*** are multiplexed with a specific hardware.

Table 2: Pins sorted by function

Ball	Ball Name	Main Function	Alternate Function		Type
			Input	Output	
Audio DAC (Digital Decoder)					
D24	DAC_SCLK	Oversampling clock		EXT_AUD_CLK	O
C26	DAC_PCMOUT0	PCM_OUT0		EXT_AUD_DATA	O
C25	DAC_PCMOUT1	PCM_OUT1	EXT_AUD_REQ		I/O
C24	DAC_PCMOUT2	PCM_OUT2			O
B26	DAC_PCMCLK	PCM_CLOCK			I/O
B25	DAC_LRCLK	Left/right clock		EXT_AUD_WCLK	O
A26	SPDIF_OUT	SPDIF_OUT			O
H22, J22	VDD_PCM	VDD frequency synthesizer: 1.8 V			PWR
D25	VSS_PCM	VSS frequency synthesizer: GND			PWR
Clock and Reset (Digital Decoder)					
P3	RESET	Chip reset			I
E19	VDD_PLL	VDD PLL = 1.8 V			PWR
P14	VSS_PLL	GND PLL = GND			PWR
N23	PIX _CLK	27MHz main clock			I
PIOs and Communication (Digital Decoder - Slave CPU)					
D3	PIO0[0]	PIO0[0]	UART0_DATA ***(SC0_DATA)***		I/O
Y2	PIO0[1]	PIO0[1]	TTX_IN_CLOCK		I/O
G1	PIO0[2]	PIO0[2]			I/O
V3	PIO0[3]	PIO0[3]		SC0_CLOCK	I/O
W3	PIO0[4]	PIO0[4]		SC0_RST	I/O
Y1	PIO0[5]	PIO0[5]		SC0_CMD_VCC	I/O
F1	PIO0[6]	PIO0[6]		SC0_DATA_DIR/ DVB_OE	I/O
G3	PIO0[7]	PIO0[7]	SC0_DETECT	DVB_IORD	I/O
U1	PIO1[0]	PIO1[0]	SSC0_DATA (MTSROUT/MRSTIN)		I/O
U2	PIO1[1]	PIO1[1]	SSC0_CLOCK		I/O
G4	PIO1[2]	PIO1[2]	SC external clock PARA_DVALID	DVB_IOWR	I/O
U3	PIO1[3]	PIO1[3]		UART2_TXD	I/O
T3	PIO1[4]	PIO1[4]	UART2_RXD		I/O
W2	PIO1[5]	PIO1[5]	PARA_SYNC	UART1_TXD	I/O
T1	TRIGGER_IN	Trigger in for DCU			I/O
G2	TRIGGER_OUT	Trigger out for DCU		DVB_WE	I/O
H3	PIO2[0]	PIO2[0]	UART3_DATA ***(SC1_DATA)***		I/O
				OSD_ACTIVE	O

Table 2: Pins sorted by function

Ball	Ball Name	Main Function	Alternate Function		Type
			Input	Output	
W1	PIO2[1]	PIO2[1]	UART1_RXD	MAFEIF_DOUT PARA_REQ	I/O
H4	PIO2[2]	PIO2[2]	PARA_STROBE	MAFEIF_HC1	I/O
H2	PIO2[3]	PIO2[3]		SC1_CLOCK	I/O
H1	PIO2[4]	PIO2[4]		SC1_RST	I/O
F4	PIO2[5]	PIO2[5]		SC1_CMD_VCC	I/O
F2	PIO2[6]	PIO2[6]		SC1_DATA_DIR	I/O
L25	PIO2[7]	PIO2[7]	SC1_DETECT/ CFC	YC_CLKOUT	I/O
K4	PIO3[0]	PIO3[0]	MAFEIF_SCLK PARA_DATA{0]		I/O
K2	PIO3[1]	PIO3[1]	MAFEIF_DIN PARA_DATA[1]		I/O
K1	PIO3[2]	PIO3[2]	MAFEIF_FSI PARA_DATA[2]		I/O
L3	PIO3[3]	PIO3[3]	CAPTURE_IN0 PARA_DATA[3]		I/O
L4	PIO3[4]	PIO3[4]	CAPTURE_IN1 PARA_DATA[4]	UART1 RTS (RTS1)	I/O
L2	PIO3[5]	PIO3[5]	CAPTURE_IN2 PARA_DATA[5]	UART2 RTS (RTS2)	I/O
L1	PIO3[6]	PIO3[6]	PARA_DATA[6] UART1 CTS (CTS1)	COMP_OUT1	I/O
M3	PIO3[7]	PIO3[7]	PARA_DATA[7] UART2 CTS (CTS2)	COMP_OUT0	I/O
E25, F23, F24, H23, H24, H25, K23, K25					
	PIO4[0:7]	PIO4[0:7]		YC[0:7]/NCO[0:7]	I/O
V1	PIO5[0]	PIO5[0]	B_WCLK		I/O
			SSC1_DATA		
V2	PIO5[1]	PIO5[1]	B_V4		I/O
			SSC1_CLOCK		
J3	PIO5[2]	PIO5[2]	IRB_IR input		I/O
M25	PIO5[3][1]	PIO5[3]	IRB_UHF input		I/O
M26	PIO5[4]	PIO5[4]		IRB_drivePPMsignal	I/O
N26	PIO5[5]	PIO5[5]		IRB_drive0orZ[1] (jack)	I/O
			OSC_IN_CLK		
Auxiliary Clock (Digital Decoder)					
T2	AUXCLK	Auxiliary clock			O

Table 2: Pins sorted by function

Ball	Ball Name	Main Function	Alternate Function		Type
			Input	Output	
EMI Interface (Digital Decoder - Slave CPU)					
C13, D13, B13, A13, C8, A7, B7, D7, C7, A6					
	CPU_ADR[1:10]	ADR[1:10]			O
B12, B6, D6, C3, C12, D12, A1, D1, D2, C2, C1					
	CPU_ADR[11:21]	ADR[11:21]			O
D10, C10, A9, B9, D9, C9, A8, B8					
	CPU_DATA[0:7]	DATA[0:7]			I/O
D5, C5, B2, A2, A3, C4, B4, A4					
	CPU_DATA[8:15]	DATA[8:15]			I/O
F3	CPU_RAS1	DRAM RAS		NOT_SDRAM_CS 1/ CHIPSEL. BANK3	I/O
E1	CPU_WAIT	Wait state			I
C11	CPU_RW	Read not write		NOT_SDRAM_WE	O
A10	CPU_BE[0]	Byte 0 enable		DQM[0]	O
B5	CPU_BE[1]	Byte 1 enable		DQM[1]	O
D11	CPU_CAS0	DRAM CAS0		SDRAM_CAS/ CPU_ADR[22]	O
A11	CPU_CAS1	DRAM		NOT_SDRAM_CS 0	O
B11	CPU_CE[0]	DRAM_RAS0		SDRAM_RAS/ NOTCHIPSELBAN K0	O
E4	CPU_CE[1]	Chip select bank 1			O
E2	CPU_CE[2]	Chip select bank 2			O
E3	CPU_CE[3]	Chip select bank 3		CS_SUB_BANK3	O
A5	CPU_PROCLK	EMI clock			O
B1	CPU_OE	Output enable			I/O
Interrupt (Digital Decoder - Slave CPU)					
J2	IRQ[0]	IRQ[0] ***(SERVO_IRQ)***			I
J1	IRQ[1]	IRQ[1]			I
K3	IRQ[2]	IRQ[2] ***(MD_IRQ)***			I
Timers					
M24	PWM0	Pulse width modula 0	HSYNC		O
L23	PWM1	Pulse width modula 1	BOOTFROMRO M[2]		O
M23	PWM2	Pulse width modula 2	VSYNC/ODDEVEN		O
JTAG (Digital Decoder - Slave CPU)					
R4	TCK	Test clock			I
R2	TDI	Test data in			I
R1	TDO	Test data out			O
R3	TMS	Test mode select			I
P4	TRST[2]	Test reset			I
Front-end (Digital Decoder)					
M4	B_DATA	I²S data	FEC_DATA		I

Table 2: Pins sorted by function

Ball	Ball Name	Main Function	Alternate Function		Type
			Input	Output	
M2	B_BCLK	I²S bit clock	FEC_B_CLK		I
M1	B_FLAG	I²S error flag	FEC_P_CLK		I
N3	B_SYNC	I²S sector/ABS time	FEC_ERROR		I
Video DAC (Digital Decoder)					
T26	R_OUT	R_OUT			O
T25	G_OUT	G_OUT			O
T23	B_OUT	B_OUT			O
R25	Y_OUT	Y_OUT			O
R26	C_OUT	C_OUT			O
P24	CV_OUT	CV_OUT			O
R23	I_REF_RGB	RGB DAC ref. current			I
R24	V_REF_RGB	RGB DAC ref. voltage			I
P25	I_REF_YCC	YCC DAC ref. current			I
P23	V_REF_YCC	YCC DAC ref. voltage			I
K22	VDD_RGB	VDDA_RGB: 3.3 V			PWR
P26	VSS_RGB	VSSA_RGB: GND			PWR
L22	VDD_YCC	VDDA_YCC: 3.3 V			PWR
M13	VSS_YCC	VSSA_YCC: GND			PWR
Shared Memory Interface (Digital Decoder)					
C23, A24, B24, A25					
	SMI_ADR[0:3]	Address bus SDRAM			O
C18, D18, B18, D17, A18, B17					
	SMI_ADR[4:9]	Address bus SDRAM			O
B23, A17, C22, A23					
	SMI_ADR [10:13]	Address bus SDRAM			O
A22, C21, D21, B21, A21, C20, D20, B20, B14, D14, C14, B15, D15, C15, A16, B16					
	SMI_DATA[0:15]	Data bus SDRAM			I/O
D22, D23	SMI_CS[0:1]	Chip select bank 0,1			O
A19	SMI_RAS	RAS SDRAM			O
B19	SMI_CAS	CAS SDRAM			O
D19	SMI_WE	SDRAM write enable			O
C19, A14	SMI_DQML, U	DQ mask enable low, up			O
D16	SMI_CLKIN	SDRAM clock in			I
C16	SMI_CLKOUT	SDRAM clock out			O
Analog Pins (Analog Decoder)					
U25	CVBS2_Y	CVBS or Y Input 2 (Selected by programming)			I
U26	C	Chroma Input (Y/C inputs used for S-Video) (Selected by programming)			I
W23	FB	Fast Blanking Input (To be used only when R_CR, G, and B_CB inputs are connected)			I

Table 2: Pins sorted by function

Ball	Ball Name	Main Function	Alternate Function		Type
			Input	Output	
AA19	REFP_RGB	Positive Reference Voltage for RGB ADCs			REF
AB19	REFM_RGB	Negative Reference Voltage for RGB ADCs			REF
W25	R_CR	R Input for RGB Insertion. Cr Input for Analog YCrCb mode.			I
W26	G	G Input for RGB Insertion.			I
V24	B_CB	B Input for RGB Insertion. Cb Input for Analog YCrCb mode.			I
W26	ADCIN	CVBS ADC Input (To be connected to Anti-Aliasing Filter output)			I
V25	VIDEOCOMM	CVBS Anti-Aliasing Filter Reference Voltage			REF
V26	VIDEO_OUT	Video Analog Front-end Multiplexer Output for external filtering			O
U21	REFP_CVBS	Positive Reference Voltage for CVBS and Chroma ADCs			REF
U20	REFM_CVBS	Negative Reference Voltage for CVBS and Chroma ADCs connected to GND			GND
U24	CVBS1_Y	CVBS or Y Input 1 (Selected by programming)			I
Digital Output (Analog Decoder)					
J26	YCRCB7	Digital Video Output 7			O
J24	YCRCB6	Digital Video Output 6			O
G26	YCRCB5	Digital Video Output 5			O
G25	YCRCB4	Digital Video Output 4			O
J23	YCRCB3	Digital Video Output 3			O
F26	YCRCB2	Digital Video Output 2			O
E24	YCRCB1	Digital Video Output 1			O
D26	YCRCB0	Digital Video Output 0			O
L26	CLK_DATA	Output Pixel Clock[3]			O
AC3	PLLLOCK	Output PLL Lock Signal Alternate Function: PIO[0] Bus extension			O
AB26	HSYNC	Horizontal Synchronization Pulse Output Alternate Function: PIO[1] Bus extension			O
AA26	VSYNC	Vertical Synchronization Pulse Output Alternate Function: PIO[2] Bus extension			O
N25	FIELD	Field (Parity) Output Signal Alternate Function: PIO[3] Bus extension			O

Table 2: Pins sorted by function

Ball	Ball Name	Main Function	Alternate Function		Type
			Input	Output	
Clock Signal Pins (analog decoder)					
AA22	XTALOUT	Crystal Pad Oscillator Output			O
AA23	XTALIN_CLKXTP	Crystal Pad Oscillator Input Alternate Function: Differential Clock input			I
Y23	CLKXTM	Differential Clock input (To be used in conjunction with CLKXTP)			I
Configuration Pins (analog decoder)					
Y22	TST_MODE	Test Mode (Must be tied low in Normal mode)			I
AB3	SDA	I²C Bus Data			I/O
AA3	SCL	I²C Bus Clock			I/O
AB22	NRESET	Hardware Reset (Active low)			I
W22	I2CADD	I²C Address Selection (Must be tied high or low according to selected I²C address). 0: 86h/87h 1: 8Eh/8Fh			I
Y25	CLKSEL	Input Clock Selection (Must be coherent with XTALIN_CLKXTP and CLKXTM connections) 0: CLKXTP and CLKXTM 1: XTAL			I
D1 Standard Definition Digital Video Input Stage					
N24	VSYNC	Vertical Sync Input			I
L24	HSYNC	Horizontal Sync Input			I
K26	CLK_DATA	Video Input Clock			I
E26	YCRCB0	4:2:2 Data Stream Input 0			I
E23	YCRCB1	4:2:2 Data Stream Input 1			I
F25	YCRCB2	4:2:2 Data Stream Input 2			I
G23	YCRCB3	4:2:2 Data Stream Input 3			I
G24	YCRCB4	4:2:2 Data Stream Input 4			I
H26	YCRCB5	4:2:2 Data Stream Input 5			I
K24	YCRCB6	4:2:2 Data Stream Input 6			I
J25	YCRCB7	4:2:2 Data Stream Input 7			I
Digital Video Output Stage					
Synchro Output and Clock Output					
AD6	Vout	Vertical Sync Output			O
AC6	Hout	Horizontal Sync Output			O
AE6	CLK_DFL	Clock Output for Video/Scan Processor			O
K5	P_VIDEO0	Digital Video Output 0			O
L5	P_VIDEO1	Digital Video Output 1			O
M5	P_VIDEO2	Digital Video Output 2			O
N5	P_VIDEO3	Digital Video Output 3			O

Table 2: Pins sorted by function

Ball	Ball Name	Main Function	Alternate Function		Type
			Input	Output	
P5	P_VIDEO4	Digital Video Output 4			O
R5	P_VIDEO5	Digital Video Output 5			O
T5	P_VIDEO6	Digital Video Output 6			O
U5	P_VIDEO7	Digital Video Output 7			O
V5	P_VIDEO8	Digital Video Output 8			O
W5	P_VIDEO9	Digital Video Output 9			O
Y4	P_VIDEO10	Digital Video Output 10			O
Y5	P_VIDEO11	Digital Video Output 11			O
AA5	P_VIDEO12	Digital Video Output 12			O
AB4	P_VIDEO13	Digital Video Output 13			O
AB5	P_VIDEO14	Digital Video Output 14			O
AC5	P_VIDEO15	Digital Video Output 15			O
AD5	P_VIDEO16	Digital Video Output 16			O
AE5	P_VIDEO17	Digital Video Output 17			O
AF5	P_VIDEO18	Digital Video Output 18			O
AB6	P_VIDEO19	Digital Video Output 19			O
AB7	P_VIDEO20	Digital Video Output 20			O
AB8	P_VIDEO21	Digital Video Output 21			O
AB9	P_VIDEO22	Digital Video Output 22			O
AB10	P_VIDEO23	Digital Video Output 23			O
AB11	P_VIDEO24	Digital Video Output 24			O
AB12	P_VIDEO25	Digital Video Output 25			O
AB13	P_VIDEO26	Digital Video Output 26			O
AB14	P_VIDEO27	Digital Video Output 27			O
AB15	P_VIDEO28	Digital Video Output 28			O
AB16	P_VIDEO29	Digital Video Output 29			O
AE4	DCLK	Digital CMOS Clock			O
AF4	DE	Digital CMOS Data Enable			O
Parallel Input/Output Pins, Master CPU Control					
AC1	PORTA0	Port A0			I/O
AC4	PORTA1	Port A1			I/O
AD9	PORTA2	Port A2			I/O
AC9	PORTA3	Port A3			I/O
T4	PORTA4	Port A4			I/O
U4	PORTA5	Port A5			I/O
W4	PORTA6	Port A6			I/O
V4	PORTA7	Port A7			I/O
AE3	PORTB0	Port B0			I/O
AD3	PORTB1	Port B1			I/O
AF2	PORTB2	Port B2			I/O
AE2	PORTB3	Port B3			I/O
AD2	PORTB4	Port B4			I/O
AF1	PORTB5	Port B5			I/O

Table 2: Pins sorted by function

Ball	Ball Name	Main Function	Alternate Function		Type
			Input	Output	
AB2	PORTC0	Port C0			I/O
AB1	PORTC1	Port C1			I/O
AA4	PORTC2	Port C2			I/O
AA2	PORTC3	Port C3			I/O
AE7	PORTC4	Port C4			I/O
AC7	PORTC5	Port C5			I/O
AD7	PORTC6	Port C6			I/O
AF6	PORTC7	Port C7			I/O
AF7	PORTD0	Port D0			I/O
AD8	PORTD1	Port D1			I/O
AC8	PORTD2	Port D2			I/O
AE8	PORTD3	Port D3			I/O
AC2	PORTD4	Port D4			I/O
AF3	PORTD5	Port D5			I/O
AF8	PORTD6	Port D6			I/O
AD1	PORTD7	Port D7			I/O
External Memory Interface, Master CPU					
Flash Data Bus, Master CPU					
AE26	FLASH_D0	Flash Data Bus 0			I
AF26	FLASH_D1	Flash Data Bus 1			I
AD25	FLASH_D2	Flash Data Bus 2			I
AE25	FLASH_D3	Flash Data Bus 3			I
AF25	FLASH_D4	Flash Data Bus 4			I
AD24	FLASH_D5	Flash Data Bus 5			I
AE24	FLASH_D6	Flash Data Bus 6			I
AF24	FLASH_D7	Flash Data Bus 7			I
AF22	FLASH_D8	Flash Data Bus 8			I
AD21	FLASH_D9	Flash Data Bus 9			I
AC21	FLASH_D10	Flash Data Bus 10			I
AE21	FLASH_D11	Flash Data Bus 11			I
AF21	FLASH_D12	Flash Data Bus 12			I
AD20	FLASH_D13	Flash Data Bus 13			I
AC20	FLASH_D14	Flash Data Bus 14			I
AE20	FLASH_D15	Flash Data Bus 15			I
SDRAM Data Bus, Master CPU					
AF20	SDRAM_D0	SDRAM Data Bus 0			I
AD19	SDRAM_D1	SDRAM Data Bus 1			I
AE19	SDRAM_D2	SDRAM Data Bus 2			I
AF19	SDRAM_D3	SDRAM Data Bus 3			I
AD18	SDRAM_D4	SDRAM Data Bus 4			I
AC18	SDRAM_D5	SDRAM Data Bus 5			I
AE18	SDRAM_D6	SDRAM Data Bus 6			I
AF18	SDRAM_D7	SDRAM Data Bus 7			I

Table 2: Pins sorted by function

Ball	Ball Name	Main Function	Alternate Function		Type
			Input	Output	
AE11	SDRAM_D8	SDRAM Data Bus 8			I
AC11	SDRAM_D9	SDRAM Data Bus 9			I
AD11	SDRAM_D10	SDRAM Data Bus 10			I
AF10	SDRAM_D11	SDRAM Data Bus 11			I
AE10	SDRAM_D12	SDRAM Data Bus 12			I
AC10	SDRAM_D13	SDRAM Data Bus 13			I
AD10	SDRAM_D14	SDRAM Data Bus 14			I
AF9	SDRAM_D15	SDRAM Data Bus 15			I
EMI Address Bus, Master CPU					
AF17	ADDR_0	Address Bus 0			3.3V
AE17	ADDR_1	Address Bus 1			3.3V
AC17	ADDR_2	Address Bus 2			3.3V
AD17	ADDR_3	Address Bus 3			3.3V
AF11	ADDR_4	Address Bus 4			3.3V
AD12	ADDR_5	Address Bus 5			3.3V
AC12	ADDR_6	Address Bus 6			3.3V
AE12	ADDR_7	Address Bus 7			3.3V
AD13	ADDR_8	Address Bus 8			3.3V
AC13	ADDR_9	Address Bus 9			3.3V
AD16	ADDR_10	Address Bus 10			3.3V
AE13	ADDR_11	Address Bus 11			3.3V
AF13	ADDR_12	Address Bus 12			3.3V
AF23	ADDR_13	Address Bus 13			3.3V
AC22	ADDR_14	Address Bus 14			3.3V
AF16	ADDR_15	Address Bus 15 / BA0			3.3V
AC16	ADDR_16	Address Bus 16 / BA1			3.3V
AE23	ADDR_17	Address Bus 17			3.3V
AD23	ADDR_18	Address Bus 18 / Not_BE2			3.3V
AE22	ADDR_19	Address Bus 19 / Not_BE3			3.3V
Controls					
AF15	RD_NOTWR	SDRAM Write Enable / Flash Write Enable*			3.3V
AC23	NOT_CS_FLASH	Flash Chip Select			3.3V
AD15	NOT_CS_SDRAM	SDRAM Chip Select			3.3V
AC15	NOT_RAS	SDRAM Row Address Strobe			3.3V
AE15	NOT_CAS	SDRAM Column Address Strobe / Flash Output Enable*			3.3V
AD14	NOT_BE0	SDRAM Byte Enable 0			3.3V
AC14	NOT_BE1	SDRAM Byte Enable 1			3.3V
AE14	CKOUT_SDRAM	Clock Output for SDRAM			27 MHz
AF14	CKIN_SDRAM	SDRAM Clock Feedback			I
Master CPU System Controls					
P1	XTALIN	27 MHz Crystal Input			n/a

Table 2: Pins sorted by function

Ball	Ball Name	Main Function	Alternate Function		Type
			Input	Output	
N2	XTALOUT	27 MHz Crystal Output			n/a
Y24	CLKXTM	27 MHz Differential Clock for STV2310			0V
AA24	CLKXTP	27 MHz Differential Clock for STV2310			1.8V
N4	SHIELD_PLL	To connect to Analog Ground Supply for PLL			GND
AB23	TCK	Test Clock Input			I
AB24	TDI	Test Data Input			I
AC26	TDO	Test Data Output			Hi-Z
AB25	TMS	Test Mode Select Input			I
AC24	TRST	Test Reset Input			I
AC25	NRESET	Master CPU System Reset Input (Active Low)			I
Power Supply (Digital Decoder)					
E5, E6, E7, E8, E9, E10, E11, E12, E13, E14, F5, G5, H5, J5					
	VDD3_3	3.3 V power supply for Digital Decoder			PWR
E15, E16, E17, E18, E20, E21, E22, G22, F22					
	VDD1_8	1.8 V power supply for Digital Decoder			PWR
Power Supply (Analog Decoder)					
T21, R21, P21	VCC18_CVBS	1.8 V Analog Voltage Supply for Analog Input Stage (Analog Decoder)			PWR
C6	GNDSUB	Analog Ground Supply (Substrate Polarization) (Analog Decoder)			PWR
AA16, AA17	VCC18SUB	1.8 V Analog Voltage Supply (Output and Pin Isolation layer) (Analog Decoder)			PWR
AA18	VCC18_CLK	1.8 V Analog Voltage Supply for Clock Generator (Analog Decoder)			PWR
D25	GND_CLK	Analog Ground Supply for Clock Generator (Analog Decoder)			PWR
D4	SHIELD	Guard Ring (Analog Input Stage) To be connected to Analog Ground Supply (Analog Decoder)			PWR
T21	VCC18_RGB	1.8 V Analog Voltage Supply (RGB) (Analog Decoder)			PWR
J4	GND_RGB	Analog Ground Supply (RGB) (Analog Decoder)			PWR
T21	VCC18_DIG	1.8 V Analog Voltage Supply (Analog Input Stage) (Analog Decoder)			PWR
L13	GND_DIG	Analog Ground Supply (Analog Input Stage) (Analog Decoder)			PWR
L14	GND_IO	Analog Ground Supply (Analog Input Stage) (Analog Decoder)			PWR

Table 2: Pins sorted by function

Ball	Ball Name	Main Function	Alternate Function		Type
			Input	Output	
V21	VCC33_IO	3.3 V Analog Voltage Supply (Analog Input Stage) (Analog Decoder)			PWR
L15	GND_CVBS	Analog Ground Supply (Analog Input Stage) (Analog Decoder)			PWR
R14, R15, R16, T14, T15, T16					
	VDD18_CORE	1.8 V Digital Voltage Supply (Digital Core) (Analog Decoder)			PWR
A12	VSS	Digital Ground Supply (Digital Core) (Analog Decoder)			PWR
A15	VSS	Digital Ground Supply (Digital Core) (Analog Decoder)			PWR
A20	VSS	Digital Ground Supply (Digital Core) (Analog Decoder)			PWR
N16, P16	VDD33_IO	3.3 V Digital Voltage Supply for Pins (Digital Core) (Analog Decoder)			PWR
B10	VSS_IO	Digital Ground Supply for Pins (Analog Decoder)			PWR
B22	VSS	Digital Ground Supply (Digital Core) (Analog Decoder)			PWR
B3	VSS_IO	Digital Ground Supply for Pins and Outputs (Output Stage) (Analog Decoder)			PWR
P23, N23	VDD33_IO	3.3 V Digital Voltage Supply for Pins (Output Stage) (Analog Decoder)			PWR
AA12, AA13	VDD18_OUT	1.8 V Digital Voltage Supply (Output Stage) (Analog Decoder)			PWR
C17	VSS_OUT	Digital Ground Supply for Pins and Outputs (Output Stage) (Analog Decoder)			PWR
AB26, AC19, AD22, AD26, AD4, AE1, AE16, AE9, AF12, AF5					
	VSS	Ground for Analog Decoder			PWR
Power Supply (Video Display Tv System, Analog Power Supplies)					
P6	VCC33_ADC	3.3 V Analog Voltage Supply for A/D Converter			PWR
N14	GND_ADC	Analog Ground Supply for ADC			PWR
M6	VCC18_IO	1.8 V Analog Voltage Supply for PLL IOs			PWR
N15	GND_IO	Analog Ground Supply for PLL IOs			PWR
N6	VCC18_PLL3	1.8 V Analog Voltage Supply for PLL 3			PWR
M16	GND_PLL3	Analog Ground Supply for PLL 3			PWR
N6	VCC18_PLL2	1.8 V Analog Voltage Supply for PLL 2			PWR
N13	GND_PLL2	Analog Ground Supply for PLL 2			PWR
L6	VDD18_PLL	1.8 V Analog Voltage Supply for PLL			PWR
P14	VSS_PLL	Analog Ground Supply for PLL			PWR

Table 2: Pins sorted by function

Ball	Ball Name	Main Function	Alternate Function		Type
			Input	Output	
Power Supply (Video Display TV System, Digital Power Supplies)					
Y6, AA6, AA7, AA8, AA9, AA10, AA11, T11, R11, P11, N11, T12, R12, P12, N12, T13, R13, P13					
	VDD33_IO	3.3 V Digital Voltage Supply			PWR
R6, T6, U6, V6, W6					
	VDD18_CORE	1.8 V Digital Voltage Supply			PWR
Power Supply Ground					
N1, AA1, AE1, P2, B3, Y3, D4, J4, N4, AD4, C6, F6, G6, H6, J6, F7, G7, H7, J7, K7, L7, M7, N7, P7, R7, T7, U7, V7, W7, Y7, D8, F8, G8, Y8, F9, G9, Y9, AE9, B10, F10, G10, Y10, F11, G11, Y11, A12, F12, G12, H12, Y12, AF12, F13, G13, L13, M13, N13, Y13, F14, G14, L14, M14, N14, P14, Y14, A15, F15, G15, L15, M15, N15, P15, Y15, F16, G16, L16, M16, Y16, AE16, C17, F17, G17, Y17, AB17, F18, G18, Y18, F19, G19, Y19, AC19, A20, F20, G20, H20, J20, K20, L20, M20, N20, P20, R20, T20, U20, V20, W20, Y20, AA20, AB20, F21, G21, H21, J21, K21, L21, M21, N21, W21, Y21, AA21, AB21, B22, L22, M22, N22, P22, R22, T22, AD22, T24, W24, D25, AA25, P26, AD26					
	VSS	Supply Ground			PWR

1. The PIO must be configured in open drain.
2. Tie low whenever JTAG is not used.
3. All other outputs are synchronous to the rising or falling edge of the output pixel clock according to programming.

Table 3: Ballout Configuration

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	
A	CPU_ADR17	CPU_DATA11	CPU_DATA12	CPU_DATA15	CPU_PROCLK	CPU_ADR10	CPU_ADR6	CPU_DATA6	CPU_DATA2	CPU_BE0	CPU_CAS1	GND	CPU_ADR4	SMI_DQMU	GND	SMI_DATA14	SMI_ADR11	SMI_ADR8	SMI_RAS	GND	SMI_DATA4	SMI_DATA0	SMI_ADR13	SMI_ADR1	SMI_ADR3	SPDIF_OUT	A
B	CPU_OE	CPU_DATA10	GND	CPU_DATA14	CPU_BE1	CPU_ADR12	CPU_ADR7	CPU_DATA7	CPU_DATA3	GND	CPU_CE0	CPU_ADR11	CPU_ADR3	SMI_DATA8	SMI_DATA11	SMI_DATA15	SMI_ADR9	SMI_ADR6	SMI_CAS	SMI_DATA7	SMI_DATA3	GND	SMI_ADR10	SMI_ADR2	DAC_IRCLK	DAC_PCMCLK	B
C	CPU_ADR21	CPU_ADR20	CPU_ADR14	CPU_DATA13	CPU_DATA9	GND	CPU_ADR9	CPU_ADR5	CPU_DATA5	CPU_DATA1	CPU_RW	CPU_ADR15	CPU_ADR1	SMI_DATA10	SMI_DATA13	SMI_CLKOUT	GND	SMI_ADR4	SMI_DQML	SMI_DATA5	SMI_DATA1	SMI_ADR12	SMI_ADR0	D_PCMOUT2	D_PCMOUT1	D_PCMOUT0	C
D	CPU_ADR18	CPU_ADR19	PIO0_0	GND	CPU_DATA8	CPU_ADR13	CPU_ADR8	GND	CPU_DATA4	CPU_DATA0	CPU_CAS0	CPU_ADR16	CPU_ADR2	SMI_DATA9	SMI_DATA12	SMI_CLKIN	SMI_ADR7	SMI_ADR5	SMI_WE	SMI_DATA6	SMI_DATA2	SMI_CS0	SMI_CS1	DAC_SCLK	GND	YCRCB0	D
E	CPU_WAIT	CPU_CE2	CPU_CE3	CPU_CE1	VDD33	VDD33	VDD33	VDD33	VDD33	VDD33	VDD33	VDD33	VDD33	VDD33	VDD18	VDD18	VDD18	VDD18	VDD_PLL	VDD18	VDD18	VDD18	YCRCB_1_PAD	YCRCB1	PIO4_0	YCRCB_0_PAD	E
F	PIO0_6	PIO2_6	CPU_RAS1	PIO2_5	VDD33	ND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD18	PIO4_1	PIO4_2	YCRCB_2_PAD	YCRCB2	F
G	PIO0_2	DCU_TRIGOUT	PIO0_7	PIO1_2	VDD33	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	VDD18	YCRCB_3_PAD	YCRCB_4_PAD	YCRCB4	YCRCB5	G
H	PIO2_4	PIO2_3	PIO2_0	PIO2_2	VDD33	GND	GND													GND	GND	VDD_PCM	PIO4_3	PIO4_4	PIO4_5	YCRCB_5_PAD	H
J	IRQ1	IRQ0	PIO5_2	GND	VDD33	GND	GND													GND	GND	VDD_PCM	YCRCB3	YCRCB6	YCRCB_7_PAD	YCRCB7	J
K	PIO3_2	PIO3_1	IRQ2	PIO3_0	P_VIDEO00	VDD18_IO	GND													GND	GND	VDD_RGB	PIO4_6	YCRCB_6_PAD	PIO4_7	CLK_DATA	K
L	PIO3_6	PIO3_5	PIO3_3	PIO3_4	P_VIDEO01	VDD18_PLL1	GND				VDD18_CORE	VDD18_CORE	GND	GND	GND	GND				GND	GND	VDD_YCC	PWM1	HSYNC	PIO2_7	CLK_DAT	L
M	BFLAG	BCLK	PIO3_7	B_data	P_VIDEO02	VCC18_IO	GND				VDD18_CORE	GND	GND	GND	GND	GND				GND	GND	GND	PWM2	PWM0	PIO5_3	PIO5_4	M
N	GND	XTALOUT	BSYNC	GND	P_VIDEO03	VCC18_PLL3	GND				VDD33_IO	VDD33_IO	GND	GND	GND	VDD33IO				GND	GND	GND	PIX_CLK	VSYNC	FIELD	PIO5_5	N
P	XTALIN	GND	RESET	TRST	P_VIDEO04	VCC33_ADC	GND				VDD33_IO	VDD33_IO	VDD33_IO	GND	GND	VDD33IO				GND	VCC18CVBS	GND	V_REF_YCC	CV_OUT	I_REF_YCC	GND	P
R	TDO	TDI	TMS	TCK	P_VIDEO05	VDD18_CORE	GND				VDD33_IO	VDD33_IO	VDD33_IO	VDD18CORE	VDD18CORE	VDD18CORE				GND	VCC18CVBS	GND	I_REF_RGB	V_REF_RGB	Y_OUT	C_OUT	R
T	DCU_TRIG_IN	AUX-CLK	PIO1_4	PORTA4	P_VIDEO06	VDD18_CORE	GND				VDD33_IO	VDD33_IO	VDD33_IO	VDD18CORE	VDD18CORE	VDD18CORE				GND	VCC18CVBS	GND	B_OUT	GND	G_OUT	R_OUT	T
U	PIO1_0	PIO1_1	PIO1_3	PORTA5	P_VIDEO07	VDD18_CORE	GND													GND	REFP_CVBS	NC	NC	CVBS1_Y	CVBS2_Y	C	U
V	PIO5_0	PIO5_1	PIO0_3	PORTA7	P_VIDEO08	VDD18_CORE	GND													GND	VCC33_IO	NC	NC	B_CB	VIDEO_COM	VIDEO_OUT	V
W	PIO2_1	PIO1_5	PIO0_4	PORTA6	P_VIDEO09	VDD18_CORE	GND													GND	GND	I2CADDR	FB	GND	R_CR	ADC-IN	W
Y	PIO0_5	PIO0_1	GND	P_VIDEO10	P_VIDEO11	VDD33_IO	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	TST_MODE	CLKXTM	CLKXTM	CLKSEL	G	Y
AA	GND	PORTC3	SCL	PORTC2	P_VIDEO12	VDD33_IO	VDD33_IO	VDD33_IO	VDD33_IO	VDD33_IO	VDD33_IO	VDD18OUT	VDD18OUT	VDD33_OUT	VCC33SUB	VCC18SUB	VCC18SUB	VCC18CLK	REFP_RGB	GND	GND	XTALOUT	XTALIN_CLKXTP	CLKXTP	GND	VSYNC	AA
AB	PORTC1	PORTC0	SDA	P_VIDEO13	P_VIDEO14	P_VIDEO19	P_VIDEO20	P_VIDEO21	P_VIDEO22	P_VIDEO23	P_VIDEO24	P_VIDEO25	P_VIDEO26	P_VIDEO27	P_VIDEO28	P_VIDEO29	GND	NC	REFM_RGB	GND	GND	NRESET	TCK	TDI	TMS	HSYNC	AB
AC	PORTA0	PORTD4	PLL_LOCK	PORTA1	P_VIDEO15	HOUT	PORTC5	PORTD2	PORTA3	SDRAM_D13	SDRAM_D9	ADDR_6	ADDR_9	NOT_BE1	NOT_RAS	ADDR_16	ADDR_2	SDRAM_D5	GND	FLASH_D14	FLASH_D10	ADDR_14	NOT_CS_FL	TRST	NRESET	TDO	AC
AD	PORTD7	PORTB4	PORTB1	GND	P_VIDEO16	VOUT	PORTC6	PORTD1	PORTA2	SDRAM_D14	SDRAM_D10	ADDR_5	ADDR_8	NOT_BE0	NOT_CS_SDR	ADDR_10	ADDR_3	SDRAM_D4	SDRAM_D1	FLASH_D13	FLASH_D9	GND	ADDR_18	FLASH_D5	FLASH_D2	GND	AD
AE	GND	PORTB3	PORTB0	DCLK	P_VIDEO17	CLK_DFL	PORTC4	PORTD3	GND	SDRAM_D12	SDRAM_D8	ADDR_7	ADDR_11	CKOUT_SDR	NOT_CAS	GND	ADDR_1	SDRAM_D6	SDRAM_D2	FLASH_D15	FLASH_D11	ADDR_19	ADDR_17	FLASH_D6	FLASH_D3	FLASH_D0	AE
AF	PORTB5	PORTB2	PORTD5	DE	P_VIDEO18	PORTC7	PORTD0	PORTD6	SDRAM_D15	SDRAM_D11	ADDR_4	GND	ADDR_12	CKIN_SDRAM	RD_NOTWR	ADDR_15	ADDR_0	SDRAM_D7	SDRAM_D3	SDRAM_D0	FLASH_D12	FLASH_D8	ADDR_13	FLASH_D7	FLASH_D4	FLASH_D1	AF
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	

3 Detailed Description

For more detailed description, refer to the standalone product datasheets:

- STV2310, Revision 2.4, Jan. 2003: Multistandard TV/VCR Digital Video Decoder and Output Scaler.
- STV3550, Revision 1.2, Jan. 2004: Integrated Up-Converter with 32 bit CPU Core with Video Enhacers and Bitmap On-Screen Display.
- STD0100, Revision 1.0, Dec. 2003: MPEG Audio and Video Decoder.

4 Product Order Codes

- STD0550Z: Standard product; Dolby Digital and Macrovision Encoding not active.
- STD0550ZD: Dolby Digital (AC3) active.
- STD0550ZM: Macrovision Encoding active.
- STD0550ZDM: Dolby Digital and Macrovision Encoding active.

5 General Package Information

5.1 Package Mechanical Data

Figure 8: 532-Ball Plastic Ball Grid Array Package with 36 Center Ball Option

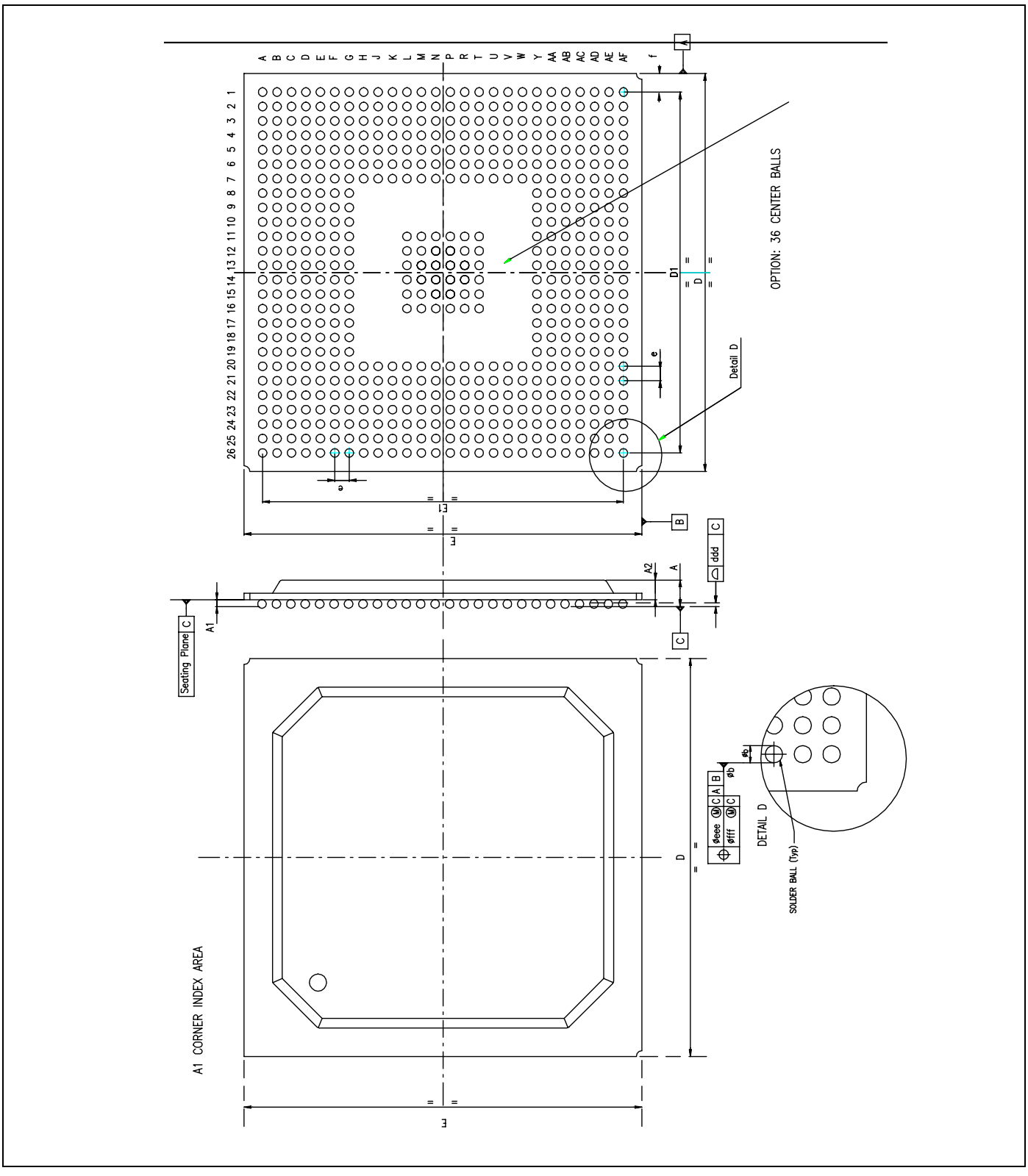


Table 4: PBGA420 Dimensions

Dim.	DATABOOK (mm)			DRAWING (mm)		
	Min.	Typ.	Max.	Min.	Typ	Max
A			2.600			2.600
A1	0.360			0.500		0.700
A2			1.900	1.630		1.900
b	0.600	0.750	0.900	0.600	0.750	0.900
D	34.800	35.000	35.200	34.800	35.000	35.200
D1		31.750			31.750	
E	34.800	35.000	35.200	34.800	35.000	35.200
E1		31.750			31.750	
e		1.270			1.270	
F		1.625			1.625	
.ddd			0.200			0.200
.eee[1]		0.150			0.150	
.fff[2]		0.075			0.075	

1. The tolerance of position that controls the location of the pattern of balls with respect to datums A and B. For each ball there is a cylindrical tolerance zone eee perpendicular to datum C and located on true position with respect to datums A and B as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone.

2. The tolerance of position that controls the location of the balls within the matrix with respect to each other. For each ball there is a cylindrical tolerance zone fff perpendicular to datum C and located on true position as defined by e. The axis perpendicular to datum C of each ball must lie within this tolerance zone. Each tolerance zone fff in the array is contained entirely in the respective zone eee above The axis of each ball must lie simultaneously in both tolerance zones.

6 Summary Of Changes

Rev.	Main Changes	Date
0.1	First Draft.	November 2003
0.2	Changes to Figure 1: STD0550 Block Diagram on page 4.	February 2004
1.0	Added ball list and ball configuration. Added Chapter 4: Product Order Codes on page 28.	February 2004