DESCRIPTION

The M5L8284AP is a clock generator and driver for use with the MELPS 86, 88 processors.

It has a synchronous delay circuit and synchronous control circuit capable of controlling two Multibus (Intel trademark) circuits.

FEATURES

- Crystal controlled stable output frequency
- Capable of synchronous operation with other M5L8284APs
- External frequency input
- A power-on reset by means of an external capacitor and resistor

APPLICATION

Clock driver and generators and driver for MELPS 86, 88

FUNCTION

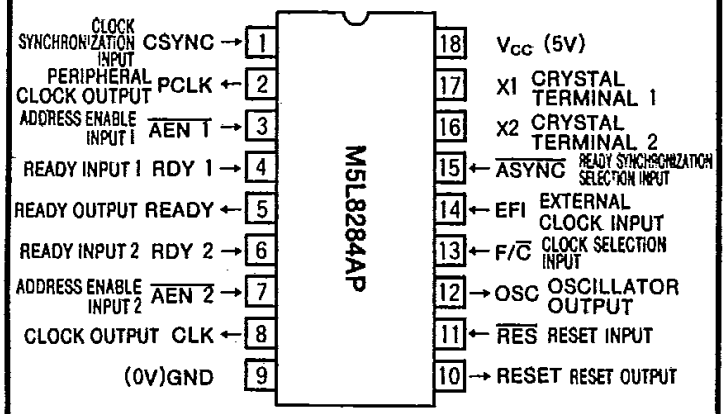
The M5L8284AP is a clock generator/driver for the MELPS 86, 88 microprocessors.

The chip contains a crystal controlled oscillator, a divided-by-3 counter, a peripheral clock output provided divided-by-2 counter, a reset circuit and ready circuit to ensure synchronization to the CLK signal.

The reset input $\overline{RES}$ is used to generate the reset output $\overline{RESET}$ as the CPU reset synched to the CLK signal. A Schmitt trigger is used at the input side.

Thus, a reset signal can be output at power on by connecting a capacitor and resistor to the $\overline{RES}$ input.

PIN CONFIGURATION (TOP VIEW)



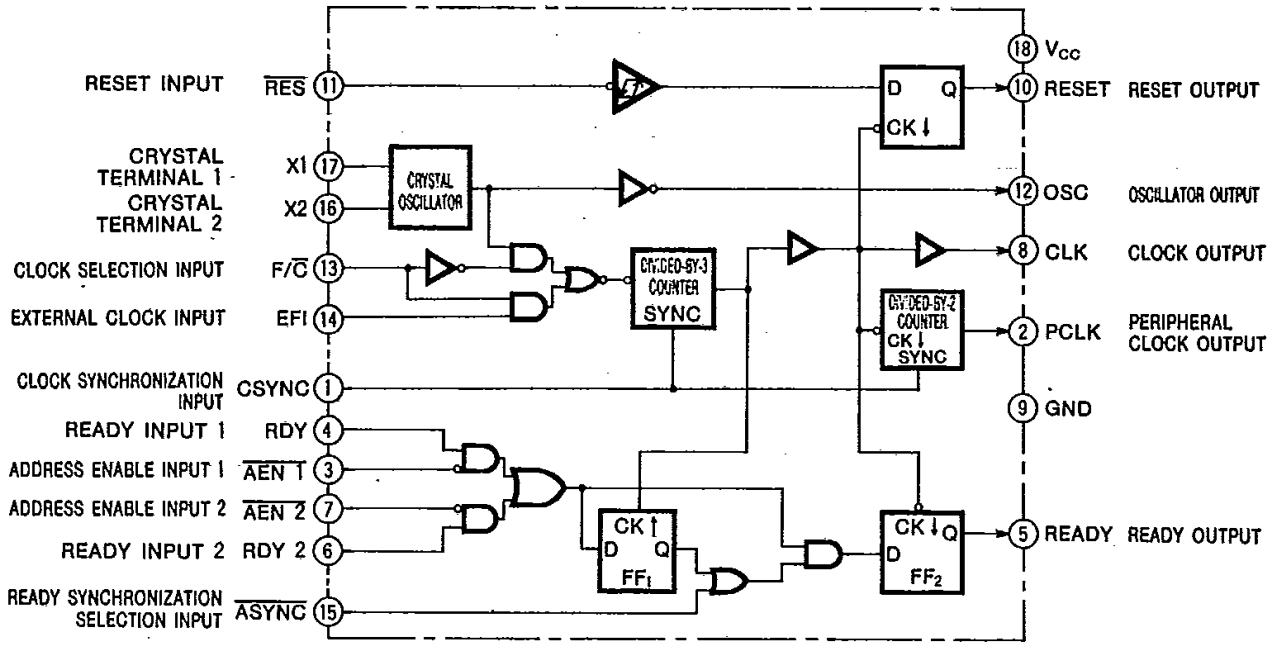
Outline 18P4

The frequency/crystal selection input F/$\overline{C}$ can be used to select the crystal oscillator circuit output or an external clock input as the input for the divide-by-three counter.

By using these pins, the M5L8284AP output can be used to drive multiple M5L8284AP devices.

The clock synchronization input CSYNC is used to operate multiple M5L8284APs in sync.

BLOCK DIAGRAM



PIN DESCRIPTIONS

Pin	Name	Input or output	Function
$\overline{AEN1}$, $\overline{AEN2}$	Address enable input	Input	When $\overline{AEN1}$ and $\overline{AEN2}$ are set low, RDY1 and RDY2 are enabled, respectively. By using these two inputs separately, the CPU can be used to access two Multibusses. When not used as a multimaster, $\overline{AEN}$ should be set to low. These inputs are active low.
RDY1, RDY2	Bus ready input	Input	These inputs are connected to the output signal indicating the completion of data reception from a system bus device or, indicating that data is valid. RDY1 and RDY2 are enabled when AEN1 and AEN2 are low, respectively. These inputs are active high.
$\overline{ASYNC}$	Active low input	Input	This signal is used to select the synchronization mode of the READY signal generation circuit. When the $\overline{ASYNC}$ signal is set low, the READY signal is generated in two synchronization steps. When the $\overline{ASYNC}$ signal is set high, the READY signal is generated in one step.
READY	Ready output	Output	The state of RDY appears at this output in synchronization with the CLK output. This is done to synchronize the READY output to the M5L8284AP internal clock because the RDY input generation is unrelated to the CLK signal. This pin is normally connected to the CPU ready input and cleared after the required hold CPU time has elapsed.
X_1, X_2	Crystal element terminals	Input	These pins are used to connect the crystal. The crystal frequency is 3 times of CPU clock frequency. The crystal should be in the 12-25MHz range with the series resistance as possible as small. Care should be taken that these pins are not shorted to ground.
F/$\overline{C}$	Clock selection input	Input	When F/$\overline{C}$ is set low, CLK and PCLK outputs are driven from the crystal oscillator circuit. When it is set high, they are driven from the EFI input.
EFI	External clock input	Input	When F/$\overline{C}$ is set high, CLK and PCLK output signals are driven from this pin. A TTL level rectangular signal and three times of the CPU frequency should be used.
CLK	Clock output	Output	This output is connected to the clock inputs of the CPU and the peripheral devices on the local bus. The output waveform is 1/3 the frequency of the crystal oscillator connected at X_1 and X_2 or the signal applied to the FEI input, and has a duty cycle of 1/3. Since for V_{CC}=5V, V_{OH}=4.5V, this output can be directly drive the CPU clock input.
PCLK	Peripheral clock output	Output	This output provides a clock signal for use with peripheral devices. The output waveform is 50% duty cycle TTL level rectangular waveform with a frequency 1/2 that of the clock output.
OSC	Oscillator output	Output	This output is a TTL level crystal oscillator output. The frequency is the same as that of the crystal connected at X_1 and X_2, but care should be taken as the frequency will be unstable if these pins are left open.
$\overline{RES}$	Reset input	Input	This active low input is used to generate the reset output signal for the CPU. The input is a schmitt trigger input so that by connecting a capacitor and a resistor, the CPU reset signal can be generated at power on.
RESET	Reset output	Output	This pin is connected to the CPU reset input. The signal at this pin is synchronized the $\overline{RES}$ input with the CLK signal. This output is active high.
CSYNC	Clock synchronization input	Input	When using multiple M5L8284AP devices, this input is used as a clock synchronization input. When CSYNC is high, the internal counter of the M5L8284AP is reset and when CSYNL is low, it begins operation. CSYNC must be synchronized with EFI. See application notes.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage		−0.5~7	V
V_I	Input voltage		−0.5~5.5	V
V_O	Output voltage		−0.5~V_{CC}	V
T_{opr}	Operating free-air temperature range		0~75	℃
T_{stg}	Storage temperature range		−65~150	℃

RECOMMENDED OPERATING CONDITIONS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter		Limits			Unit
			Min	Nom	Max	
V_{CC}	Supply voltage		4.5	5	5.5	V
I_{OH}	High-level output current	CLK V_{OH}=4V	0		−1	mA
		Other outputs V_{OH}=2.4V				
I_{OL}	Low-level output current	V_{OL}≦0.45V	0		5	mA

ELECTRIC CHARACTERISTICS (T_a=0~75℃, unless otherwise noted)

Symbol	Parameter		Test conditions	Limits			Unit
				Min	Typ	Max	
V_{IH}	High-level input voltage	$\overline{RES}$		2.6			V
		Other inputs $\overline{RES}$		2			
V_{IL}	Low-level input voltage					0.8	V
$V_{T+}-V_{T-}$	Hysteresis width	$\overline{RES}$	V_{CC}=5V	0.25			V
V_{IC}	Input clamp voltage		V_{CC}=4.5V, I_{IC}=−5mA			−1	V
V_{OH}	High-level output voltage	CLK	V_{CC}=4.5V, I_{OH}=−1mA	4			V
		Other outputs CLK		2.4			
V_{OL}	Low-level output voltage		V_{CC}=4.5V, I_{OL}=5mA			0.45	V
I_{IH}	High-level input current		V_{CC}=5.5V, V_I=5.25V			50	μA
I_{IL}	Low-level input current	ASYNC	V_{CC}=5.5V, V_I=0.45V			−1.3	mA
		Other inputs ASYNC				−0.5	
I_{CC}	Supply current		V_{CC}=5.5V			162	mA

SWITCHING CHARACTERISTICS (V_{CC}=5V±10%, T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Alternate symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
T_C	CLK repetition period	t_{CLCL}		100			ns
$T_{W(CLKH)}$	CLK high pulse width	t_{CHCL}	(Note 5 a, b) $CLKF_{req}$≦8MHz	(⅓t_{CLCL})+2			ns
			$CLKF_{req}$=10MHz	39			
$T_{W(CLKL)}$	CLK low pulse width	t_{CLCH}	(Note 5 a, b) $CLKF_{req}$≦8MHz	(⅔t_{CLCL})−15			ns
			$CLKF_{req}$=10MHz	53			
t_{TLH}	CLK low-high transition time	t_{CH1CH2}	1~3.5V			10	ns
t_{THL}	CLK high-low transition time	t_{CL2CL1}	3.5~1V			10	ns
$T_{W(PCLKH)}$	PCLK high pulse width	t_{PHPL}		t_{CLCL}−20			ns
$T_{W(PCLKL)}$	PCLK low pulse width	t_{PLPH}		t_{CLCL}−20			ns
t_{dIV}	READY inhibit time with respect to CLK (Note 1)	t_{RYLCL}	(Note 5 c, d)	−8			ns
t_{dV}	READY enable time with respect to CLK (Note 2)	t_{RYHCH}	(Note 5 c, d) $CLKF_{req}$≦8MHz	53			ns
			$CLKF_{req}$=10MHz				
$T_{DHL(CLK-RESET)}$	High-low delay time from CLK to RESET	t_{CLIL}				40	ns
$T_{DLH(CLK-PCLK)}$	Low-high delay time from CLK to PCLK	t_{CLPH}				22	ns
$T_{DHL(CLK-PCLK)}$	High-low delay time from CLK to PCLK	t_{CLPL}				22	ns
$T_{DLH(OSC-CLK)}$	Low-high delay time from OSC to CLK	t_{OLCH}		−5		22	ns
$T_{DHL(OSC-CLK)}$	High-low delay time from OSC to CLK	t_{OLCL}		2		35	ns
T_r	Output rise time	t_{OLOH}	0.8~2V (except CLK)			20	ns
t_f	Output fall time	t_{OHOL}	2~0.8V (except CLK)			12	ns

Note 1 : Applies to T2 state time
2 : Applies to T3 and TW state times

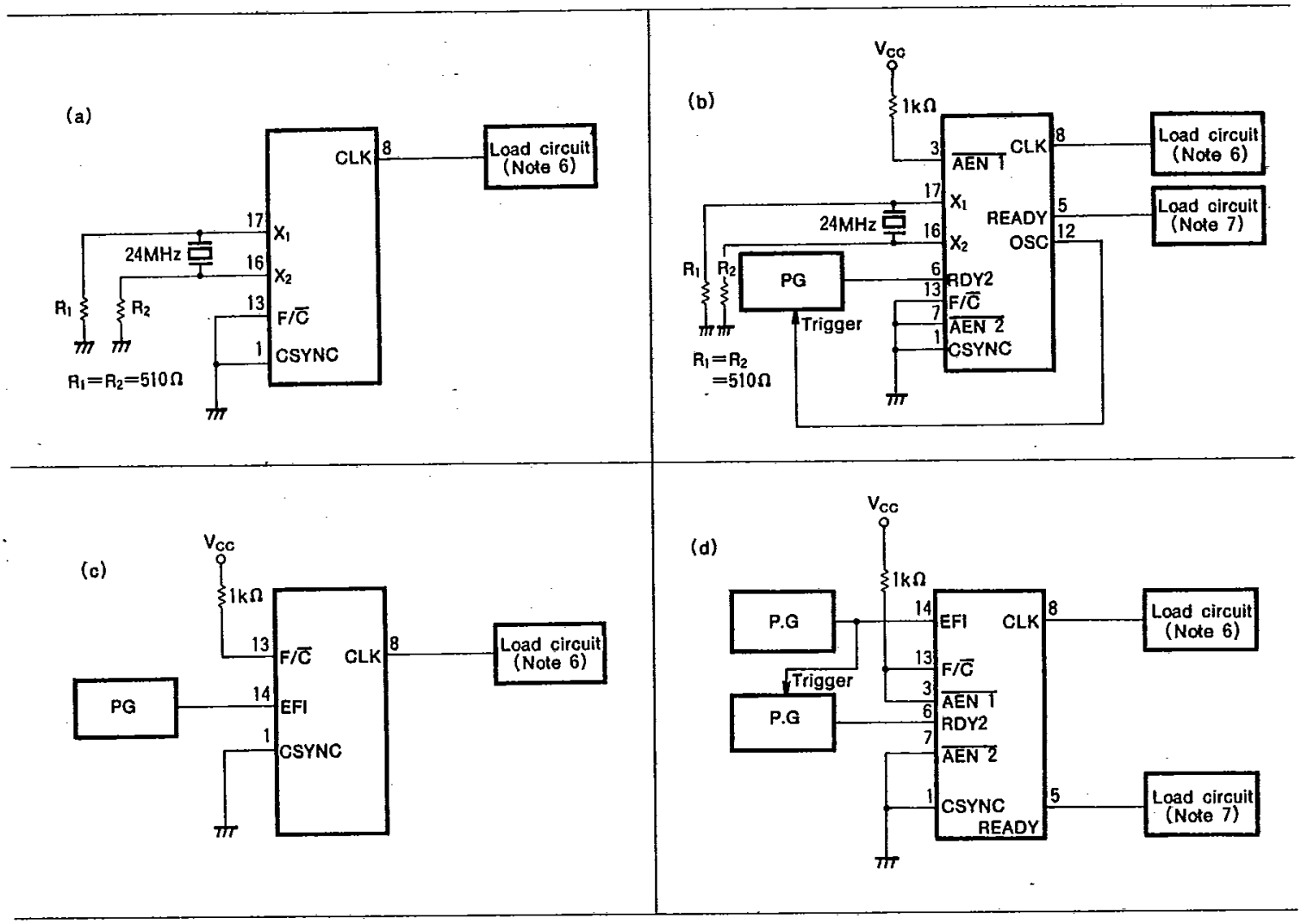
TIMING REQUIREMENTS (V_{CC}=5V ±10%, T_a=0~75℃, unless otherwise noted)

Symbol	Parameter	Alternate symbol	Test conditions	Limits			Unit
				Min	Typ	Max	
$f_{(xtal)max}$	Crystal frequency			12		25	MHz
$t_{W(EFIH)}$	EFI high pulse width	t_{EHEL}	90%—90%V_{IN}	13			ns
$t_{W(EFIL)}$	EFI low pulse width	t_{ELEH}	10%—10%V_{IN}	13			ns
$T_{C(EFI)}$	EFI repetition period (Note 3)	t_{ELEL}		$t_{EHEL}+t_{ELEH}+\delta$			ns
$t_{SU(RDY)}$	RDY1 and RDY2 active setup time with respect to CLK	t_{RIVCL}	$\overline{ASYNC}$=HIGH	35			ns
$t_{SU(RDY)}$	RDY1 and RDY2 active hold time with respect to CLK	t_{RIVCH}	$\overline{ASYNC}$=LOW	35			ns
$t_{SU(RDY)}$	RDY1 and RDY2 inactive setup time with respect to CLK	t_{RIVCL}		35			ns
$t_{h(RDY)}$	RDY1 and RDY2 hold time with respect to CLK	t_{CLRIX}		0			ns
$t_{SU(\overline{ASYNC})}$	$\overline{ASYNC}$ setup time with respect to CLK	t_{AYVCL}		50			ns
$t_{h(\overline{ASYNC})}$	$\overline{ASYNC}$ hold time with respect to CLK	t_{CLAYX}		0			ns
$t_{SU(AEN)}$	$\overline{AEN1}$ and $\overline{AEN2}$ setup time with respect to RDY1 and RDY2	t_{AIVRIV}		15			ns
$t_{h(AEN)}$	$\overline{AEN1}$ and $\overline{AEN2}$ hold time with respect to CLK	t_{CLAIX}		0			ns
$t_{SU(CSYNC)}$	CSYNC setup time with respect to EFI	t_{YHEH}		20			ns
$t_{h(CSYNC)}$	CSYNC hold time with respect to EFI	t_{EHYL}		20			ns
$t_{W(CSYNC)}$	CSYNC pulse width	t_{YHYL}		$2t_{ELEL}$			ns
$t_{SU(\overline{RES})}$	$\overline{RES}$ setup time with respect to CLK (Note 4)	t_{I1HCL}		65			ns
$t_{h(\overline{RES})}$	$\overline{RES}$ hold time with respect to CLK (Note 4)	t_{CLI1H}		20			ns
t_r	Input rise time	t_{ILIH}	0.8~2V			20	ns
t_f	Input fall time	t_{IHIL}	2~0.8V			12	ns

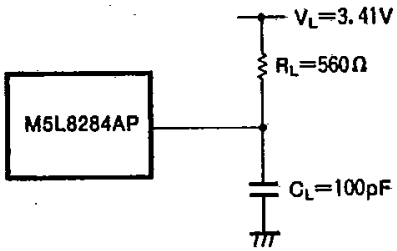
Note 3 : $\delta = t_r$(5ns max)+EFI + t_f(5ns max)+EFI

4 : $t_{SU(\overline{RES})}$ and $t_{h(\overline{RES})}$ are theoretically only to guarantee logic in the next clock period

Note 5 : Test Circuits

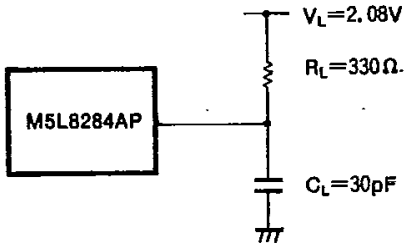


Note 6 : Load Circuit



CLK pins

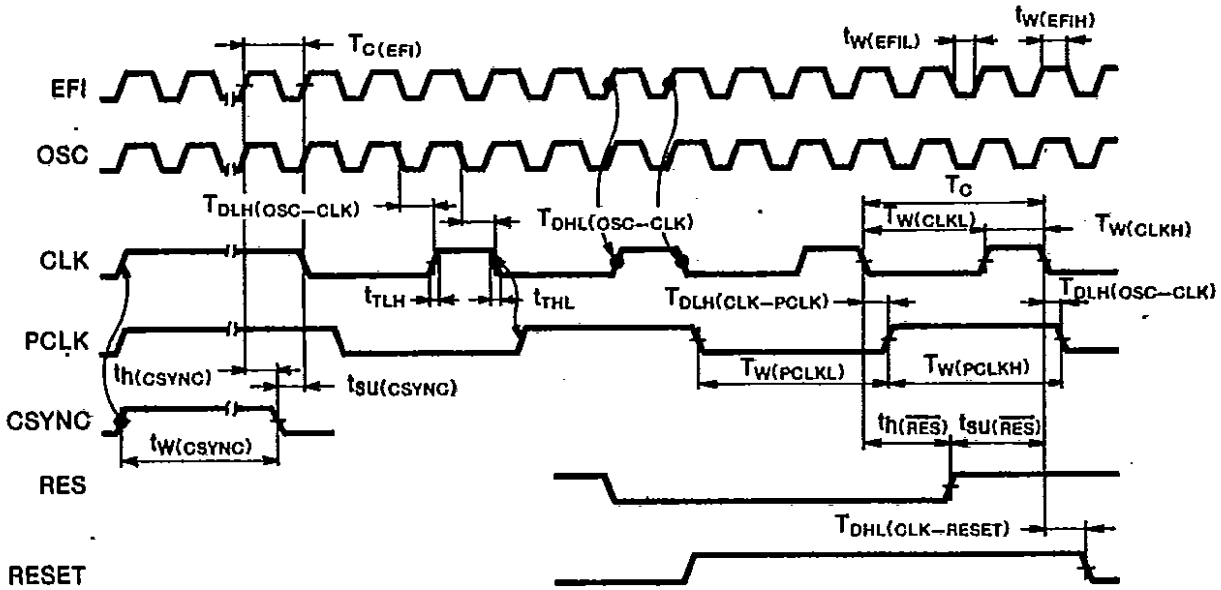
Note 7 : Load circuit



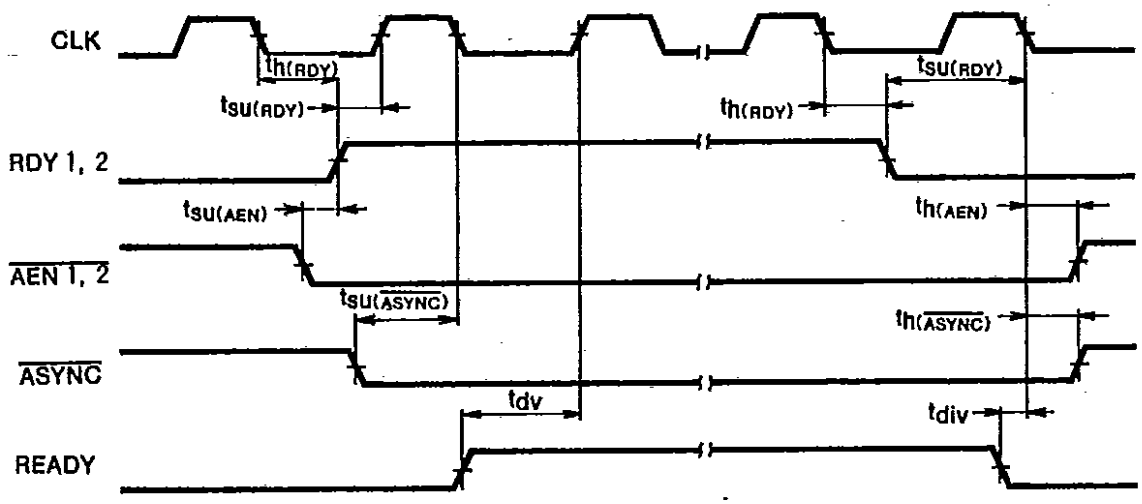
Other pins

TIMING DIAGRAM (Reference level=1.5V)

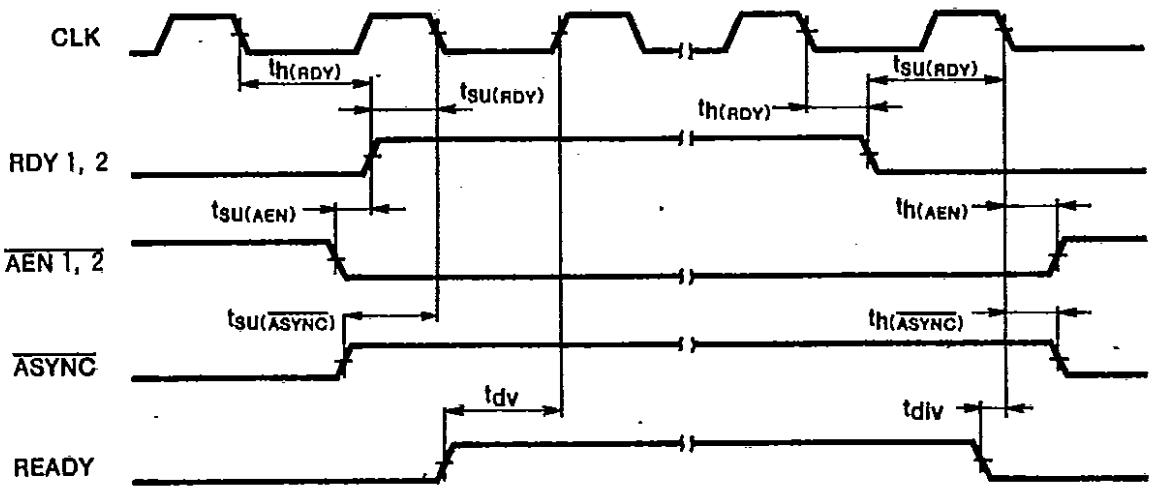
CLK, RESET Signals



READY Signal (with asynchronous device)

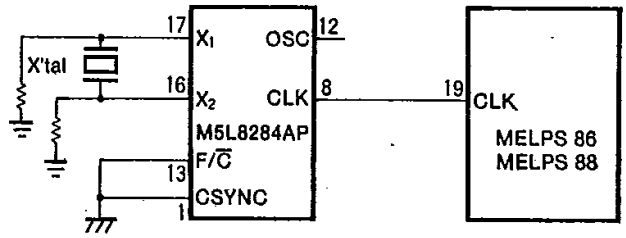


READY Signal (with synchronous device)



APPLICATION NOTES

(1) Connecting the crystal

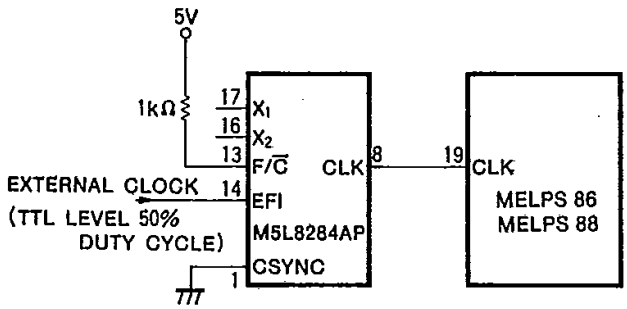


The crystal frequency should be three times the cycle time of the 8086, 8088 or 8089, and the crystal should be located as close to the M5L8284AP as possible.

PRECAUTIONS FOR USE

(1) The oscillator circuit of the M5L8284AP is designed for use with the fundamental mode crystal.
If noise is allowed to enter the XTAL1, XTAL2 or V_{CC} pins, the oscillator frequency will be pulled of the parallel resident frequency and the stray capacitance between XTAL1 and XTAL2 may cause the circuit to go into relaxation oscillation. To prevent this, care should be given to the following points.
(1) The should be one with a small parallel capacitance.
(2) A 0.01 — 0.1μF capacitor should be connected between V_{CC} and ground. This capacitor should be located as close as possible to the IC.

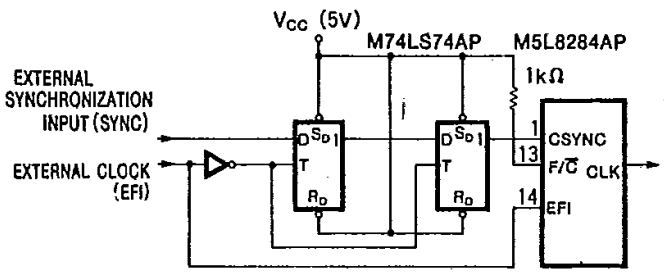
(2) External clock connections



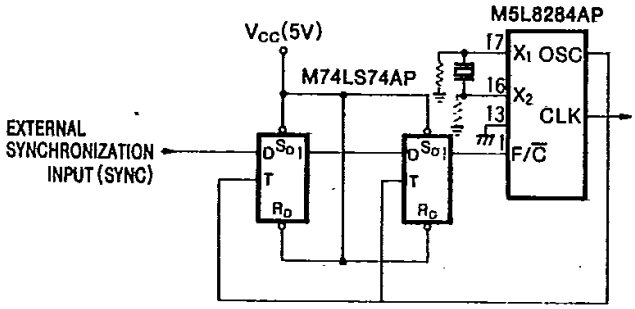
The frequency should be three times the CPU cycle frequency .

(3) Synchronizing using the CSYNC input

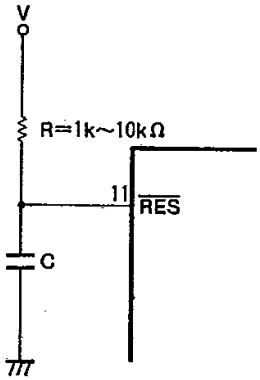
● When the EFI input is used



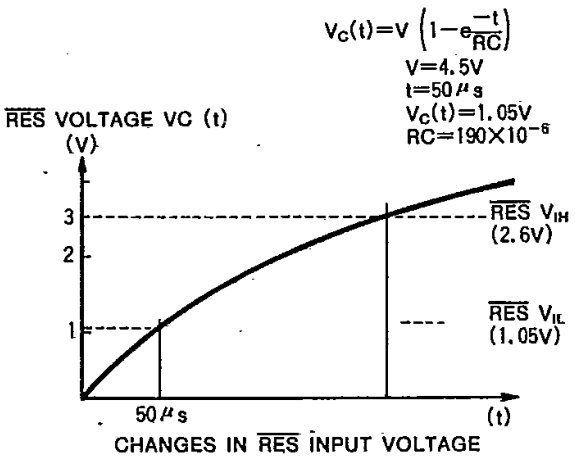
● When the EFI input is not used



(4) Power-on reset circuit



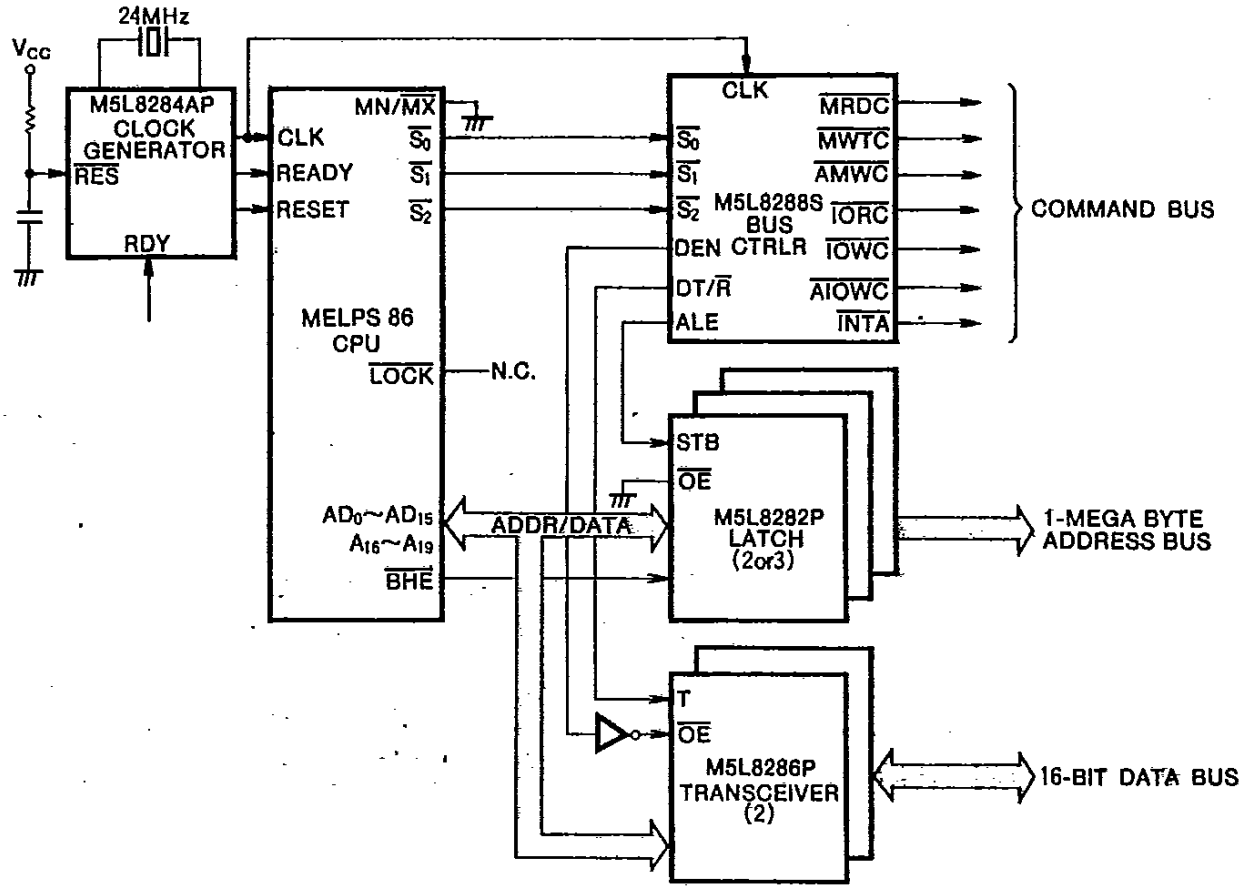
Since the MELPS 86, 88 require a reset pulse over 50μs after V_{CC} reaches 4.5V upon power on, the capacitor value should be determined by the graph shown below. Note that the time for V_{CC} to reach 4.5V has not been considered, so that it is necessary to choose the characteristics value of capacitance under consideration of the power supply.



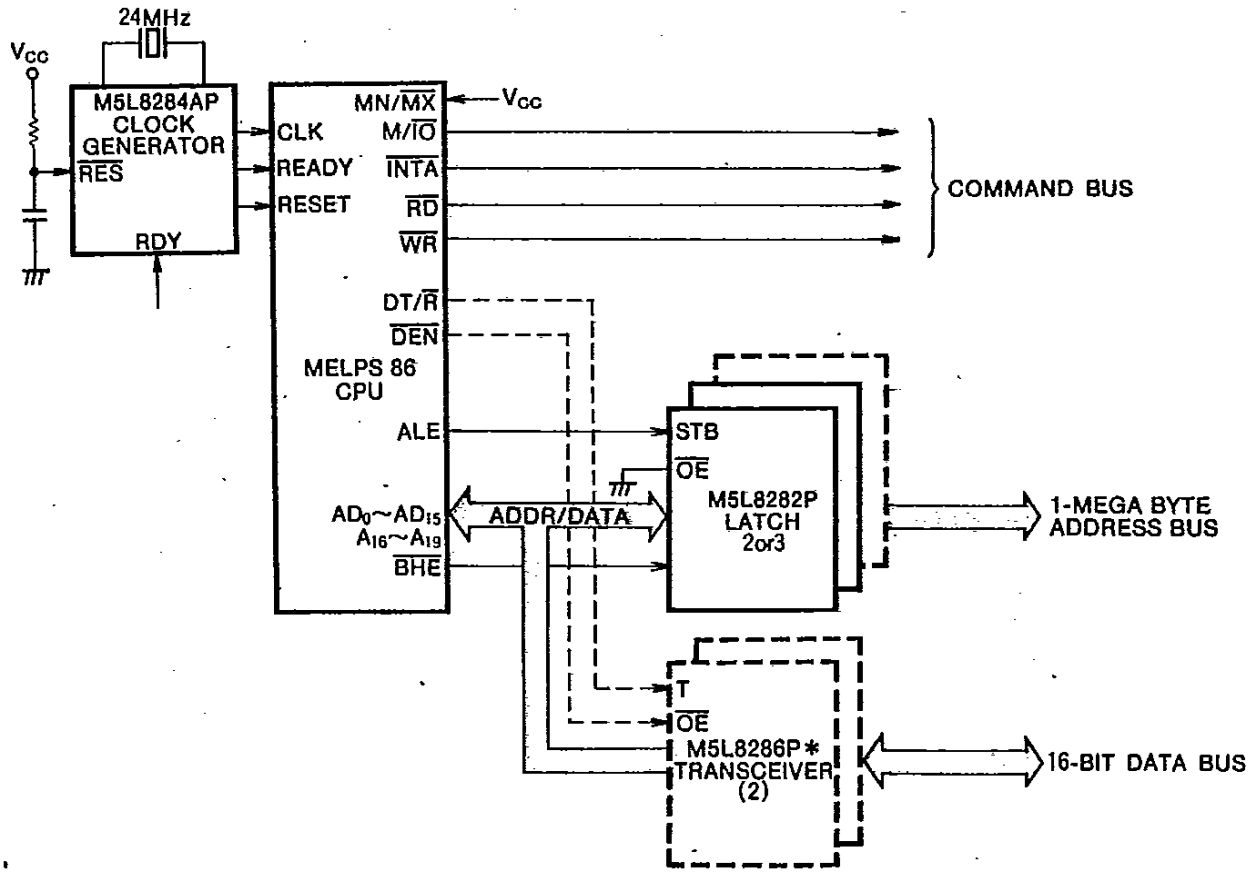
CHANGES IN $\overline{RES}$ INPUT VOLTAGE

APPLICATION EXAMPLES

(1) Use in the maximum mode



(2) Use in the minimum mode



* : Option
Required when the number of devices driving the bus increases