VTC Incorporated

VA033
UNITY GAIN VIDEO BUFFER

FEATURES
- Low Offset: 8mV
- High Slew Rate: 2000V/µs.
- Fast Rise Time:1.8ns
- High Output Current: ±100mA
- Wide Power Bandwidth: DC to 85MHz
- Replace Costly Hybrids
- Pin-Compatible with HA-5033 and LH0033
- Available in Commercial Versions

DESCRIPTION
The VA033 is a high-speed unity gain buffer capable of ±100mA output current, 2000 V/µs slew rate and a small signal bandwidth in excess of 250MHz. It is intended to fulfill a wide range of buffer applications such as high-speed line drivers, video impedance transformation, op amp isolation buffer for driving reactive loads, and high impedance input buffers for high-speed A-to-Ds and comparators.

The device is available in 8-pin ceramic and plastic DIP and SOIC (surface mount) packages.

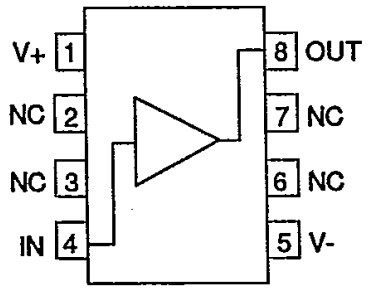
ABSOLUTE MAXIMUM RATINGS
Supply Voltages ..... ±6V
Input Voltage ..... ±Vs
Output Current (Peak) ..... ±200mA
Power Dissipation (Note 1):
T_A = 25°C ..... 1.15W: Plastic DIP
0.83W: SOIC, Ceramic DIP, TO-99

Note 1: Power derating above 25°C shall be based on a maximum junction temperature of 175°C and the following thermal resistance factors:

Packages	θ_{JC} (°C/W)	θ_{JA} (°C/W)
Plastic DIP	60	130
SOIC/Ceramic DIP	100	100

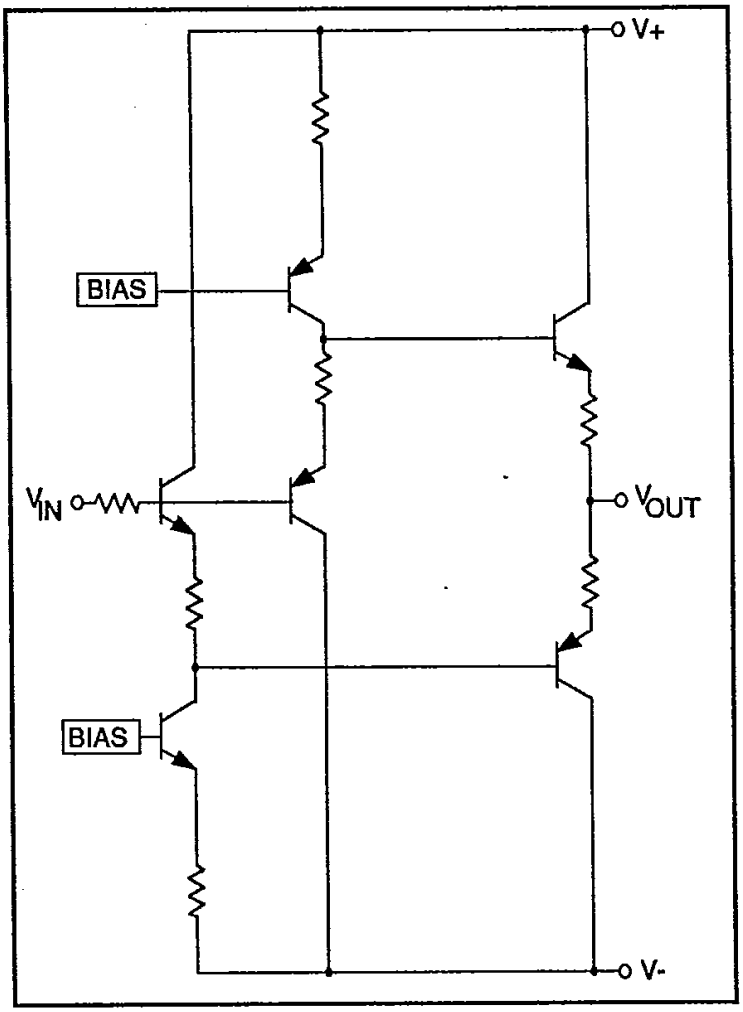
PACKAGE TYPES AVAILABLE
- 8-Pin Plastic DIP
- 8-Pin CERDIP
- 8-Pin SOIC

CONNECTION DIAGRAM
8-Lead Dual In-Line/SOIC Package



Top View

SIMPLIFIED SCHEMATIC



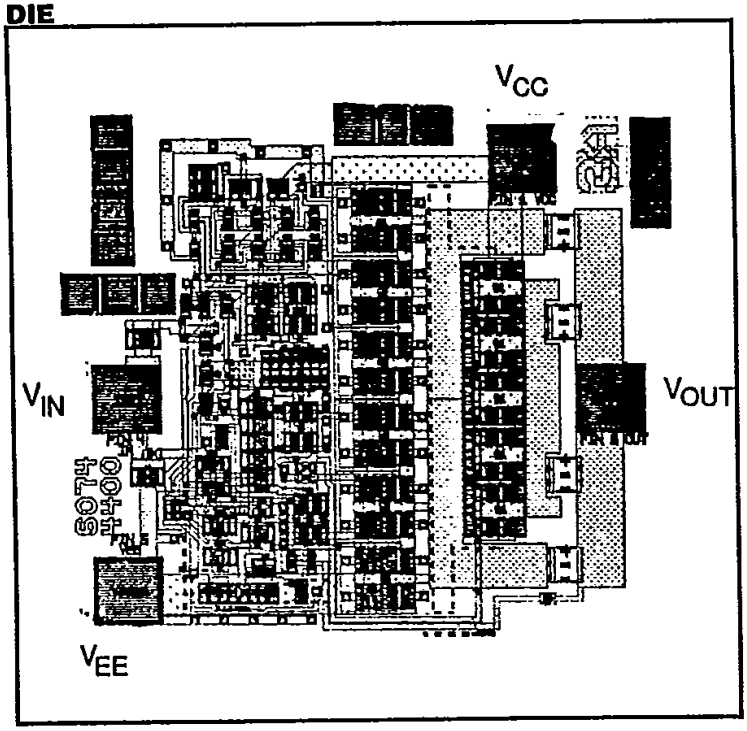
ELECTRICAL CHARACTERISTICS (V_S= ±5V, R_L= 50Ω, T_A = 25° C unless otherwise stated)

PARAMETER	SYM	CONDITIONS	VA033J MIN	VA033J TYP	VA033J MAX	UNITS
Output Offset Voltage	V_{OS}	V_{IN} = OV		8	20	mV
		0° ≤ T_A ≤ 70°C		12	30	
		-55°C ≤ T_A ≤ 125°C				
Input Bias Current	I_B	R_L =1kΩ		15	35	µA
		0° ≤ T_A ≤ 70°C		20	50	
		-55°C ≤ T_A ≤ 125°C				
Input Resistance	R_{IN}	V_{IN} =±3V R_L=1kΩ	30K	60K		Ω
Input Capacitance	C_{IN}			2.5		pF
Input Noise Voltage	e_N	10Hz to 2MHz		60		µV
Voltage Gain	A_V	V_{IN} = ±3V, R_L = 50Ω	0.85	0.88		V/V
		V_{IN} = ±3V, R_L =1kΩ	0.95	0.97		
		V_{IN} = ±3V, 0° ≤ T_A ≤ 70°C, R_L=1kΩ	0.94			
		V_{IN} = ±3V, -55°C ≤ T_A ≤ 125°C, R_L=1kΩ				
Output Voltage Swing	V_{OUT}	V_{IN} =+3.5V R_L=25Ω	±2.5			V
		V_{IN} =± 4V R_L=1kΩ	±3.5			
Output Resistance	R_{OUT}	R_L = 1k		6		Ω
Rise / Fall Time	t_r / t_f	(Figure 1) V_O = ± 0.25V		1.8		ns
Small Signal Bandwidth	BW	(Figure 1) R_L= 50Ω		300		MHz
Slew Rate	SR	(Figure 2) C_L =10pF V_{IN} =±3V R_L = 1k	1500	2000		V/µs
Full Power Bandwidth	FPBW	(Figure 1) C_L =10pF V_{IN} = 1VRMS R_L=1k		85		MHz
Supply Current	I_S	V_{IN} =0V		28	40	mA

WAFER TEST LIMITS (V_S= ±5V, T_A = 25° C unless otherwise stated)

PARAMETER	SYMBOL	CONDITIONS	VAO33XS LIMITS			UNITS
			MIN	TYP	MAX	
Output Offset Voltage	V_{OS}	V_{IN} = 0V R_L = 50Ω		10	30	mV
Input Bias Current	I_B	R_L= 1KΩ		30	50	µA
Input Resistance	R_{IN}			60K		Ω
Input Noise Voltage	C_N	10Hz to 2MHz		60		µV
Voltage Gain	A_V	R_L = 1KΩ V_{IN} = ±3.0V	0.93	0.97		V/V
Output Voltage Swing	V_{OUT}	V_{IN} = ±4V R_L= 1KΩ	±3.5			V
Output Resistance	R_{OUT}	R_L = 1KΩ		6		Ω
Rise/Fall Times	tr/tf	V_O= ±0.25V		1.8		ns
Small Signal Bandwidth	BW	R_L = 50Ω		300		MHz
Slew Rate	SR	C_L = 10pF V_{IN} = ±3.5V R_L = 1KΩ		2000		V/µs
Full Power Bandwidth	FPBW			85		MHz
Supply Current	I_S	V_{IN}= OV		28	40	mA

DIE



Die size = 0.050 X 0.050 inch (2500sq mils)
= 1.27 X 1.27mm (1.61sq mm)

DICE POLICY

Electrical Characteristics

Each die is electrically tested to the commercial or military grade DC parameters to guard band limits at 25°C to guarantee operation over the full temperature range.

Quality Assurance

All dice are 100% visually inspected to the requirement of MIL-STD-883C, Method 2010.2, Condition 3.

All dice are glass passivated to provide scratch protection, with only the bonding pads exposed.

All dice are provided with gold backing.

Shipping Packages/Order Information

All dice are packaged in die crates with individual compartments which prevent damage to the die during shipping. Minimum order for dice is 100, supplied only in multiples of 100.

Layout Considerations

In order to fully realize the high speed capability of the VA033, certain layout considerations need to be followed. A ground plane should be used since it is the best method for minimizing stray inductance and distributed circuit capacitance. All connections to the amplifier should be kept as short as possible including the power supplies which should be bypassed with 0.1µF capacitors; or better yet, a capacitor combination of 1µF to 10µF aluminum electrolytic or solid tantalum in parallel with a 0.01µF ceramic.

Figure 1: DC/AC Test Circuits

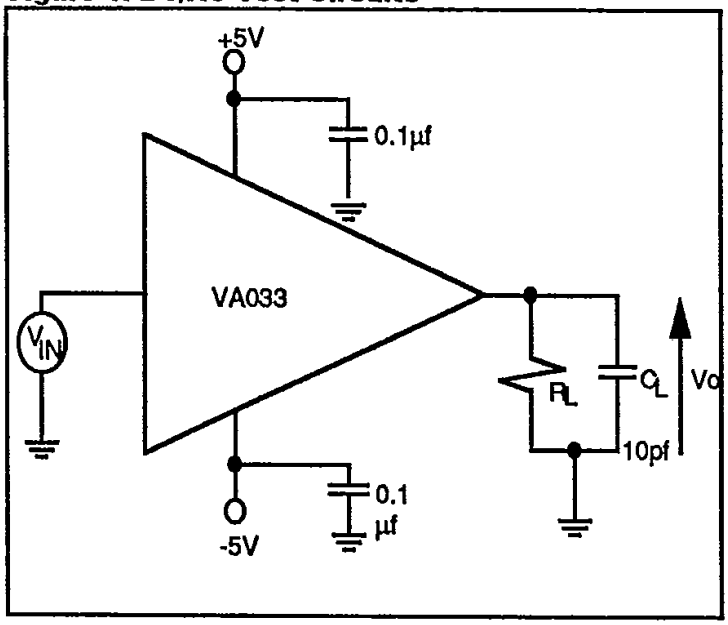


Figure 2: AC Response Characteristics

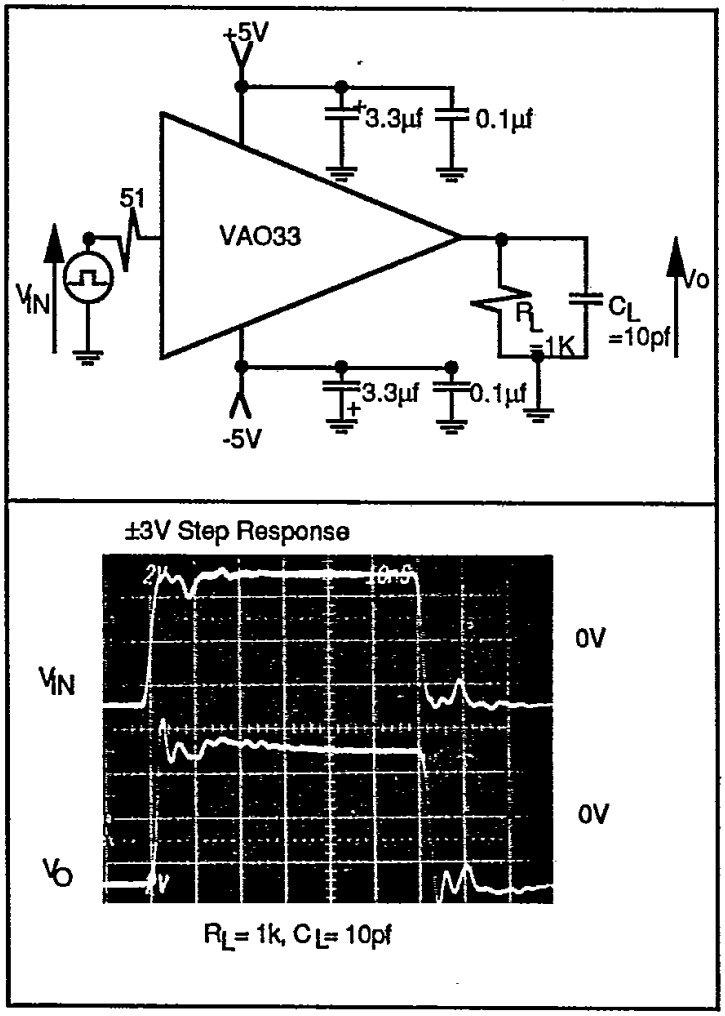
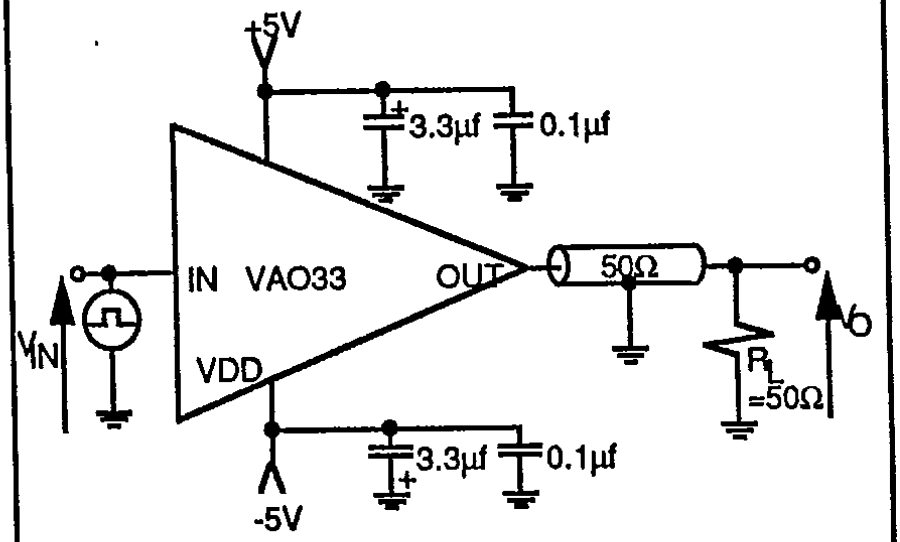
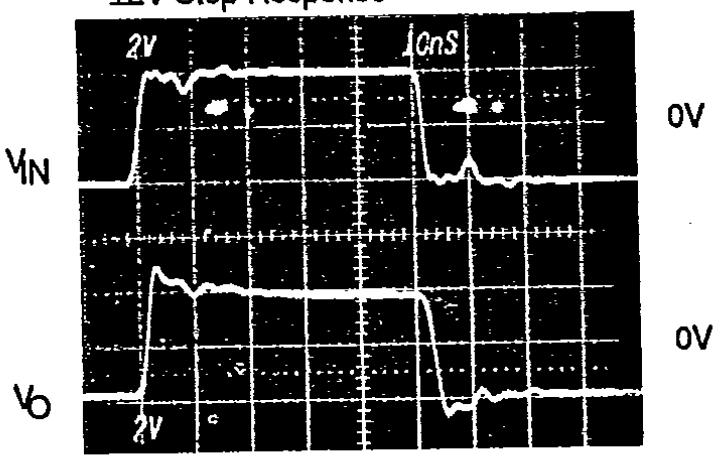


Figure 3: AC Response Characteristics

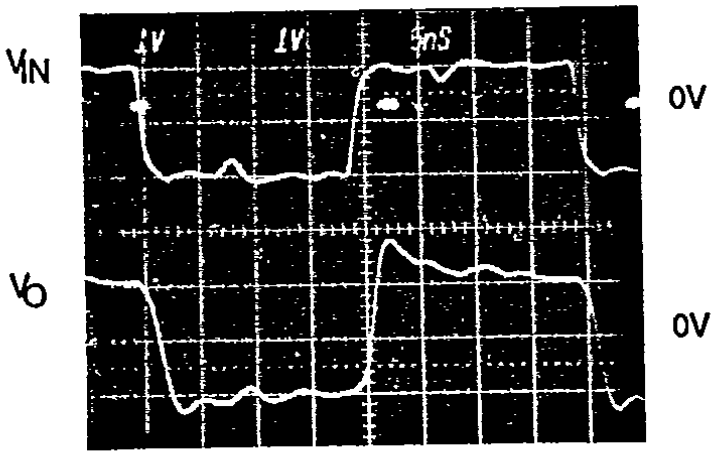


±2V Step Response



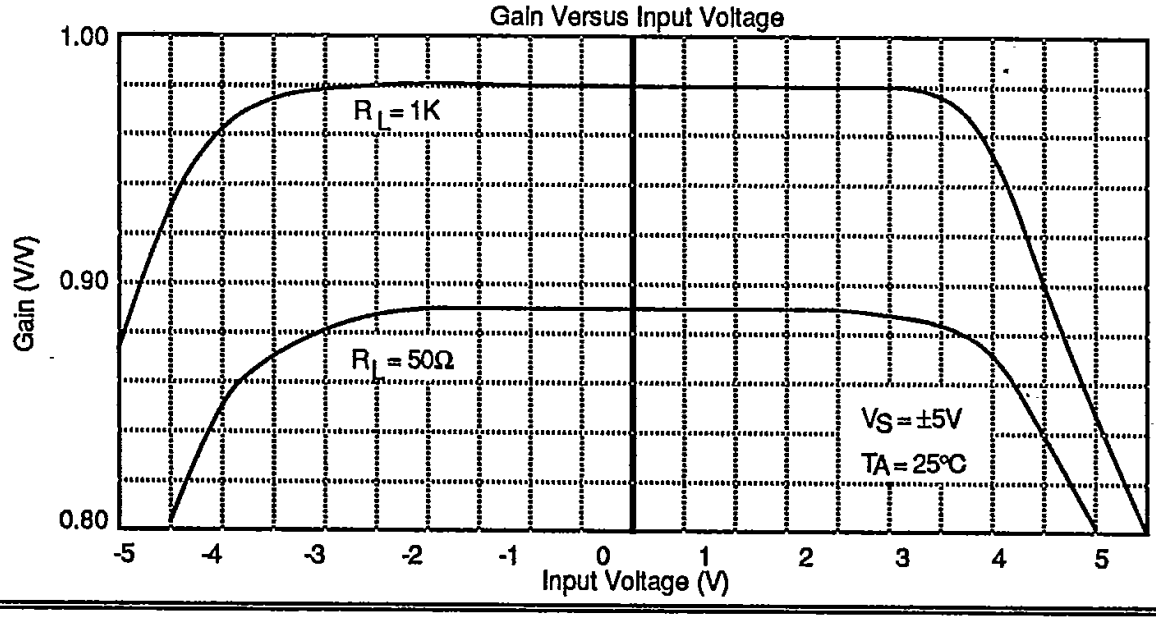
$R_L = 50\Omega$

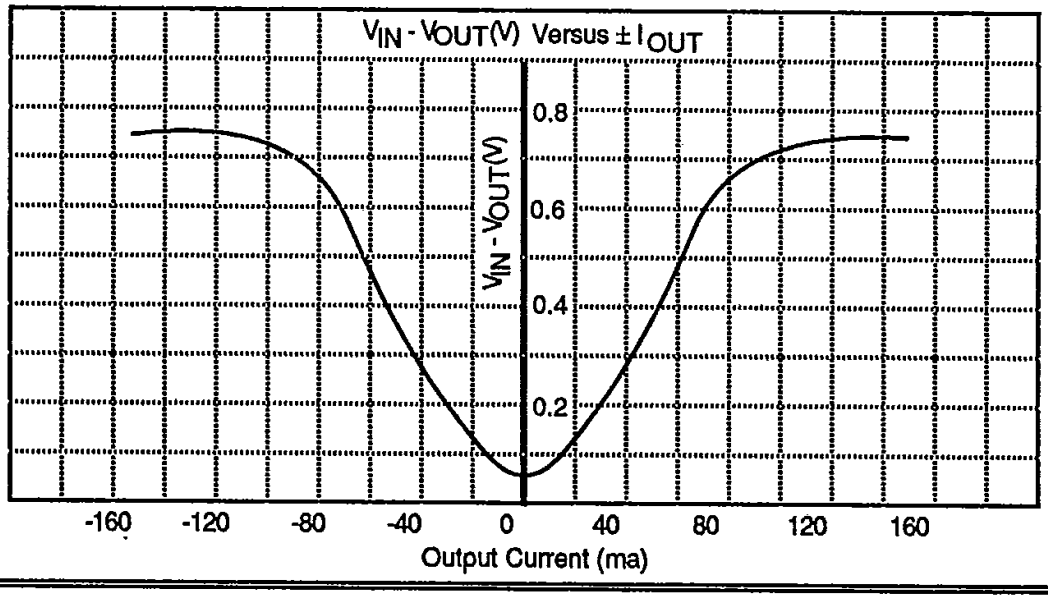
25MHz Square Wave Response

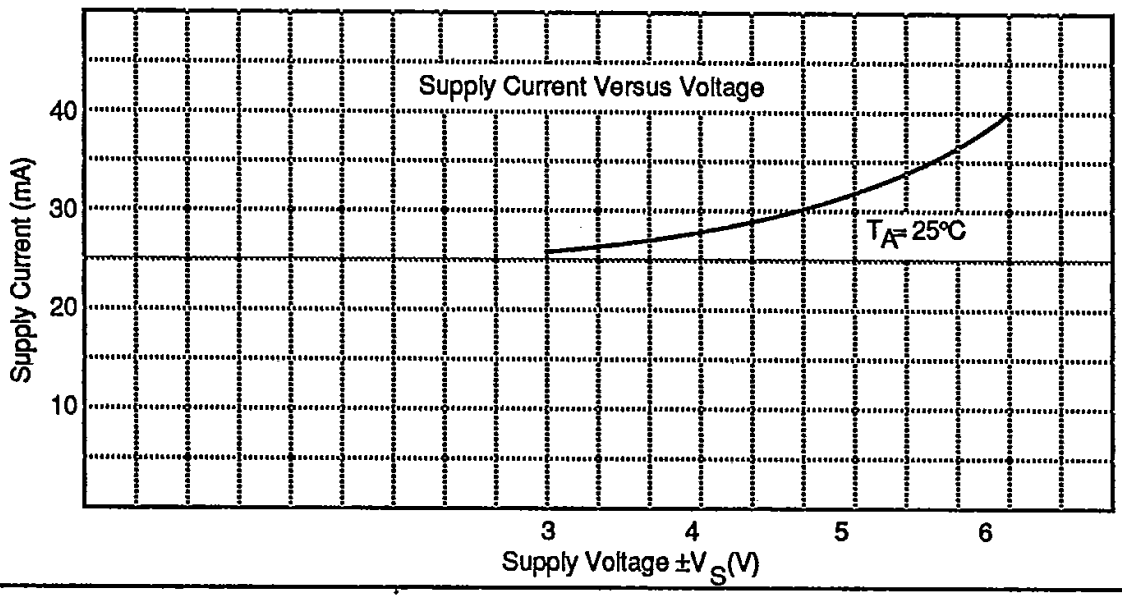


$V_{IN} = \pm 1V, R_L = 50\Omega$

TYPICAL PERFORMANCE CURVES







TYPICAL PERFORMANCE CURVES