

32K x 8 Bit Static RAM

FEATURES

- Fast Access Time: 80,100,120 ns (max.)
- Low Power Dissipation  
Standby (CMOS): 10µW (typ.) L/LL-Version  
Operating: 247.5mW (max.)
- Single 5V ± 10% Power Supply
- TTL compatible inputs and outputs
- Fully Static Operation  
— No clock or refresh required
- Three State Output
- Low Data Retention Voltage: 2V (min.)
- JEDEC Standard pin Configuration  
KM62256AP/ALP/ALP-L: 28-pin DIP (600 mil.)  
KM62256AG/ALG/ALG-L: 28-pin SOP (330 mil.)

GENERAL DESCRIPTION

The KM62256A/AL/AL-L is 262,144-bit high-speed Static Random Access Memory organized as 32,768 words by 8 bit.

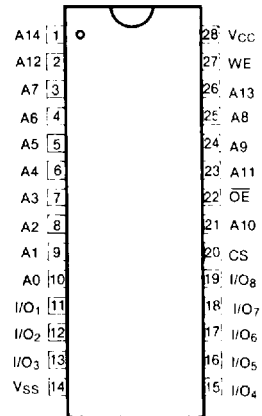
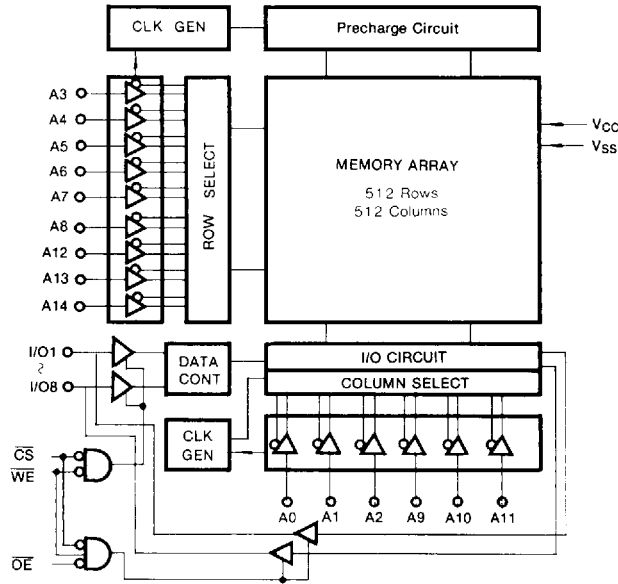
The device is fabricated using Samsung's advanced CMOS technology with polyresistors.

The KM62256A/AL/AL-L has an output enable input for precise control of the data outputs. It also has a chip select input for the minimum current power down mode. The KM62256A/AL/AL-L has been designed for high speed and low power applications.

It is particularly well suited for battery back-up non-volatile memory applications.

FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATION



Pin Name	Pin Function
A <sub>0</sub> -A <sub>14</sub>	Address Inputs
WE	Write Enable
CS	Chip Select
OE	Output Enable
I/O <sub>1</sub> -I/O <sub>8</sub>	Data Input/Outputs
V <sub>CC</sub>	Power (+ 5V)
V <sub>SS</sub>	Ground

## ABSOLUTE MAXIMUM RATINGS\*

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to $V_{SS}$	$V_{IN}, V_{OUT}$	-0.5 to 7.0	V
Voltage on $V_{CC}$ Supply Relative to $V_{SS}$	$V_{CC}$	-0.5 to 7.0	V
Power Dissipation	$P_D$	1.0	W
Storage Temperature	$T_{stg}$	-65 to +150	°C
Operating Temperature	$T_A$	0 to 70	°C
Soldering Temperature and Time	$T_{solder}$	260°C, 10 sec (Lead only)	—

\* Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED OPERATING CONDITIONS ( $T_A = 0$  to 70°C)

Item	Symbol	Min	Typ	Max	Unit
Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V
Ground	$V_{SS}$	0	0	0	V
Input High Voltage	$V_{IH}$	2.2		$V_{CC} + 0.5$	V
Input Low Voltage	$V_{IL}$	-0.5*		0.8	V

\*  $V_{IL}(\text{min.}) = -3.0\text{V}$  for  $\leq 50\text{ns}$  pulse

## DC AND OPERATING CHARACTERISTICS

( $T_A = 0$  to 70°C,  $V_{CC} = 5\text{V} \pm 10\%$ , unless otherwise specified)

Item	Symbol	Test Conditions	Min	Typ*	Max	Unit
Input Leakage Current	$I_{LI}$	$V_{IN} = V_{SS}$ to $V_{CC}$	-1		1	$\mu\text{A}$
Output Leakage Current	$I_{LO}$	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ $V_{I/O} = V_{SS}$ to $V_{CC}$	-1		1	$\mu\text{A}$
Operating Power Supply Current	$I_{CC1}$	$\overline{CS} = V_{IL}$ , $V_{IN} = V_{IH}$ or $V_{IL}$ $I_{I/O} = 0\text{mA}$			45	$\text{mA}$
Average Operating Current	$I_{CC2}$	Min Cycle, 100% Duty, $\overline{CS} = V_{IL}$ $I_{I/O} = 0\text{mA}$		35	70	$\text{mA}$
Standby Power Supply Current	$I_{SB}$	$\overline{CS} = V_{IH}$			2	$\text{mA}$
	$I_{SB1}$	$\overline{CS} \geq V_{CC} - 0.2\text{V}$ , $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$			1	$\text{mA}$
			L		2	100
	LL			2	50	$\mu\text{A}$
Output Low Voltage	$V_{OL}$	$I_{OL} = 2.1\text{mA}$			0.4	V
Output High Voltage	$V_{OH}$	$I_{OH} = -1\text{mA}$	2.4			V

\* Typ.:  $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$

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**CAPACITANCE** (f = 1MHz, T<sub>A</sub> = 25°C)

Item	Symbol	Test Condition	Min	Max	Unit
Input Capacitance	C <sub>IN</sub>	V <sub>IN</sub> = 0V	—	6	pF
Input/Output Capacitance	C <sub>I/O</sub>	V <sub>I/O</sub> = 0V	—	8	pF

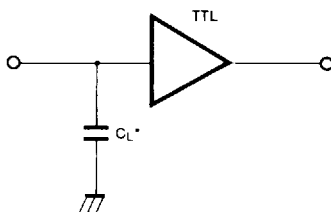
\* Note: Capacitance is sampled and not 100% tested.

**AC CHARACTERISTICS**

**TEST CONDITIONS** (T<sub>a</sub> = 0 to 70°C, V<sub>CC</sub> = 5V ± 10%, unless otherwise specified)

Parameter	Value
Input Pulse Level	0.8 to 2.4V
Input Rise and Fall Time	5ns
Input and Output Timing Reference Levels	1.5V
Output Load	C <sub>L</sub> = 100pF + 1 TTL

**TEST CIRCUIT**



\* Including Scope and Jig Capacitance

**READ CYCLE**

Parameter	Symbol	KM62256A-8 KM62256AL-8		KM62256A-10 KM62256AL-10L		KM62256A-12 KM62256AL-12L		Unit
		Min	Max	Min	Max	Min	Max	
		Read Cycle Time	t <sub>RC</sub>	80		100		
Address Access Time	t <sub>AA</sub>		80		100		120	ns
Chip Select to Output	t <sub>CO</sub>		80		100		120	ns
Output Enable to Valid Output	t <sub>OE</sub>		40		50		60	ns
Chip Enable to Low-Z Output	t <sub>LZ</sub>	5		10		10		ns
Output Enable to Low-Z Output	t <sub>OLZ</sub>	5		5		5		ns
Chip Disable to High-Z Output	t <sub>HZ</sub>	0	30	0	35	0	40	ns
Output Disable to High-Z Output	t <sub>OHZ</sub>	0	30	0	35	0	40	ns
Output Hold from Address Change	t <sub>OH</sub>	5		10		10		ns

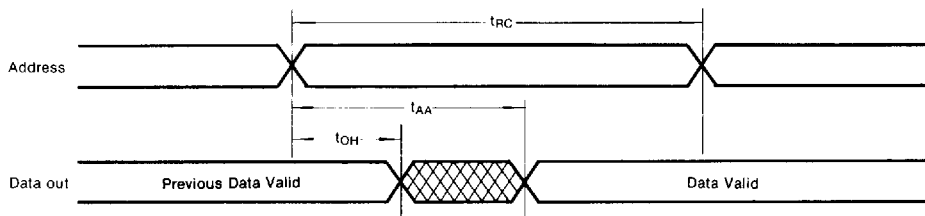
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## WRITE CYCLE

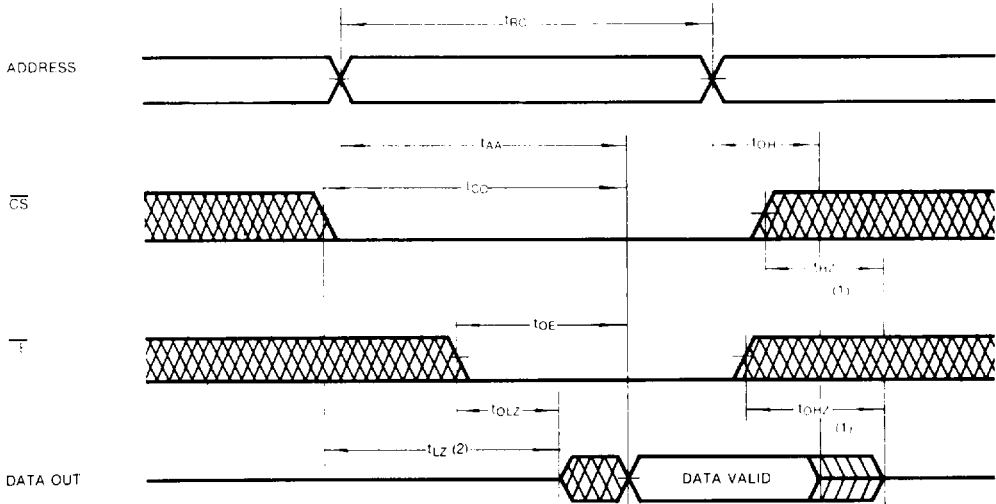
Parameter	Symbol	KM62256A-8 KM62256AL-8 KM62256AL-8L		KM62256A-10 KM62256AL-10 KM62256AL-10L		KM62256A-12 KM62256AL-12 KM62256AL-12L		Unit
		Min	Max	Min	Max	Min	Max	
		Write Cycle Time	$t_{WC}$	80		100		
Chip Select to End of Write	$t_{CW}$	70		80		85		ns
Address Set-Up Time	$t_{AS}$	0		0		0		ns
Address Valid to End of Write	$t_{AW}$	70		80		85		ns
Write Pulse Width	$t_{WP}$	55		60		70		ns
Write Recovery Time	$t_{WR}$	0		0		0		ns
Write to Output High-Z	$t_{WZ}$	0	30	0	35	0	40	ns
Data to Write Time Overlap	$t_{DW}$	40		50		60		ns
Data Hold from Write Time	$t_{DH}$	0		0		0		ns
End Write to Output Low-Z	$t_{OW}$	5		10		10		ns

## TIMING DIAGRAMS

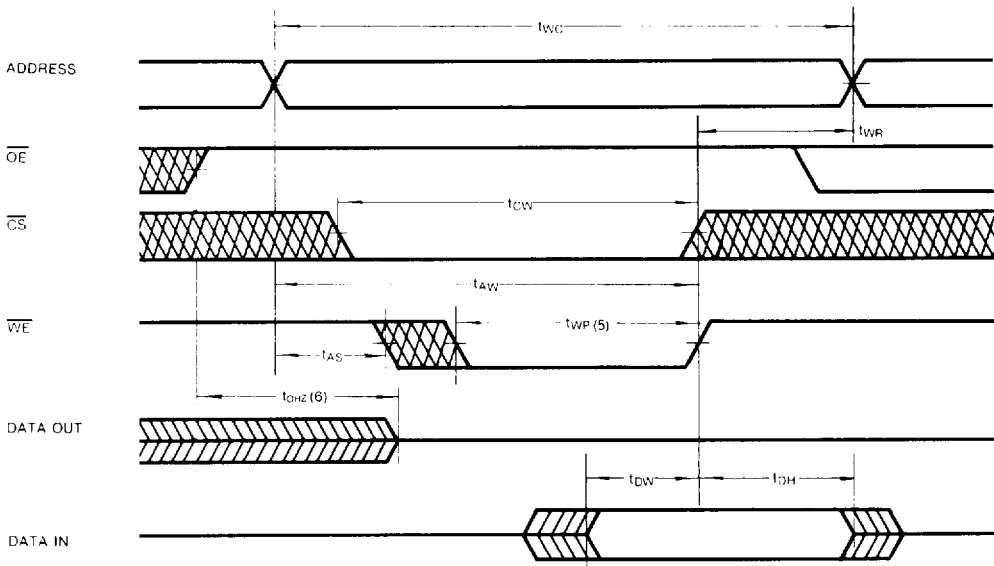
## TIMING WAVEFORM OF READ CYCLE NO: 1

(CS = OE = V<sub>IL</sub>, WE = V<sub>IH</sub>)

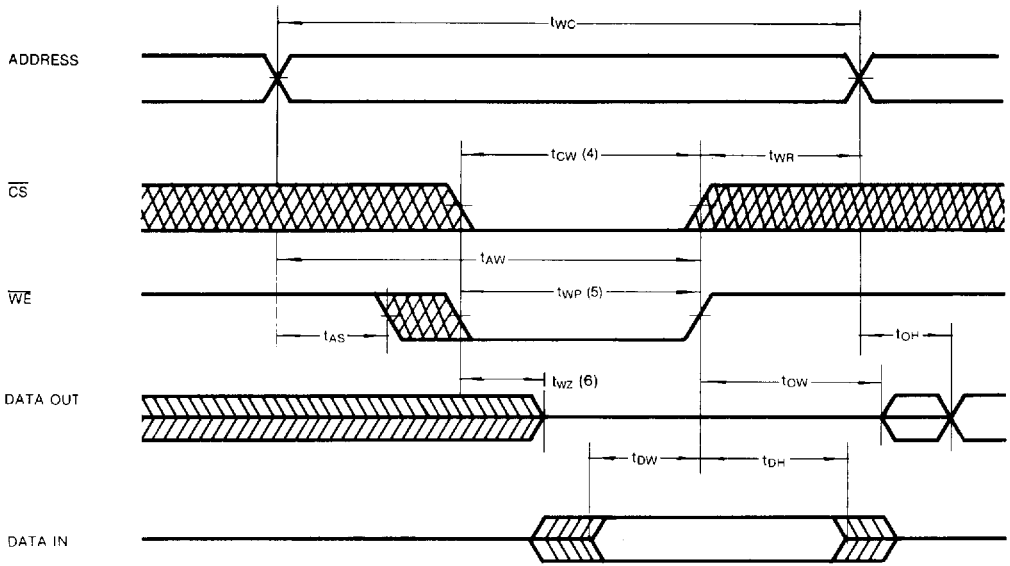
TIMING WAVEFORM OF READ CYCLE NO. 2 ( $\overline{WE} = V_{IH}$ ) (Note 1, 2, 3, 4)



TIMING WAVEFORM OF WRITE CYCLE NO. 3 ( $\overline{OE}$  Clocked) (Note 5, 6, 7, 8)



**TIMING WAVEFORM OF WRITE CYCLE NO. 4 ( $\overline{OE}$  Low Fixed) (Note 5, 6, 7, 8, 9)**



- Notes:**
1.  $t_{HZ}$  and  $t_{OHZ}$  are defined as the time at which the outputs achieve the open circuit condition and are not referenced to the  $V_{OH}$  or  $V_{OL}$  Level.
  2. At any given temperature and voltage condition,  $t_{HZ}(\max)$  is less than  $t_{LZ}(\min)$  both for a given device and from device to device.
  3.  $\overline{WE}$  is high for Read Cycle.
  4. Address valid prior to or coincident with  $\overline{CS}$  transition Low.
  5. A write occurs during the overlap ( $t_{WP}$ ) of a low  $\overline{CS}$  and low  $\overline{WE}$ .
  6. During this period, I/O pins are in the output state. The input signals out of phase must not applied.
  7.  $\overline{CS}$  or  $\overline{WE}$  must be high during address transition state.
  8. If  $\overline{OE}$  is high, I/O pins remain in a high-impedance state.
  9.  $\overline{OE}$  is continuously low. ( $\overline{OE} = V_{IL}$ )

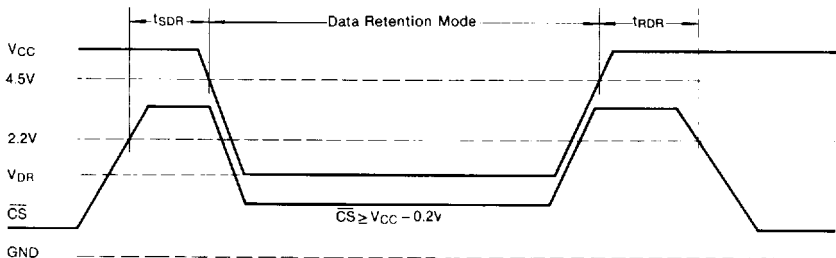
**FUNCTIONAL DESCRIPTION**

$\overline{CS}$	$\overline{WE}$	$\overline{OE}$	Mode	I/O Pin	$V_{CC}$ Current
H	X*	X	Power Down	High-Z	$I_{SB}, I_{SB1}$
L	H	H	Output Disable	High-Z	$I_{CC}$
L	H	L	Read	$D_{OUT}$	$I_{CC}$
L	L	X	Write	$D_{IN}$	$I_{CC}$

\* Note: X means Don't Care.

DATA RETENTION CHARACTERISTICS ( $T_A = 0$  to  $70^\circ\text{C}$ )

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
$V_{CC}$ for Data Retention	$V_{DR}$	$\overline{CS} \geq V_{CC} - 0.2V$	2.0		5.5	V
Data Retention Current	$I_{DR}$	$V_{CC} = 3V$ $\overline{CS} \geq V_{CC} - 0.2V$	L	1	50	$\mu\text{A}$
			LL	1	20*	$\mu\text{A}$
Data Retention Set-up Time	$t_{SDR}$	See Data Retention Wave forms (below)	0			ns
Recovery Time	$t_{RDR}$		$t_{RC}^{**}$			ns

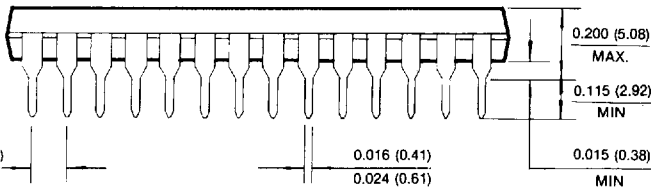
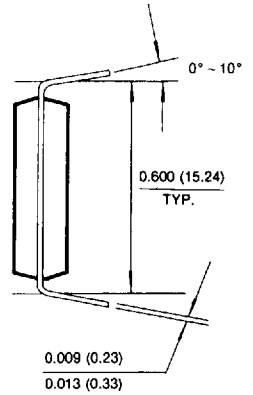
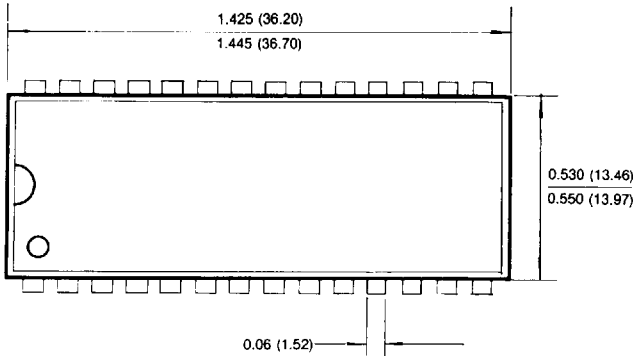
\*  $3\mu\text{A}$  (max.) at  $0^\circ\text{C} \sim 40^\circ\text{C}$ \*\*  $t_{RC}$  = Read cycle timeDATA RETENTION WAVEFORM ( $\overline{CS}$  Controlled)

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**PACKAGE DIMENSIONS**

**28 PIN PLASTIC DUAL IN LINE PACKAGE**

Unit: Inches (Millimeters)



**28 PIN PLASTIC SMALL OUT LINE PACKAGE**

