iT3018E

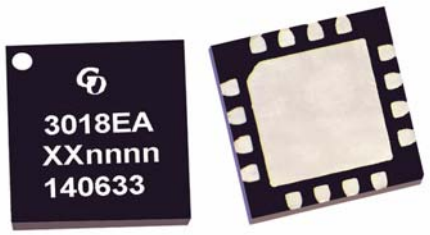
12.5-Gb/s High-Gain RX Limiter Amplifier

Description

The iT3018E is a RoHS-6-compliant limiting amplifier for use as a post amplifier in OC-192 and STM-64 optical receivers. Differential signals as small as +/-6 mVpp can be amplified to 2.2 Vpp differential. The device includes offset correction and output voltage control. Both AC and DC coupling are allowed at both input and output. The high sensitivity of the iT3018E allows the device to be used at the output of a transimpedance amplifier.

Features

- 3 dB bandwidth: 10 GHz
- Differential gain: 50 dB
- Saturated output: 1.1 Vpp, each output into 50 ohms
- Input sensitivity 3.0 mVpp at BER<1E-12
- Single bias supply: -5.2 V
- Power consumption: 624 mW
- Bias current: 120 mA
- DC offset correction
- Amplitude voltage control
- Low RMS jitter
- RoHS-6-compliant 4x4 mm QFN (MO-220) package



Absolute Maximum Ratings

Symbol	Parameters/conditions	Min.	Max.	Units
Vee1,2	Power supply voltage	-8	0	V
Vd	Applied voltage at data input (differential)		3	V
Vm	Applied voltage at data input (single ended)		1.5	V
Ioffset(+),(-)	Offset control current		5	mA
Tch	Maximum channel temperature		150	°C
Tstg	Storage temperature	-65	150	°C

Recommended Operating Conditions

Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
Tc	Operating temperature range (Tcase)	0		85	°C
Vee1	Power supply voltage	-5.45	-5.2	-4.95	V
Vee2	Power supply voltage	-5.45	-5.2	-4.95	V
Iee1+Iee2	Total bias supply current	102	120	132	mA
Voffset (+)	Offset control voltage	-5		5	V
Voffset (-)	Offset control voltage	-5		5	V
Vctrl	Amplitude voltage control	-5.2		0	V
Vd	Applied peak to peak voltage at data input (differential)	6		1000	mV
Vm	Applied peak to peak voltage at data input (single ended)	12		1000	mV
	Input/output interface	AC and DC coupled			
Vindc	DC input voltage (with DC-coupled input)	-0.5		0.5	V
R	Bit rate			12.5	Gb/s

Electrical Characteristics

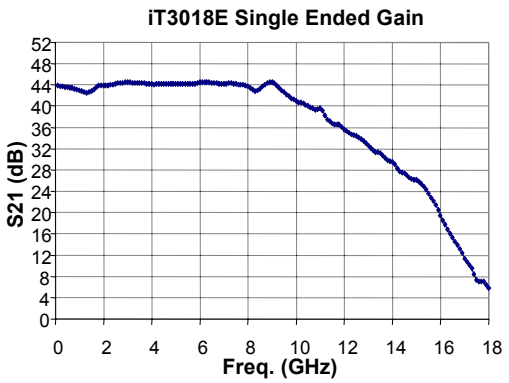
At ambient temperature
Vee1,2 = -5.2 V

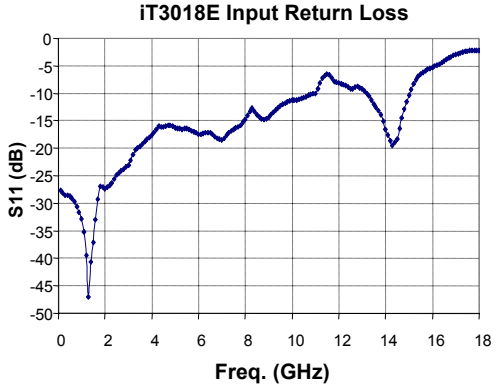
Symbol	Parameters/conditions	Min.	Typ.	Max.	Units
P	Power consumption	530	624	686	mW
G	Differential small signal gain	49	50		dB
B3dB	3 dB bandwidth	9	10		GHz
RLin	Input return loss (up to 10 GHz)	10	20		dB
RLout	Output return loss (up to 10 GHz)	10	15		dB
Vin	Input sensitivity -- differential input (BER<1E-12, 2^{23}-1PRBS, 12.5 Gb/s)	+/-3			mVpp
Vout	Output peak to peak voltage (either Q or /Q)				
	Output DC coupled (Vctrl=0 V for max. voltage)	1010	1100		mVpp
	Output AC coupled (Vctrl=0 V for max. voltage)	740	800		mVpp
ΔVout	Vout sensitivity vs bias (Vee=-5.2 V +/-5%)			+/-11	%
Voutdc	DC output voltage (DC coupled to 50 ohm load)	-750	-650	-550	mV
Trse	Rise time (20% - 80%)		24	30	ps
Tfse	Fall time (20% - 80%)		22	26	ps
Jpp	Jitter peak to peak		12	17	ps
Jrms*	Jitter RMS degradation Jrms*=(Jmeas^2-Jthru^2)^.5		1.2	1.8	ps

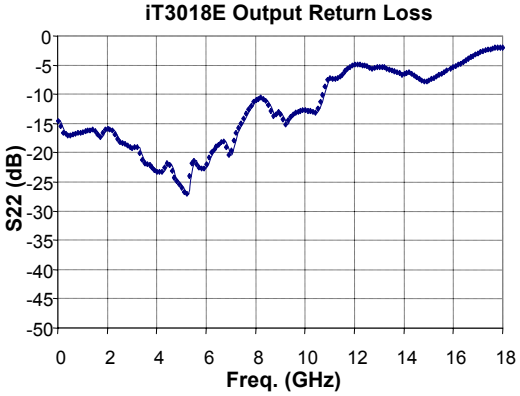
S-Parameter Data

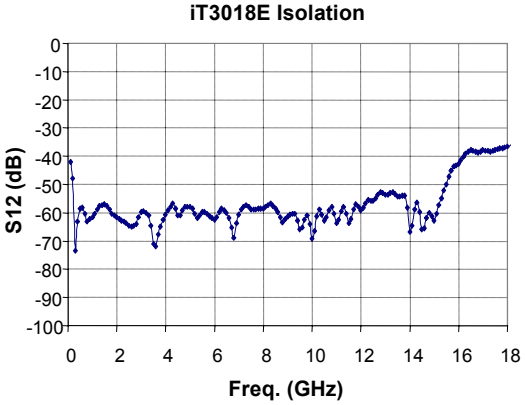
Measured on connectorized evaluation board

Vee1 = Vee2 = -5.2 V
Iee1+Iee2 = 120 mA



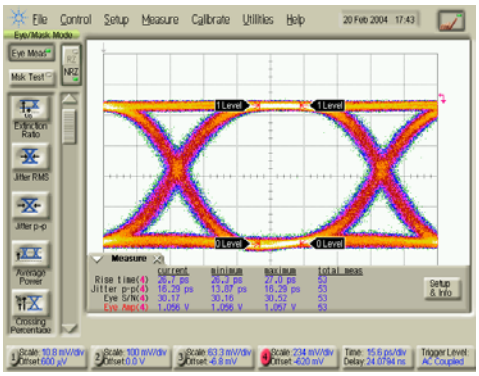




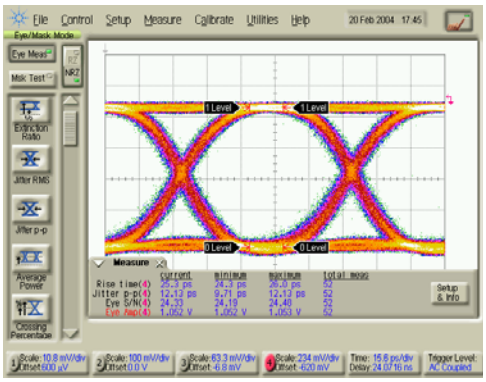


Eye Diagram Performance

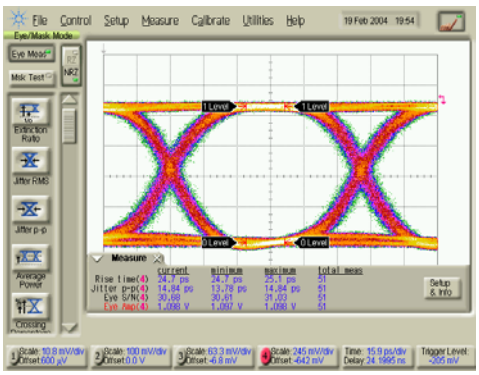
Vee1 = Vee2 = -5.2 V
Iee1+Iee2 = 120 mA



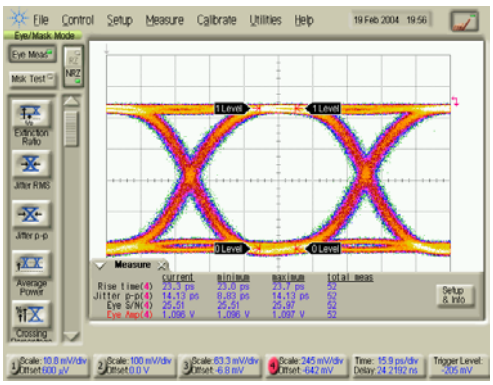
Bit rate: 10.7 Gb/s
Vin=+/-5 mVpp, Vout=+/-1 Vpp



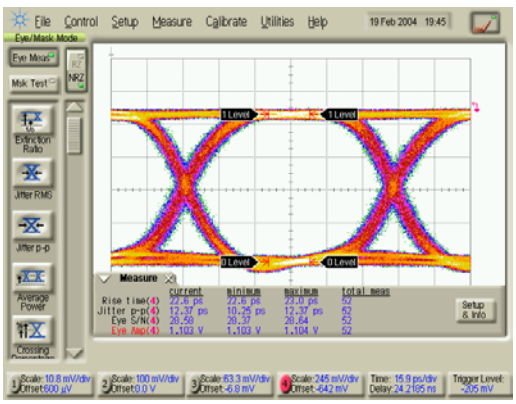
Bit rate: 12.5 Gb/s
Vin=+/-5 mVpp, Vout=+/-1Vpp



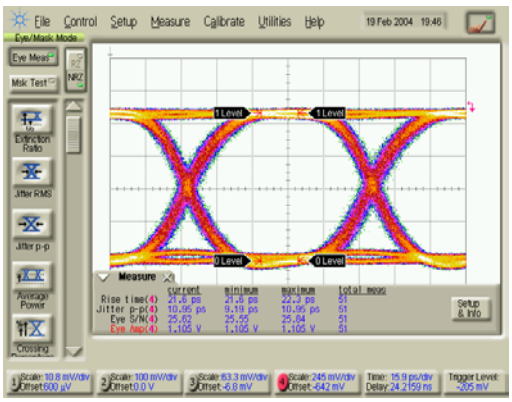
Bit rate: 10.7 Gb/s
Vin=+/-8 mVpp, Vout=+/-1.1 mVpp



Bit rate: 12.5 Gb/s
Vin=+/-8 mVpp, Vout=+/-1.1 mVpp

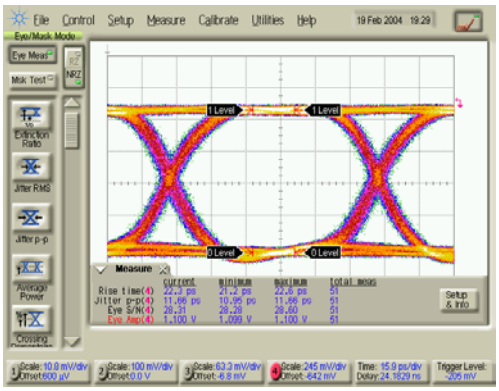


Bit rate: 10.7 Gb/s
Vin=+/-30 mVpp, Vout=+/-1.1 Vpp

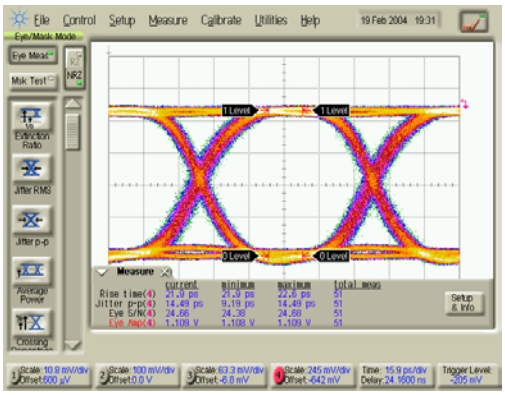


Bit rate: 12.5 Gb/s
Vin=+/-30 mVpp, Vout=+/-1.1 Vpp

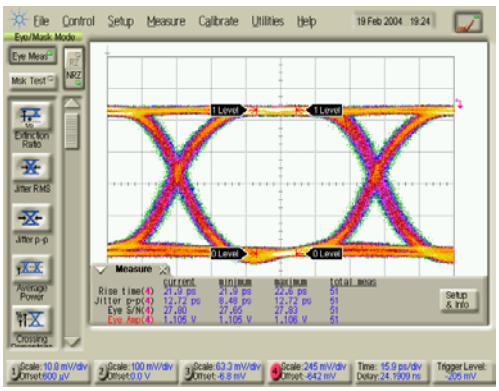
Eye Diagram Performance vs. Input Voltage (cont.)



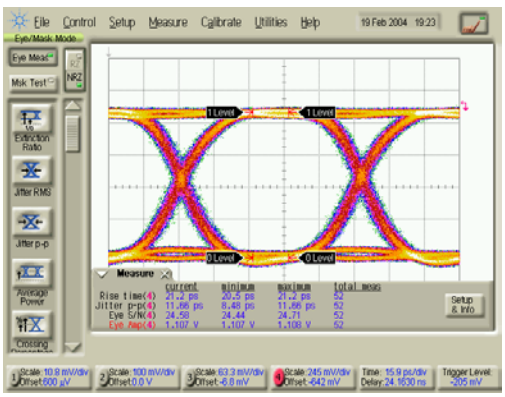
Bit rate: 10.7 Gb/s
Vin=+/-200 mVpp, Vout=+/-1.1 Vpp



Bit rate: 12.5 Gb/s
Vin=+/-200 mVpp, Vout=+/-1.1 Vpp



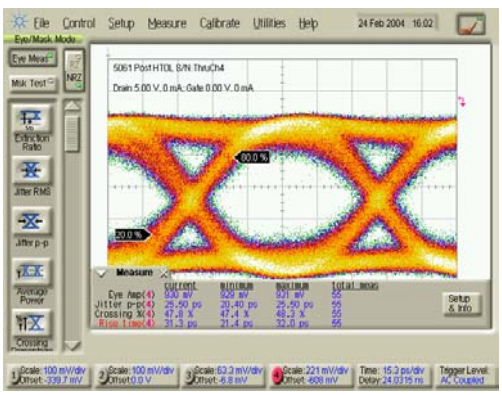
Bit rate: 10.7 Gb/s
Vin=+/-1 Vpp, Vout=+/-1.1 Vpp



Bit rate: 12.5 Gb/s
Vin=+/-1 Vpp, Vout=+/-1.1 Vpp

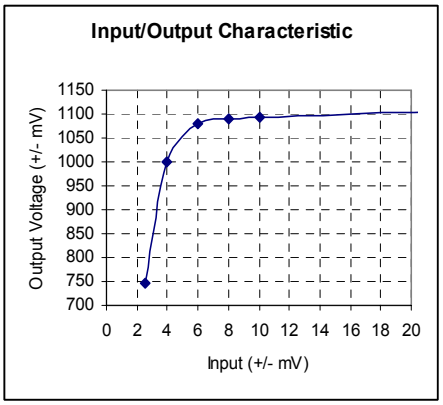
Input Sensitivity

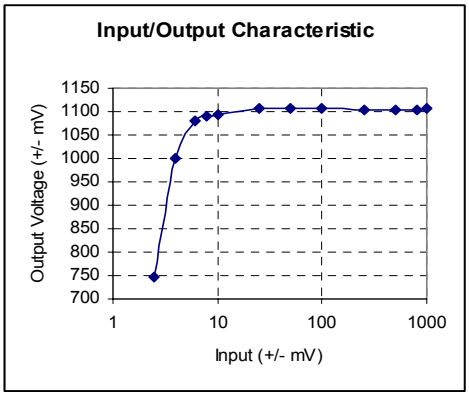
Vee1 = Vee2 = -5.2 V
Iee1+Iee2 = 120 mA

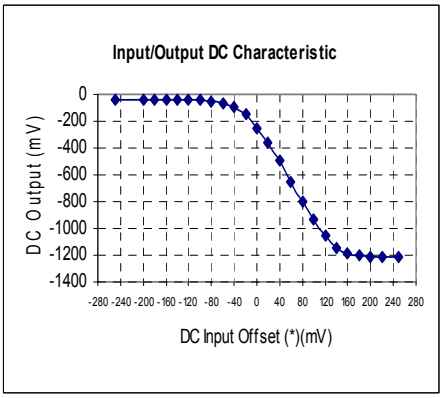


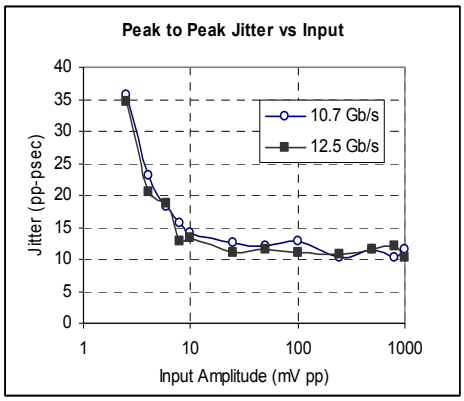
Input Sensitivity= 3mVpp Differential input up to 12.5 Gb/s
BER<1E-12. Output voltage = 930 mVpp single-ended

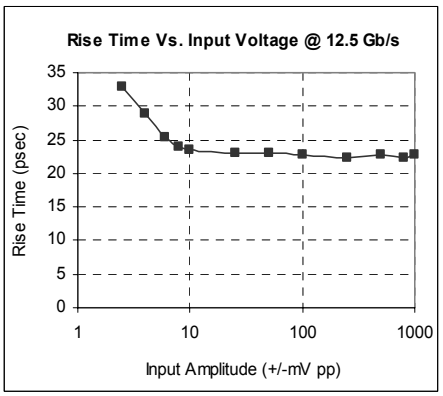
Performance As Function Of Input Voltage

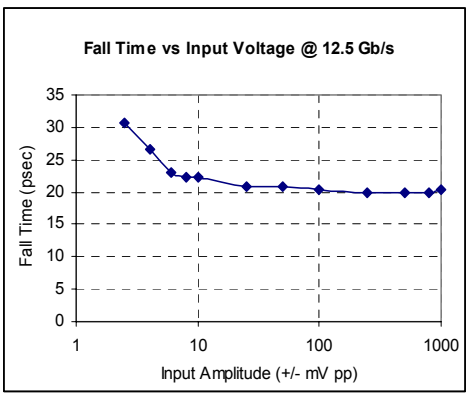






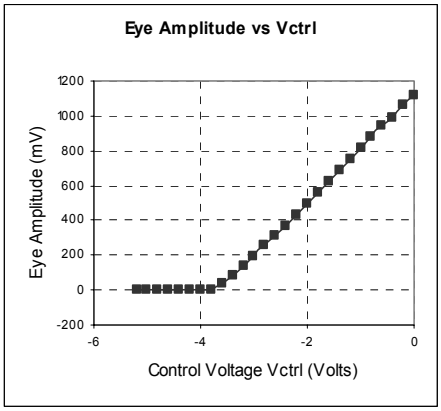


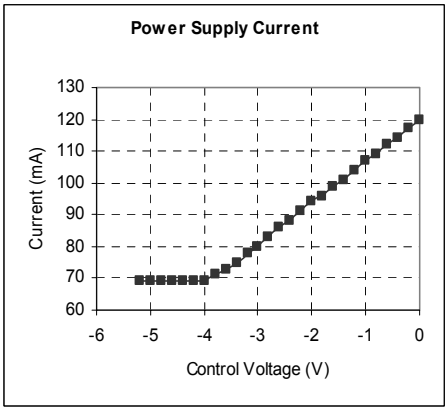


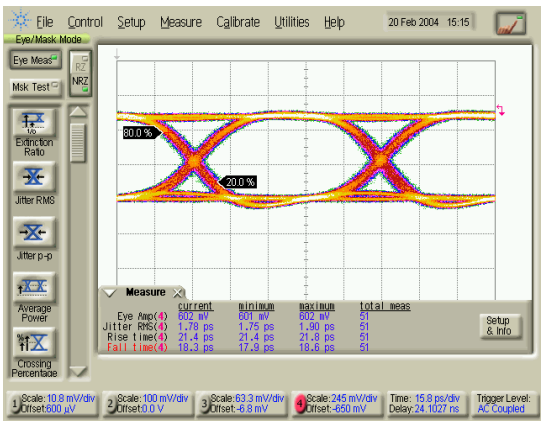


(*) Input applied to the offset control pin (Voffset1), open output.

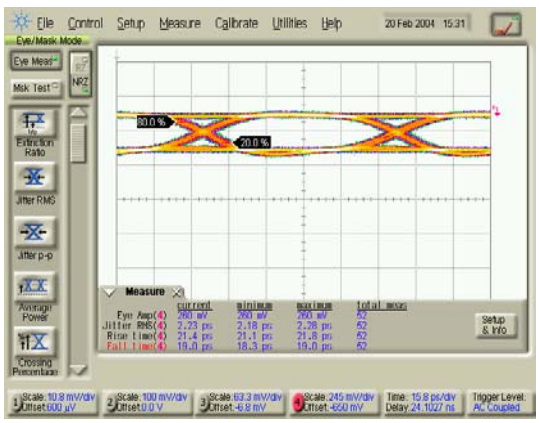
Output Voltage Control







Bit rate: 12.5 Gb/s, Vtrl=-1.7 V
Vin = +/-200 mVpp, Vout = +/-602 mVpp

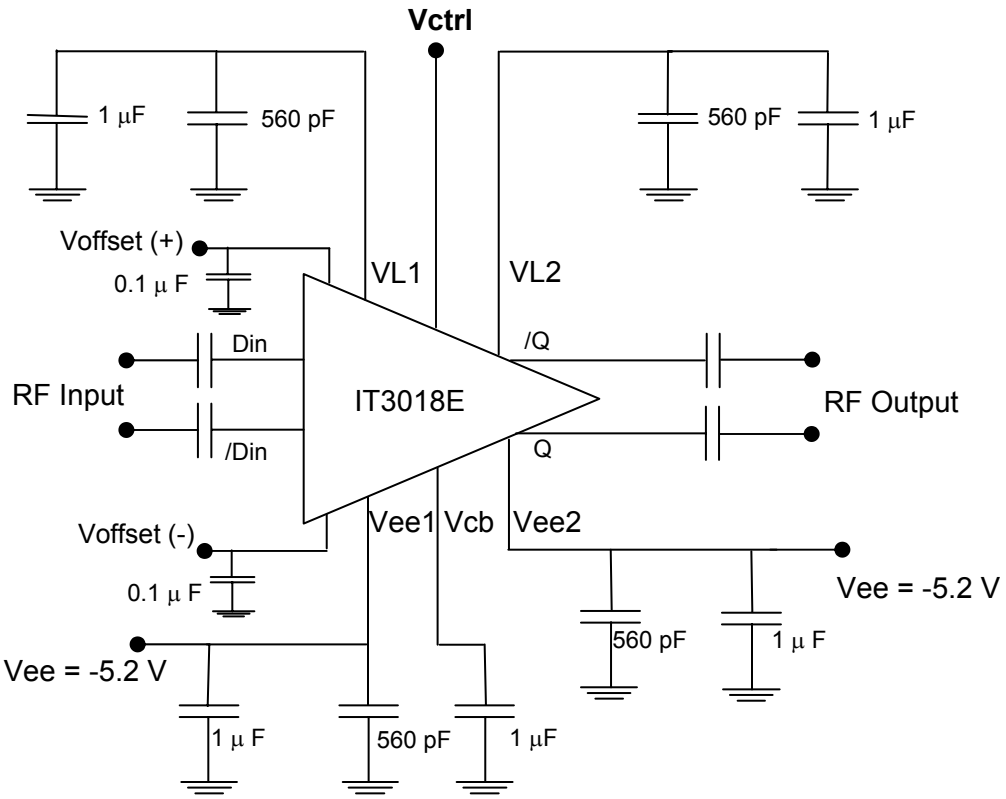


Bit rate: 12.5 Gb/s, Vtrl=-2.8 V
Vin = +/-200 mVpp, Vou t= +/-260 mVpp

Recommended Operational Setup

Apply –5.2 V at Vee1 and Vee2
Apply 0 V at Vctrl for maximum output

DC blocking capacitors optional



"E" Package Drawings, Pinouts, Marking

Notes:
Dimensions in inches (mm)

Tolerances are ±0.0039 in. (0.100 mm)

Package drawing encompasses JEDEC MO-220 Version VGGC-2.

See iTerra Application Note 10 for recommended pad layout. RoHS parts are backward compatible if application note pad layout is followed.

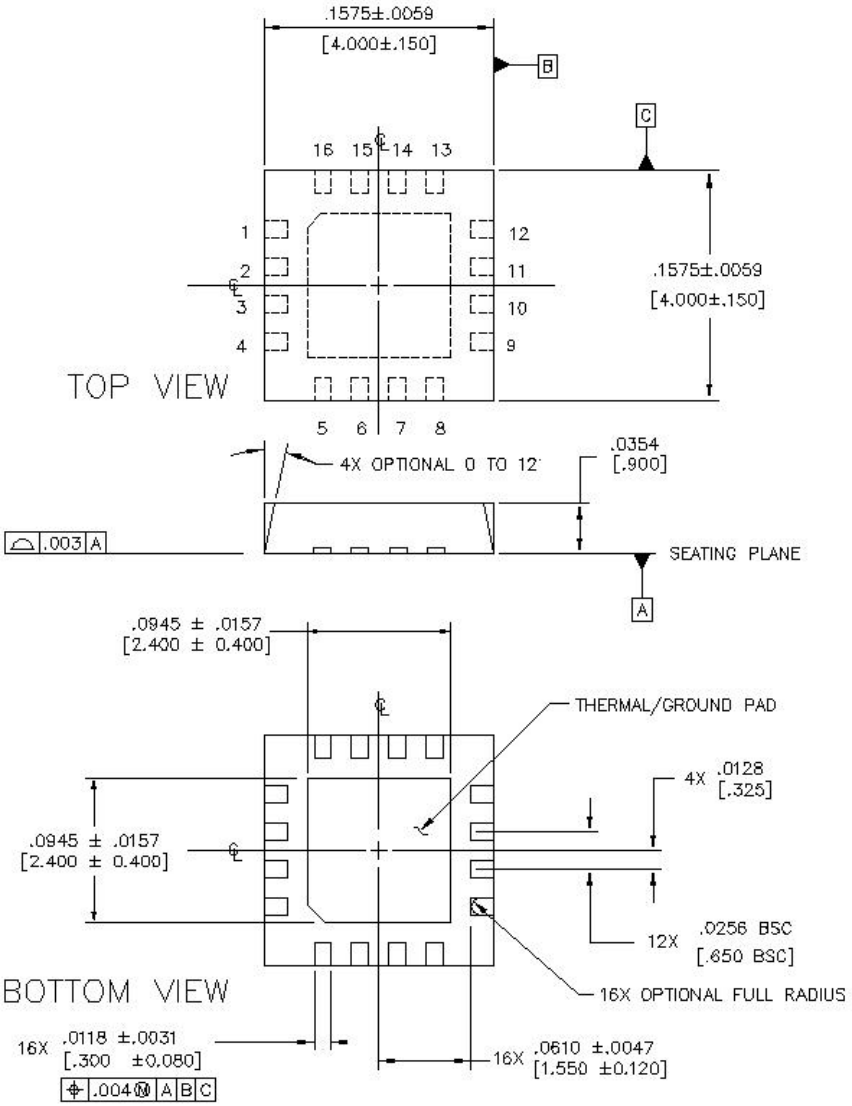
Lead frame material is copper alloy.

Mold compound is UL94V0 compliant.

Lead finish is NiPdAu.

Marking Information
iTerra
MMMMEA
XXNNNN
LLYYWW

Where,
MMMM = part no.
E = Package Type
A =Temp. Range
XX = Wafer Lot
NNNN = Ser. No.
LLYYWW =MFG D/C



Pinouts

P1: GND	P9: GND
P2: Din (RF input)	P10: Q (RF Out)
P3: /Din (/RF input)	P11: /Q (/RF Out)
P4: GND	P12: GND
P5: Voffset (-)	P13: VL1
P6: Vee1	P14: Vctrl (voltage control)
P7: Vcb	P15: VL2
P8: Vee2	P16: Voffset (+)