AN-6747

Applying FAN6747 to Control a Flyback Power Supply with Peak Current Output

1. Introduction

Highly integrated PWM controller, FAN6747, is optimized for applications with motor load, such as printers and scanners, that inherently impose some kind of overload condition on the power supply during acceleration mode. FAN6747 provides a two-level OCP function that allows the SMPS to stably deliver peak power during the motor acceleration without causing premature shutdown, while protecting the SMPS from overload condition.

Green-mode and burst-mode functions with a low operating current maximize the light-load efficiency so that the power supply can meet stringent standby power regulations.

The frequency-hopping function reduces electro-magnetic interference (EMI) of a power supply by spreading the energy over a wider frequency range. The constant power limit function minimizes the component stress in abnormal condition and helps optimize the power stage. Protection functions such as OCP, OLP, OVP, and OTP are fully integrated into FAN6747, which improves the SMPS reliability without increasing system cost.

This application note presents design considerations to apply FAN6747 to a flyback power supply with peak load current profile. It covers designing the transformer, selecting the components, and closing the feedback loop. Figure 1 shows a typical application circuit using FAN6747.

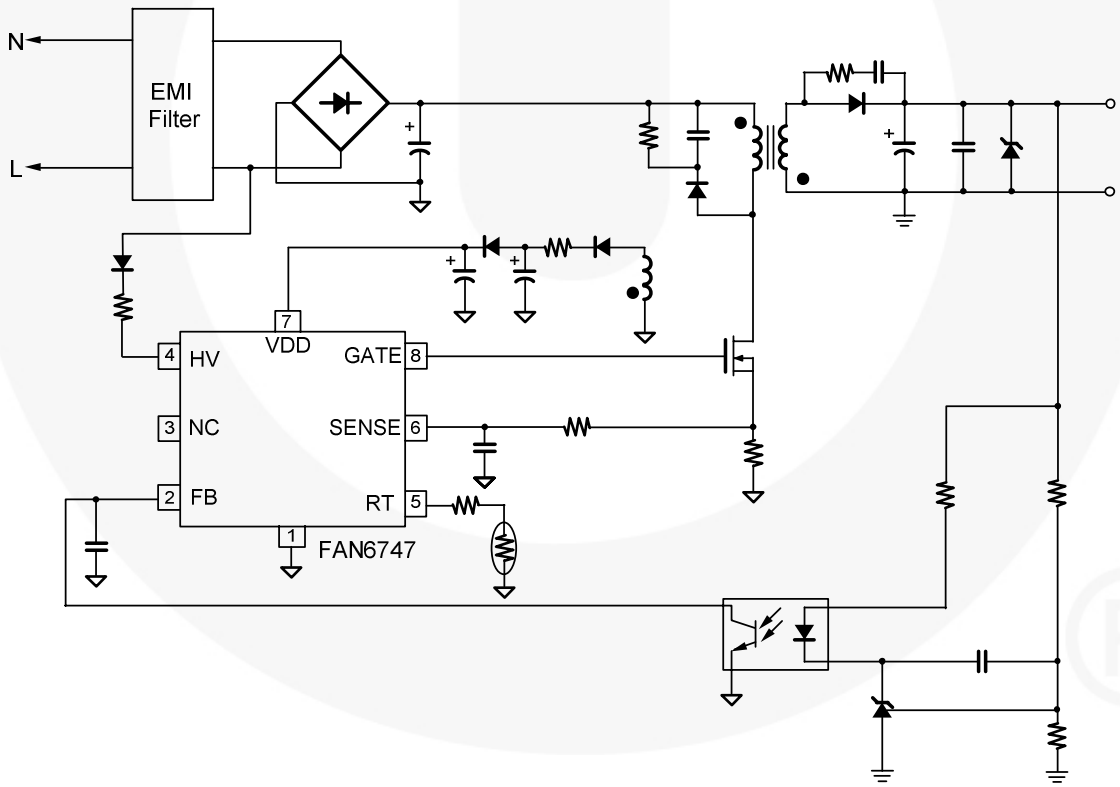

Figure 1. Typical Application

2. Design Considerations

Flyback converters have two operation modes; continuous conduction mode (CCM) and discontinuous conduction mode (DCM). CCM and DCM each have advantages and disadvantages. In general, DCM provides better switching conditions for the rectifier diodes, since the diodes are operating at zero current just before becoming reverse biased and the reverse recovery loss is minimized. The transformer size can be reduced using DCM because the average energy storage is low compared to CCM. However, DCM causes high RMS current, which increases the conduction loss of the MOSFET severely for low line condition. Thus, especially for applications with peak load profile, such as printer and scanner; it is typical to design the converter such that the converter operates in CCM for low line and peak load condition to maximize efficiency.

In this section, a design procedure is presented using the schematic of Figure 1 as a reference. An offline SMPS with 20W/32V nominal output power and 70W/32V peak output power has been selected as a design example.

[STEP-1] Define the System Specifications

Designing a power supply with peak load current profile, the following specifications should be determined first:

- Line voltage range (V_{LINE}^{MIN} and V_{LINE}^{MAX})
- Line frequency (f_L)
- Nominal output power (P_{NO})
- Peak output power (P_{PO}) and its duration (t_{PO})
- Estimated efficiencies for nominal load (η_N) and peak load (η_P).

  The power conversion efficiency must be estimated to calculate the input powers for each condition. Typically, the efficiency at peak load condition is lower than that of nominal load since most of the components of power supply are selected for nominal load condition. If no reference data is available, set η_N = 0.7~0.75 and η_P = 0.65~0.7 for low-voltage output applications and η_N = 0.8~0.85 and η_P = 0.75~0.8 for high-voltage output applications.

  With the estimated efficiency, the input power for peak load condition is given by:

$$P_{INP} = \frac{P_{PO}}{\eta_P} \quad (1)$$

  The input power for nominal load condition is given by:

$$P_{INN} = \frac{P_{NO}}{\eta_N} \quad (2)$$

(Design Example) The specifications of the target system are:

V_{LINE}^{MIN} =90V_{RMS}, V_{LINE}^{MAX}=264V_{RMS}
Line frequency (f_L) = 60Hz
Nominal output power (P_{NO}) = 20W (32V/0.625A)
Peak output power (P_{PO}) = 70W (32V/2.187A)
Peak load duration (t_{PO}) < 100ms
Estimated efficiency: η_N = 0.87 and η_P = 0.83

$$P_{INP} = \frac{P_{PO}}{\eta_P} = \frac{70}{0.83} = 84W$$

$$P_{INN} = \frac{P_{NO}}{\eta_N} = \frac{20}{0.87} = 23W$$

FAN6747 can be used for this application because the peak load duration is less than the OCP delay time of 220ms.

[STEP-2] Determine the Input Capacitor (C_{IN}) and the Input Voltage Range

It is typical to select the input capacitor as 1.5~2μF per watt of peak input power for universal input range (85-265V_{RMS}) and 0.7~0.8μF per watt of peak input power for European input range (195V-265V_{RMS}). With the input capacitor chosen, the minimum input capacitor voltage at peak load condition is obtained as:

$$V_{INP}^{MIN} = \sqrt{2 \bullet \left(V_{LINE}^{MIN}\right)^2 - \frac{P_{INP} \bullet (1 - D_{CH})}{C_{IN} \bullet f_L}} \quad (3)$$

The minimum input capacitor voltage at nominal load condition is obtained as:

$$V_{INN}^{MIN} = \sqrt{2 \bullet \left(V_{LINE}^{MIN}\right)^2 - \frac{P_{INN} \bullet (1 - D_{CH})}{C_{IN} \bullet f_L}} \quad (4)$$

where D_{CH} is the input capacitor charging duty ratio defined as shown in Figure 2, which is typically about 0.2.

The maximum input capacitor voltage is given as:

$$V_{IN}^{MAX} = \sqrt{2} V_{LINE}^{MAX} \quad (5)$$

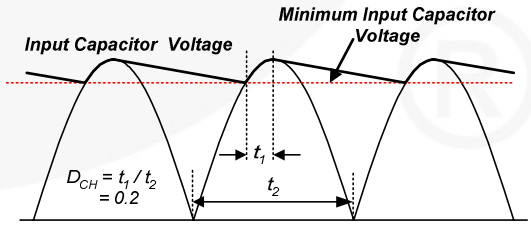

Figure 2. Input Capacitor Voltage Waveform

(Design Example) By choosing a 120μF capacitor for the input capacitor, the minimum input voltages for peak and nominal load are obtained, respectively, as:

$$V_{INP}^{MIN} = \sqrt{2 \bullet \left(V_{LINE}^{MIN}\right)^2 - \frac{P_{INP} \bullet (1 - D_{CH})}{C_{IN} \bullet f_L}}$$

$$= \sqrt{2 \bullet (90)^2 - \frac{84 \bullet (1 - 0.2)}{120 \times 10^{-6} \bullet 60}} = 83V$$

$$V_{INN}^{MIN} = \sqrt{2 \bullet \left(V_{LINE}^{MIN}\right)^2 - \frac{P_{INN} \bullet (1 - D_{CH})}{C_{IN} \bullet f_L}}$$

$$= \sqrt{2 \bullet (90)^2 - \frac{23 \bullet (1 - 0.2)}{120 \times 10^{-6} \bullet 60}} = 117V$$

The maximum input voltage is obtained as:

$$V_{IN}^{MAX} = \sqrt{2} \bullet V_{LINE}^{MAX} = \sqrt{2} \bullet 264 = 373V$$

[STEP-3] Determine the Reflected Output Voltage (V_{RO})

When the MOSFET is turned off, the input voltage (V_{IN}), together with the output voltage reflected to the primary, (V_{RO}) are imposed across the MOSFET, as shown in Figure 3. With a given V_{RO}, the maximum duty cycle (D_{MAX}) and the maximum nominal MOSFET voltage (V_{DS}^{NOM}) are obtained as:

$$D_{MAX} = \frac{V_{RO}}{V_{RO} + V_{INP}^{MIN}} \quad (6)$$

$$V_{DS}^{NOM} = V_{IN}^{MAX} + V_{RO} \quad (7)$$

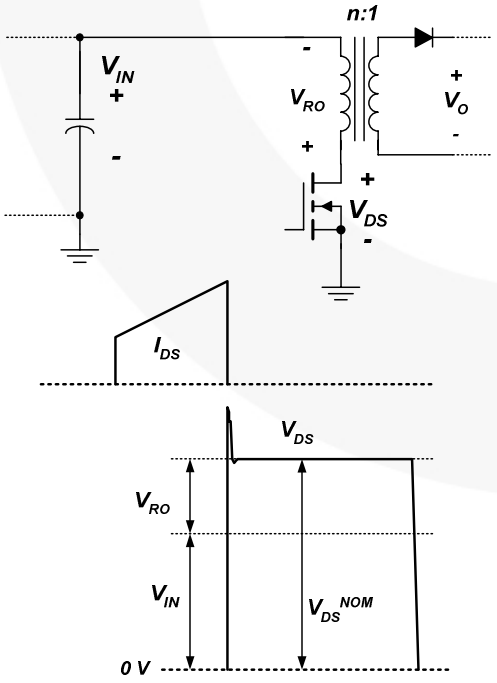

Figure 3. Output Voltage Reflected to the Primary

As can be seen in Equation (7), the voltage stress across the MOSFET can be reduced by reducing V_{RO}; however, this increases the voltage stresses on the rectifier diodes in the secondary side. Therefore, V_{RO} should be determined by a trade-off between the voltage stresses of MOSFET and diode. Because the actual drain voltage rises above the nominal MOSFET voltage due to the leakage inductance of the transformer, as shown in Figure 3, it is typical to set V_{RO} around 70~100V so that V_{DS}^{NOM} is 430~450V for 600V MOSFET (73~78% of MOSFET voltage rating).

(Design Example) By determining V_{RO} as 100V:

$$D_{MAX} = \frac{V_{RO}}{V_{RO} + V_{INP}^{MIN}} = \frac{100}{100 + 83} = 0.55$$

$$V_{DS}^{NOM} = V_{IN}^{MAX} + V_{RO} = 373 + 100 = 473V$$

[STEP-4] Determine the Transformer Primary-Side Inductance (L_M)

The transformer primary-side inductance is determined for the minimum input voltage and peak load condition. With the D_{MAX} from step 3, the primary-side inductance (L_M) of the transformer is obtained as:

$$L_M = \frac{\left(V_{INP}^{MIN} \bullet D_{MAX}\right)^2}{2 P_{INP} f_{SW} K_{RF}} \quad (8)$$

where f_{SW} is the switching frequency and K_{RF} is the ripple factor at peak load and minimum input voltage condition, as shown in Figure 4.

The ripple factor is closely related to the transformer size and the RMS value of the MOSFET current. Even though the conduction loss in the MOSFET can be reduced by reducing the ripple factor, too small a ripple factor forces an increase in transformer size. From a practical point of view, it is reasonable to set K_{RF} = 0.3~0.6 for the universal input range and K_{RF} = 0.4~0.8 for the European input range.

Once L_M is calculated by determining K_{RF} from Equation (8), the peak current and RMS current of the MOSFET for minimum input voltage and peak load condition are obtained as:

$$I_{DS}^{PK} = I_{EDC} + \frac{\Delta I}{2} \quad (9)$$

$$I_{DS}^{RMS} = \sqrt{\left[3\left(I_{EDC}\right)^2 + \left(\frac{\Delta I}{2}\right)^2\right] \frac{D_{MAX}}{3}} \quad (10)$$

where $$I_{EDC} = \frac{P_{INP}}{V_{INP}^{MIN} \bullet D_{MAX}} \quad (11)$$

and $$\Delta I = \frac{V_{INP}^{MIN} D_{MAX}}{L_M f_{SW}} \quad (12)$$

$$K_{RF} = \frac{\Delta I}{2I_{EDC}}$$

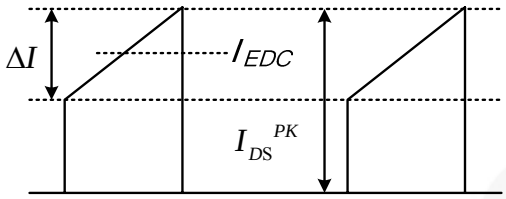

Figure 4. MOSFET Current and Ripple Factor (K_{RF})

(Design Example) Determining the ripple factor as 0.375:

$$L_M = \frac{\left(V_{INP}^{MIN} \bullet D_{MAX}\right)^2}{2P_{INP}f_{SW}K_{RF}} = \frac{(83 \bullet 0.55)^2}{2 \bullet 84 \bullet 65 \times 10^3 \bullet 0.375} = 508\mu H$$

$$I_{EDC} = \frac{P_{INP}}{V_{INP}^{MIN} \bullet D_{MAX}} = \frac{84}{83 \bullet 0.55} = 1.84A$$

$$\Delta I = \frac{V_{INP}^{MIN} D_{MAX}}{L_M f_{SW}} = \frac{83 \bullet 0.55}{508 \times 10^{-6} \bullet 65 \times 10^3} = 1.38A$$

$$I_{DS}^{PK} = I_{EDC} + \frac{\Delta I}{2} = 1.84 + 0.69 = 2.53$$

$$I_{DS}^{RMS} = \sqrt{\left[3(I_{EDC})^2 + \left(\frac{\Delta I}{2}\right)^2\right]\frac{D_{MAX}}{3}}$$

$$= \sqrt{\left[3(1.84)^2 + (0.69)^2\right]\frac{0.55}{3}} = 1.4A$$

[STEP-5] Determine the Sensing Resistor Value

The current sensing resistor value should be determined considering the over-current protection threshold and the pulse-by-pulse current limit threshold, as shown in Figure 5. The peak value of current sensing voltage (V_{CS}) should be lower than the pulse-by-pulse current limit level for peak load condition. It should be lower than the OCP threshold for nominal load conditions to prevent false triggering of OCP protection during normal operation.

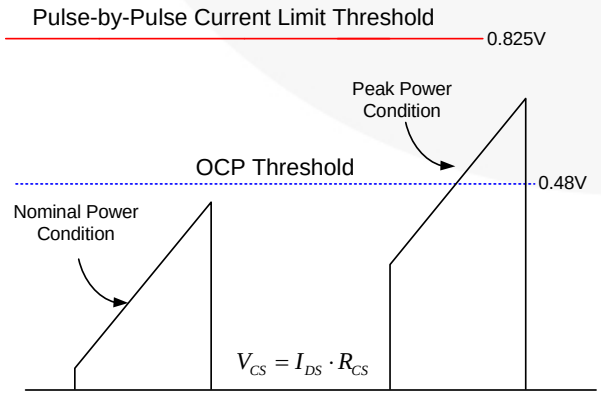

Figure 5. Determining Current Sensing Resistor

The peak drain current at minimum input voltage and peak load condition was obtained from Equation (9) in step 4. The peak drain current at minimum input voltage and nominal load condition is given as:

CCM:

$$I_{DS.N}^{PK} = \frac{P_{INN} \bullet \left(V_{IN}^{MIN} + V_{RO}\right)}{V_{INN}^{MIN} \bullet V_{RO}} + \frac{V_{INN}^{MIN} \bullet V_{RO}}{2L_M f_{SW} \bullet \left(V_{INN}^{MIN} + V_{RO}\right)} \quad (13)$$

DCM:

$$I_{DS.N}^{PK} = \sqrt{\frac{2 \bullet P_{INN}}{f_{SW} \bullet L_M}} \quad (14)$$

Whether the converter operates in CCM or DCM at minimum input voltage and nominal load condition is determined by:

$$\text{CCM: } \sqrt{2P_{INN}L_M f_{SW}} \bullet \frac{\left(V_{INN}^{MIN} + V_{RO}\right)}{V_{INN}^{MIN} \bullet V_{RO}} > 1 \quad (15)$$

$$\text{DCM: } \sqrt{2P_{INN}L_M f_{SW}} \bullet \frac{\left(V_{INN}^{MIN} + V_{RO}\right)}{V_{INN}^{MIN} \bullet V_{RO}} < 1 \quad (16)$$

The condition for the sensing resistor is given as:

$$R_{CS} < \frac{0.48}{I_{DS.N}^{PK}} \quad (17)$$

$$R_{CS} < \frac{0.825}{I_{DS.N}^{PK}} \quad (18)$$

(Design Example) For minimum input voltage and nominal load condition, the operation mode is DCM as:

$$\sqrt{2P_{INN}L_M f_{SW}} \bullet \frac{\left(V_{INN}^{MIN} + V_{RO}\right)}{V_{INN}^{MIN} \bullet V_{RO}}$$

$$= \sqrt{2 \bullet 23 \bullet 508 \times 10^{-6} \bullet 65 \times 10^3} \bullet \frac{(117 + 100)}{117 \bullet 100} < 1$$

The peak drain current at minimum input voltage and nominal power condition is given as:

$$I_{DS.N}^{PK} = \sqrt{\frac{2 \bullet P_{INN}}{f_{SW} \bullet L_M}} = \sqrt{\frac{2 \bullet 23}{65 \times 10^3 \bullet 508 \times 10^{-6}}} = 1.18A$$

The conditions for the sensing resistor are given as:

$$R_{CS} < \frac{0.48}{I_{DS.N}^{PK}} = \frac{0.48}{1.18} = 0.41\Omega$$

$$R_{CS} < \frac{0.825}{I_{DS.P}^{PK}} = \frac{0.825}{2.53} = 0.33\Omega$$

A 0.33Ω resistor is selected for the current-sensing resistor.

[STEP-6] Determine the Minimum Primary Turns

With a given core, the minimum number of turns for the transformer primary side to avoid the core saturation is given by:

$$N_P{}^{MIN} = \frac{L_M I_{LIM}}{B_{SAT} A_e} \times 10^6 = \frac{L_M \bullet 0.825 / R_{CS}}{B_{SAT} A_e} \times 10^6 \quad (19)$$

where A_e is the cross-sectional area of the core in mm^2, I_{LIM} is the pulse-by-pulse current limit level determined by 0.825V threshold, R_{CS} is current sensing resistor, and B_{SAT} is the saturation flux density in Tesla.

The pulse-by-pulse current limit level is included in Equation (19) because the inductor current reaches the pulse-by-pulse current limit level during the load transient or overload condition. Figure 6 shows the typical characteristics of ferrite core from TDK (PC40). Since the saturation flux density (B_{SAT}) decreases as the temperature rises, the high-temperature characteristics should be considered. If there is no reference data, use B_{MAX} =0.3T.

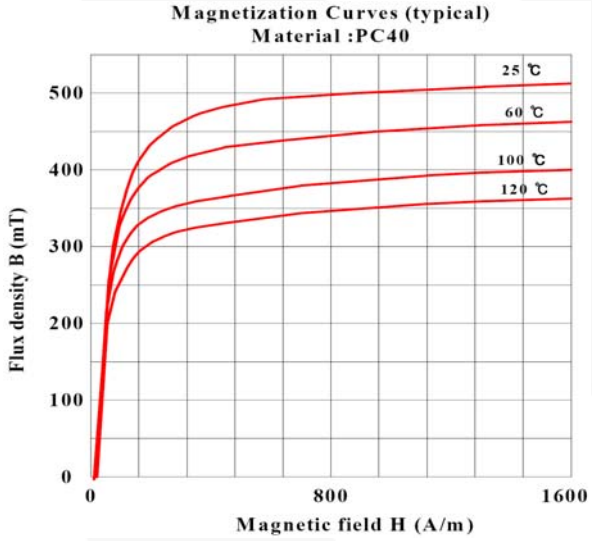

Figure 6. Typical B-H Characteristics of Ferrite Core (TDK/PC40)

(Design Example) An EF25/13/11 core is selected with effective cross-sectional area of 78mm^2. Choosing the saturation flux density as 0.27T, the minimum number of turns for the primary side is obtained as:

$$N_P{}^{MIN} = \frac{L_M \bullet 0.825 / R_{CS}}{B_{SAT} A_e} \times 10^6 = \frac{508 \times 10^{-6} \bullet 0.825 / 0.33}{0.27 \bullet 78} \times 10^6 = 60$$

[STEP-7] Determine the Number of Turns for Each Winding

Figure 7 shows a simplified diagram of the transformer. First, calculate the turn ratio (n) between the primary side and the secondary side from the reflected output voltage determined in step 3 as:

$$n = \frac{N_P}{N_S} = \frac{V_{RO}}{V_O + V_F} \quad (20)$$

where N_P and N_S are the number of turns for primary side and secondary side, respectively, V_O is the output voltage; and V_F is the diode (D_O) forward-voltage drop.

Determine the proper integer for N_S such that the resulting N_P is larger than $N_P{}^{min}$ obtained from Equation (19).

The number of turns for the auxiliary winding for V_{DD} supply is determined as:

$$N_A = \frac{V_{DD}{}^* + V_{FA}}{V_O + V_F} \bullet N_S \quad (21)$$

where V_{DD} is the nominal value of the supply voltage and V_{FA} is the forward-voltage drop of D_{DD} as defined in Figure 7. Since V_{DD} increases as the output load increases, it is proper to set V_{DD} at 3~5V higher than V_{DD} UVLO level (9V) to avoid the over-voltage protection condition during the peak load operation.

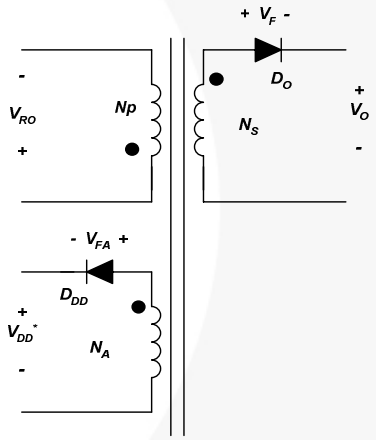

Figure 7. Simplified Transformer Diagram

(Design Example) Assuming the diode forward-voltage drop is 1V, the turn ratio is obtained as:

$$n = \frac{N_P}{N_S} = \frac{V_{RO}}{V_O + V_F} = \frac{100}{32 + 1} = 3.03$$

Then, determine the proper integer for N_S such that the resulting N_P is larger than $N_P{}^{min}$ as:

$$N_S = 20, N_P = n \bullet N_S = 61 > N_P{}^{MIN}$$

Setting V_{DD}* as 13V, the number of turns for the auxiliary winding is obtained as:

$$N_A = \frac{V_{DD}{}^* + V_{FA}}{V_O + V_F} \bullet N_S = \frac{13 + 1}{32 + 1} \bullet 20 = 9$$

[STEP-8] Determine the Wire Diameter for Each Winding Based on the RMS Current of Winding

The maximum RMS current of the secondary winding is obtained as:

$$I_{SEC}^{RMS} = n \bullet I_{DS}^{RMS} \sqrt{\frac{1-D_{MAX}}{D_{MAX}}} \quad (22)$$

The current density is typically 6~10A/mm^2 when the wire is long (>1m). When the wire is short with a small number of turns, a current density of 8~14A/mm^2 is also acceptable. These current densities are based on the peak load condition and therefore almost twice conventional power supply design. Avoid using wire with a diameter larger than 1mm to avoid severe eddy current losses and to make winding easier. For high current output, use parallel windings with multiple strands of thinner wire to minimize skin effect.

(Design Example) The RMS current of the primary-side winding is obtained from step 4 as 1.4A. The RMS current of the secondary-side winding is calculated as:

$$I_{SEC}^{RMS} = n \bullet I_{DS}^{RMS} \sqrt{\frac{1-D_{MAX}}{D_{MAX}}}$$

$$= 3.03 \bullet 1.4 \sqrt{\frac{1-0.55}{0.55}} = 3.84\ A$$

0.45mm (8A/mm^2) and 0.55mm (12A/mm^2) diameter wires are selected for primary and secondary windings, respectively.

[STEP-9] Choose the Rectifier Diode in the Secondary-Side Based on Voltage and Current Ratings

The maximum reverse voltage and the RMS current of the rectifier diode are obtained as:

$$V_{DO} = V_O + \frac{V_{IN}^{MAX}}{n} \quad (23)$$

$$I_{DO}^{RMS} = n \bullet I_{DS}^{RMS} \sqrt{\frac{1-D_{MAX}}{D_{MAX}}} \quad (24)$$

The typical voltage and current margins for the rectifier diode are:

$$V_{RRM} > 1.3 \bullet V_{DO} \quad (25)$$

$$I_F > 1.5 \bullet I_{DO}^{RMS} \quad (26)$$

where V_{RRM} is the maximum reverse voltage and I_F is the current rating of the diode.

(Design Example) The diode voltage and current are calculated as:

$$V_{DO} = V_O + \frac{V_{IN}^{MAX}}{n} = 32 + \frac{373}{3.03} = 155V$$

$$I_{DO}^{RMS} = n \bullet I_{DS}^{RMS} \sqrt{\frac{1-D_{MAX}}{D_{MAX}}}$$

$$= 3.03 \bullet 1.4 \sqrt{\frac{1-0.55}{0.55}} = 3.84\ A$$

10A and 200V diode is selected, assuming a very small heat-sink is used for the diode.

[STEP-10] Feedback Circuit Configuration

The FAN6747 employs peak-current-mode control, as shown in Figure 8. A current-to-voltage conversion is accomplished externally with current-sense resistor R_{CS}. Under normal operation, the FB level controls the peak inductor current as:

$$I_{DS} \bullet R_{CS} + V_{SLOPE} = I_{DS} \bullet R_{CS} + 0.35 \bullet D = \frac{V_{FB} - 0.6}{4} \quad (27)$$

where V_{FB} is the voltage of FB pin, V_{SLOPE} is synchronized positive-going ramp, and D is duty cycle ratio.

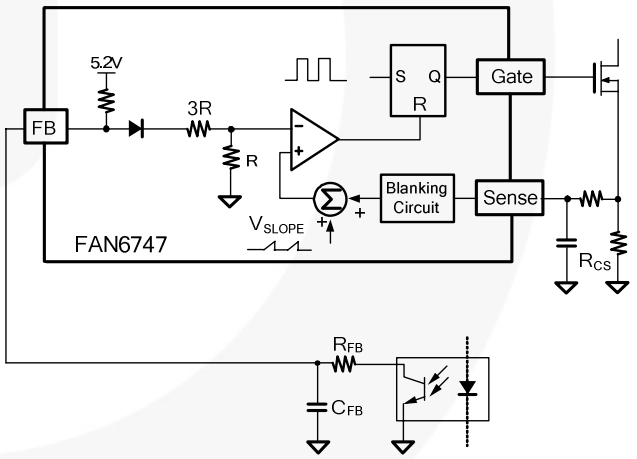

Figure 8. Peak Current Mode Circuit

Figure 9 is a typical feedback circuit mainly consisting of a shunt regulator and a photo-coupler. R1 and R2 form a voltage divider for output voltage regulation. R_F and C_F are adjusted for control-loop compensation. A small-value RC filter (e.g. R_{FB}= 100Ω, C_{FB}= 1nF) placed from the FB pin to GND can increase stability substantially. The maximum source current of the FB pin is about 325μA. The phototransistor must be capable of sinking this current to pull the FB level down at no load. The value of the biasing resistor, R_{BIAS}, is determined as:

$$\frac{V_O - V_{OPD} - V_{KA}}{R_{BIAS}} \bullet CTR > 325 \times 10^{-6} \quad (28)$$

where V_{OPD} is the drop voltage of photodiode, about 1.2V; V_{KA} is the minimum cathode to anode voltage of shunt regulator (2.5V); and CTR is the current transfer rate of the opto-coupler.

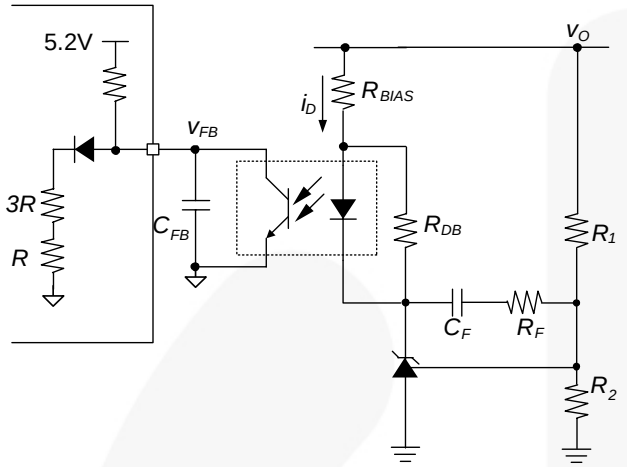

Figure 9. Feedback Circuit

The feedback compensation network transfer function of Figure 9 is obtained as:

$$\frac{\hat{v}_{FB}}{\hat{v}_O} = -\frac{\omega_I}{s} \bullet \frac{1 + s/\omega_{ZC}}{1 + s/\omega_{PC}} \quad (29)$$

where $\omega_I = \frac{R_B}{R_1 R_{DB} C_F}$; $\omega_{ZC} = \frac{1}{(R_F + R_1)C_O}$; $\omega_{PC} = \frac{1}{R_B C_{FB}}$

R_B is the internal feedback bias resistor; and R_1, R_D, R_F, C_F, and C_{FB} are shown in Figure 9.

(Design Example) Assuming CTR is 100%;

$$\frac{V_O - V_{OPD} - V_{KA}}{R_{BIAS}} \bullet CTR > 325 \times 10^{-6}$$

$$R_{BIAS} < \frac{V_O - V_{OPD} - V_{KA}}{325 \times 10^{-6}} = \frac{32 - 1.2 - 2.5}{325 \times 10^{-6}} = 87k\Omega$$

5.1kΩ resistor is selected for R_{DB}.

The voltage divider resistors for V_O sensing are selected as 120kΩ and 10kΩ.

[STEP-11] Design the Startup Circuit

Figure 10 shows the typical startup circuit for FAN6747. HV pin has an internal high-voltage startup circuit that is disabled when V_{DD} reaches its turn-on threshold. Since HV pin is also used to obtain line voltage information for brownout protection and power limit line compensation, it is typical to connect the HV pin to the AC line through a resistor and diode.

A two-stage hold-up capacitor configuration (C_{DD1} and C_{DD2}) is typically used to increase the hold-up time while minimizing startup time. Initially, the FAN6747 HV startup circuit is enabled before it begins normal switching operation. Therefore, the current supplied by the HV pin can charge capacitor C_{DD1} while supplying the startup current to FAN6747. When V_{DD} reaches the turn-on voltage of 16.5V (V_{DD-ON}), FAN6747 begins switching operation and the HV startup circuit is disabled. Then the current required by FAN6747 is supplied from the auxiliary winding of transformer.

It is typical to use a 150~250kΩ resistor for the HV pin to improve the immunity against line surge.

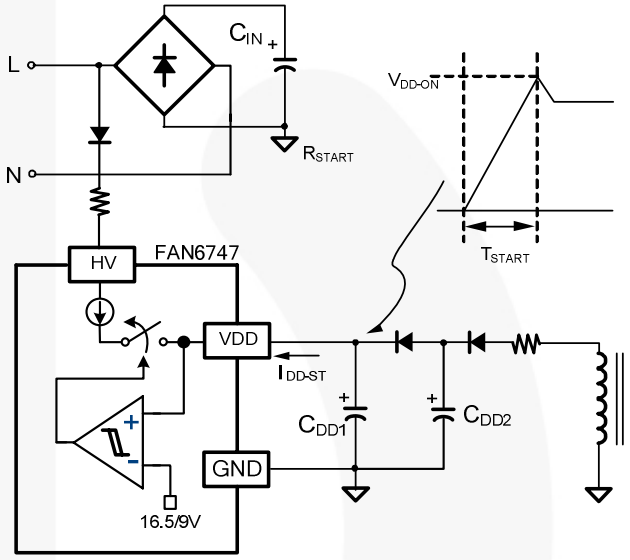

Figure 10. Startup Circuit

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike occurs across the sense resistor, caused by primary-side capacitance and secondary-side rectifier reverse recovery. To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period (270ns), the PWM comparator is disabled and cannot switch off the gate driver. Thus, an RC filter with a small RC time constant is enough for current sensing (e.g. 100Ω + 470pF). A non-inductive resistor is recommended for R_{CS}.

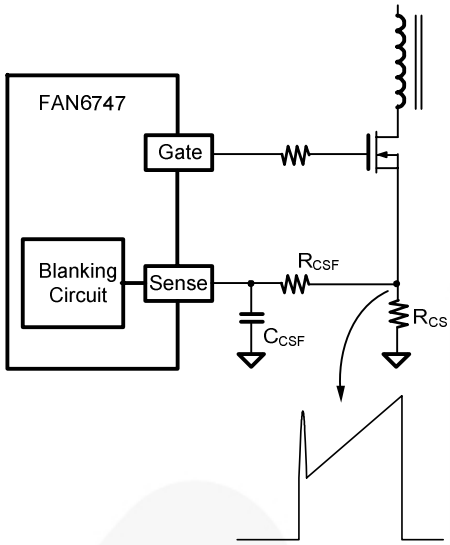

Figure 11. Current Sensing

Thermal Protection

Figure 12 shows the internal blocks for thermal protection. A constant current, I_{RT}, of 100μA is provided from the RT pin. For over-temperature protection, an NTC thermistor in series with a resistor can be connected between the RT and GND pins. As temperature increases, the impedance of NTC thermister decreases and RT pin voltage drops. When the voltage of the RT pin is less than 1.05V but over 0.7V, the PWM turns off after 16ms ($t_{D\_OTP-LATCH}$). When RT pin voltage is less than 0.7V, OTP is triggered after the 185μs ($t_{D\_OTP2-LATCH}$) debounce time.

If the RT pin is not connected to the NTC resistor for over-temperature protection, a 100KW resistor to ground to prevent noise interference is recommended. This pin is limited by the internal clamping circuit.

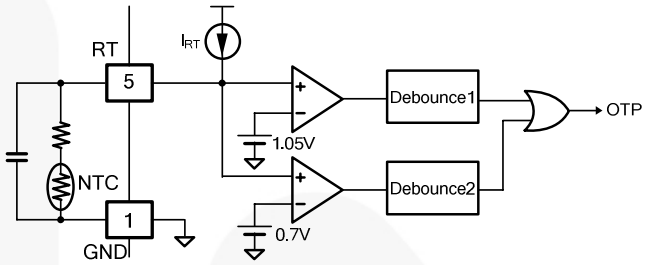

Figure 12. Thermal Protection Circuit

Printed Circuit Board (PCB) Layout

PCB layout is a very important design issue for high-frequency switching current/voltage application. Good PCB layout minimizes excessive EMI and helps the power supply survive during surge / ESD tests.

Guidelines:

- To get better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C1 first, then to the switching circuits.
- The high-frequency current loop is in **C1 – transformer – MOSFET – R_S – C1**. The area enclosed by this current loop should be as small as possible. Keep the traces (especially 4→1) short, direct, and wide. High-voltage traces related to the drain of MOSFET and RCD snubber should be kept far way from control circuits to prevent unnecessary interference. If a heatsink is used for the MOSFET, connect this heatsink to ground.
- As indicated by 3, the ground of control circuits should be connected first, then to other circuitry.
- As indicated by 2, the area enclosed by **transformer auxiliary winding, D1, C2, D2, and C3** should also be kept small. Place C3 close to the FAN6747 for good decoupling.

Two suggestions with different advantages and disadvantages for ground connections are offered:

- GND3 → 2 → 4 → 1: This could avoid common impedance interference for sense signal.
- GND3 → 2 → 1 → 4: This could be better for ESD testing where the earth ground is not available on the power supply. Regarding the ESD discharge path, the charges go from secondary through the transformer stray capacitance to GND2 first. The charges then go from GND2 to GND1 and back to the mains. Control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high-frequency impedance and increase ESD immunity.
- Should a Y-cap between primary and secondary be required, connect this Y-cap to the **positive terminal of C1**. If this Y-cap is connected to the primary GND, it should be connected to the **negative terminal of C1 (GND1)** directly. Point discharge of this Y-cap also helps for ESD. However, the creepage between these two pointed ends should be large enough to satisfy the requirements of applicable standards.

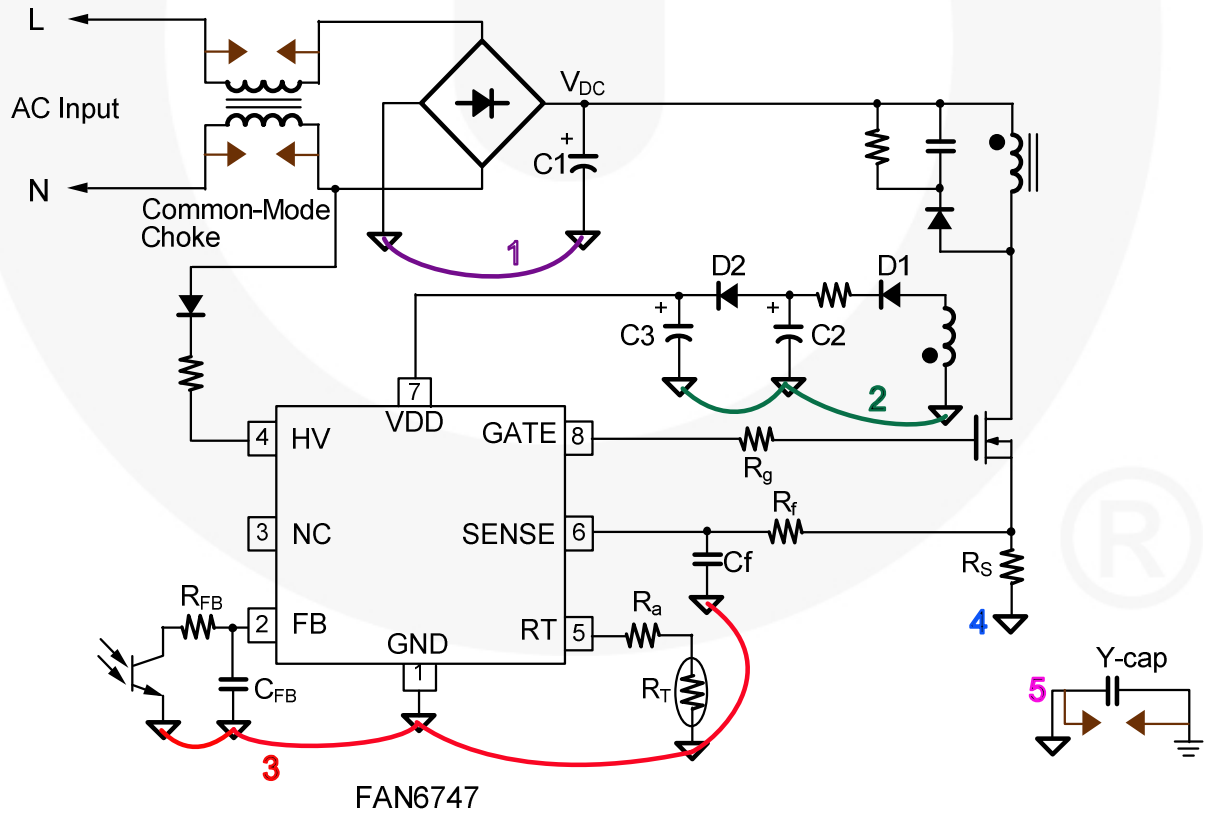

Figure 13. Layout Considerations

Design Summary

Figure 14 shows the final schematic of the 20W (70W peak) power supply of the design example.

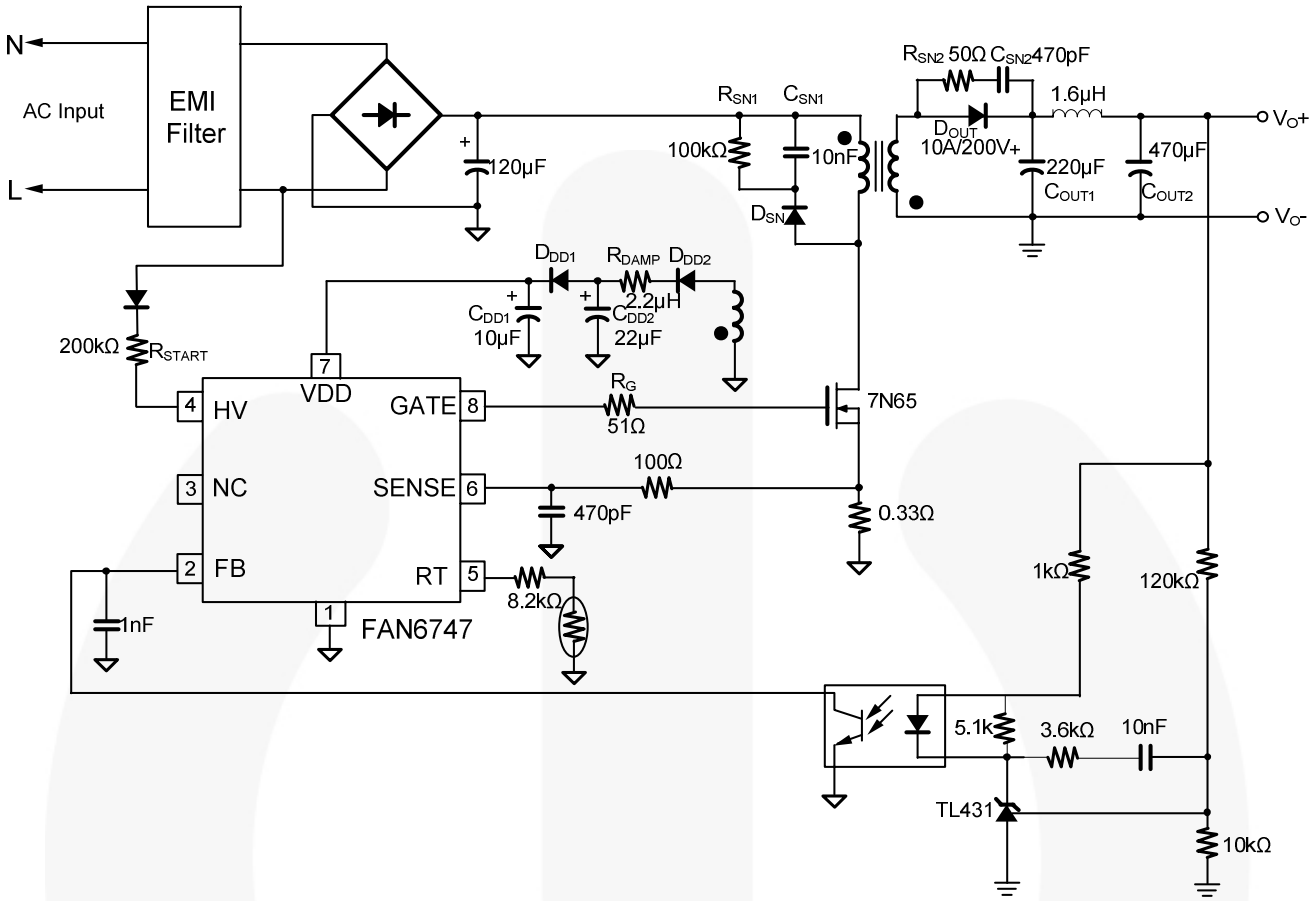

Figure 14. Final Schematic of Design Example

Transformer Specification

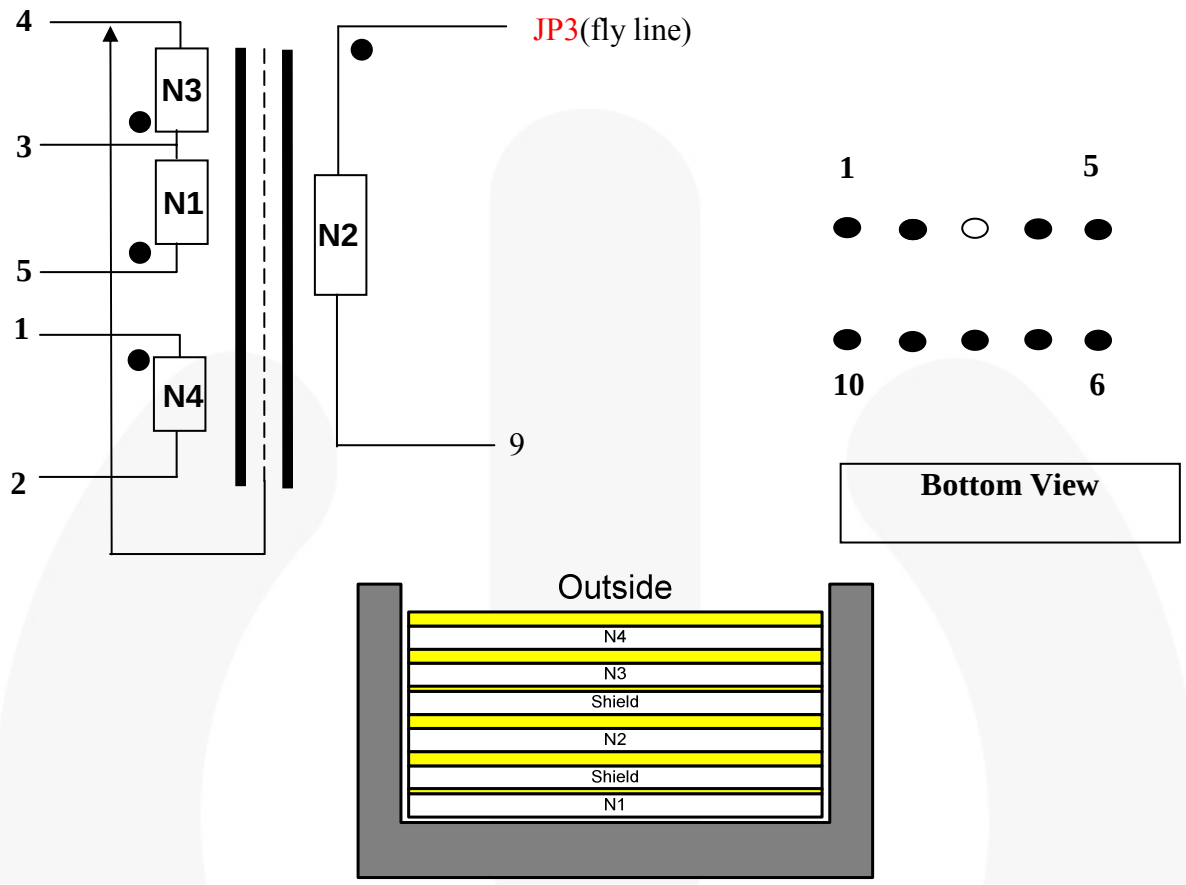

Figure 15. Transformer Specification

Winding Specification

	Pin	Diameter / Thickness	Turns
N1	5 → 3	0.45mm	30
Insulation Tape			3
Shielding Lead to Pin 4			65
Insulation Tape			3
N2	JP3 → 9	0.55mm	20
Insulation Tape			3
Shielding Lead to Pin 4			65
Insulation Tape			3
N3	3 → 4	0.45mm	30
Insulation Tape			6
N4	1 → 2	0.2mm	9
Insulation Tape			3

Core: EF25/13/11 (Ae=78 mm^2)
Bobbin: EF25/13/11
Inductance: 508μH

Related Datasheets

FAN6747 — Highly Integrated Green-Mode PWM Controller for Peak Power Management