

8-Bit Shift Registers

LS91

FEATURES

- For Use In Digital Computer Systems
- For Use In Data-Handling Systems
- For Use In Control Systems

DESCRIPTION

These monolithic serial-in, serial-out, 8-bit shift registers utilize transistor-transistor logic (TTL) circuits and are composed of eight R-S master-slave flip-flops, input gating, and a clock driver. Single-rail data and input control are gated through inputs A and B and an internal inverter to form the complementary inputs to the first bit of the shift register. Drive for the internal common clock line is provided by an inverting clock driver. This clock pulse inverter/driver causes these circuits to shift information one bit on the positive edge of an input clock pulse.

FUNCTION TABLE

Inputs		Outputs	
AT t_n		AT t_{n+8}	
A	B	Q_H	\bar{Q}_H
H	H	H	H
L	X	L	H
X	L	L	H

H = high, L = low,

X = irrelevant

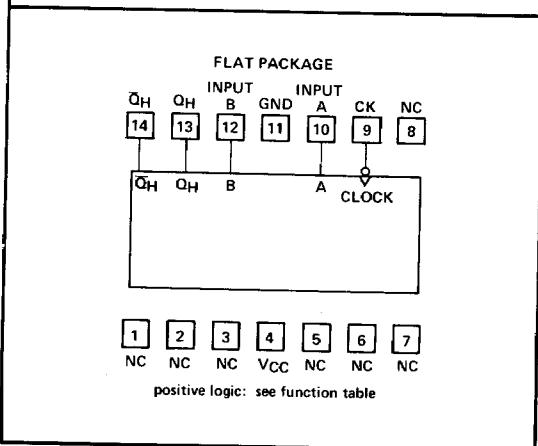
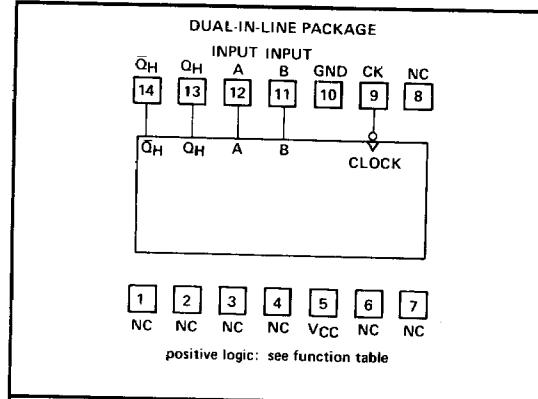
t_n = Reference bit time, clock low

t_{n+8} = Bit time after 8

low-to-high

clock transitions.

PIN-OUT DIAGRAM

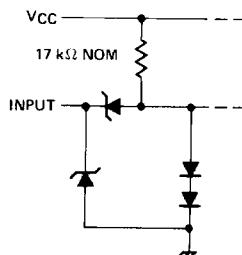


NC—No Internal Connection

SCHEMATICS OF INPUTS AND OUTPUTS

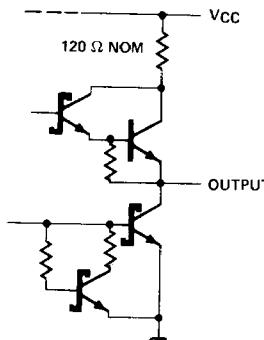
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EQUIVALENT OF EACH INPUT

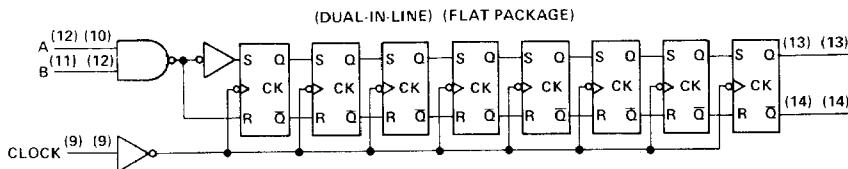


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TYPICAL OF BOTH OUTPUTS



FUNCTIONAL BLOCK DIAGRAM



Recommended Operating Conditions

	9LS/54LS			9LS/74LS			Unit
	Min.	Nom.	Max.	Min.	Nom.	Max.	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
High-level output current, I_{OH}			-400			-400	μA
Low-level output current, I_{OL}			4			8	mA
Width of clock input pulse, t_W	25			25			ns
Setup time, t_{SU} (See Figure 1)	25			25			ns
Hold time, t_h (See Figure 1)	0			0			ns
Operating free-air temperature, T_A	-55		125	0		70	$^{\circ}C$

Electrical Characteristics Over Recommended Operating Free-Air Temperature Range
(Unless Otherwise Noted)

Parameter	Test Conditions†	9LS/54LS			9LS/74LS			Unit
		Min.	Typ.‡	Max.	Min.	Typ.‡	Max.	
I_{IH} High-level input voltage		2			2			V
I_{IL} Low-level input voltage				0.7			0.8	V
V_{IK} Input clamp voltage	$V_{CC} = \text{Min}, I_I = -18 \text{ mA}$			-1.5			-1.5	V
V_{OH} High-level output voltage	$V_{CC} = \text{Min}, V_{IH} = 2V$ $V_{IL} = V_{IL} \text{ max}, I_{OH} = -400 \mu A$	2.5	3.5		2.7	3.5		V
V_{OL} Low-level output voltage	$V_{CC} = \text{Min}, V_{IH} = 2V$ $V_{IL} = V_{IL} \text{ max}$	$I_{OL} = 4 \text{ mA}$	0.25	0.4	0.25	0.4	0.35	V
I_I Input current at maximum input voltage	$V_{CC} = \text{Max}, V_I = 7V$			0.1			0.1	mA
I_{IH} High-level input current	$V_{CC} = \text{Max}, V_I = 2.7V$			20			20	μA
I_{IL} Low-level input current	$V_{CC} = \text{Max}, V_I = 0.4V$			-0.4			-0.4	mA
I_{OS} Short-circuit current§	$V_{CC} = \text{Max}$	15		-100	15		-100	mA
I_{CC} Supply current	$V_{CC} = \text{Max}, \text{See Note 1}$		12	20		12	20	mA

†For conditions shown as Min or Max, use the appropriate value specified under recommended operating conditions.

‡All typical values are at $V_{CC} = 5 \text{ V}$, $T_A = 25^{\circ}\text{C}$.

§Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

NOTE 1. I_{CC} is measured after the eighth clock pulse with the output open and A and B inputs grounded.

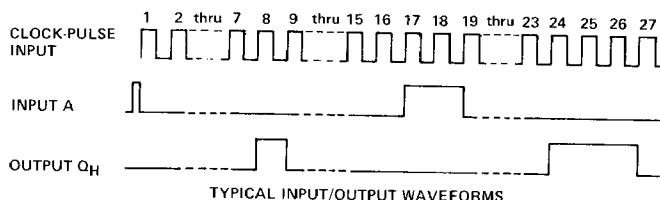
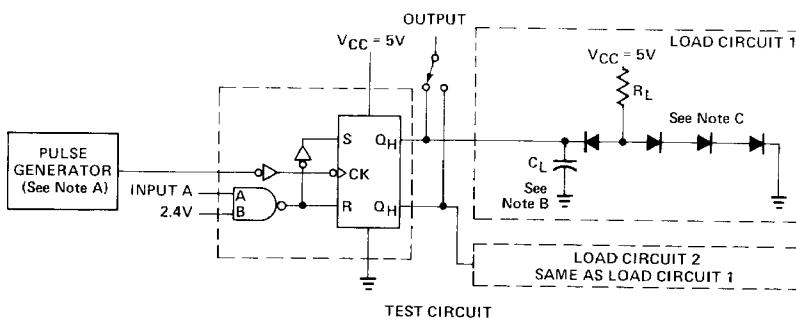
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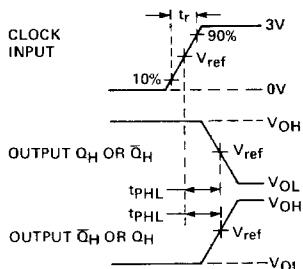
Switching Characteristics $V_{CC} = 5.0V$ Over Recommended Free-Air Temperature Range.

Parameter	From (Input)	To (Output)	9LS/54LS									Unit	
			-55°C			+25°C			+125°C				
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Test Conditions: $C_L = 15\text{pF}$, $R_L = 2.0\text{k}\Omega$ (See Fig. A, page 2-174 and Fig. 1, page 2-55)													
f(max)						10	18					MHz	
T_{PLH}	clock	Q_H		26	42		24	40		26	42	ns	
T_{PHL}	clock	Q_H		28	45		27	40		28	45	ns	
Test Conditions: $C_L = 50\text{pF}$, $R_L = 2.0\text{k}\Omega$ (See Fig. A, page 2-174 and Fig. 1, page 2-55)													
T_{PLH}	clock	Q_H		30	47		27	45		30	47	ns	
T_{PHL}	clock	Q_H		33	52		30	48		33	52	ns	

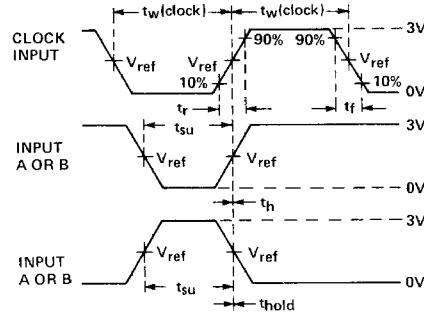
PARAMETER MEASUREMENT INFORMATION



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PROPAGATION DELAY TIMES VOLTAGE WAVEFORMS



SWITCHING TIMES VOLTAGE WAVEFORMS

FIGURE 1. SWITCHING TIMES

- NOTES:
- A. The generator has the following characteristics: $t_w(\text{clock}) = 500 \text{ ns}$; PRR $\leq 1 \text{ MHz}$; $Z_{\text{out}} \approx 50 \Omega$; $t_r = 15 \text{ ns}$, and $t_f = 6 \text{ ns}$.
 - B. C_1 includes probe and j:s capacitance
 - C. All diodes are 1N3064 or 1N916
 - D. $V_{\text{ref}} = 1.3 \text{ V}$