NE58633

Noise reduction class-D headphone driver amplifier

Rev. 01 — 22 January 2009 Product data sheet

1. General description

The NE58633 is a stereo, noise reduction, class-D, Bridge-Tied Load (BTL) headphone driver amplifier. Each channel comprises a class-D BTL headphone driver amplifier, an electret microphone low noise preamplifier, feedback noise reduction circuit and a music amplifier input.

The NE58633 operates with a battery voltage of 0.9 V to 1.7 V. The chip employs an on-chip DC-to-DC boost converter and internal V_{ref} voltage reference which is filtered and output to ground for noise decoupling. It features mute control and plop and click reduction circuitry. The gain of the microphone amplifier and filter amplifier is set using external resistors. Differential architecture provides increased immunity to noise.

The NE58633 is capable of driving 800 mV_{rms} across a 16 Ω or 32 Ω load and provides ElectroStatic Discharge (ESD) and short-circuit protection.

It is available in the 32-pin HVQFN32 (5 mm × 5 mm × 0.85 mm) package suitable for high density small-scale layouts and is an ideal choice for noise reduction headphones and educational audio aids.

2. Features

- Low current consumption of 4.4 mA
- 0.9 V to 1.7 V battery operating voltage range
- 1 % THD+N at V_O = 1 V_M driving 16 Ω with a battery voltage of 1.5 V
- 10 % THD+N at 800 mV_{rms} output voltage driving 16 Ω and 32 Ω loads with a battery voltage of 1.5 V
- Output noise voltage with noise reduction circuit typically 31 mV_{rms} for $G_{v(cl)}$ = 25 dB
- On-chip mute function
- Plop and click reduction circuitry
- Class-D BTL differential output configuration
- Electret microphone noise reduction polarization amplifier with external gain adjustment using resistors
- Music and filter amplifier with external gain adjustment using resistors
- DC-to-DC converter circuitry (3 V output) with 2.5 mA (typical) load current
- Internal voltage reference pinned out for noise decoupling
- Available in HVQFN32 package

founded by Philips

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
NE58633BS	HVQFN32	plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 × 5 × 0.85 mm	SOT617-1

4. Block diagram

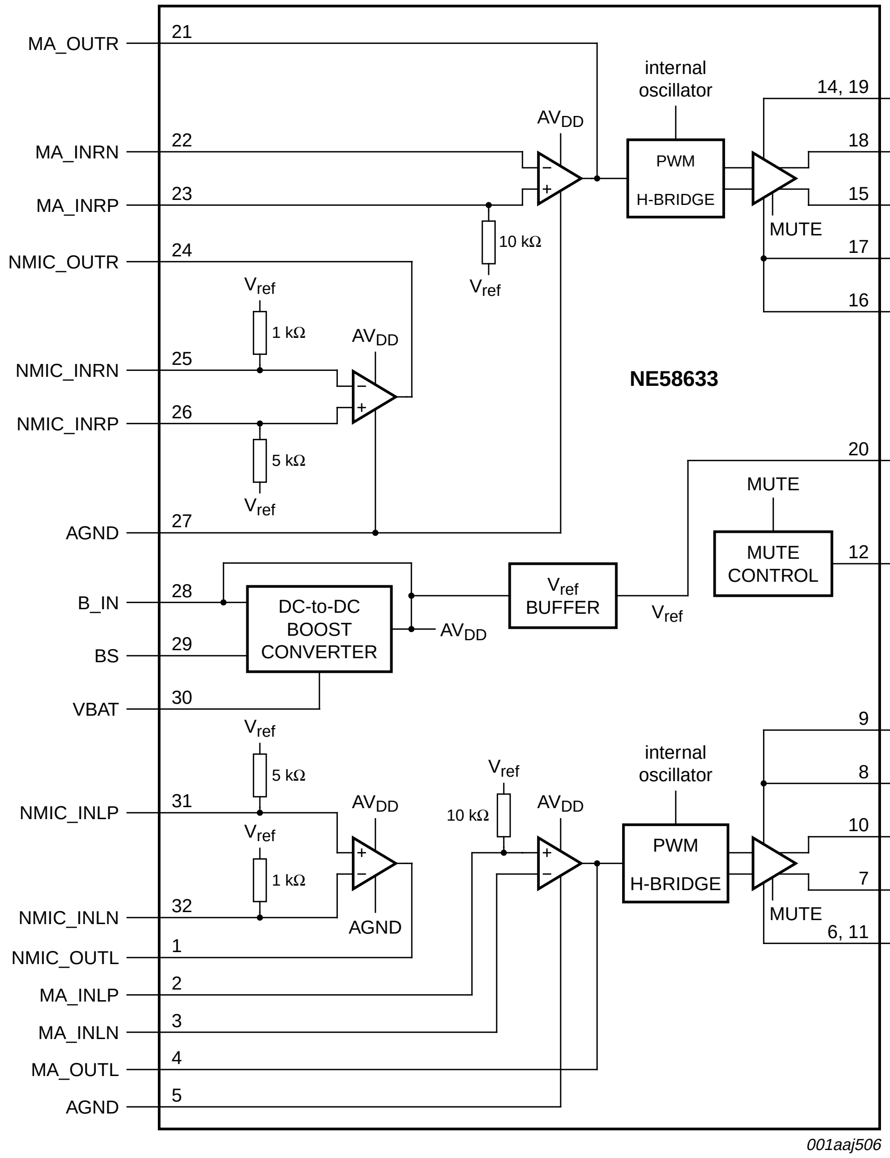


Fig 1. Block diagram

5. Pinning information

5.1 Pinning

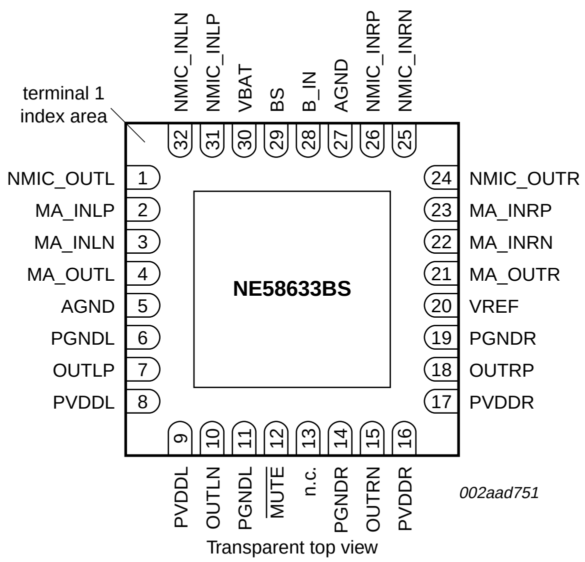


Fig 2. Pin configuration for HVQFN32

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
NMIC_OUTL	1	noise reduction microphone preamplifier output, left channel
MA_INLP	2	music amplifier positive input, left channel
MA_INLN	3	music amplifier negative input, left channel
MA_OUTL	4	music amplifier output, left channel
AGND	5	analog ground
PGNDL	6	power ground, headphone driver, left channel
OUTLP	7	headphone positive output, left channel
PVDDL	8, 9	battery supply voltage, headphone driver output, left channel
OUTLN	10	headphone negative output, left channel
PGNDL	11	power ground, headphone driver, left channel
$\overline{\text{MUTE}}$	12	mute, headphone outputs (active LOW)
n.c.	13	not connected internally; connect pin to ground
PGNDR	14	power ground, headphone driver, right channel
OUTRN	15	headphone negative output, right channel
PVDDR	16, 17	battery supply voltage, headphone driver output, right channel
OUTRP	18	headphone positive output, right channel
PGNDR	19	power ground, headphone driver, right channel
VREF	20	internal voltage reference output

Table 2. Pin description *...continued*

Symbol	Pin	Description
MA_OUTR	21	music amplifier output, right channel
MA_INRN	22	music amplifier negative input, right channel
MA_INRP	23	music amplifier positive input, right channel
NMIC_OUTR	24	noise reduction microphone preamplifier output, right channel
NMIC_INRN	25	noise reduction microphone preamplifier negative input, right channel
NMIC_INRP	26	noise reduction microphone preamplifier positive input, right channel
AGND	27	ground, analog
B_IN	28	boost converter input
BS	29	boost converter switching transistor collector
VBAT	30	battery supply voltage
NMIC_INLP	31	Noise reduction microphone preamplifier positive input, left channel
NMIC_INLN	32	Noise reduction microphone preamplifier negative input, left channel

6. Limiting values

Table 3. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).
T_{amb} = 25 °C, unless otherwise specified.

Symbol	Parameter	Conditions	Min	Max	Unit
V_{BAT}	battery supply voltage	pins VBAT, PVDDL, PVDDR			
		in active mode	–0.3	+1.7	V
		in mute mode	–0.3	+1.7	V
V_I	input voltage		–0.3	+2.0	V
T_{amb}	ambient temperature	operating	0	70	°C
T_j	junction temperature	operating	0	150	°C
T_{stg}	storage temperature		0	150	°C

7. Recommended operating conditions

Table 4. Operating conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{BAT}	battery supply voltage	AVDD, PVDD	0.9	1.7	V
$V_{i(cm)}$	common-mode input voltage	music and noise reduction amplifier inputs	0.2	$V_{bst} - 1$	V
V_{IH}	HIGH-level input voltage	unmuted; $\overline{MUTE}$	1	V_{BAT}	V
V_{IL}	LOW-level input voltage	muted; $\overline{MUTE}$	0	0.8	V
T_{amb}	ambient temperature	operating	0	70	°C

8. Characteristics

Table 5. Electrical characteristics

T_{amb} = 25 °C; unless otherwise specified.

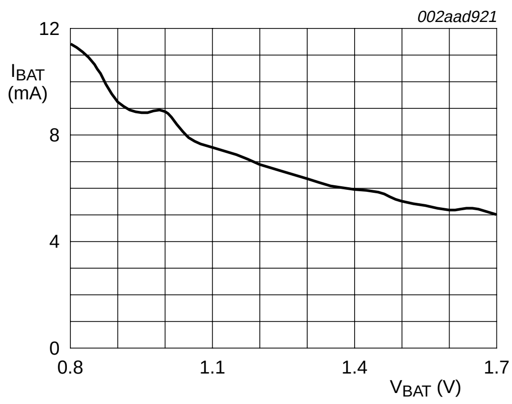
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\lvert V_{O(offset)} \rvert$	output offset voltage	measured differentially; inputs AC grounded; $G_{v(cl)}$ = 25 dB; V_{BAT} = 0.9 V to 1.7 V	-	5	25	mV
$\lvert V_{I(offset)} \rvert$	input offset voltage	music amplifier and noise reduction microphone amplifier; measured differentially	-	1	-	mV
Z_i	input impedance	music amplifier, non-inverting terminal; V_{BAT} = 0.9 V to 1.7 V	-	10	-	kΩ
		microphone preamplifier; V_{BAT} = 0.9 V to 1.7 V				
		inverting terminal noise reduction	-	1	-	kΩ
		non-inverting terminal noise reduction	-	5	-	kΩ
I_{LI}	input leakage current	music amplifier; inverting terminal V_{BAT} = 0.9 V to 1.7 V	-	-	500	nA
V_{OH}	HIGH-level output voltage	music amplifier and noise reduction microphone preamplifier; I_{OH} = 1 mA; V_{BAT} = 0.9 V to 1.7 V	2.6	-	-	V
V_{OL}	LOW-level output voltage	music amplifier and noise reduction microphone preamplifier; I_{OH} = 1 mA; V_{BAT} = 0.9 V to 1.7 V	-	-	0.35	V
V_{ref}	reference voltage	V_{BAT} = 0.9 V to 1.7 V	-	$0.5V_{bst}$	-	V
I_{DD}	supply current	AC grounded; no load [1]				
		V_{BAT} = 1.7 V	-	5.0	6.0	mA
		V_{BAT} = 1.5 V	-	6.0	-	mA
		V_{BAT} = 1.3 V	-	7.0	-	mA
		V_{BAT} = 1.05 V	-	8.0	-	mA
		V_{BAT} = 0.9 V	-	9.0	11	mA
R_{DSon}	drain-source on-state resistance	V_{BAT} = 0.9 V to 1.7 V; no load	-	2.8	-	Ω
f_{sw}	switching frequency	V_{BAT} = 0.9 V to 1.7 V	250	300	350	kHz
$G_{v(cl)}$	closed-loop voltage gain	with noise reduction microphone circuit; V_{BAT} = 0.9 V to 1.7 V; R_F = 18 kΩ	-	25	-	dB
$V_{th(mute)}$	mute threshold voltage	V_{BAT} = 0.9 V to 1.7 V				
		LOW-level; active LOW (muted)	0	-	0.8	V
		HIGH-level; inactive HIGH (unmuted)	1.0	-	-	V

[1] Music amplifier at unity gain; noise preamplifier at 25 dB gain; noise preamplifier output connected to corresponding inverting input of music amplifier; non-inverting inputs.

Table 6. Operating characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
ΔV_o	output voltage variation	per channel; R_L = 16 Ω; f = 1 kHz; THD+N = 10 %				
		V_{BAT} = 1.7 V	-	800	-	V_{rms}
		V_{BAT} = 1.5 V	-	800	-	V_{rms}
		V_{BAT} = 1.05 V	-	550	-	V_{rms}
P_o	output power	per channel; f = 1 kHz; THD+N = 10 %				
		R_L = 16 Ω; V_{BAT} = 1.5 V	-	40	-	mW
		R_L = 32 Ω; V_{BAT} = 1.5 V	-	20	-	mW
		R_L = 16 Ω; V_{BAT} = 1.05 V	-	19	-	mW
THD+N	total harmonic distortion-plus-noise	V_o = 1 V_{peak}; f = 1 kHz; V_{BAT} = 1.5 V to 1.7 V	-	1.0	-	%
		V_o = 620 mV_{peak}; f = 1 kHz; V_{BAT} = 1.05	-	1.0	-	%
$G_{v(ol)}$	open-loop voltage gain	music amplifier and noise reduction microphone preamplifier; V_{BAT} = 1.5 V	-	100	-	dB
α_{ct}	crosstalk attenuation	f = 1 kHz; V_{BAT} = 1.5 V; R_g = 1 kΩ; R_L = 16 Ω; V_o = 800 mV_{rms}	40	50	-	dB
SVRR	supply voltage ripple rejection	$V_{bst(ripple)}$ = 100 mV_{rms}; $G_{v(cl)}$ = 25 dB; f = 1 kHz				
		V_{BAT} = 0.9 V	30	40	-	dB
		V_{BAT} = 1.5 V	-	60	-	dB
Z_i	input impedance	microphone preamplifier; $G_{v(cl)}$ = 25 dB (from noise reduction microphone to class-D output)	-	1	-	kΩ
$V_{n(i)}$	input noise voltage	spectral noise; V_{BAT} = 1.5 V; f = 20 to 20 kHz; $G_{v(cl)}$ = 25 dB; R_g = 1 kΩ	-	12	-	nV/√Hz
$V_{n(o)}$	output noise voltage	V_{BAT} = 1.5 V; f = 20 to 20 kHz; inputs AC grounded; $G_{v(cl)}$ = 25 dB				
		no weighting	-	26	-	µV
		A weighting	-	20	-	µV
DC-to-DC boost converter						
V_I	input voltage		1.05	-	1.7	V
$V_{I(startup)min}$	minimum start-up input voltage		-	0.9	1.05	V
V_{bst}	boost voltage	V_{BAT} = 1.05 V to 1.7 V; 2.65 mA external load	2.75	3.1	3.45	V
$I_{bst(load)O}$	output load boost current	V_{BAT} = 1.05 V to 1.7 V; V_{bst} > 2.8 V	-	2.65	-	mA
η_{bst}	boost efficiency	V_{BAT} = 1.05 V to 1.7 V; $R_{L(tot)}$ = 600 Ω	-	80	-	%

9. Typical performance curves



V_{bst} = 3.14 V

Fig 3. Battery supply current as a function of battery supply voltage

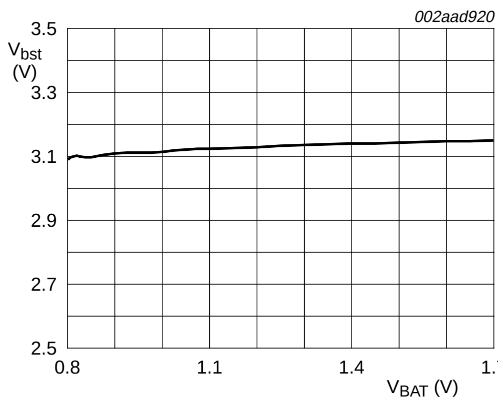


Fig 4. Boost voltage as a function of battery supply voltage

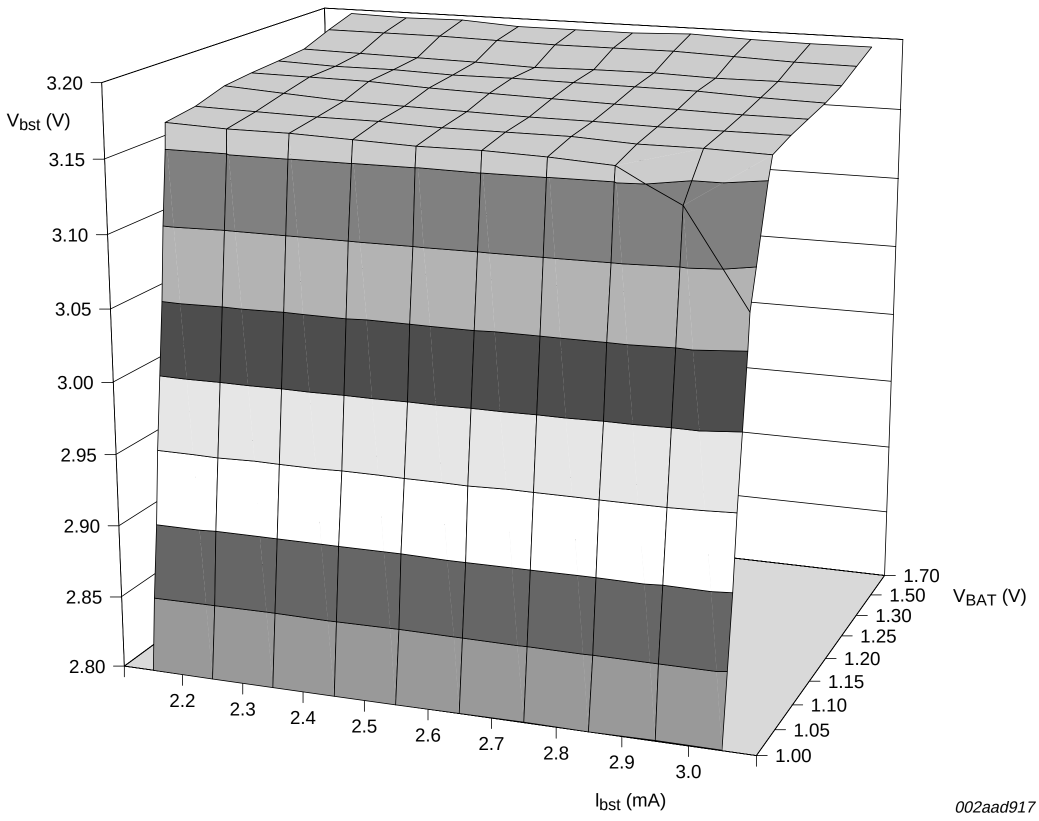
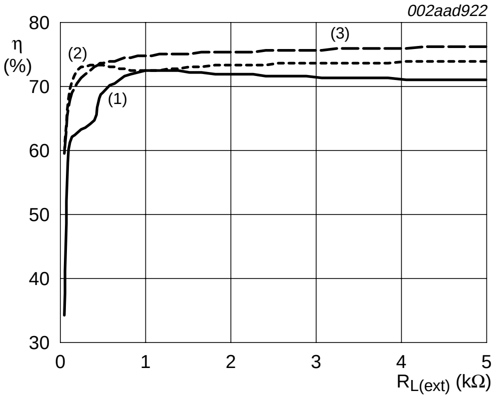


Fig 5. Boost voltage, battery supply voltage and boost current 3D profile

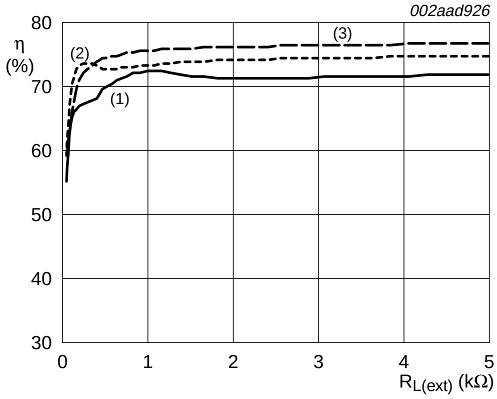


(1) V_{BAT} = 0.9 V

(2) V_{BAT} = 1.2 V

(3) V_{BAT} = 1.5 V

a. Battery supply voltage = 0.9 V, 1.2 V and 1.5 V

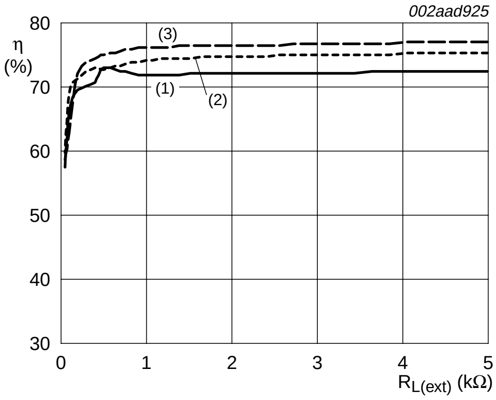


(1) V_{BAT} = 1.0 V

(2) V_{BAT} = 1.3 V

(3) V_{BAT} = 1.6 V

b. Battery supply voltage = 1.0 V, 1.3 V and 1.6 V



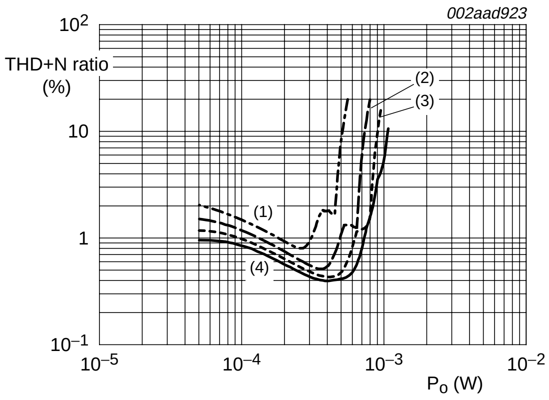
(1) V_{BAT} = 1.1 V

(2) V_{BAT} = 1.4 V

(3) V_{BAT} = 1.7 V

c. Battery supply voltage = 1.1 V, 1.4 V and 1.7 V

Fig 6. Efficiency as a function of external load resistance; boost voltage = 3.14 V



R_L = 16 Ω speaker load + 2 × ferrite bead + 2 × 18 Ω resistor; measured across 16 Ω speaker; f_i = 1 kHz; A-weighting filter for THD+N.

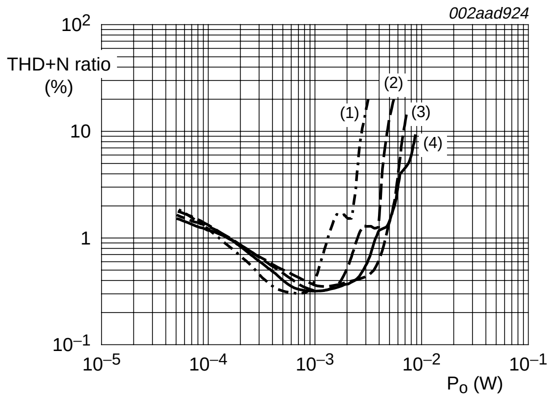
(1) V_{BAT} = 1.05 V

(2) V_{BAT} = 1.3 V

(3) V_{BAT} = 1.5 V

(4) V_{BAT} = 1.7 V

Fig 7. Total harmonic distortion-plus-noise as a function of output power; 16 Ω load



R_L = 16 Ω speaker load + 2 × ferrite bead + 2 × 18 Ω resistor; measured across 32 Ω speaker; f_i = 1 kHz; A-weighting filter for THD+N

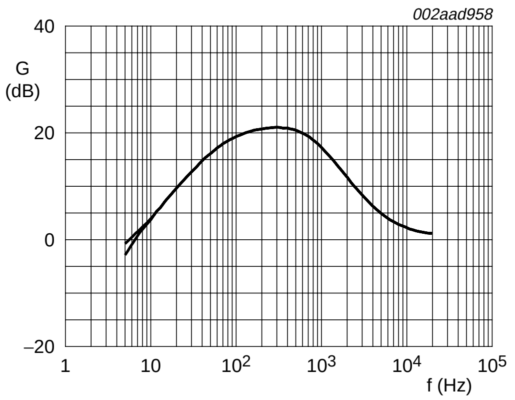
(1) V_{BAT} = 1.05 V

(2) V_{BAT} = 1.3 V

(3) V_{BAT} = 1.5 V

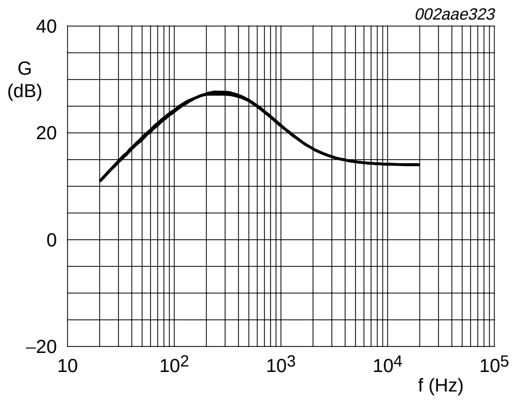
(4) V_{BAT} = 1.7 V

Fig 8. Total harmonic distortion-plus-noise as a function of output power; 32 Ω load



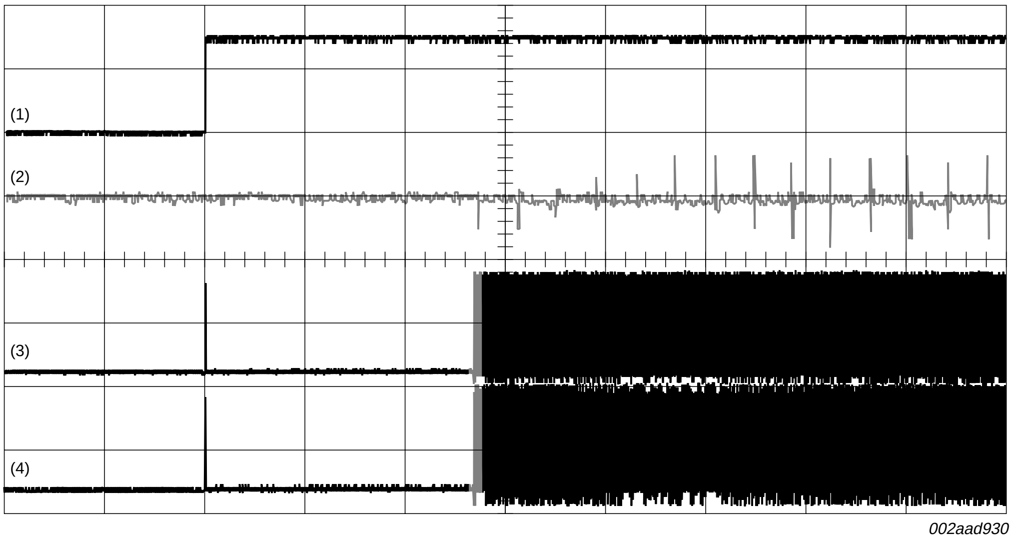
V_{NMIC_IN} = 6.3 mV_{RMS}; V_{bst} = 3 V; V_{BAT} = 1.5 V

Fig 9. Gain as a function of frequency response of feedforward noise reduction circuit; NMIC_INx to MA_OUTx for feedforward application circuit



V_{NMIC_IN} = 10 mV to 50 mV; V_{BAT} = 1.5 V; V_{bst} = 3.1 V

Fig 10. Gain as a function of frequency; NMIC_INx to MA_OUTx for feedback application circuit



At start-up, no signal on music input. No pop or click. The small glitches on trace (2) are just noise from the noise reduction amplifier feed-through. Start-up delay approximately 135 ms.

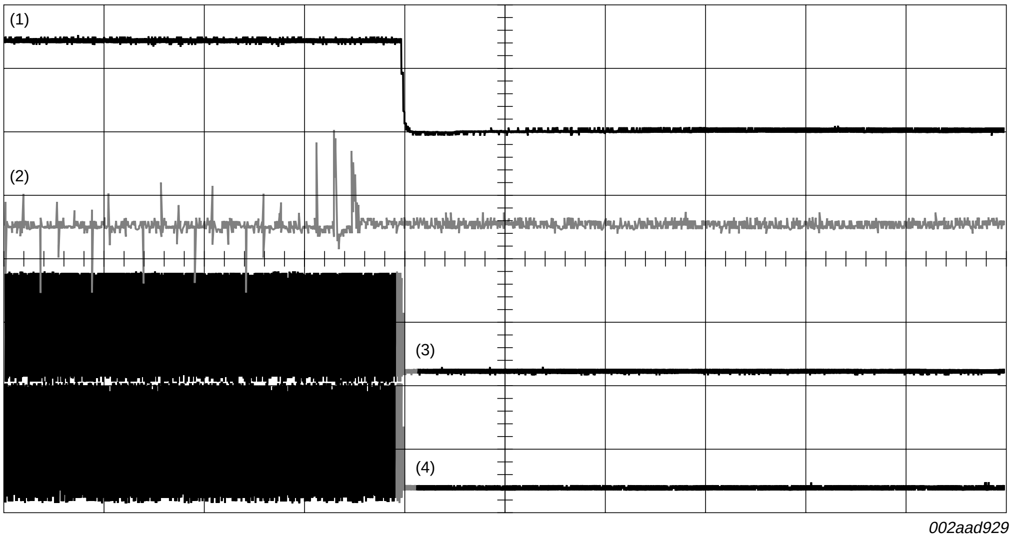
(1) VBAT switch ON to 1.5 V (50 ms; 1.0 V)

(2) Difference between trace (3) and (4), which equates to the pop or click (0.5 ms; 0.54 V)

(3) OUTLP (50 ms; 1.0 V)

(4) OUTLN (50 ms; 1.0 V)

Fig 11. Power-on delay and pop-on noise performance



(1) 50 ms; 1.0 V

(2) 1 ms; 0.5 V

(3) 50 ms; 1.0 V

(4) 50 ms; 1.0 V

Fig 12. Pop-off click performance

10. Application information

10.1 General application description

The NE58633 is a stereo noise reduction IC with a boost converter output at 3.2 V with 2.5 mA load current. Using the on-chip boost converter, it operates from a single cell alkaline battery (0.9 V to 1.7 V). The NE58633 is optimized for low current consumption at 6 mA quiescent current for V_{BAT} = 1.5 V.

Each channel is comprised of a low noise preamplifier which is driven by an electret microphone, a music amplifier and class-D, BTL headphone driver amplifier (see Figure 1 “Block diagram”).

The NE58633 output drivers are capable of driving 800 mV_{rms} across 16 Ω and 32 Ω loads. THD+N performance is 1 % at V_O = 1 V_M and 10 % THD+N at 800 mV_{rms} output voltage driving 16 Ω at a battery voltage of 1.5 V.

The internal reference voltage is set for ½ V_{bst} and is pinned out so it can be externally decoupled to enhance noise performance. The NE58633 differential architecture provides immunity to noise. The output noise is typically 26 μV_{rms} for $G_{v(cl)}$ = 25 dB.

The NE58633 provides ESD and short-circuit protection. It features mute control and plop and click reduction circuitry.

As shown in the application circuit schematics (Figure 13 and Figure 14), the NE58633 may be used for Active Noise Reduction (ANR) in either feedforward or feedback noise-cancelling headphones and earphones in consumer and industrial applications. The gain and filter characteristics of the ANR circuit are set using external resistors and capacitors.

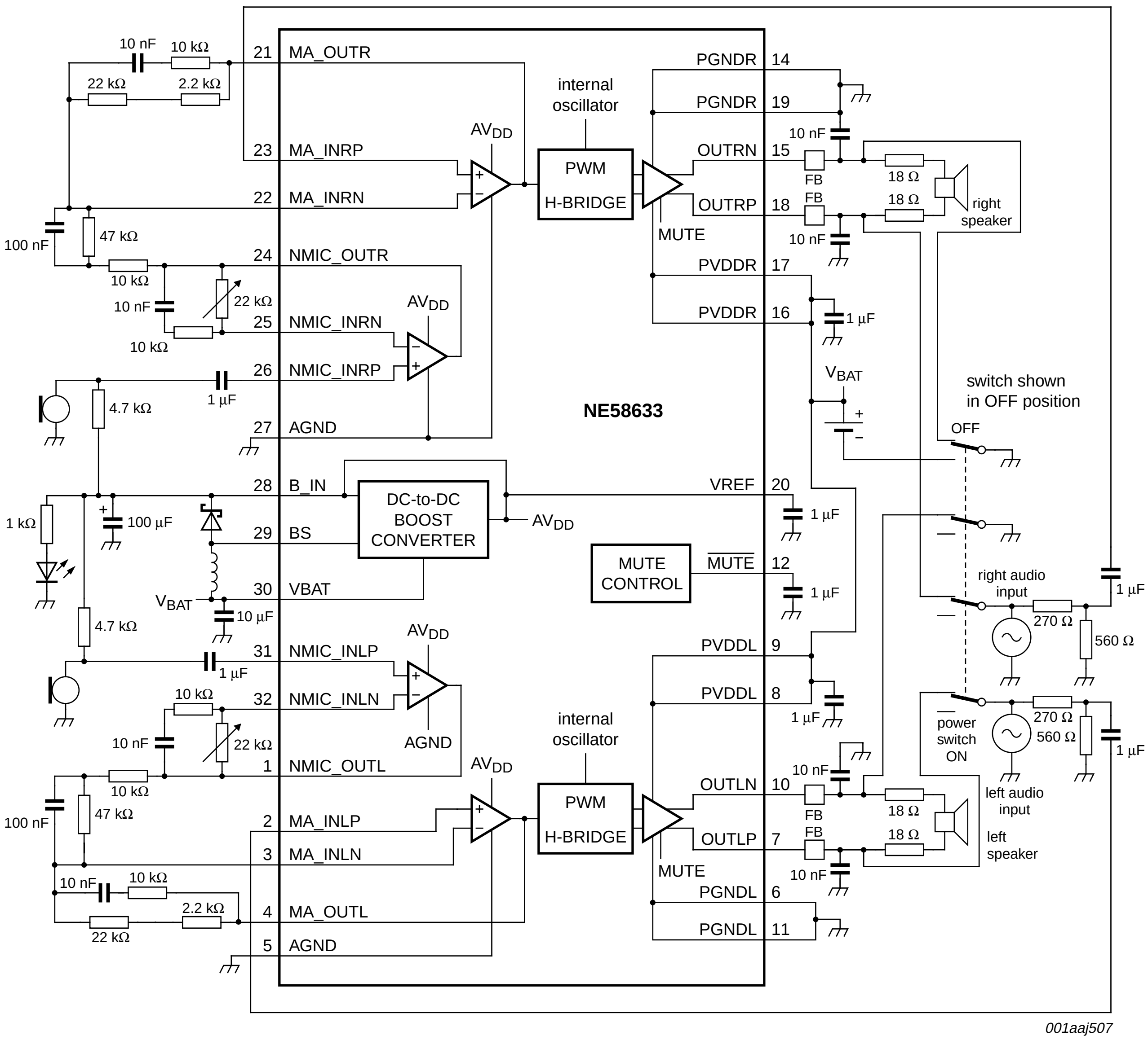


Fig 13. NE58633 feedback application schematic

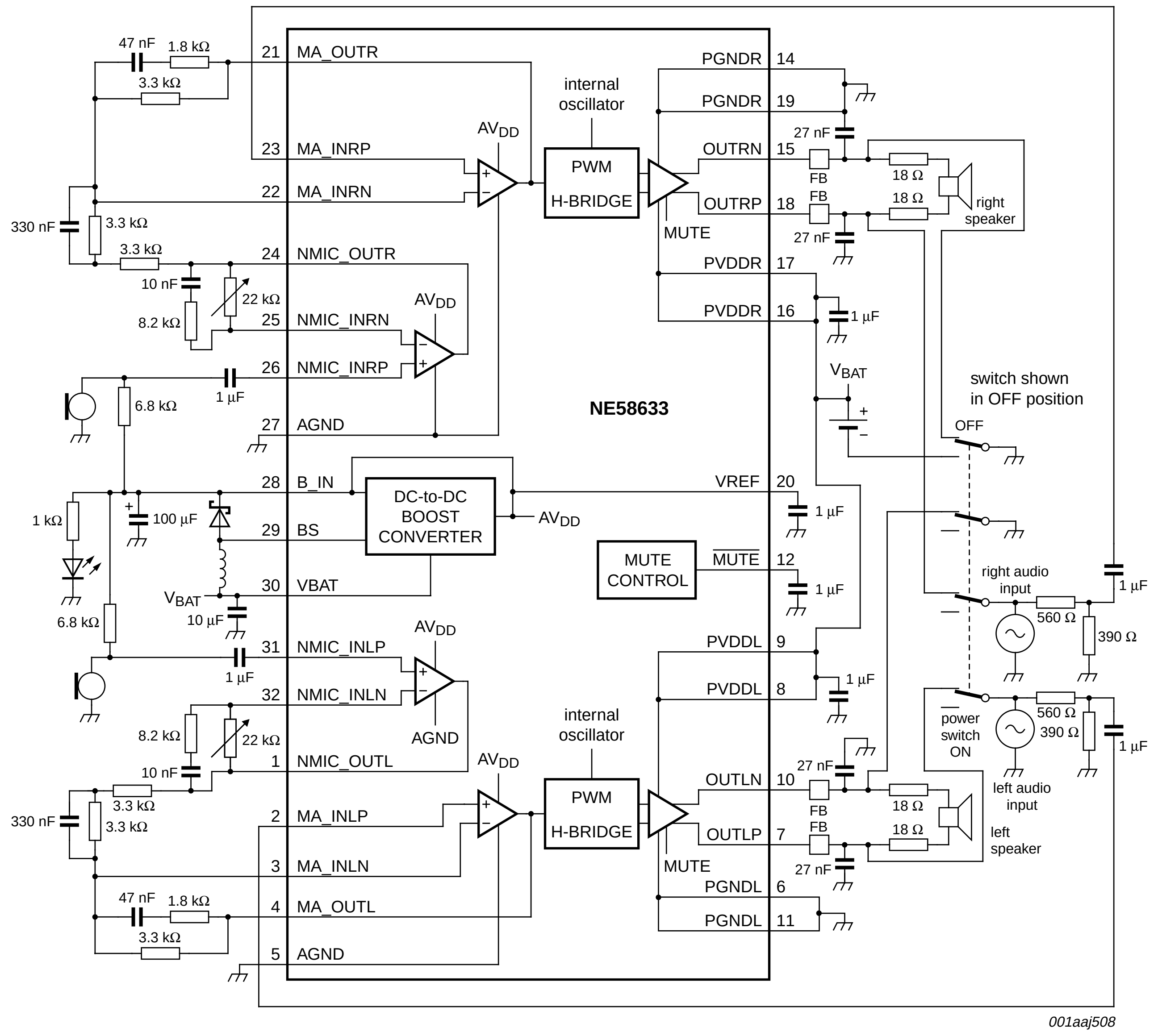


Fig 14. NE58633 feedforward application schematic

10.2 Power supply decoupling

The power supply pins B_IN, PVDDL and PVDDR are decoupled with 1 μF capacitors directly from the pins to ground.

10.3 Speaker output filtering considerations

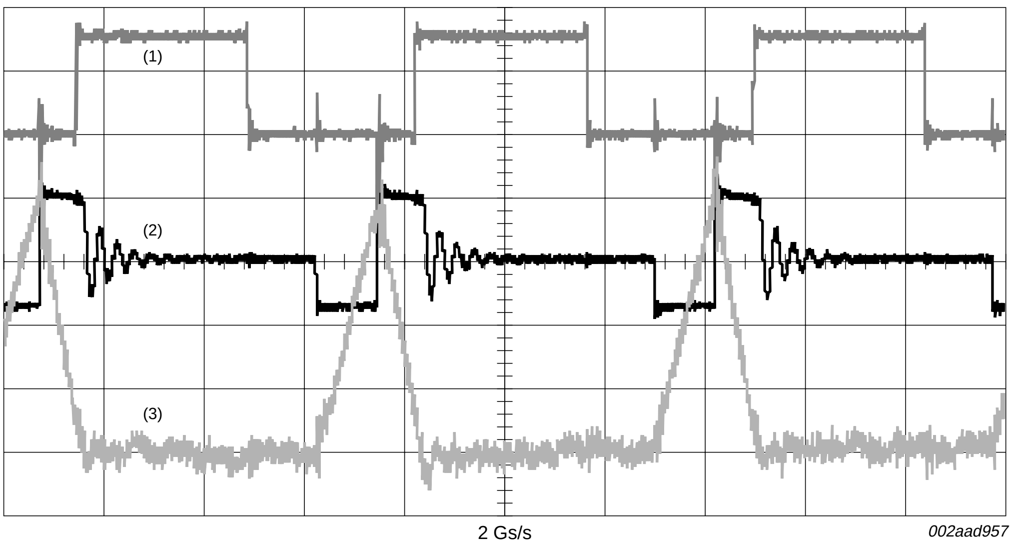
The ferrite beads form a low-pass filter with a shunt capacitor to reduce radio frequency > 1 MHz. Choose a ferrite bead with high-impedance at high frequencies and low-impedance at low frequencies. A typical ferrite bead is 600 Ω at 100 MHz. The low frequency impedance is not as important as in power amplifiers because headphone speakers are stabilized with a series impedance of about 18 Ω on each output. A shunt capacitor is added to complete the low-pass filter.

10.4 Boost converter and layout considerations

10.4.1 Boost converter operation

The boost converter operates in asynchronous mode as shown in Figure 15. As V_{BAT} drops, the boost converter efficiency decreases (see Figure 3 and Figure 6). The boost converter is capable of driving 2.65 mA external load (see Figure 5).

If the NE58633 is operated without the boost converter, pins B_IN, PVDDL and PVDDR may be powered directly from a 3 V power supply source such as 2 AAA alkaline batteries. The VBAT pin is not used.



(1) Positive or negative output of the class-D driver with V_{BAT} at 1.5 V.

(2) Pin BS ($V_{BS} = V_{bst}$).

Remark: This is a normal pulse. It does not change with V_{BAT} but remains at the level of the boosted voltage.

(3) Current at pin B_IN ($I_{bst(load)O}$) measures approximately 40 mA peak, but averaged DC current is a few milliamperes per the specification.

Fig 15. Switching waveform at the BS pin

10.4.2 Critical layout consideration and component selection

The trace between pin BS and the switching inductor must be kept as short as possible. The VBAT side of the boost switching inductor is decoupled by use of a low Equivalent Series Resistance (ESR) 10 μF, 6 V capacitor. A power inductor with low ESR (typically 50 mΩ) should be used. The boost inductor must be 22 μH minimum and 47 μH maximum to ensure proper operation. Pin B_IN is decoupled by use of a 1 μF capacitor directly at the pin with 33 μF to 47 μF at the V_{bst} output at the Schottky diode.

10.5 Mute

Mute may be invoked by directly grounding the pin with a momentary switch. The $\overline{\text{MUTE}}$ pin is active LOW. The outputs are muted automatically when V_{BAT} is less than or equal to 0.9 V. The $\overline{\text{MUTE}}$ pin is decoupled to ground with a 1 μF capacitor.

10.6 Internal reference, VREF pin

The internal reference is pinned out so it can be filtered with a capacitor to ground. The recommended value is 1 μF to 10 μF. Ensure that the biasing time constant at pin VREF does not exceed the power-on delay time or a pop-on click will heard.

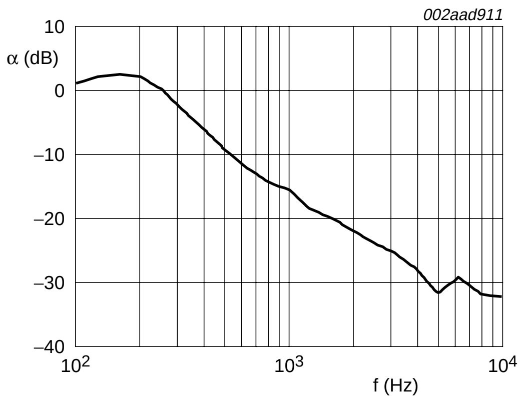
10.7 Power-on delay time and pop and click performance

Power-on delay time of typically 135 ms is imposed to allow the input biasing to power-up and stabilize. This eliminates pop-on noise.

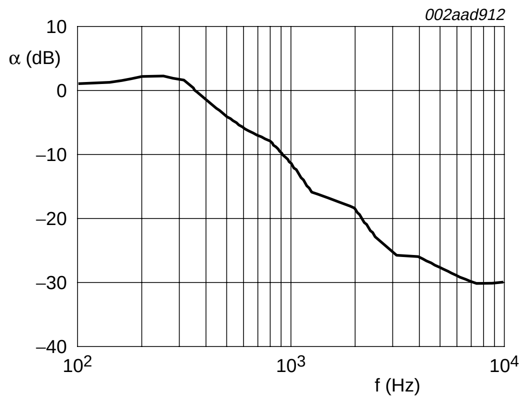
10.8 Active Noise Reduction (ANR) concepts

10.8.1 Basic concept

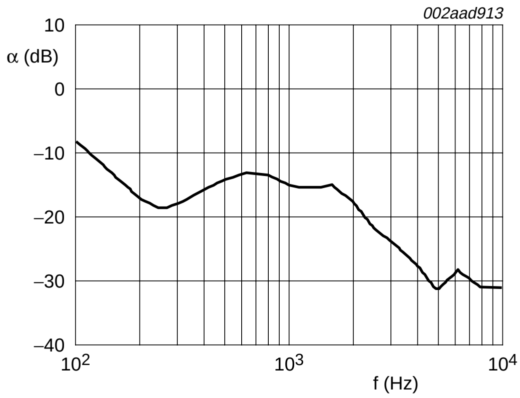
Noise reduction headphones utilize Passive Noise Reduction (PNR) provided by the passive noise reduction of the headphone acoustical plant alone. The amount of PNR is greatest at the high frequencies and least at the low frequencies. The addition of Active Noise Reduction (ANR) greatly increases the amount of noise reduction at low frequencies. The combined effect of PNR and ANR provides noise reduction over an appreciable hearing range. Figure 16 shows the combined effect of both PNR and ANR in an over-the-ear noise-cancelling FB headphone.



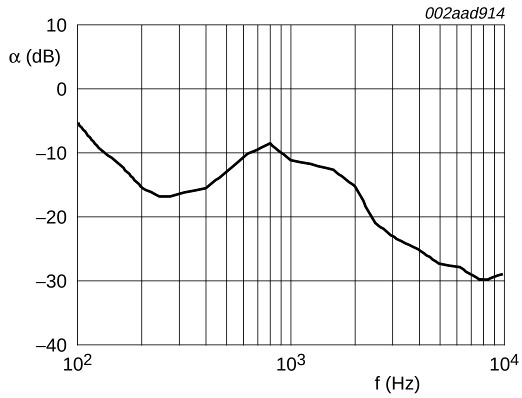
a. Passive attenuation left



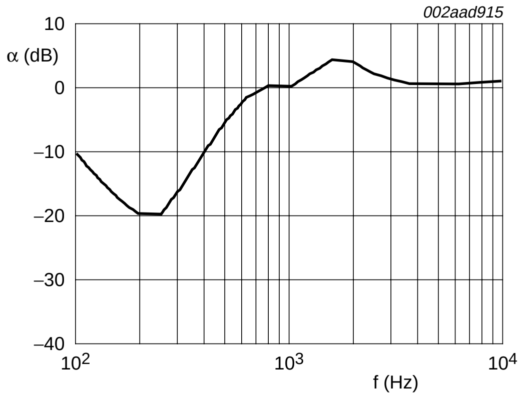
b. Passive attenuation right



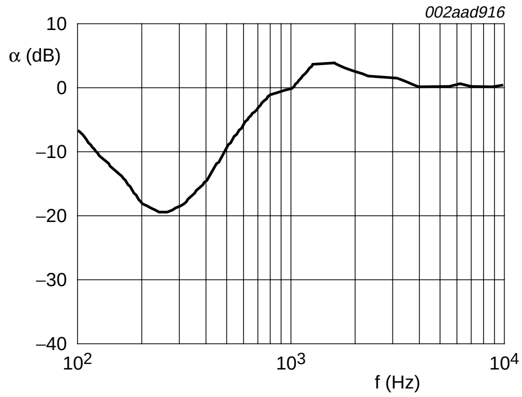
c. Total attenuation left



d. Total attenuation right



e. Active attenuation left



f. Active attenuation right

Fig 16. Combined noise reduction (PNR + ANR) of typical over-the-ear FB application

10.8.2 Feedforward circuit

10.8.2.1 Conceptual diagram of feedforward application

Figure 17 shows the typical feedforward application diagram in which the noise cancelling microphone samples the noise outside the acoustic plant of the headphone or earphone.

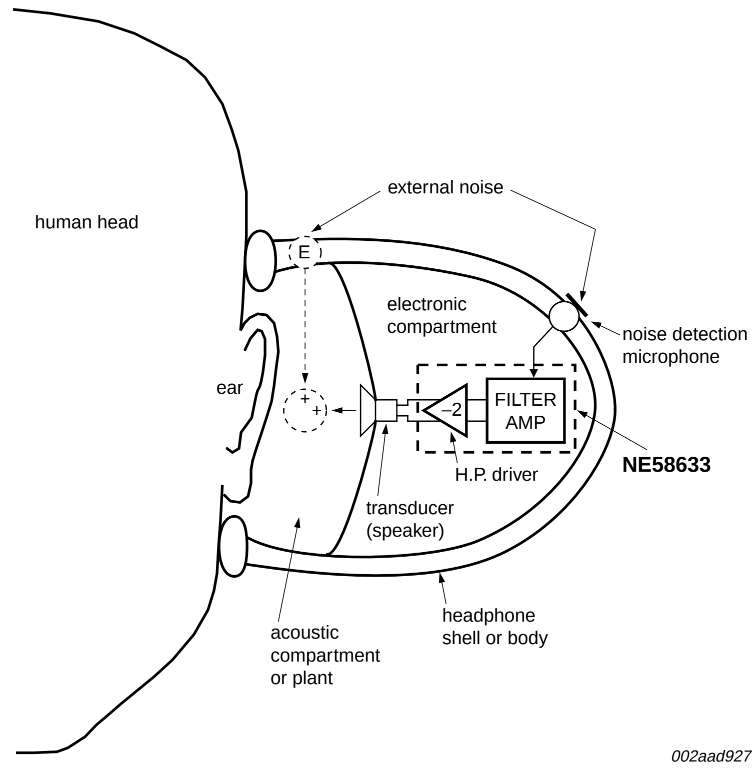


Fig 17. Feedforward conceptual diagram

This method produces a noise-cancelling signal that tries to replicate the noise in the acoustical plant at the loudspeaker and entrance to the ear. The replication is never exact because the microphone is located outside the headphones; the noise sampled is not a perfect replica of the noise inside the ear cup, which is altered by passing through the ear cup as well as by the internal reflections. In fact, in some cases the anti-noise may actually introduce noise inside the headphones.

The headphone loudspeaker or transducer is used to send the normal audio signal as well as the feedforward signal providing noise cancellation. The microphone detects the external noise and its output is amplified and filtered, and phase is inverted by the low noise preamplifier and music amplifier in the NE58633.

10.8.2.2 Feedforward demo board schematic

The evaluation demo board uses a typical filter design and may not yield the optimal noise cancelling performance for a given headphone mechanical-acoustical plant.

10.8.3 Feedback circuit

10.8.3.1 Conceptual diagram of feedback application

Figure 18 shows the typical feedback application diagram in the which the noise cancelling microphone samples the noise and music inside the acoustical plant.

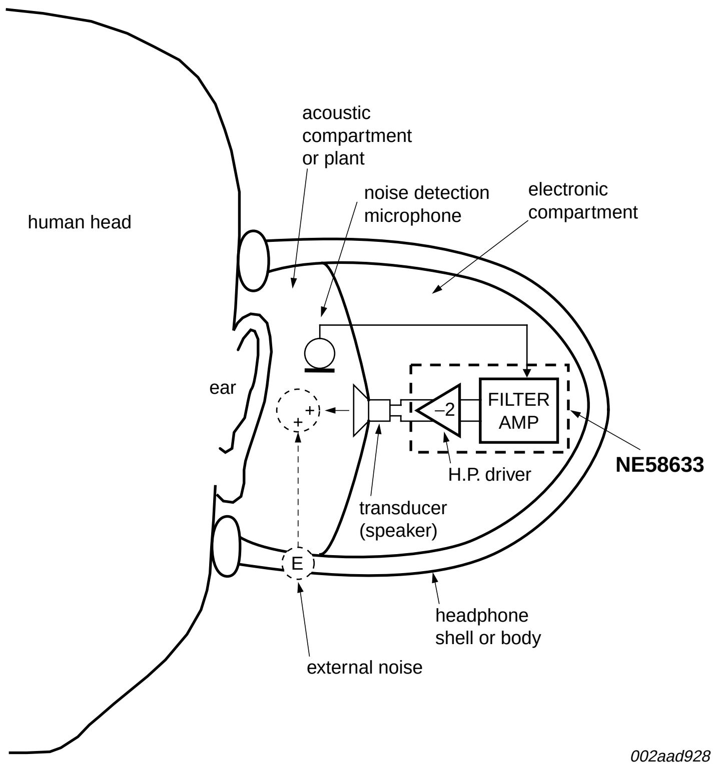


Fig 18. Feedback conceptual diagram

The feedback solution employs a low cost, battery operated analog Active Noise Reduction (ANR) technique. The topology uses negative feedback circuitry in which the noise reduction microphone is placed close to the ear and headphone loudspeaker. By detecting the noise with the microphone in the position closer to the ear, a noise cancelling effect with high accuracy is realized. This technique produces a noise cancelling signal that always minimizes the noise in the ear canal or entrance to the ear canal. The audio signal is analyzed with exact timing with the noise cancelling signal. The noise cancelling signal increases with increasing noise level.

The headphone loudspeaker or transducer is used to send the normal audio signal as well as the feedback signal providing noise cancellation. The microphone is placed near the loudspeaker and its output is amplified, filtered, and phase inverted by the feedback network and sent back to the loudspeaker.

The design of the feedback filter for a given headphone plant involves a trade-off between performance on one hand and stability and robustness with respect to variations of the headphone plant on the other. Traditional feedback design methods use filter elements such as, lead, lag and notch filters which are appropriately tuned to shape the audio response of the system to obtain good performance with sufficient stability margins.

Since the attenuation performance of an analog ANR headphone is defined in the design stage, it has limited applicability to work in different environments. Overall noise cancelling performance is achieved by first characterizing the passive attenuation of headphone plant and then designing the ANR circuitry to obtain the optimal overall noise reduction performance and stability. Figure 16 shows combined noise reduction results of typical over-the-ear feedback headphone. The combined noise reduction is the sum of the PNR of the plant and the active noise reduction of the feedback filter circuit.

10.8.3.2 Feedback demo board schematic

The evaluation demo board embodies a typical filter design and may not yield the optimal noise cancelling performance for a given headphone mechanical-acoustical plant.

11. Test information

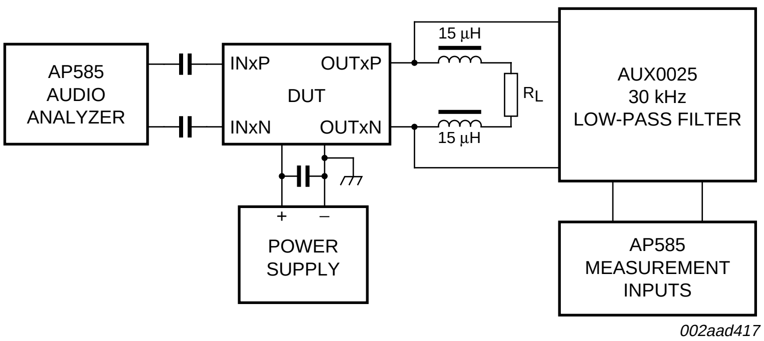
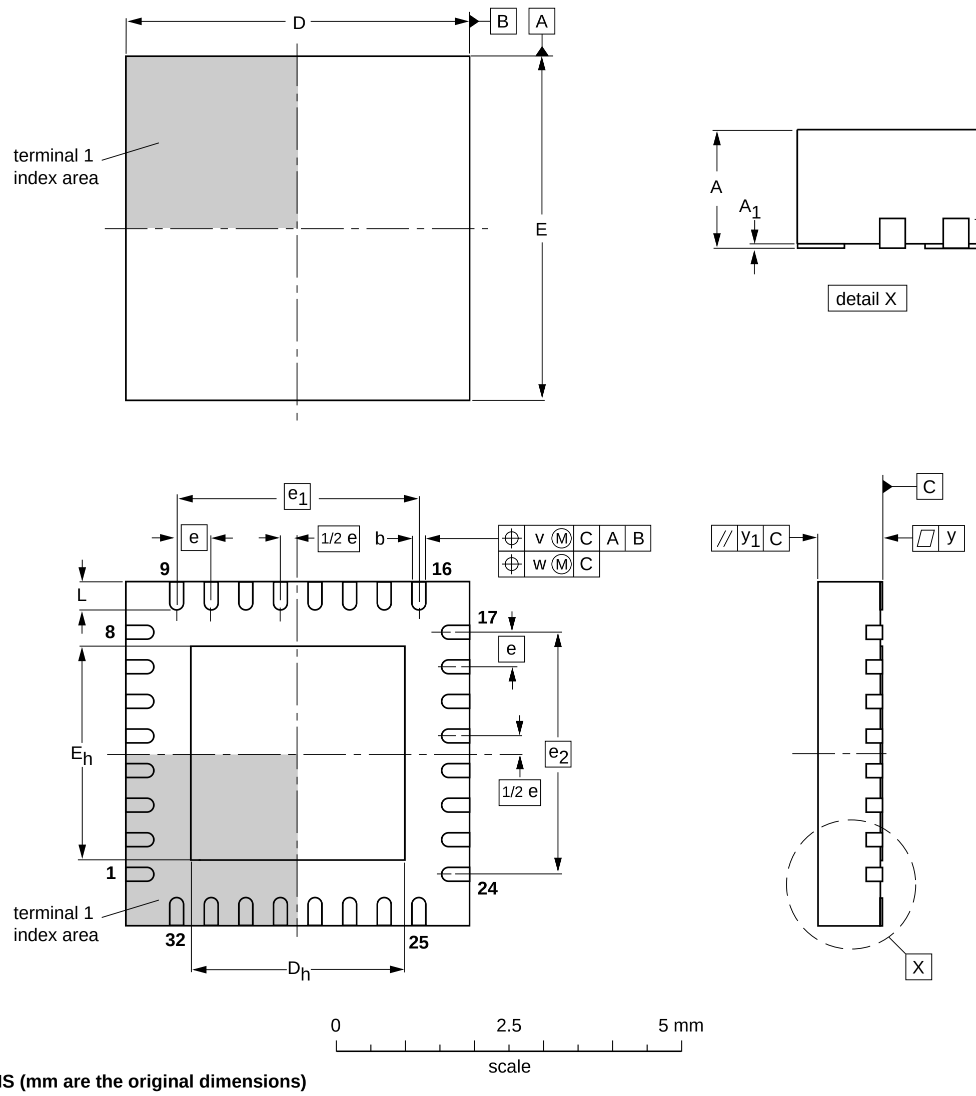


Fig 19. NE58633 test circuit

12. Package outline

HVQFN32: plastic thermal enhanced very thin quad flat package; no leads; 32 terminals; body 5 x 5 x 0.85 mm **SOT617-1**



DIMENSIONS (mm are the original dimensions)

UNIT	A(1) max.	A_1	b	c	D(1)	D_h	E(1)	E_h	e	e_1	e_2	L	v	w	y	y_1
mm	1	0.05 0.00	0.30 0.18	0.2	5.1 4.9	3.25 2.95	5.1 4.9	3.25 2.95	0.5	3.5	3.5	0.5 0.3	0.1	0.05	0.05	0.1

Note

1. Plastic or metal protrusions of 0.075 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT617-1	- - -	MO-220	- - -			~~01-08-08~~ 02-10-18

Fig 20. Package outline SOT617-1 (HVQFN32)

13. Soldering of SMD packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering ICs can be found in Application Note *AN10365 "Surface mount reflow soldering description"*.

13.1 Introduction to soldering

Soldering is one of the most common methods through which packages are attached to Printed Circuit Boards (PCBs), to form electrical circuits. The soldered joint provides both the mechanical and the electrical connection. There is no single soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and Surface Mount Devices (SMDs) are mixed on one printed wiring board; however, it is not suitable for fine pitch SMDs. Reflow soldering is ideal for the small pitches and high densities that come with increased miniaturization.

13.2 Wave and reflow soldering

Wave soldering is a joining technology in which the joints are made by solder coming from a standing wave of liquid solder. The wave soldering process is suitable for the following:

- Through-hole components
- Leaded or leadless SMDs, which are glued to the surface of the printed circuit board

Not all SMDs can be wave soldered. Packages with solder balls, and some leadless packages which have solder lands underneath the body, cannot be wave soldered. Also, leaded SMDs with leads having a pitch smaller than ~0.6 mm cannot be wave soldered, due to an increased probability of bridging.

The reflow soldering process involves applying solder paste to a board, followed by component placement and exposure to a temperature profile. Leaded packages, packages with solder balls, and leadless packages are all reflow solderable.

Key characteristics in both wave and reflow soldering are:

- Board specifications, including the board finish, solder masks and vias
- Package footprints, including solder thieves and orientation
- The moisture sensitivity level of the packages
- Package placement
- Inspection and repair
- Lead-free soldering versus SnPb soldering

13.3 Wave soldering

Key characteristics in wave soldering are:

- Process issues, such as application of adhesive and flux, clinching of leads, board transport, the solder wave parameters, and the time during which components are exposed to the wave
- Solder bath specifications, including temperature and impurities

13.4 Reflow soldering

Key characteristics in reflow soldering are:

- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 21) than a SnPb process, thus reducing the process window
- Solder paste printing issues including smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature) and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic). In addition, the peak temperature must be low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 7 and 8

Table 7. SnPb eutectic process (from J-STD-020C)

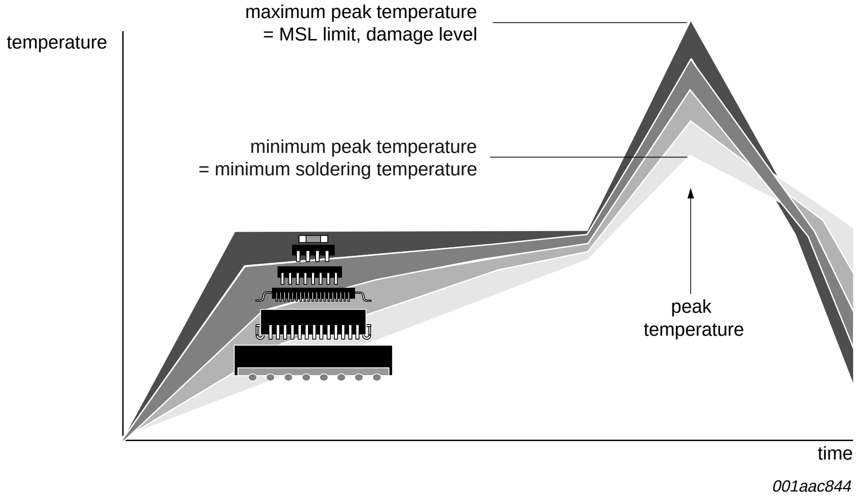
Package thickness (mm)	Package reflow temperature (°C)	
	Volume (mm^3)	
	< 350	≥ 350
< 2.5	235	220
≥ 2.5	220	220

Table 8. Lead-free process (from J-STD-020C)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 21.



MSL: Moisture Sensitivity Level

Fig 21. Temperature profiles for large and small components

For further information on temperature profiles, refer to Application Note *AN10365 “Surface mount reflow soldering description”*.

14. Abbreviations

Table 9. Abbreviations

Acronym	Description
ANR	Active Noise Reduction
BTL	Bridge Tied Load
DUT	Device Under Test
ESD	ElectroStatic Discharge
ESR	Equivalent Series Resistance
FB	FeedBack
RMS	Root Mean Squared
PNR	Passive Noise Reduction
PWM	Pulse Width Modulation

15. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
NE58633_1	20090122	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term ‘short data sheet’ is explained in section “Definitions”.

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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18. Contents

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Date of release: 22 January 2009
Document identifier: NE58633_1