AN-6755

Design Guideline to Replace FAN6753 with FAN6755

Introduction

FAN6755 is a highly integrated PWM controller featuring green-mode, frequency hopping, constant power limit, and a number of protection functions. Green mode and burst mode function with a low operating current to maximize the light-load efficiency so the power supply can meet stringent standby power regulations. Frequency hopping reduces the Electro-Magnetic Emission (EMI) by spreading the frequency spectrum. The constant power limit function minimizes the component stress in abnormal conditions and helps optimize the power stage. Protection functions such as brownout, overload/open-loop (OLP), over-voltage (OVP), and over-temperature (OTP) are fully integrated, which improves the reliability of switched-mode power supplies (SMPS) without increasing system cost. This application note explains how to replace PWM controller FAN6753 with FAN6755. Only VIN and Latch pins are different; however, some functional improvements have been made to FAN6755 for higher efficiency, lower power consumption, and better performance. Therefore, several external components should be changed accordingly. Table 1 summarizes the differences between these two devices. The operating current is reduced to achieve lower standby power consumption, which allows less than 100mW standby power consumption for most of LCD monitor power supply designs. The typical application circuit and internal block diagram are shown in Figure 1 and Figure 2, respectively.

Table 1. Comparison of FAN6753 and FAN6755

	FAN6753	FAN6755
HV Pin Input Voltage	500V	700V
Brownout Protection	No	Line Sensing Using VIN Pin
Line Voltage Compensation for Pulse-by-Pulse Current Limit ($V_{limit-L}$ / $V_{limit-H}$)	Saw-Limit (0.9V/0.56V)	Adjusted by VIN Pin (0.83V/0.7V)
Sense Pin Short-Circuit Protection (SCP)	V_{SENSE}<0.15V Longer than 150μs	No
Gate Source Current	250mA	700mA
FB Impedance (Z_{FB})	5KΩ	15KΩ
Operating Current (I_{DD-OP})	2.7mA	2mA
Leading-Edge Blanking Time (t_{LEB})	150ns	290ns
Minimum Operating Voltage (UVLO)	9.5V	7.8V
Maximum Duty Cycle	65%	75%
Soft-Start (t_{SS})	5.0ms	5.5ms
Package	8-Pin SOP Package	7-Pin SOP Package

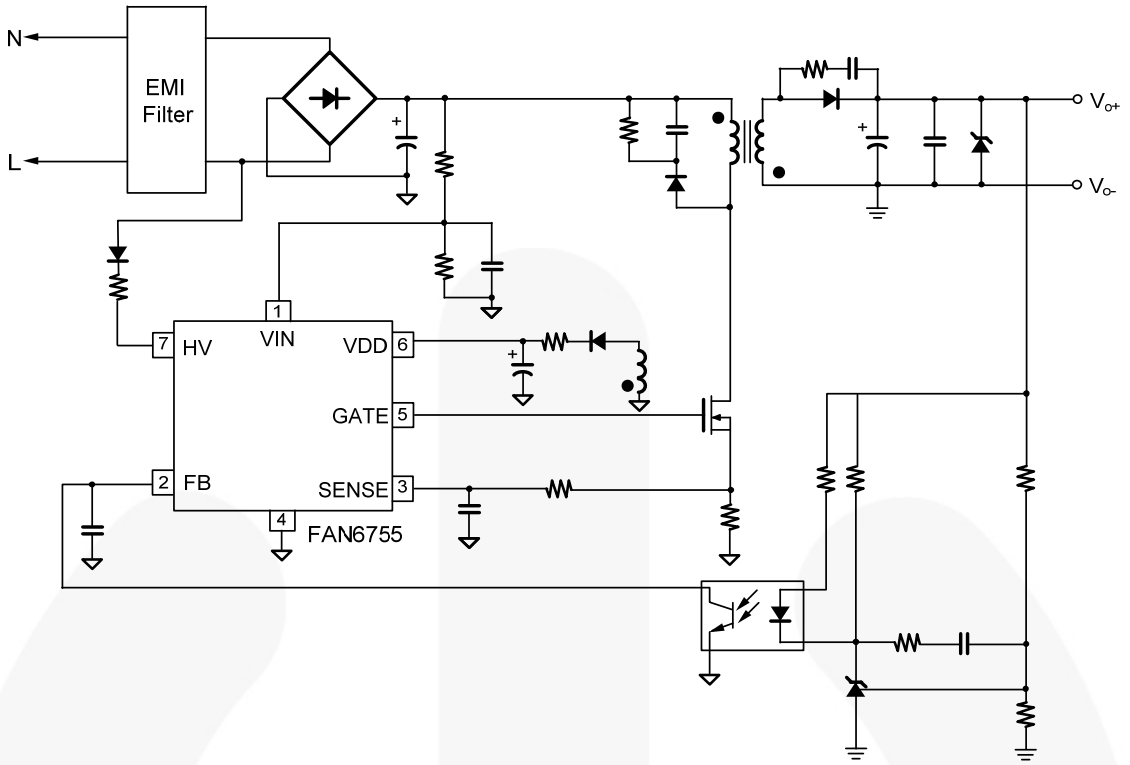

Figure 1. Typical Application

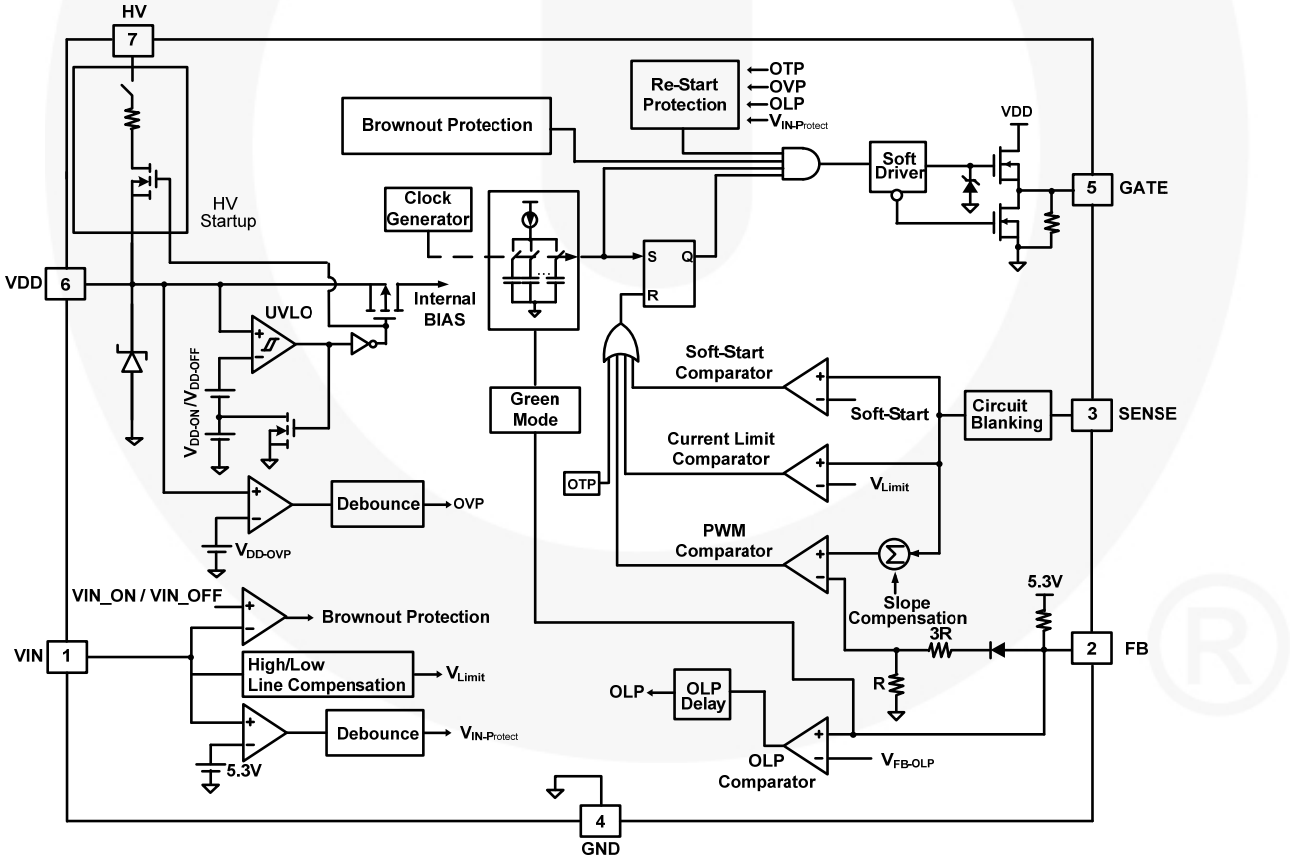

Figure 2. Internal Block Diagram

HV Startup Circuit

Figure 3 shows the simplified schematic for the HV startup circuit. When the AC line is applied to the power supply, the internal high-voltage current source charges the hold-up capacitor C_1 through a startup resistor R_{HV}. As the V_{DD} pin voltage reaches the turn-on threshold V_{DD-ON}, the PWM controller is enabled and starts normal operation. Then, the high-voltage current source is switched off and the supply current is drawn from the auxiliary winding of the main transformer, as shown in Figure 3. For better line surge immunity of the HV pin, it is typical to use a R_{HV} resistor larger than 100kΩ. When a large capacitor is required for V_{DD}, the R_{HV} resistor limits the charging current for the V_{DD} capacitor, increasing the startup time. A two-stage V_{DD} capacitor circuit as shown in Figure 3 is typically used to shorten the startup time.

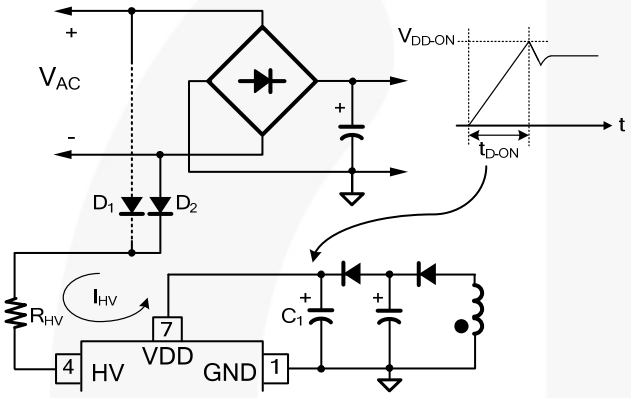

Figure 3. Startup Circuit

Soft-Start

FAN6755 has an internal soft-start circuit that progressively increases the pulse-by-pulse current limit level, as shown in Figure 4. The built-in soft-start circuit significantly reduces the input current overshoot during startup, which also minimizes output voltage overshoot.

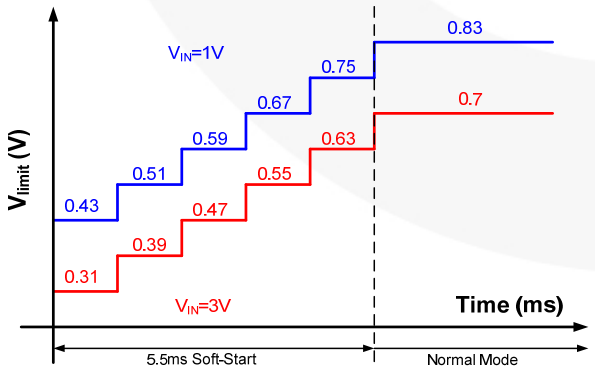

Figure 4. Pulse-by-Pulse Current Limit Level for Soft-Start

Under-Voltage Lockout (UVLO)

The FAN6755 has an under-voltage lockout (UVLO) on the VDD pin to ensure that the chip has enough voltage to drive the MOSFET. The UVLO circuit of FAN6755 has a two-level UVLO threshold, as depicted in Figure 5.

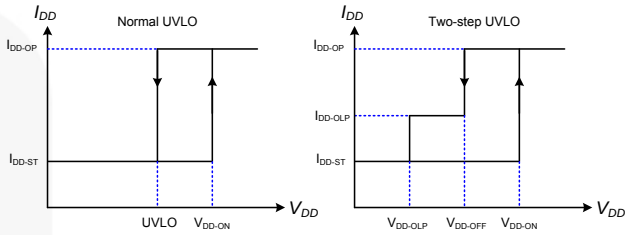

Figure 5. UVLO Specification

Normal Operation

The turn-on and turn-off thresholds are internally fixed at 16V and 7.8V for normal operation. During startup, the IC is enabled when V_{DD} reaches 16V. Once the IC is enabled, the V_{DD} capacitor continues supplying V_{DD} until enough voltage is established across the transformer auxiliary winding by the switching operation.

The FAN6755 has a low UVLO, allowing designers to reduce the auxiliary winding voltage to supply at the low-voltage IC operation. This method reduces the IC losses and switching losses.

The IC losses and switching losses are calculated by:

$$P_{IC\_Loss} = V_{DD} \times I_{OP} \quad (1)$$

$$P_{Switch\_Loss} = \frac{1}{2} \times C_{iss} \times V_{DD}^{2} \times f_{SW} \quad (2)$$

The one-step UVLO appears under normal condition. Figure 7 shows the one-step UVLO method.

Abnormal Operation

If the output is shorted, is overloaded, or the feedback loop is opened; the FB voltage remains above V_{FB-OLP} for OLP delay time (t_{D-OLP}) until the protection is triggered. During that time, the MOSFET drain-to-source current reaches its pulse-by-pulse current limit level for every switching cycle, causing a large amount of power dissipation to the switching devices and transformer. With the two-step UVLO mechanism, the average input power during overload or open-loop condition is greatly reduced. The FAN6755 protection is a two-step UVLO (V_{IN-OFF}, $V_{IN-Protect}$ and V_{DD-OVP}). This method is convenient for designers to check the protection mechanism. Figure 6 shows the two-step UVLO method.

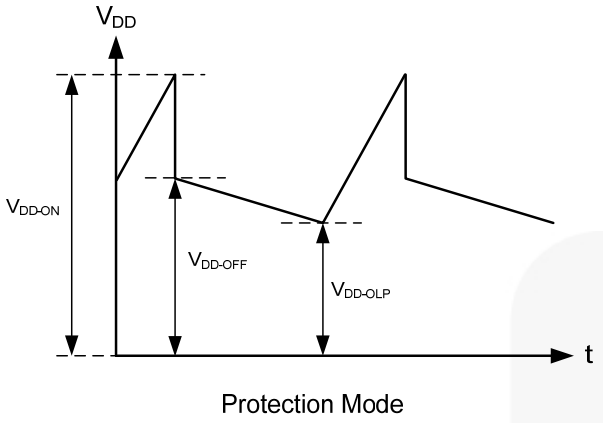

Figure 6. Two-Step UVLO

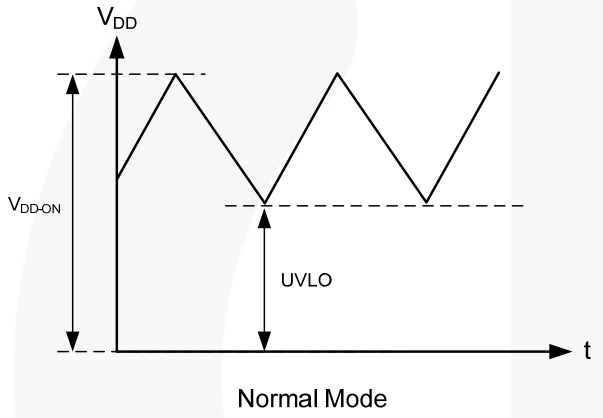

Figure 7. One-Step UVLO

Green-Mode Operation

The FAN6755 uses feedback voltage (V_{FB}) as an indicator of the output load and modulates the PWM frequency, as shown in Figure 8 such that the switching frequency decreases as load decreases. In heavy load conditions, the switching frequency is 65KHz. Once V_{FB} decreases below V_{FB-N} (3.0V), the PWM frequency starts to linearly decrease from 65KHz to 23kHz to reduce the switching losses. As V_{FB} decreases below V_{FB-G} (2.4V), the switching frequency is fixed at 23kHz. As V_{FB} decreases below V_{FB-ZDC} (1.6V), FAN6755 enters burst-mode operation. When V_{FB} drops below V_{FB-ZDC}, FAN6755 stops switching and the output voltage starts to drop, which causes the feedback voltage to rise. Once V_{FB} rises above $V_{FB-ZDCR}$ (1.8V), switching resumes. Burst mode alternately enables and disables switching, thereby reducing switching loss in standby mode, as shown in Figure 9.

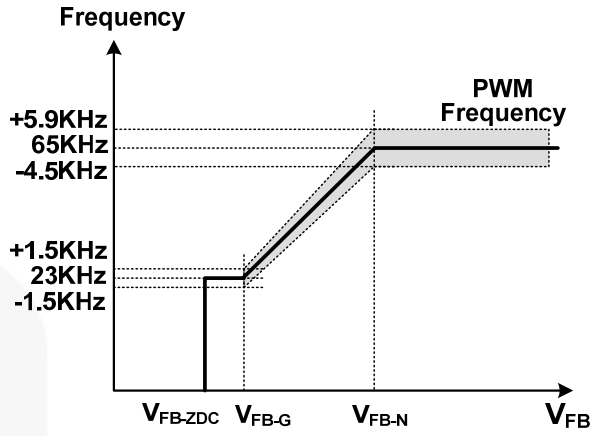

Figure 8. Frequency Modulation

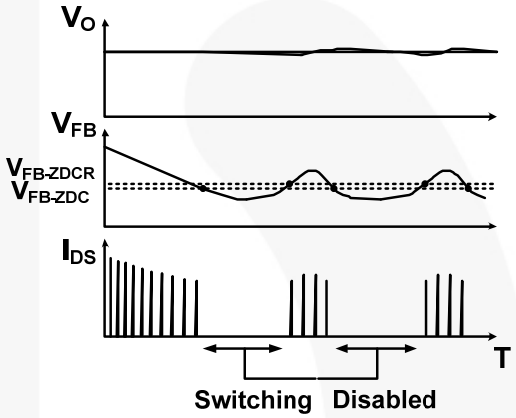

Figure 9. Burst-Mode Operation

FB Input

The FAN6755 is designed for peak-current-mode control. A current-to-voltage conversion is accomplished externally with a current-sense resistor, R_S. Under normal operation, the FB level controls the peak inductor current:

$$I_{pk} = \frac{V_{FB} - 0.6}{4 \times R_S} \quad (3)$$

where V_{FB} is the voltage on the FB pin and 4 is an internal divider ratio.

When V_{FB} is less than 0.6V, the FAN6755 does not output the gate drive signals.

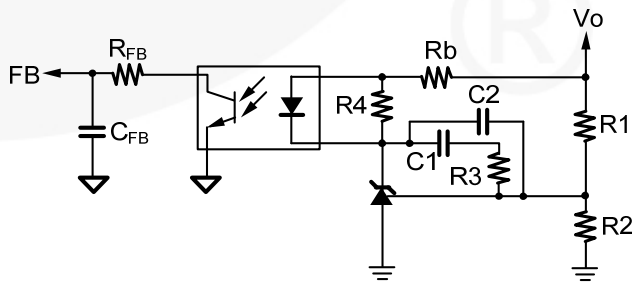

Figure 10. Feedback Circuit

Figure 10 is a typical feedback circuit consisting mainly of a shunt regulator and an opto-coupler. R_1 and R_2 form a voltage divider for the output voltage regulation. R_3 and C_1 are adjusted for control-loop compensation. A small-value RC filter (e.g. R_{FB}= 47Ω, C_{FB}= 1nF) placed across the FB pin and the GND can further increase the stability.

The compensation network is designed around the error amplifier implemented with the shunt regulator. A certain amount of laboratory adjustment is inevitable, but in general, the type-II compensation scheme shown in Figure 10 handles most compensation requirements. There is a pole at the origin that contributes a –1 slope in the gain plot. A low-frequency zero, f_{EAZERO} (Equation 4), flattens out the slope so the midrange gain is equal to R_3/R_1. A high-frequency pole, f_{EAPOLE} (Equation 5), helps suppress any high-frequency noise from propagating through the system. R_2 forms a voltage divider with R_1 and provides a DC offset. By combining the Bode plots of the PWM and power stage with the error amplifier compensation, a plot of the entire system is realized.

$$f_{EAZERO} = \frac{1}{2\times\pi\times R_3\times C_1} \quad (4)$$

$$f_{EAPOLE} = \frac{1}{2\times\pi\times R_3\times C_2} \quad (5)$$

The maximum sourcing current of the FB pin is 0.35mA. The phototransistor must be capable of sinking this current to pull the FB level down at no load. Thus, the value of the biasing resistor R_b is determined as:

$$\frac{V_o - V_D - V_Z}{R_b}\cdot K \geq 0.35mA \quad (6)$$

where:

V_D is the drop voltage of photodiode, approximately 1.2V;

V_Z is the minimum operating voltage, 2.5V of the shunt regulator; and

K is the Current Transfer Rate (CTR) of the opto-coupler.

For an output voltage V_O=5V with CTR=100%, the maximum value of R_b is 1.2KΩ.

There are some technologies to improve power saving by changing the impedance of the FB pin. This method can reduce the operating current (I_{DD-OP}) when the feedback voltage drops below V_{FB-ZDC}, which can further reduce IC power consumption. Figure 10 exhibits the range of the FB pin impedance change. Z_{FB} is switched from 15KΩ to 75KΩ when FB is lower than V_{FB-ZDC}. On the other hand, Z_{FB} is switched from 75KΩ to 15KΩ when FB is higher than $V_{FB-ZDCR}$.

The change of impedance to 75KΩ reduces the CTR, as well as the DC gain of the feedback loop. Therefore, loop stability is a critical concern. Refer to the following DC gain calculation equation: the minimum R_b value should be estimated by Z_{FB}=75KΩ to restrain loop instability:

$$DC\ \ Gain = CTR\times\frac{Z_{FB}}{R_b} \quad (7)$$

where:

Z_{FB} is input impedance of FB pin.

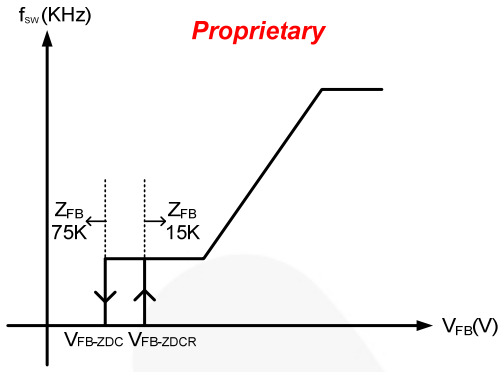

Figure 11. Power-Saving Improvement by Z_{FB} Soft Switching

The internal pull-up resistor in FAN6753 is 5kΩ, but FAN6755 has a larger pull-up resistor (15kΩ) to reduce power consumption. Therefore, R_b should be three times the original value when FAN6753 is replaced with FAN6755 to have to same loop gain.

Leading-Edge Blanking (LEB)

Each time the power MOSFET is switched on, a turn-on spike may occur across the sense-resistor caused by primary-side capacitance and secondary-side rectifier reverse recovery (*see Figure 12*). To avoid premature termination of the switching pulse, a leading-edge blanking time is built in. During this blanking period (290ns), the PWM comparator is disabled and cannot switch off the gate driver. Thus, an RC filter with a small RC time constant (e.g. 100Ω + 470pF) is enough for current sensing. A non-inductive resistor for R_S is recommended.

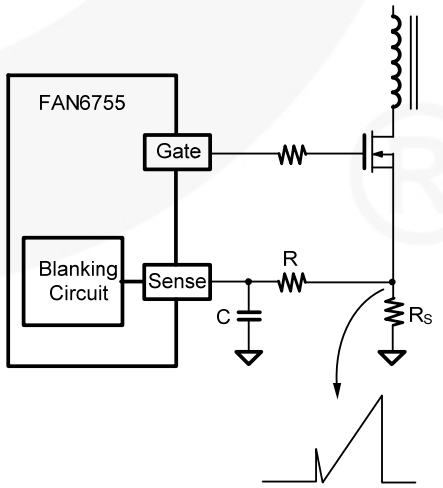

Figure 12. Turn-On Spike

Output Driver / Soft Driving

The output stage is a fast totem-pole gate driver capable of directly driving external MOSFETs. An internal Zener diode clamps the driver voltage under 18V to protect the MOSFET gate from over voltage. Due to integrated circuits that control the switching speed, the external resistor R_G (Figure 13) may not be necessary to reduce switching noise.

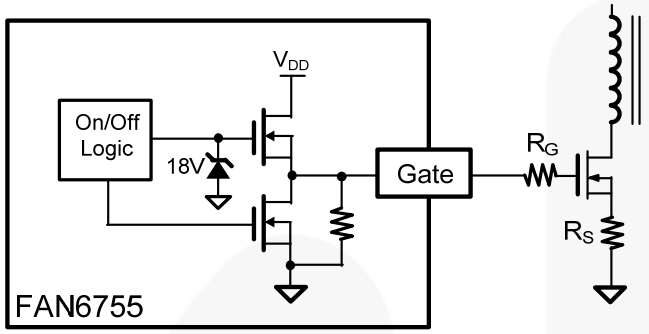

Figure 13. Gate Driver

High / Low Line Compensation in VIN Pin

The conventional pulse-by-pulse current-limiting scheme has a constant threshold for current limit comparator, which results in higher power limit for high line voltage. FAN6755 has a current-limit threshold that decreases as line voltage increases to make the actual power limit level almost constant over different line voltages of universal input range, as shown in Figure 14. In the FAN6755, the peak-current-limiting threshold is adjusted by the peak voltage of the VIN pin. When the circuit senses the bulk capacitor input voltage (V_{Bulk}) at the VIN pin and for R_1, R_2, and C_1 set to 20MΩ (10MΩ +10MΩ), 160KΩ, and 2.2μF; then when V_{Bulk} is around 126V and the threshold voltage for current limit is around 0.83V as measured from the reference board design.

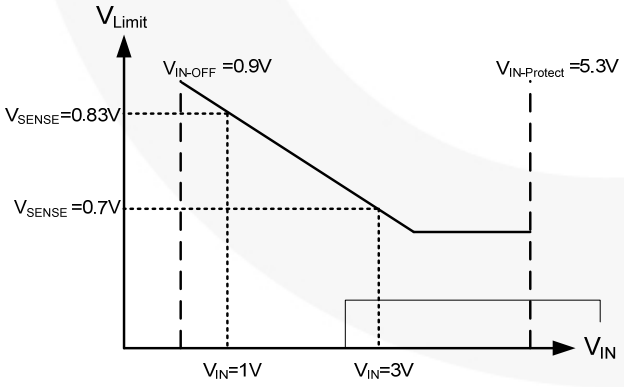

Figure 14. V_{Limit} Level vs. V_{IN}

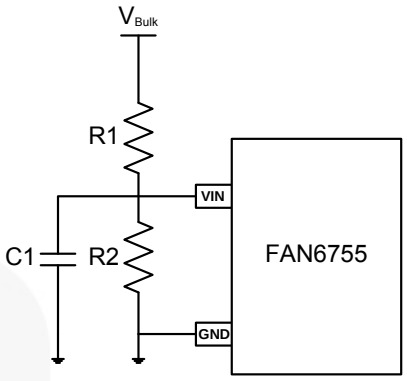

Figure 15. Input Voltage Compensation for Constant Output Power Limit

Brownout Protection in VIN Pin

Since the VIN pin is connected through a resistive divider to the bulk capacitor voltage, it can also be used for brownout protection. If the V_{IN} voltage is less than 0.7V, the PWM output is shut off. As the V_{IN} voltage reaches 0.9V, the PWM output is enabled again. The hysteresis window for ON/OFF is around 0.2V. The recommended values for R_1, R_2, and C_1 are 20MΩ (10MΩ +10MΩ), 160KΩ, and 2.2μF. Using these values in the test board, the power supply is turned off at 62V (maximum load) and recovered at 80V.

The V_{IN-ON} and V_{IN-OFF} are calculated by:

$$V_{IN-ON}(RMS) = (0.9 \times \frac{R_1 + R_2}{R_2}) / \sqrt{2} \quad (8)$$

$$V_{IN-OFF}(RMS) = (0.7 \times \frac{R_1 + R_2}{R_2}) / \sqrt{2} \quad (9)$$

Recovery Function in VIN Pin

The recovery function using the VIN pin is available in the FAN6755. When V_{IN} is higher than 5.3V, FAN6755 stops operation, then restarts. Figure 16 shows the external circuit for secondary-side output OVP. If output voltage (V_O) is higher than the Zener diode voltage (V_Z), the VIN pin is pulled HIGH and the FAN6755 is in recovery.

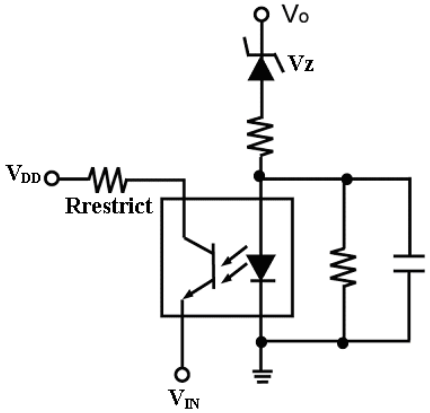

Figure 16. External Circuit for Second OVP

Overload / Open-Loop Protection (OLP)

When output is overloaded, the drain current reaches its pulse-by-pulse current limit level, limiting the input power. Then, the output voltage drops and no current flows through the opto-diode, which causes the feedback voltage to increase above the OLP protection threshold (4.6V). This behavior is similar to when the feedback loop is open and no current flows through the opto-diode.

When the feedback voltage is higher than 4.6V longer than the OLP delay time, the OLP protection is triggered, as shown in Figure 17.

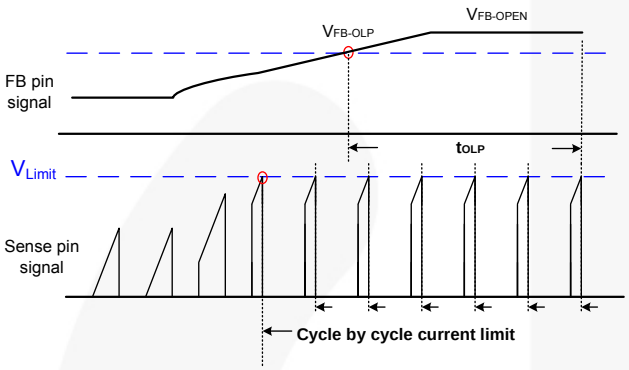

Figure 17. OLP Behavior

V_{DD} Over-Voltage Protection (V_{DD_OVP})

V_{DD} over-voltage protection protects the VDD pin from damage by over-voltage. The V_{DD} voltage rises when an open-feedback loop failure occurs. Once the V_{DD} voltage exceeds 26V (V_{DD-OVP}) for longer than 125µs, the FAN6755 stops switching until V_{DD} is discharged below V_{DD-LH}.

Over-Temperature Protection (OTP)

The FAN6755 has a built-in temperature sensing circuit to disable PWM output if the junction temperature exceeds 135°C. While PWM output is disabled, the V_{DD} voltage gradually drops to the UVLO voltage (around 7.8V). Then V_{DD} is charged up to the startup threshold voltage of 16V through the startup resistor until PWM output is restarted. This "hiccup" mode protection continues as long as the temperature remains above 135°C The temperature hysteresis window for the OTP circuit is 25°C.

Printed Circuit Board (PCB) Layout

High-frequency switching current / voltage makes PCB layout a very important design consideration. Good PCB layout minimizes excessive EMI and helps the power supply survive during surge / ESD tests.

Guidelines:

To improve EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C1 first, then to the switching circuits.

The high-frequency current loop shown in Figure 18 is **C1 – Transformer – MOSFET – R_S**. The area enclosed by this current loop should be as small as possible. Keep the traces (especially 4→1) short, and wide. High-voltage traces related to the drain of the MOSFET and RCD snubber should be kept way from control circuits to prevent unnecessary interference. If a heatsink is used for the MOSFET, connect this heatsink to ground.

As indicated by 3, the ground for the control circuits should be connected together, then to the current-loop ground 2 at a single point close to the ground connection of capacitor C3.

As indicated by 2, the area enclosed by **transformer auxiliary winding, D1, C2, D2, and C3** should also be kept small. Place C3 close to the FAN6755 for good decoupling. For high-level surge, this auxiliary ground must be connected to the bulk capacitor directly. This method can improve the surge capability of the system.

Two suggestions with different pro and cons for ground connections are offered:

GND3→2→4→1: This may avoid common impedance interference for sense signals.

GND3→2→1→4: This can be better for EMI testing where the earth ground is not available on the power supply. Regarding the EMI discharge path, the charges go from secondary through the transformer stray capacitance to GND2 first. The charges then go from GND2 to GND1 and back to the mains. Control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high-frequency impedance and increase EMI immunity.

Should a Y-cap between primary and secondary be required, connect this Y-cap to the **positive terminal of C1**. If this Y-cap is connected to the primary GND, it should be connected to the **negative terminal of C1 (GND1)** directly. Point discharge of this Y-cap also helps for EMI; however, the creepage between these two pointed ends should be large enough to satisfy the requirements of applicable standards.

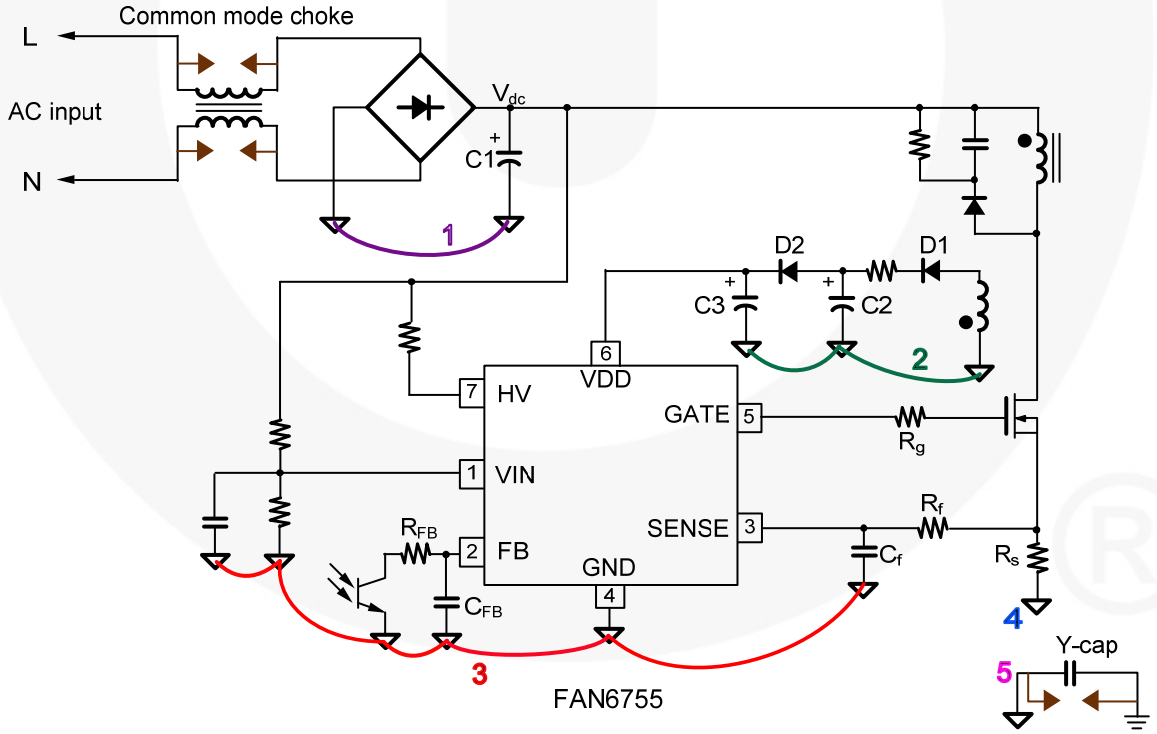

Figure 18.Layout Considerations

Related Resources

FAN6755 — Highly Integrated Green-Mode PWM Controller