Ordering Information

EM 42 AM 16 8 4 R T A – 75 L

EOREX MEMORY

EDO/FPM : 40
D-RAMBUS : 41
DDRSDRAM : 42
DDRSGRAM : 43
SGRAM : 46
SDRAM : 48

Density

32M : 32 Mega Bits **4M** : 4 Mega Bits
16M : 16 Mega Bits **2M** : 2 Mega Bits
8M : 8 Mega Bits **1M** : 1 Mega Bit

Organization

4 : x4 **16** : x16
8 : x8 **18** : x18
9 : x9 **32** : x32

Refresh

1 : 1K **8** : 8K
2 : 2K **6** :16K
4 : 4K

Bank

2 : 2Bank **6** : 16Bank
4 : 4Bank **3** : 32Bank
8 : 8Bank

Interface

V : 3.3V
R : 2.5V

Package

C : CSP **B** : uBGA
T : TSOP **Q** : TQFP
P : PQFP (QFP)
L : LQFP

Revision

A : 1st **B** : 2nd
C : 3rd **D** : 4th
G : for VGA version only

Min Cycle Time (Max Freq.)

-5 : 5ns (200MHz)
-6 : 6ns (167MHz)
-7 : 7ns (143MHz)
-75 : 7.5ns (133MHz)
-8 : 8ns (125MHz)
-10 : 10ns (100MHz)

Power

S : Standard
L : Low power

Package

F : Pb-free
G: Green

256Mb(4Banks) Double Data Rate SDRAM

EM42AM1684RTA (16Mx16)

Description

The EM42AM1684RTA is a high speed synchronous graphic RAM fabricated with ultra high performance CMOS process containing 268,435,456 bits which organized as 4 Banks, each banks has 8,192 rows x 512 columns x 16 bits. The 256Mb DDR SDRAM uses a double data rate architecture to accomplish high-speed operation. The data path internally prefetches multiple bits and it transfers the data for both rising and falling edges of the system clock. It means the doubled data bandwidth can be achieved at the I /O pins.

Features

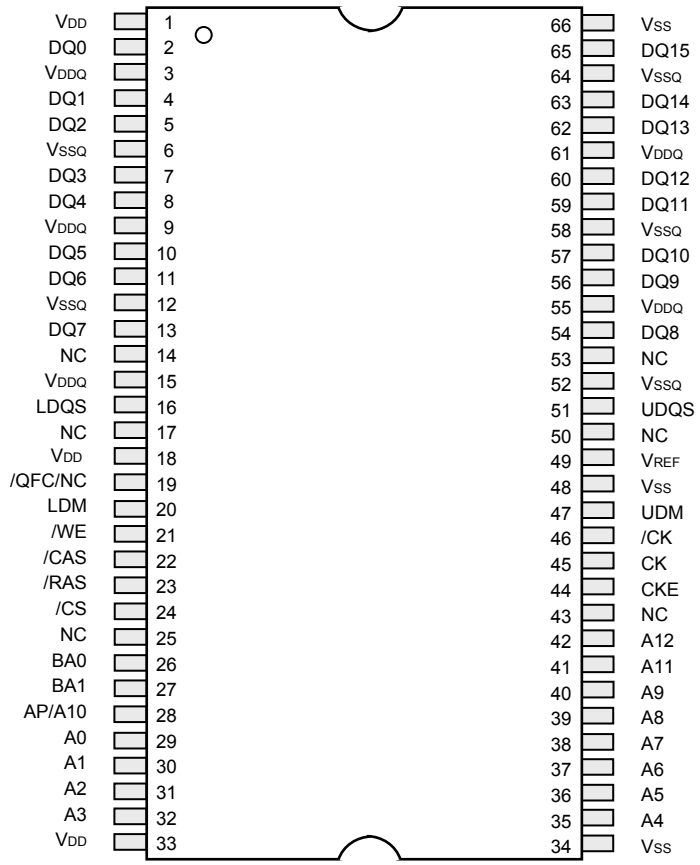
- Internal Double-data-rate architecture with 2 accesses per clock cycle
- 4 banks operation
- Bi-directional, intermittent data strobe (DQS)
- All inputs except data and DM are sampled at the positive edge of the system clock.
- Data Mask (DM) for write data
- Auto & self refresh supported
- 8K Refresh cycle / 64ms
- Burst length of 2,4,8
- Sequential & Interleaved Burst type available
- 2,2.5, 3 Clock read latency
- Auto Precharge option for each burst accesses
- DQS edge-aligned with data for Read cycles
- DQS center-aligned with data for Write cycles
- DLL aligns DQ & DQS transitions with CLK transition
- 2.5V+/- 0.2V VDD
- 2.5V SSTL-2 compatible I/O

Ordering Information

Part Number	Max. Frequency	I/O Interface	Package
EM42AM1684RTA-5	200 MHz	SSTL-2	66 pins, TSOPII
EM42AM1684RTA-6	166 MHz	SSTL-2	66 pins, TSOPII
EM42AM1684RTA-75	133 MHz	SSTL-2	66 pins, TSOPII

** EOREX reserves the right to change products or specification without notice.*

Pin Assignment (Top View)

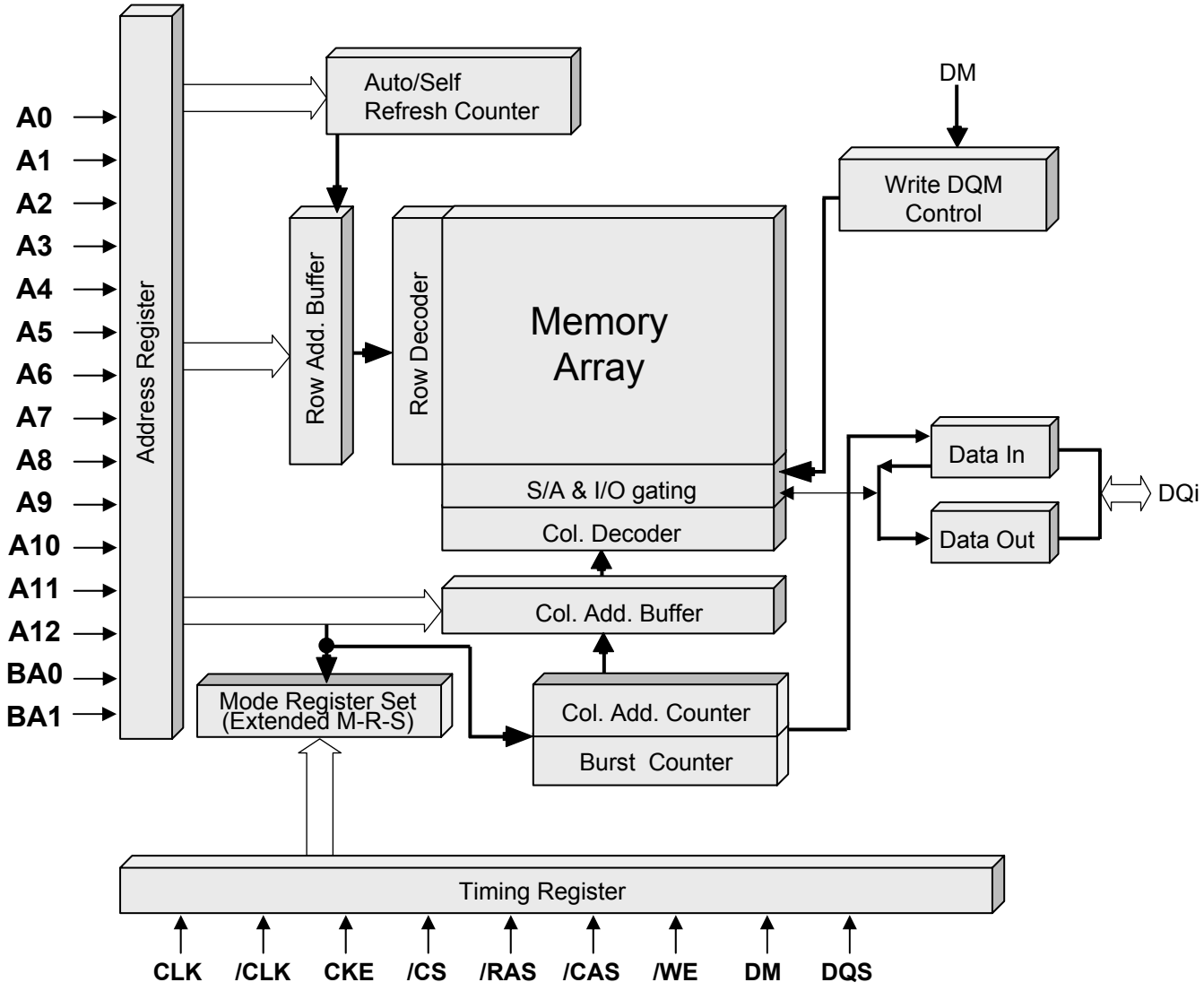


66pin TSOP-II
(400mil x 875 mil)
(0.65mm Pin pitch)

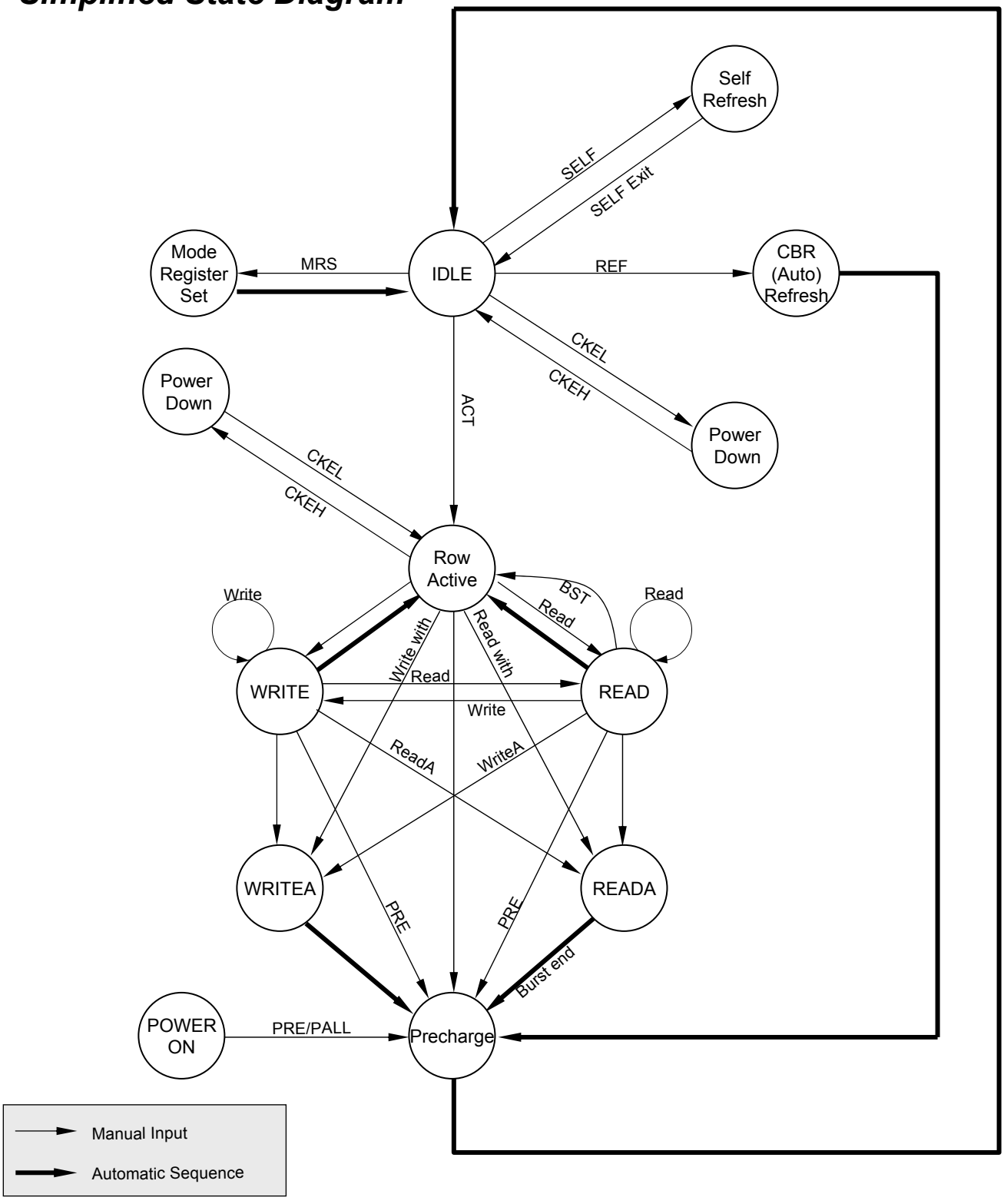
Pin Descriptions (Simplified)

Pin	Name	Pin Function
CLK, /CLK	System Clock	Clock input active on the Positive rising edge except for DQ and DM are active on both edge of the DQS. Clock and /Clock are differential clock inputs.
/CS	Chip select	/CS enables the command decoder when “L” and disabled the command decoder when “H”. The new commands are over-looked when the command decoder is disabled but previous operation will still continue.
CKE	Clock Enable	Activates the CLK when “H” and deactivates when “L”. when deactivate the clock, CKE low signifies the power down or self refresh mode.
A0 ~ A12	Address	Row address (A0 to A12) and Column address (CA0 to CA8) are multiplexed on the same pins. CA10 defines auto precharge at Column address .
BA0, BA1	Bank Address	Selects which bank is to be active.
/RAS	Row address strobe	Latches Row Addresses on the positive rising edge of the CLK with /RAS “L”. Enables row access & pre-charge.
/CAS	Column address strobe	Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access.
/WE	Write Enable	Latches Column Addresses on the positive rising edge of the CLK with /CAS low. Enables column access.
LDQS,UDQS	Data input/output	Data Inputs and Outputs are synchronized with both edge of DQS.
LDM,UDM	Data input/output Mask	DM controls data inputs. LDM corresponds to the data on DQ0-DQ7. UDM corresponds to the data on DQ8-DQ15
/QFC	Data output	FET Control : EMRS Option output during every Read and Write access. It can be used to control isolation switches on modules.
DQ0 ~ 15	Data input/output	Data inputs and outputs are multiplexed on the same pin.
V_{DD}/V_{SS}	Power supply/Ground	V_{DD} and V_{SS} are power supply pins for internal circuits.
V_{DDQ}/V_{SSQ}	Power supply/Ground	V_{DDQ} and V_{SSQ} are power supply pins for the output buffers.
NC/ RFU	No connection / Reserved for Future Use	This pin is recommended to be left No Connection on the device.
V_{REF}	Input	SSTL-2 Reference voltage for input buffer.

Block Diagram



Simplified State Diagram



Absolute Maximum Ratings

Symbol	Item	Rating	Units
V_{IN}, V_{OUT}	Input, Output Voltage	-0.3 ~ 3.6	V
V_{DD}, V_{DDQ}	Power Supply Voltage	-0.3 ~ 3.6	V
T_{OP}	Operating Temperature	0 ~ 70	°C
T_{STG}	Storage Temperature	-55 ~ 150	°C
P_D	Power Dissipation	1	W
I_{OS}	Short Circuit Current	50	mA

Note : Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended DC Operation Conditions (Ta = 0 ~ 70 °C)

Symbol	Parameter	Min.	Typical	Max.	Units
V_{DD}	Power Supply Voltage	2.3	2.5	2.7	V
V_{DDQ}	Power Supply Voltage (for I/O Buffer)	2.3	2.5	2.7	V
V_{REF}	I/O Logic high voltage	1.15	1.25	1.35	V
V_{TT}	I/O Termination voltage	V_{REF}-0.04	-	V_{REF}+0.04	V
V_{IH}	Input Logic high voltage	V_{REF}+0.18	-	V_{DDQ}+0.3	V
V_{IL}	Input Logic low voltage	-0.3	-	V_{REF}-0.18	V

Capacitance (Vcc =2.5V, f = 1MHz, Ta = 25 °C)

Symbol	Parameter	Min.	Max.	Units
C_{CLK}	Clock capacitance (CLK, /CLK)	2.5	4.0	pF
C_I	Input capacitance for CKE, Address, /CS, /RAS, /CAS, /WE	2.5	4.5	pF
C_O	DM , Data & DQS Input/Output capacitance	4.0	6.5	pF

Recommended DC Operating Conditions

(Ta = 0 ~ 70 °C)

Parameter	Symbol	Test condition		Speed			Units	Notes
				-5	-6	-75		
Operating current	I_{DD1}	Burst length = 2, $t_{RC} \geq t_{RC}$ (min), IOL = 0 mA, One bank active		110	95	85	mA	1
Precharge standby current in power down mode	I_{DD2P}	CKE ≤ V_{IL} (max.), t_{CK} = min		4.5			mA	
Precharge standby current in non-power down mode	I_{DD2N}	CKE ≥ V_{IH} (min.), t_{CK} = min, /CS ≥ V_{IH} (min.) Input signals are changed one time during 2clks		40			mA	
Active standby current in power down mode	I_{DD3P}	CKE ≤ V_{IL}(max.), t_{CK} = min		15			mA	
Active standby current in non-power down mode	I_{DD3N}	CKE ≥ V_{IH}(min), t_{CK} = min, / CS ≥ V_{IH}(min) Input signals are changed one time during 2clks		45			mA	
Operating current (Burst mode)	I_{DD4}	$t_{CK} \geq t_{CK}$(min.), I_{OL} = 0 mA All banks active	READ	100			mA	1
			WRITE	110				
Refresh current	I_{DD5}	$t_{RC} \geq t_{RFC}$(min.), All banks active		160			mA	2
Self Refresh current	I_{DD6}	CKE ≤ 0.2V		2			mA	

Note : 1. IDD1 and IDD4 depends on output loading and cycle rates.
Specified values are obtained with the output open.
2. Min. of t_{RFC} (Auto Refresh Row Cycle Times) is shown at AC Characteristics.

Recommended DC Operating Conditions (Continued)

Parameter	Symbol	Min.	Max.	Unit	Note
Input leakage current	I_{LI}	-5	5	uA	1
Output leakage current	I_{LO}	-5	5	uA	2
High level output voltage	V_{OH}	V_{TT} + 0.76	-	V	I_{OH}=-15.2mA
Low level output voltage	V_{OL}	-	V_{TT} - 0.76	V	I_{OH}=-15.2mA

Note : 1. V_{IN}= 0 to 3.6V All other pins are not tested under V_{IN}= 0V.
2. DOUT is disabled, V_{IN}= 0 to 2.7V.

Operating AC Characteristics

(V_{DD} = 2.5V +/- 0.2 V, Ta = 0 ~ 70 °C)

Parameter	Symbol		-5		-6		-75		Units
			Min.	Max.	Min.	Max.	Min.	Max.	
DQ output access from CLK, /CLK	t_{DQCK}		-0. 5	+0. 5	-0.7	+0.7	-0.75	+0.75	ns
DQS output access from CLK, /CLK	t_{DQSCK}		-0. 5	+0. 5	-0.6	+0.6	-0.75	+0.75	ns
CK low / high level width	t_{CL},t_{CH}		0.45	0.55	0.45	0.55	0.45	0.55	tCK
Clock cycle time	t_{CK}	CL=2	7.5	12	6	12	7.5	12	ns
		CL=2.5	6	12	6	12	7.5	12	ns
DQ and DM hold / setup time	t_{DH},t_{DS}		0.4		0.45		0.5		ns
DQ and DM input pulse width for each input	t_{DIPW}		1.75		1.75		1.75		ns
Data out high / low impedance time from CLK, /CLK	t_{HZ}, t_{LZ}		-0.7	+0.7	-0.7	+0.7	-0.75	+0.75	ns
DQS-DQ skew for associated DQ signal	t_{DQSQ}		0.4		0.45		0.5		ns
Write command to first latching DQS transition	t_{DQSS}		0.7	1.25	0.75	1.25	0.75	1.25	tCK
DQS input valid window	t_{DSL}, t_{DSH}		0.35		0.35		0.35		tCK
Mode Register Set command cycle time	t_{MRD}		2		2		2		tCK
Write Preamble setup time	t_{WPRES}		0		0		0		ns
Write Postamble	t_{WPST}		0.4	0.6	0.4	0.6	0.4	0.6	tCK
Address /control input hold / setup time	t_{IH},t_{IS}		0.7		0.8		1.0		ns
Read Preamble	t_{RPRE}		0.9	1.1	0.9	1.1	0.9	1.1	tCK
Read Postamble	t_{RPST}		0.4	0.6	0.4	0.6	0.4	0.6	tCK
Active to Precharge command period	t_{RAS}		40	70K	42	70K	45	70K	ns
Active to Active command period	t_{RC}		55		60		65		ns
Auto Refresh Row Cycle Time	t_{RFC}		70		72		75		ns
Active to Read or write delay	t_{RCD}		15		18		20		ns
Precharge command period	t_{RP}		15		18		20		ns
Active bank A to B command period	t_{RRD}		10		12		15		ns
Column address to column address delay	t_{CCD}		1		1		1		tCK

Operating AC Characteristics (Continued)

(V_{DD} = 2.5V +/- 0.2 V, Ta = 0 ~ 70 °C)

Parameter	Symbol	-75		-8		-10		Units
		Min.	Max.	Min.	Max.	Min.	Max.	
Last data in to Read command	t_{CDLR}	2.5t_{CK}-t_{DQSS}		2.5t_{CK}-t_{DQSS}		2.5t_{CK}-t_{DQSS}		t_{CK}
Last data in to Write command	t_{CDLW}	0		0		0		t_{CK}
Last data in to Precharge Command	t_{DPL}	2		2		2		t_{CK}
Exit self Refresh to non-read command	t_{XSNR}	75		75		75		ns
Exit self Refresh to read command	t_{XSRD}	200		200		200		ns
Average periodic refresh interval	t_{REFI}		15.6		15.6		15.6	us
/QFC preamble during reads	t_{QPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
/QFC postamble during reads	t_{QPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
/QFC output access time from CK/ /CK	t_{QCK}	0		0		0		ns
/QFC output hold time	t_{QOH}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}

Truth Table

1. Command Truth Table

Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	BA0, BA1	A10	A12 ~A0
		n-1	n							
Ignore Command	DESL	H	X	H	X	X	X	X	X	X
No operation	NOP	H	X	L	H	H	H	X	X	X
Burst stop	BSTH	H	X	L	H	H	L	X	X	X
Read	READ	H	X	L	H	L	H	V	L	V
Read with auto pre-charge	READA	H	X	L	H	L	H	V	H	V
Write	WRIT	H	X	L	H	L	L	V	L	V
Write with auto pre-charge	WRITA	H	X	L	H	L	L	V	H	V
Bank activate	ACT	H	X	L	L	H	H	V	V	V
Pre-charge select bank	PRE	H	X	L	L	H	L	V	L	X
Pre-charge all banks	PALL	H	X	L	L	H	L	X	H	X
Mode register set	MRS	H	X	L	L	L	L	L	L	V

Note : H = High level, L = Low level, X = High or Low level (Don't care), V = Valid data input

2. CKE Truth Table

Command	Command	Symbol	CKE		/CS	/RAS	/CAS	/WE	Addr.
			n-1	n					
Idle	CBR refresh command	REF	H	H	L	L	L	H	X
Idle	Self refresh entry	SELF	H	L	L	L	L	H	X
Self refresh	Self refresh exit		L	H	L	H	H	H	X
			L	H	H	X	X	X	X
Idle	Power down entry		H	L	X	X	X	X	X
Power down	Power down exit		L	H	X	X	X	X	X

Remark H = High level, L = Low level, X = High or Low level (Don't care)

3. Operative Command Table

Current state	/CS	/R	/C	/W	Addr.	Command	Action	Notes
Idle	H	X	X	X	X	DESEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	TERM	NOP	
	L	H	L	X	BA/CA/A10	READ/WRIT/BW	ILLEGAL	1
	L	L	H	H	BA/RA	ACT	Bank active , Latch RA	
	L	L	H	L	BA/A10	PRE/PREA	NOP	3
	L	L	L	H	X	REFA	Auto refresh	4
	L	L	L	L	Op-Code, Mode-Add	MRS	Mode register	
Row active	H	X	X	X	X	DESEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	TERM	NOP	
	L	H	L	H	BA/CA/A10	READ/READA	Begin Read, Latch CA, Determine auto-precharge	
	L	H	L	L	BA/CA/A10	WRITE/WRITEA	Begin Write, Latch CA, Determine auto-precharge	
	L	L	H	H	BA/RA	ACT	ILLEGAL	1
	L	L	H	L	BA/A10	PRE/PREA	Precharge / Precharge all	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
Read	H	X	X	X	X	DESEL	NOP (Continue burst to end)	
	L	H	H	H	X	NOP	NOP (Continue burst to end)	
	L	H	H	L	X	TERM	Terminal burst	
	L	H	L	H	BA/CA/A10	READ/READA	Terminal burst. Latch CA,Begin new read, Determine Auto-precharge	
	L	H	L	L				
	L	L	H	H	BA/RA	ACT	ILLEGAL	1
	L	L	H	L	BA/A10	PRE/PREA	Terminate burst, Precharge	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

Remark: H =High Level, L=Low level, X=High or Low level (Don't care), AP= Auto Precharge

Current state	/CS	/R	/C	/W	Addr.	Command	Action	Notes
Write	H	X	X	X	X	DESEL	NOP (Continue burst to end)	
	L	H	H	H	X	NOP	NOP (Continue burst to end)	
	L	H	H	L	X	TERM	ILLEGAL	
	L	H	L	H	BA/CA/A10	READ/READA	Terminate burst with DM="H", Latch CA , Begin read,Determine auto-precharge	2
	L	H	L	L	BA/CA/A10	WRITE/WRITEA	Terminate burst , Latch CA ,Begin new write, Determine auto-precharge	2
	L	L	H	H	BA/RA	ACT	ILLEGAL	1
	L	L	H	L	BA/A10	PRE/PREA	Terminate burst with DM="H", Precharge	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
Read with Auto-precharge	H	X	X	X	X	DESEL	NOP (Continue burst to end)	
	L	H	H	H	X	NOP	NOP (Continue burst to end)	
	L	H	H	L	BA/CA/A10	TERM	ILLEGAL	
	L	H	L	X	BA/RA	READ/WRITE	ILLEGAL	1
	L	L	H	H	BA/A10	ACT	ILLEGAL	1
	L	L	H	L	X	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
Write with Auto-precharge	H	X	X	X	X	DESEL	NOP (Continue burst to end)	
	L	H	H	H	X	NOP	NOP (Continue burst to end)	
	L	H	H	L	X	TERM	ILLEGAL	
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL	1
	L	L	H	H	BA/RA	ACT	ILLEGAL	1
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

Remark: H =High Level, L=Low level, X=High or Low level (Don't care), AP= Auto Precharge

Current state	/CS	/R	/C	/W	Addr.	Command	Action	Notes
Write recovering	H	X	X	X	X	DESEL	NOP	
	L	H	H	H	X	NOP	NOP	
	L	H	H	L	X	TERM	NOP	
	L	H	L	H	BA/CA/A10	READ	ILLEGAL	1
	L	H	L	L	BA/CA/A10	WRITE/WRITEA	New write, Determine AP	
	L	L	H	H	BA/RA	ACT	ILLEGAL	1
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
Refreshing	H	X	X	X	X	DESEL	NOP (Idle after t_{RP})	
	L	H	H	H	X	NOP	NOP (Idle after t_{RP})	
	L	H	H	L	X	TERM	NOP	
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL	
	L	L	H	H	BA/RA	ACT	ILLEGAL	
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL	
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
Precharging	H	X	X	X	X	DESEL	NOP (Idle after t_{RP})	
	L	H	H	H	X	NOP	NOP (Idle after t_{RP})	
	L	H	H	L	X	TERM	NOP	
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL	1
	L	L	H	H	BA/RA	ACT	ILLEGAL	1
	L	L	H	L	BA/A10	PRE/PREA	NOP(Idle after t_{RP})	3
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	
Row activating	H	X	X	X	X	DESEL	NOP (Row active after t_{RCD})	
	L	H	H	H	X	NOP	NOP (Row active after t_{RCD})	
	L	H	H	L	X	TERM	NOP	
	L	H	L	X	BA/CA/A10	READ/WRITE	ILLEGAL	1
	L	L	H	H	BA/RA	ACT	ILLEGAL	1
	L	L	H	L	BA/A10	PRE/PREA	ILLEGAL	1
	L	L	L	H	X	REFA	ILLEGAL	
	L	L	L	L	Op-Code, Mode-Add	MRS	ILLEGAL	

Remark: H =High Level, L=Low level, X=High or Low level (Don't care), AP= Auto Precharge

Note 1. ILLEGAL to bank in specified state:
→ Function may be legal in the Bank indicated by Bans Address (BA), depending on the state of the bank.
2. Must satisfy bus contention, bus turn around, and/or write recovery requirements.
3. NOP to bank precharging or in idle sate. May precharge bank indicated by BA.
4. ILLEGAL of any bank is not idle.

4. Command Truth Table for CKE

Current state	CKE		/CS	/R	/C	/W	Addr.	Action	Notes
	n-1	n							
Self refreshing	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exist Self-Refresh	1
	L	H	L	H	H	H	X	Exist Self-Refresh	1
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Self-refresh)	
Both bank precharge power down	H	X	X	X	X	X	X	INVALID	
	L	H	H	X	X	X	X	Exist Power down	2
	L	H	L	H	H	H	X	Exist Power down	2
	L	H	L	H	H	L	X	ILLEGAL	
	L	H	L	H	L	X	X	ILLEGAL	
	L	H	L	L	X	X	X	ILLEGAL	
	L	L	X	X	X	X	X	NOP (Maintain Power down)	
All Banks Idle	H	H	X	X	X	X	X	Refer to function true table	
	H	L	H	X	X	X	X	Enter power down	3
	H	L	L	H	H	H	X	Enter power down	3
	H	L	L	H	H	L	X	ILLEGAL	
	H	L	L	H	L	X	X	ILLEGAL	
	H	L	L	L	H	H	RA	Row active / Bank active	
	H	L	L	L	L	H	X	Enter self-refresh	3
	H	L	L	L	L	L	OP Code	Mode register access	
	H	L	L	L	L	L	Op-Code	Special mode register access	
	L	X	X	X	X	X	X	Refer to current state	
Any state other than listed above	H	H	X	X	X	X	X	Refer to command truth table	

Remark : H = High level, L = Low level, X = High or Low level (Don't care)

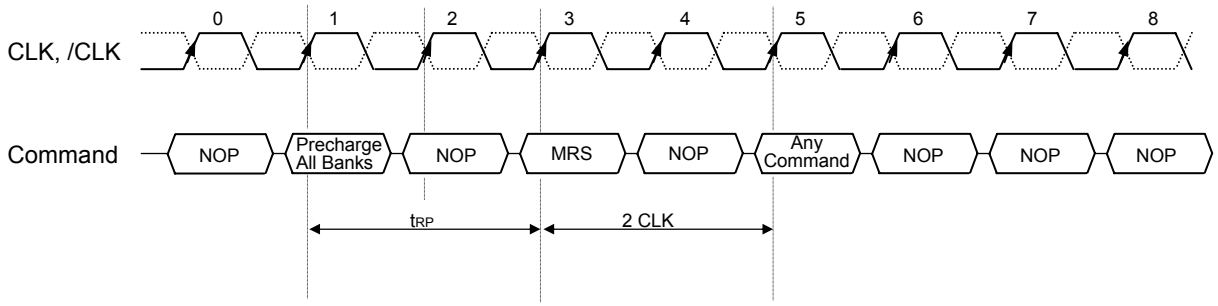
Notes 1. After CKE's low to high transition to exist self refresh mode. And a time of t_{RC} (min) has to be elapse after CKE's low to high transition to issue a new command.
2. CKE low to high transition is asynchronous as if restarts internal clock.
3. Power down and self refresh can be entered only from the idle state of all blanks.

Mode Register Definition

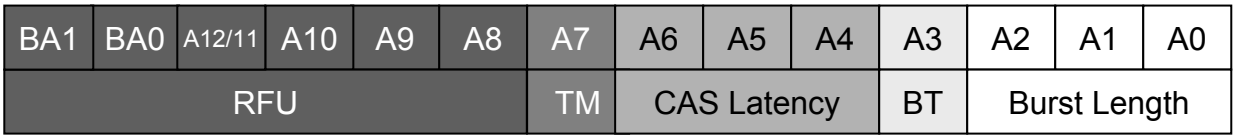
Mode Register Set

The mode register stores the data for controlling the various operating modes of DDR SDRAM which contains addressing mode, burst length, /CAS latency, test mode, DLL reset and various vendor's specific opinions. The defaults values of the register is not defined, so the mode register must be written after EMRS setting for proper DDR SDRAM operation. The mode register is written by asserting low on /CS, /RAS, /CAS, /WE and BA0 (The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the mode register.) The state of the address pins A0-A12 in the same cycle as /CS, /RAS, /CAS, /WE and BA0 going low is written in the mode register. Two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operating as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A0-A2, addressing mode uses A3, /CAS latency (read latency from column address) uses A4-A6. A7 is used for test mode. A8 is used for DDR reset. A7 must be set to low for normal MRS operation.

MRS Cycle



Address Input for Mode Register Set



A8	DLL Reset
0	No
1	Yes

Burst Length				
Sequential	Interleave	A2	A1	A0
Reserved	Reserved	0	0	0
2	2	0	0	1
4	4	0	1	0
8	8	0	1	1
Reserved	Reserved	1	0	0
Reserved	Reserved	1	0	1
Reserved	Reserved	1	1	0
Reserved	Reserved	1	1	1

BA0	An – A0
0	MRS Cycle
1	EMRS

Burst Type	A3
Sequential	0
Interleave	1

CAS Latency	A6	A5	A4
Reserved	0	0	0
Reserved	0	0	1
2	0	1	0
Reserved	0	1	1
Reserved	1	0	0
Reserved	1	0	1
2.5	1	1	0
Reserved	1	1	1

A7	Operation Mode
0	Normal
1	Test

Burst Type (A3)

Burst Length	A2 A1 A0	Sequential Addressing	Interleave Addressing
2	X X 0	0 1	0 1
	X X 1	1 0	1 0
4	X 0 0	0 1 2 3	0 1 2 3
	X 0 1	1 2 3 0	1 0 3 2
	X 1 0	2 3 0 1	2 3 0 1
	X 1 1	3 0 1 2	3 2 1 0
8	0 0 0	0 1 2 3 4 5 6 7	0 1 2 3 4 5 6 7
	0 0 1	1 2 3 4 5 6 7 0	1 0 3 2 5 4 7 6
	0 1 0	2 3 4 5 6 7 0 1	2 3 0 1 6 7 4 5
	0 1 1	3 4 5 6 7 0 1 2	3 2 1 0 7 6 5 4
	1 0 0	4 5 6 7 0 1 2 3	4 5 6 7 0 1 2 3
	1 0 1	5 6 7 0 1 2 3 4	5 4 7 6 1 0 3 2
	1 1 0	6 7 0 1 2 3 4 5	6 7 4 5 2 3 0 1
	1 1 1	7 0 1 2 3 4 5 6	7 6 5 4 3 2 1 0

* Page length is a function of I/O organization and column addressing

DLL Enable / Disable

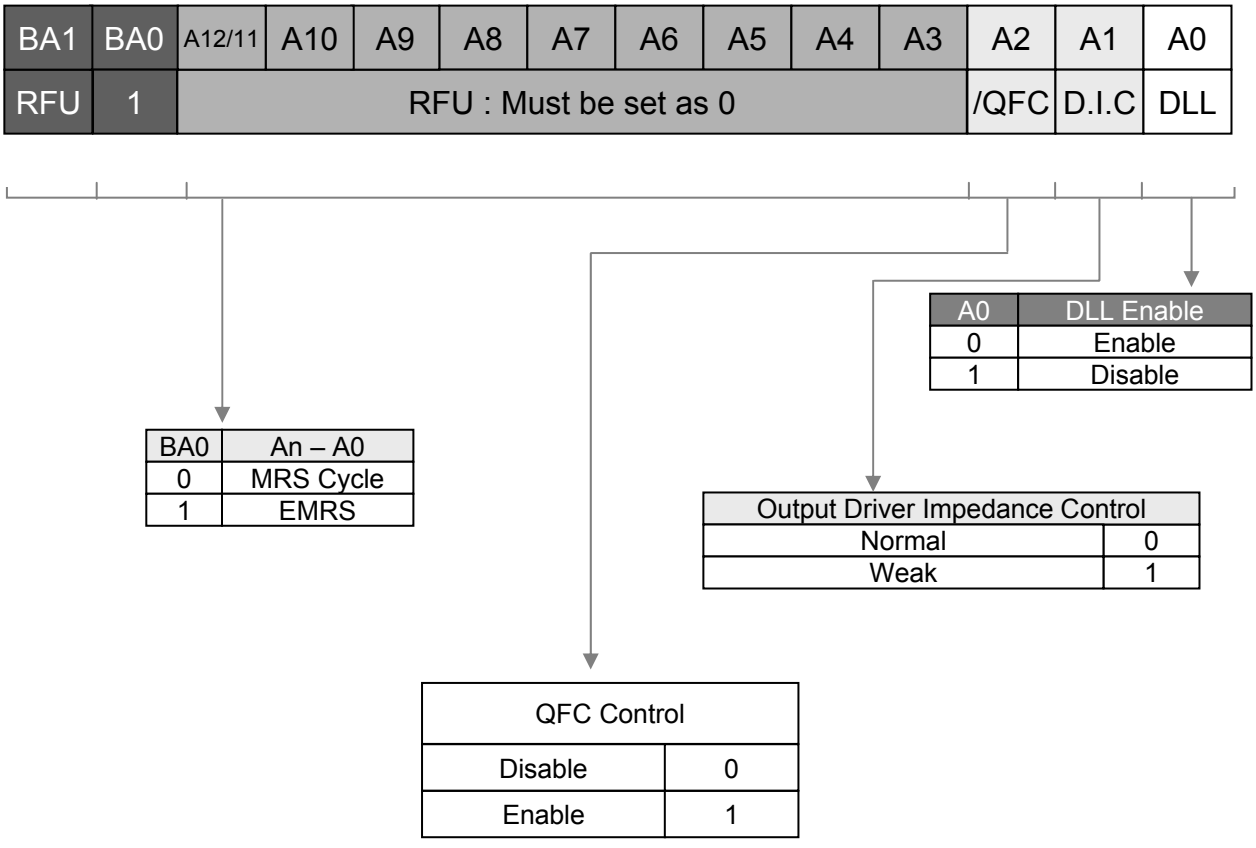
The DLL must be enabled for normal operation. DLL enable is required during power-up initialization and upon returning to normal operation after having disable the DLL for the purpose of debug or evaluation (upon existing Self Refresh Mode, the DLL is enable automatically.) Any time the DLL is enabled, 200 clock cycles must occur before a READ command can be issued.

Output Drive Strength

The normal drive strength got all outputs is specified to be SSTL-2, Class II. Some vendors might also support a weak drive strength option, intended for lighter load and/or point to point environments.

Extended Mode Register Set (EMRS)

The Extended mode register stores the data enabling or disabling DLL. The value of the extended mode register is not defined, so the extended mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on /CS, /RAS, /CAS, /WE and high on BA0 (The DDR SDRAM should be in all bank precharge with CKE already prior to writing into the extended mode register.) The state of address pins A0-A10 and BA1 in the same cycle as /CS, /RAS, /CAS, and /WE going low is written in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. High on BA0 is used for EMRS. All the other address pins except A0 and BA0 must be set to low for proper EMRS operation.



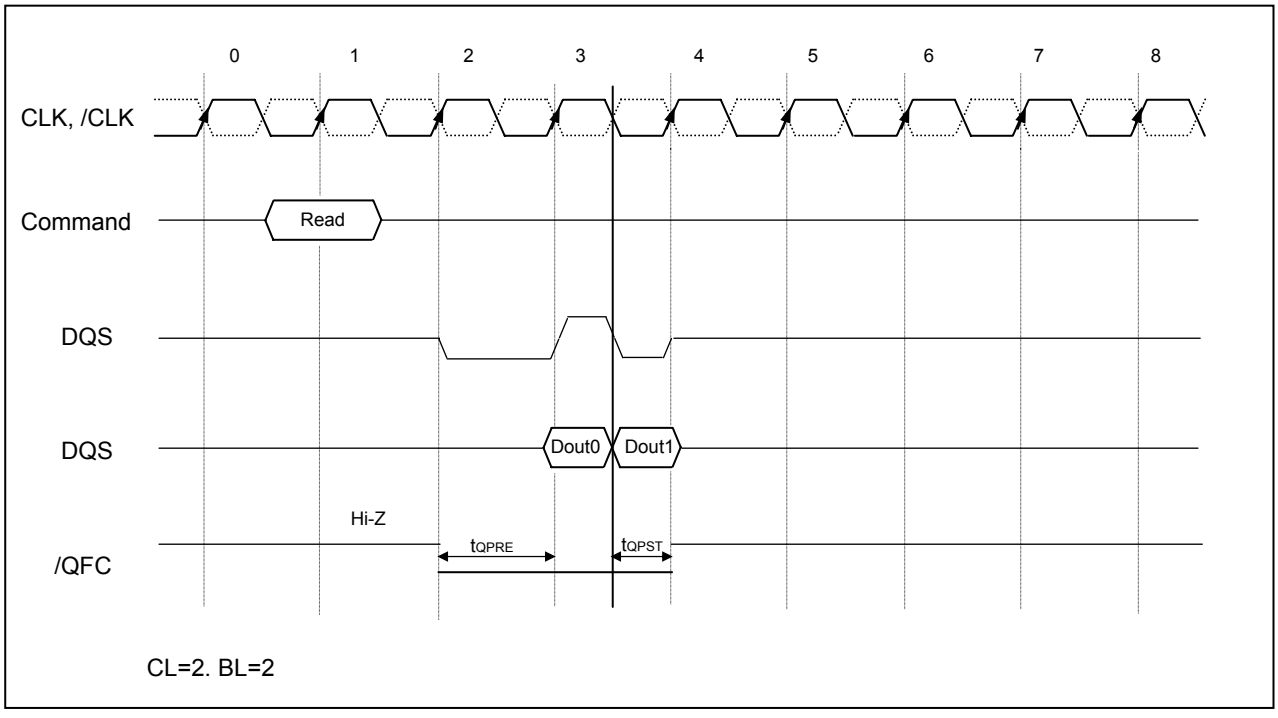
/QFC Function

/QFC Definition

When drive low in reads coincident with the start of DQS, this DRAM output signal says that one cycle later there will be the first valid DQS output and returned on Hi-Z after this finishing a burst operation. It is also driven low shortly after a write command is received and returned to Hi-Z shortly after the last data strobe transition is received. Whenever the device is in standby, the signal is Hi-Z. DQS is intended to enable an external data switch. QFC can be enabled or disabled through EMRS control.

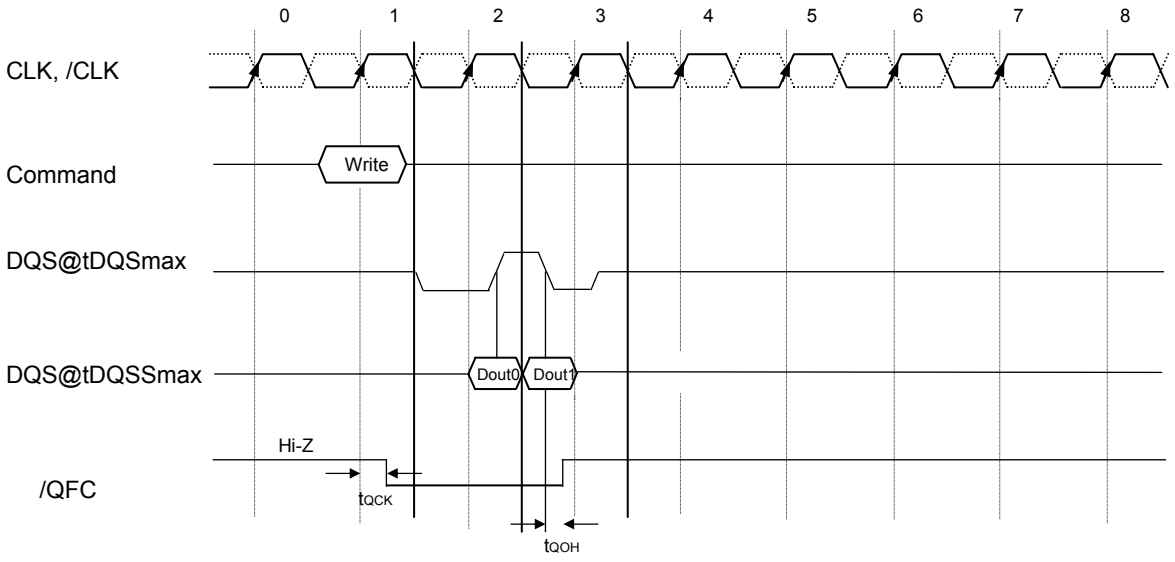
/QFC Timing or Read Operation

QFC on reads is enabled coincident with the start of DQS preamble, and disabled coincident with the end of DQS postamble



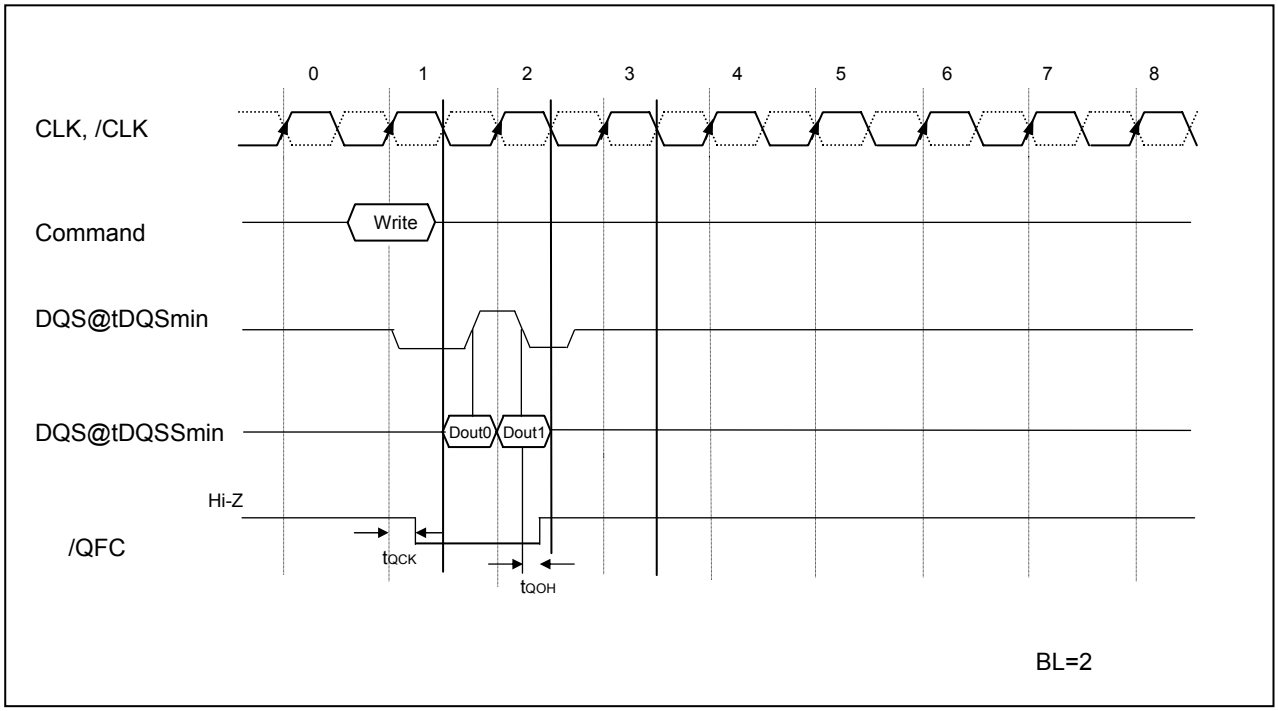
/QFC Timing on Write Operation with tDQSSmax

/QFC on writes is enabled as soon as possible after the clock edge of write command and disabled as soon as possible after the last DQS-in low going edge.

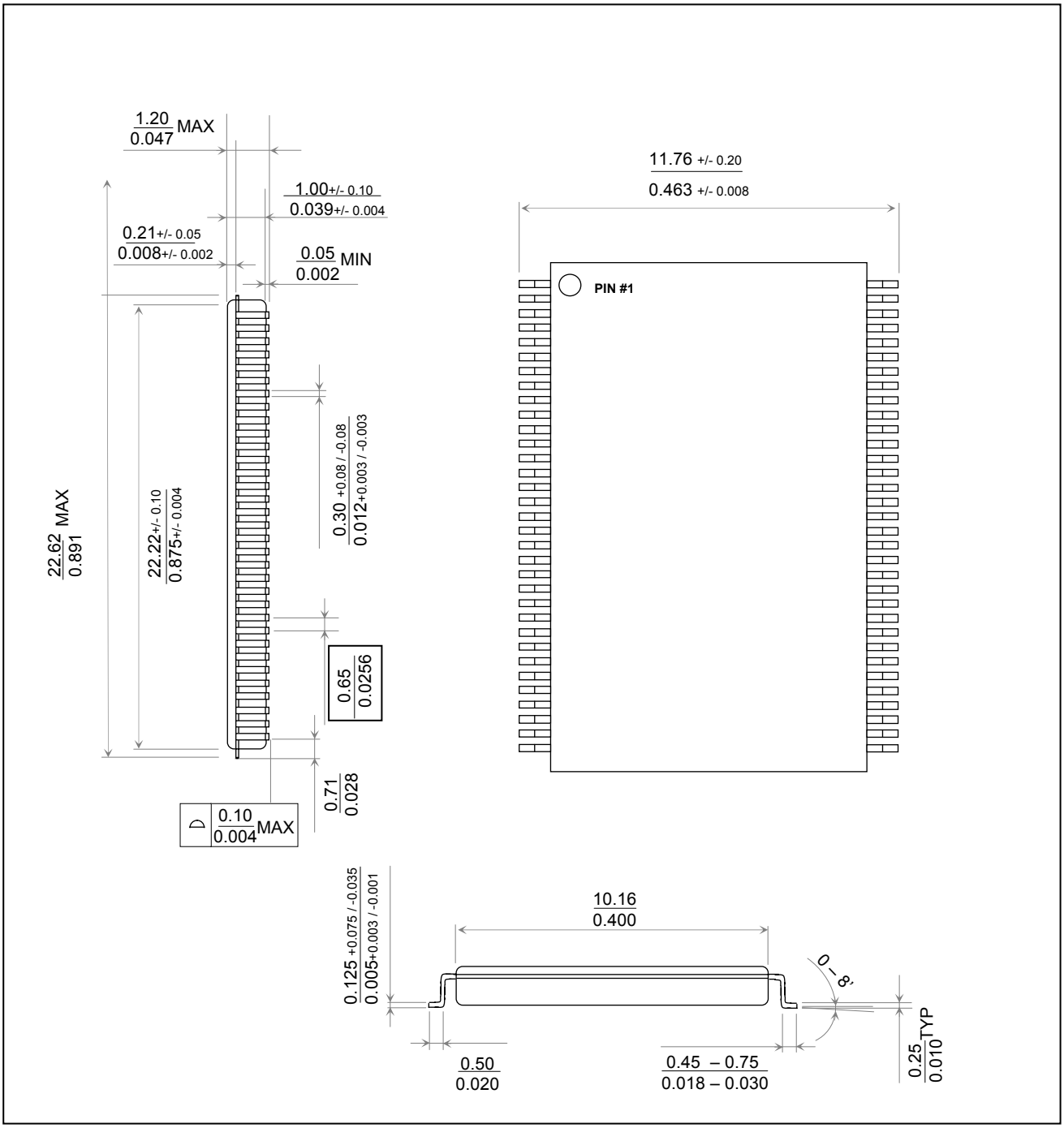


/QFC Timing on Write Operation with tDQSSmin

/QFC on writes is enabled as soon as possible after the clock edge of write command and disabled as soon as possible after the last DQS-in low going edge.



Package Dimension



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