AN-6846

Applying SG6846 to Control a Flyback Power Supply with Surge Current Output

Summary

This application note describes a detailed design strategy for a high-efficiency, compact flyback converter. Design considerations, mathematical equations, and guidelines for printed circuit board layout are presented.

Applications

General-purpose switch-mode power supplies and flyback power converters, including:

- Power Adapters
- Open-frame SMPS
- SMPS with Surge-current Output, such as for Printers, Scanners, Motor Drivers

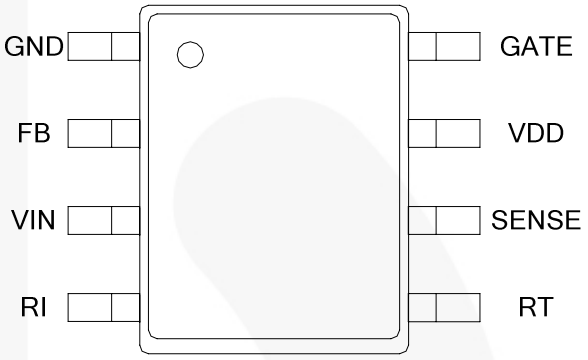

Figure 1. Pin Configuration

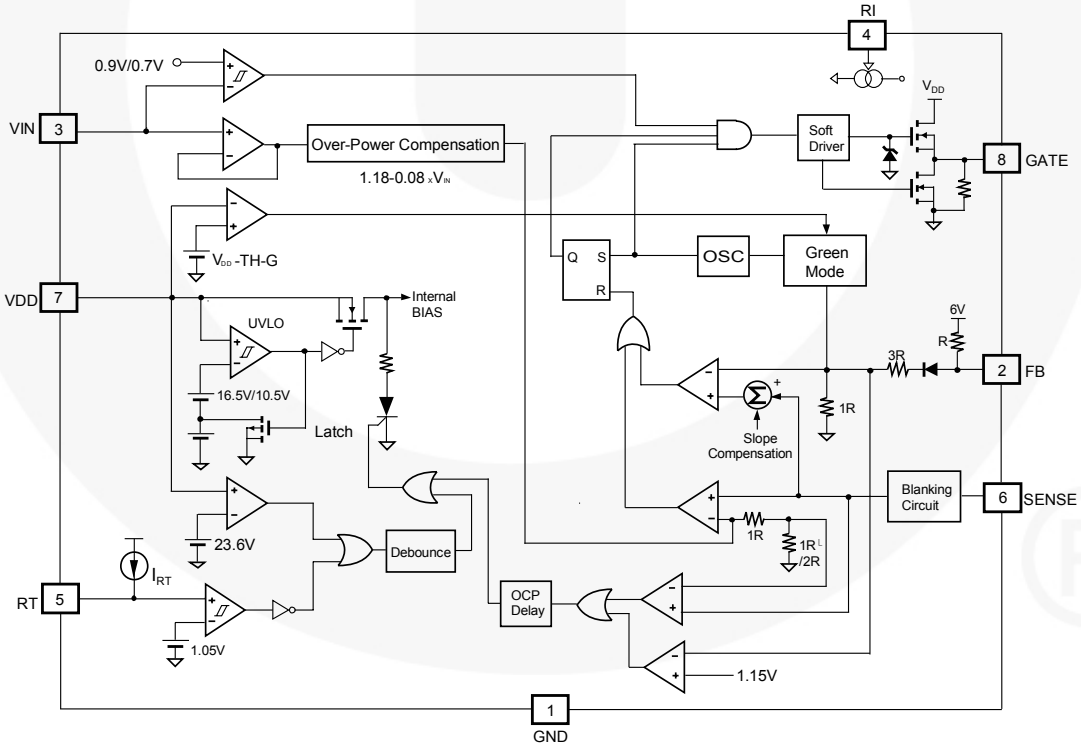

Figure 2. Block Diagram

Table 1. Comparison

Symbol	Parameter	SG6846A	SG6846B	SG6846C SG6846G
Feedback Input Section				
t_{D-OLP}	Delay Time for Open-Loop Protection (R_I = 26kΩ)	1700ms	NA	110ms
Over-Temperature Protection (OTP) Section				
$t_{DOTP-LATCH}$	Over-Temperature Latch-off Debounce (R_I = 26kΩ)	100ms		100μs
Current Sense Section				
t_{D-SCP}	Delay Time for output short circuit protection (R_I = 26kΩ)	100ms	7ms	NA
t_{D-OCP}	Delay Time for Over-Current Protection (R_I = 26kΩ)	1700ms	200ms	110ms
$V_{STH\ (VIN=1V)}$	Threshold Voltage for Current Limit	0.83V		1.1V
$V_{STH\ (VIN=3V)}$	Threshold Voltage for Current Limit	0.7V		0.94V
$V_{STH\ –\ 2/3\ (1/2)}$	Threshold Voltage for Over Current Protection	$V_{STH} \times 2/3$		$V_{STH} \times 1/2$

Symbol	Parameter	SG6846A/B/C	SG6846G
Oscillator Section			
V_{FB-N}	FB Threshold Voltage For Frequency Reduction (R_I = 26kΩ)	2.1	2.8V
V_{FB-G}	FB Voltage at Green-mode Minimum Frequency (R_I = 26kΩ)	1.6	2.3V
V_{FB-ZDC}	FB Threshold Voltage for Zero-duty	V_{FB-G}	2V

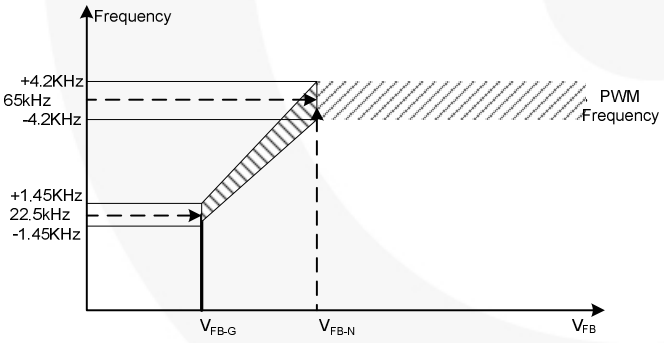

Figure 3. SG6846A/B/C PWM Frequency

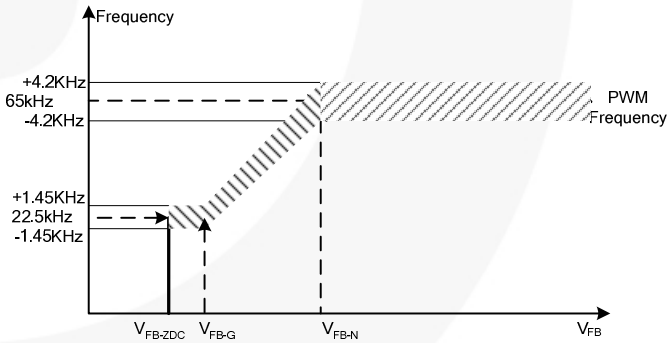

Figure 4. SG6846G PWM Frequency

Description

The SG6846 is a highly integrated PWM controller IC that provides special features satisfying the needs for low standby power consumption. It also incorporates multiple protection functions. With low start-up current and low operating current, high-efficiency power conversion is achieved. The typical start-up current is only 8μA and the operating current is around 3.7mA. In nominal loading conditions, the SG6846 operates at a fixed PWM frequency. To minimize standby power consumption, a proprietary green-mode function provides off-time modulation to continuously decrease the switching frequency under light-load conditions. Under no-load conditions, the power supply enters burst-mode. Green mode dramatically cuts the power loss at no-load and light-load conditions, enabling the power supply to meet stringent power conservation requirements.

The SG6846 is specially designed for SMPS with surge-current output, incorporated with a two-level OCP function. Besides the cycle-by-cycle current limiting; if the switching current is higher than OCP threshold for a delay time, over-current protection is activated such that the SG6846 is totally shutdown. Other protection functions include AC input brownout protection with hysteresis and V_{DD} over-voltage protection. For over-temperature protection, an external NTC thermistor can be applied to sense the ambient temperature. When OCP, V_{DD} OVP, or OTP are activated, an internal latch circuit is used to latch-off the controller. If the latch circuit is triggered by over-temperature conditions, it resets when the temperature cools off sufficiently (SG6846CX) or when the AC supply is disconnected (SG6846LX). When the latch is triggered by V_{DD} over-voltage conditions, the latch resets only when the AC supply is disconnected.

Other features of this controller include built-in synchronized slope compensation and proprietary internal compensation for constant output power limit over universal AC input range. The gate output is clamped at 18V to protect the external MOSFET from over-voltage damage.

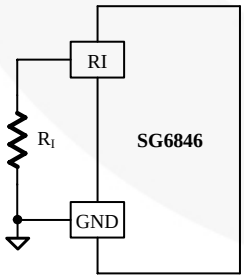

Figure 5. Setting PWM Frequency

Startup Circuitry

When the power is turned on, the input voltage charges the hold-up capacitor C1 via the startup resistors. As shown in Figure 2, one or two resistors from the AC utility are both practical. As the voltage of V_{DD} reaches the startup threshold voltage V_{TH-ON}, the SG6846 activates and drives the entire power supply. The IC then operates based on the auxiliary winding energy.

Using one startup resistor (510KΩ) with a 10μF/50V hold-up capacitor C1 can satisfy the three-second maximum power-on delay requirement in most applications. After startup, the energy is supplied from C2. The capacitance at V_{DD} must be large enough to hold V_{DD} above the off threshold voltage, V_{TH-OFF}, at a step change of load. When an output short circuit occurs, the duration before V_{DD} drops to below the off threshold voltage must be longer than the OCP delay time or it fails to trigger the internal latch circuit. A 100μF/50V capacitor is suggested for C2.

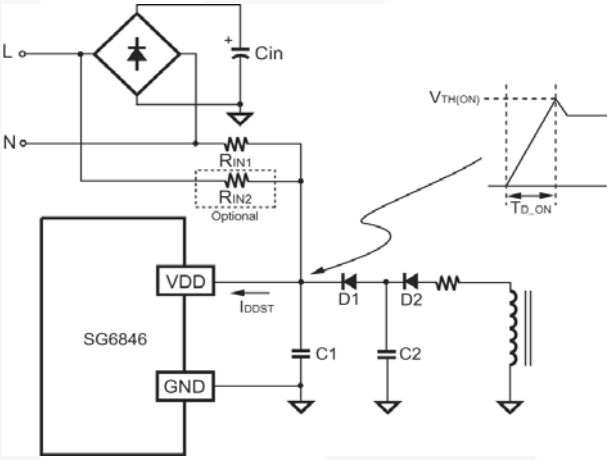

Figure 6. Circuit Providing Power

The maximum power dissipation of R_{IN} is:

$$P_{RIN,\max} \cong \frac{V_{AC,\max}^2}{2 \times R_{IN}} \quad (1)$$

where $V_{AC,max}$ is the maximum rectified input voltage.

Taking a wide-range input ($90V_{AC}$-$264V_{AC}$) as an example, $V_{AC,max}$ =264V:

$$P_{RIN,\max} = \frac{264^2}{2 \times 510 \times 10^3} \cong 68mW \quad (2)$$

In addition to the low startup current, SG6846 consumes less operating current than a traditional UC384x.

Oscillator and Green-Mode Operation

Resistor R_I programs the frequency of the internal oscillator. A 26Ω resistor R_I determines PWM frequency as 65kHz:

$$f_{PWM}(kHz) = \frac{1690}{R_I(k\Omega)} \quad (3)$$

A PWM frequency range of between 47kHz ~ 109kHz is recommended.

The proprietary green mode provides off-time modulation to reduce the PWM frequency at light-load and no-load conditions. The feedback voltage of the FB pin is taken as a reference. As shown in Figure 7, when the feedback voltage is lower than about 2.1V, the PWM frequency decreases. Because most losses in a switching-mode power supply are proportional to the PWM frequency, the off-time modulation reduces the power consumption of the power supply at light-load and no-load conditions. For a typical case of R_I=26KΩ, the PWM frequency is 65kHz at nominal load and decreases to 22.5kHz at light loads, about one third of the nominal PWM frequency. The power supply enters burst mode at zero-load conditions.

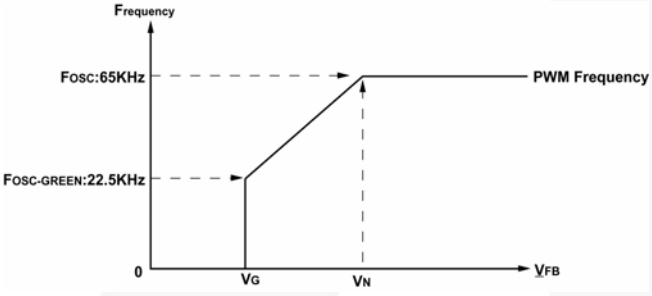

Figure 7. PWM Frequency vs. FB Voltage

FB Input

The SG6846 is designed for peak-current-mode control. A current-to-voltage conversion is accomplished externally with current-sense resistor R_S. Under normal operation, the FB level controls the peak inductor current:

$$I_{pk} = \frac{V_{FB} - 1.2}{4.2 \cdot R_S} \quad (4)$$

where V_{FB} is the voltage of FB pin.

When V_{FB} is less than 1.6V, the SG6846 terminates the output pulses.

0 is a typical feedback circuit mainly consisting of a shunt regulator and an opto-coupler. R1 and R2 form a voltage divider for output voltage regulation. R3 and C1 are adjusted for control-loop compensation. A small-value RC filter (e.g. R_{FB}= 47Ω, C_{FB}= 1nF) placed from the FB pin to GND can increase stability substantially. The maximum source current of the FB pin is about 2mA. The phototransistor must be capable of sinking this current to pull the FB level down at no load. The value of the biasing resistor, R_b, is determined as:

$$\frac{V_o - V_D - V_Z}{R_b} \cdot K \geq 2mA \quad (5)$$

where:
V_D is the drop voltage of photodiode, about 1.2V;
V_Z is the minimum operating voltage, 2.5V of the shunt regulator; and
K is the current transfer rate (CTR) of the opto-coupler.

For an output voltage V_O=5V, with CTR=100%, the maximum value of R_b is 650Ω.

Built-in Slope Compensation

A flyback converter can be operated in discontinuous current mode (DCM) or continuous current mode (CCM). With the same output power, a converter in CCM exhibits smaller peak inductor current than in DCM. Therefore, a small-sized transformer and a low-rating MOSFET can be applied. On the secondary side of the transformer, the rms output current of DCM can be up to twice that of CCM. Larger wire gauge and output capacitors with larger ripple current ratings are required. DCM operation also results in higher output voltage spikes. A large LC filter has to be added. Therefore, a flyback converter in CCM achieves better performance with lower component cost.

Despite the above advantages of CCM operation, there is one concern – stability. In CCM operation, the output power is proportional to the average inductor current, while the peak current is controlled. This causes the well-known sub-harmonic oscillation when the PWM duty cycle exceeds 50%. Adding slope compensation (reducing the current-loop gain) is an effective way to prevent oscillation. The SG6846 introduces a synchronized positive-going ramp (V_{SLOPE}) in every switching cycle to stabilize the current loop. Therefore, the SG6846 enables design of a cost-effective, highly efficient, compact flyback power supply operating in CCM without adding external components.

The positive ramp added is:

$$V_{SLOPE} = V_{SL} \cdot D \quad (6)$$

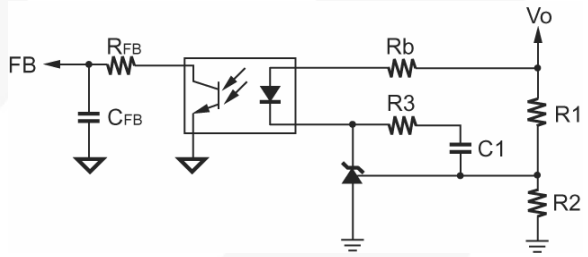

Figure 8. Feedback Circuit

where V_{SL} = 0.33V and D = duty cycle.

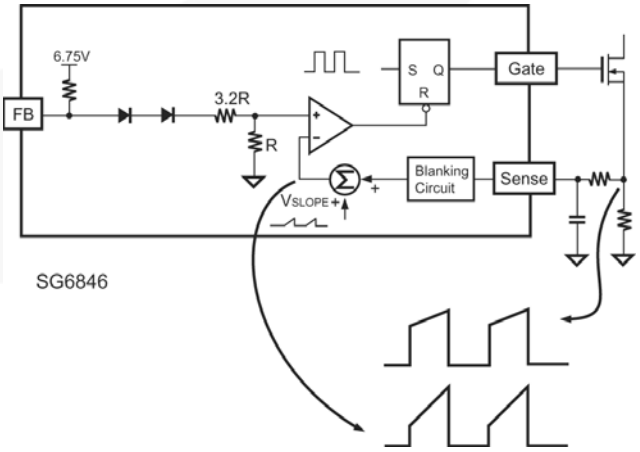

Figure 9. Synchronized Slope Compensation

Leading-Edge Blanking (LEB)

A voltage signal proportional to the MOSFET current develops on the current-sense resistor R_S. Each time the MOSFET is turned on, a spike induced by the diode reverse recovery and by the output capacitances of the MOSFET and diode, appears on the sensed signal. A leading-edge blanking time (about 360ns) is introduced to avoid premature termination of the MOSFET by the spike. Therefore, only a small-value RC filter (e.g. 100Ω + 470pF) is required between the SENSE pin and R_S. A non-inductive resistor for R_S is recommended.

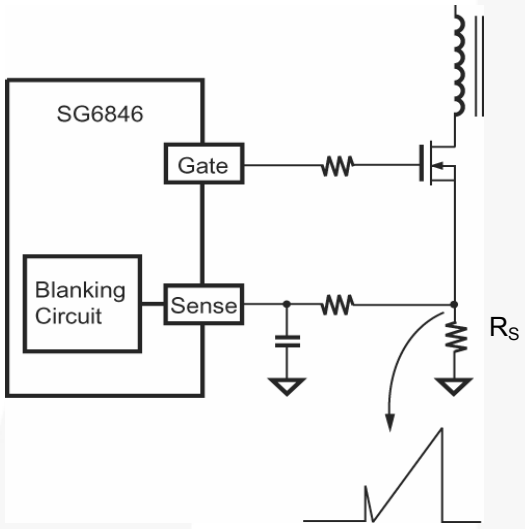

Figure 10.Turn-on Spike

Output Driver / Soft Driving

The output stage is a fast totem-pole gate driver capable of directly driving external MOSFETs. An internal Zener diode clamps the driver voltage under 18V to protect MOSFETs against over voltage. By integrating circuits to control the slew rate of switch-on rising time, the external resistor R_G may not be necessary to reduce switching noise, thereby improving EMI performance.

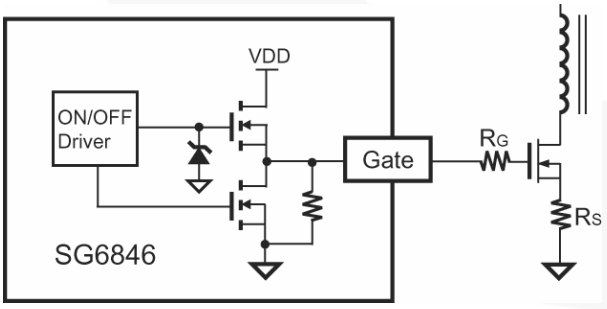

Figure 11.Gate Driver

Constant Output Power Limit

The maximum output power of a flyback converter can be designed by the current-sense resistor R_S. When the load increases, the peak inductor current increases accordingly. As the current-sense signal of the SENSE pin exceeds the internal limit V_{SENSE}, 0.9V typically, the SG6846 stops the PWM pulses immediately. The output power of a flyback power supply in DCM is calculated as:

$$P_{OUT} = \frac{1}{2} \cdot L \cdot I_{pk}^2 \cdot f_S \cdot \eta \quad (7)$$

where:
L is the inductance;
I_{pk} is the peak inductor current;
f_s is the PWM frequency; and
η is the conversion efficiency.

If the conversion efficiency remains unchanged for a wide input voltage range, the maximum output power would be the same for a fixed I_{pk}, which is limited by the internal current limiting threshold voltage V_{TH} and R_S. However, due to the time delay from the comparator to output stage inside the SG6846, the maximum output power with high line input is always higher than with low line. A 30% error is common for the universal input voltage range if the converter is operated in DCM. In CCM operation, the deviation becomes even worse. For the purpose of constant output power limit, the peak current limit V_{TH} must be adjustable according to the input voltage.

In the SG6846, the peak-current threshold is adjusted by the voltage of the VIN pin for constant output power limit over universal input-voltage range. Since the VIN pin is connected to the rectified AC input line voltage through the resistive divider, a higher line voltage generates a higher V_{IN} voltage. The threshold voltage decreases as the V_{IN} voltage increases, making the maximum output power at high line input voltage equal to that at low line input.

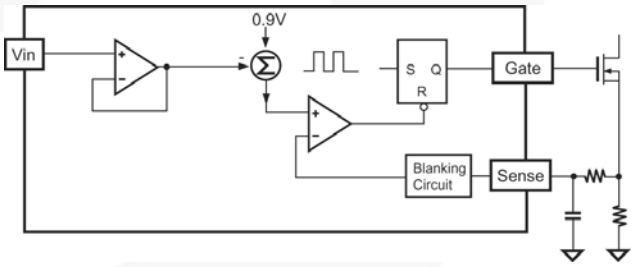

Figure 12.Universal Line Voltage Compensation for Constant Output Power Limit

Brownout Protection

Since the VIN pin is connected through a resistive divider to the rectified AC input line voltage, it can also be used for brownout protection. If the V_{IN} voltage is less than 0.7V, the PWM output shuts off. As the V_{IN} voltage reaches 0.9V, the PWM output is turned on again. The hysteresis window for on/off is around 0.2V.

The recommended values for R1, R2, and C1 are 2M (1M+1M), 16.2K, and 4.7µF. Using these values in the evaluation board, the power supply is turned off at 75V (max. load) / 64V (min. load) and recovered at 82V.

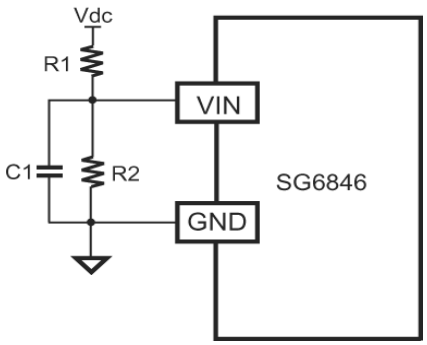

Figure 13. Universal Line Voltage Compensation for Constant Output Power Limit

Two-level Over-Current Protection (OCP)

The cycle-by-cycle current limiting shuts down the PWM immediately when the switching current is over the peak-current threshold. In addition, an over-current protection circuit is built-in. When the switching current is higher than the OCP threshold, the internal counter starts counting up. When the switching current is lower than the OCP threshold, the internal counter counts down. When the total accumulated counting time is more than OCP delay time (SG6846A: 1600ms; SG6846C: 110ms), the controller is latched off.

By adjusting the R_S resistance to let the peak-current at maximum load under OCP threshold and over this threshold at peak load condition, the two-level OCP protection is enabled. These functions are especially designed for an SMPS with surge current output, such as for printers, scanners, and motor drivers.

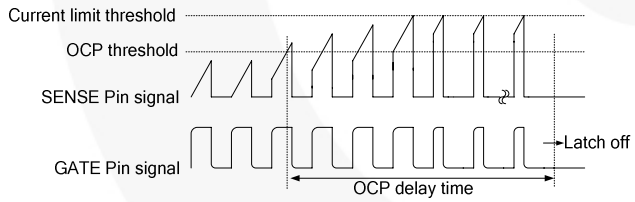

Figure 14. Timing Chart for Two-level Over-Current Protection (OCP)

V_{DD} Over-Voltage Protection (OVP)

V_{DD} over-voltage protection prevents the controller from over-voltage destruction. The V_{DD} voltage rises when an open-loop failure occurs. Once the V_{DD} voltage exceeds 23.6V for around 100μs, the power supply latches off.

Thermal Protection

A constant current, I_{RT}, is provided from the pin RT. The resistor connected to pin R_I determines its magnitude:

$$I_{RT} = 1.8V / R_I \quad (8)$$

For example, I_{RT} = 70μA if R_I = 26KΩ.

For over-temperature protection (OTP), an NTC thermistor RT in series with a resistor R_a can be connected between the RT pin and ground. When the voltage of the RT pin drops below 1.065V, PWM output is latched off. A debounce time around 100μs is added to prevent false triggering. After the latch is reset and cleared (SG6846CX: V_{RT}>1.165V; SG6846LX: AC unplugged), PWM turns on again. If the RT pin is not used, connect a 100kΩ resistor between the RT pin and ground to disable this thermal protection function. Beside NTC and R_a, a capacitor should be connected to RT pin to eliminate switching noise. This capacitor's value is less than 1nF (shown as Figure 14).

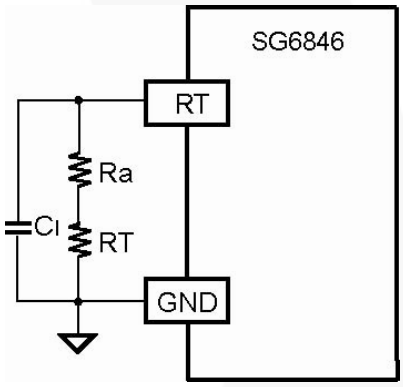

Figure 15. T C1 (<1nF) Connect to RT Pin

Lab Note

Before rework or solder/desolder on the power supply, discharge the primary capacitors by an external bleeding resistor. Otherwise, the PWM IC may be destroyed by external high voltage during solder/desolder.

This device is sensitive to ESD discharge. To improve production yield, the production line should be ESD protected according to ANSI ESD S1.1, ESD S1.4, ESD S7.1, ESD STM 12.1, and EOS/ESD S6.1.

Printed Circuit Board (PCB) Layout

High-frequency switching current/voltage makes PCB layout a very important design issue. Good PCB layout minimizes excessive EMI and helps the power supply survive during surge/ESD tests.

Guidelines:

- To get better EMI performance and reduce line frequency ripples, the output of the bridge rectifier should be connected to capacitor C1 first, then to the switching circuits.
- The high-frequency current loop is in **C1 – Transformer – MOSFET – R_S – C1**. The area enclosed by this current loop should be as small as possible. Keep the traces (especially **4→1**) short, direct, and wide. High-voltage traces related to the drain of MOSFET and RCD snubber should be kept far way from control circuits to prevent unnecessary interference. If a heatsink is used for the MOSFET, connect this heatsink to ground.
- As indicated by **3**, the ground of control circuits should be connected first, then to other circuitry.
- As indicated by **2**, the area enclosed by **transformer auxiliary winding, D1, C2, D2, and C3** should also be kept small. Place C3 close to the SG6846 for good decoupling.

Two suggestions with different pro and cons for ground connections are offered:

- GND**3** → **2** → **4** → **1**: This could avoid common impedance interference for sense signal.
- GND**3**→**2**→**1**→**4**: This could be better for ESD testing where the earth ground is not available on the power supply. Regarding the ESD discharge path, the charges go from secondary through the transformer stray capacitance to GND**2** first. The charges then go from GND**2** to GND**1** and back to the mains. Note that control circuits should not be placed on the discharge path. Point discharge for common choke can decrease high-frequency impedance and help increase ESD immunity.
- Should a Y-cap between primary and secondary be required, connect this Y-cap to the **positive terminal of C1**. If this Y-cap is connected to the primary GND, it should be connected to the **negative terminal of C1 (GND1)** directly. Point discharge of this Y-cap also helps for ESD. However, the creepage between these two pointed ends should be large enough to satisfy the requirements of applicable standards.

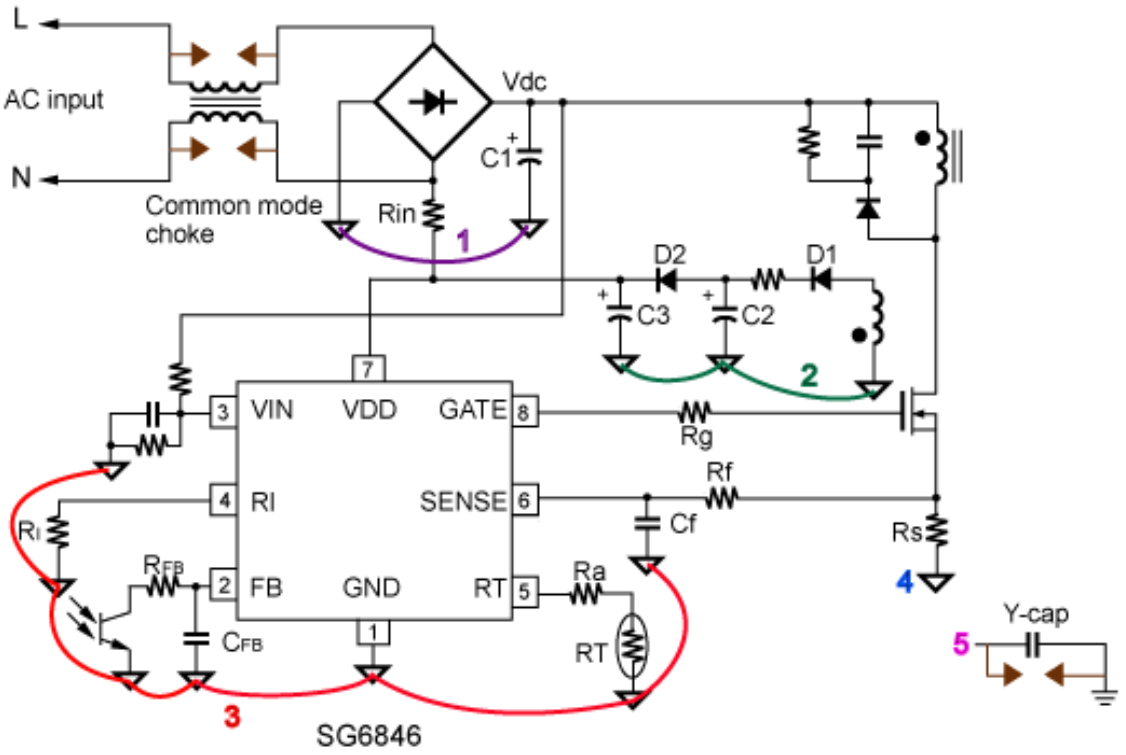

Figure 16.Layout Considerations

Related Datasheets

SG6846 — Highly Integrated Green-Mode PWM Controller
SG6846A — Highly Integrated Green-Mode PWM Controller
SG6846B — Highly Integrated Green-Mode PWM Controller
SG6846C — Highly Integrated Green-Mode PWM Controller
SG6846G — Highly Integrated Green-Mode PWM Controller