

DAC1408D750

Dual 14-bit DAC; up to 750 Msps; 2×, 4× or 8× interpolating with JESD204A interface

Rev. 2 — 2 December 2010

Product data sheet

1. General description

The DAC1408D750 is a high-speed 14-bit dual channel Digital-to-Analog Converter (DAC) with selectable 2×, 4× or 8× interpolating filters optimized for multi-carrier WCDMA transmitters.

Because of its digital on-chip modulation, the DAC1408D750 allows the complex pattern provided through lane 0, lane 1, lane 2 and lane 3, to be converted up from baseband to IF. The mixing frequency is adjusted via a Serial Peripheral Interface (SPI) with a 32-bit Numerically Controlled Oscillator (NCO) and the phase is controlled by a 16-bit register.

The DAC1408D750 also includes a 2×, 4× or 8× clock multiplier which provides the appropriate internal clocks and an internal regulation to adjust the output full-scale current.

The input data format is serial according to JESD204A specification. This new interface has numerous advantages over the traditional parallel one: easy PCB layout, lower radiated noise, lower pin count, self-synchronous link, skew compensation. The maximum number of lanes of the DAC1408D750 is 4 and its maximum serial data rate is 3.125 Gbps.

The Multiple Device Synchronization (MDS) guarantees a maximum skew of one output clock period between several DAC devices. MDS incorporates modes: Master/slave and All slave mode.

2. Features and benefits

- Dual 14-bit resolution
- 750 Msps maximum update rate
- Selectable 2×, 4× or 8× interpolation filters
- Input data rate up to 312.5 Msps
- Very low-noise cap-free integrated PLL
- 32-bit programmable NCO frequency
- Four JESD204A serial input lanes
- 1.8 V and 3.3 V power supplies
- LVDS compatible clock inputs
- IMD3: 80 dBc; $f_s = 737.28$ Msps; $f_o = 140$ MHz
- ACPR: 71 dBc; two carriers WCDMA; $f_s = 737.28$ Msps; $f_o = 153.6$ MHz
- Typical 1.28 W power dissipation at 4× interpolation, PLL off and 740 Msps
- Power-down mode and Sleep modes
- Differential scalable output current from 1.6 mA to 22 mA
- On-chip 1.25 V reference
- External analog offset control (10-bit auxiliary DACs)
- Internal digital offset control
- Inverse (sin x) / x function



- Two's complement or binary offset data format
- LMF = 421 or LMF = 211 support
- Differential CML receiver with embedded termination
- Synchronization of multiple DAC outputs
- Fully compatible SPI port
- Industrial temperature range from -40 °C to +85 °C
- Integrated PLL can be bypassed
- Embedded complex modulator

3. Applications

- Wireless infrastructure: LTE, WiMAX, GSM, CDMA, WCDMA, TD-SCDMA
- Communication: LMDS/MMDS, point to point
- Direct Digital Synthesis (DDS)
- Broadband wireless systems
- Digital radio links
- Instrumentation
- Automated Test Equipment (ATE)

4. Ordering information

Table 1. Ordering information

| Type number | Package | | Version |
|---------------|---------|--|----------|
| | Name | Description | |
| DAC1408D750HN | HVQFN64 | plastic thermal enhanced very thin quad flat package; no leads; 64 terminals; body 9 × 9 × 0.85 mm | SOT804-3 |

5. Block diagram

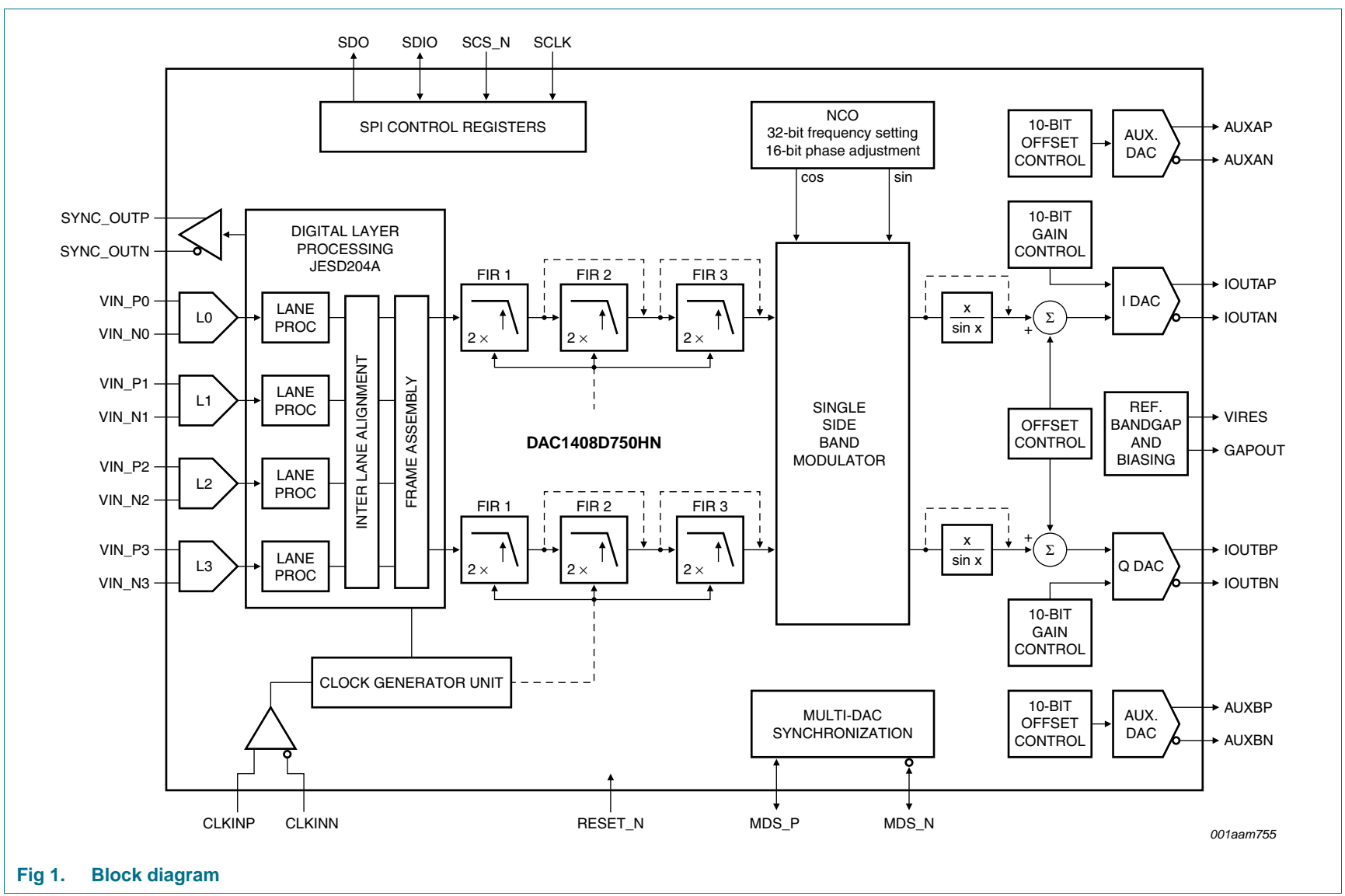


Fig 1. Block diagram

001aam755

6. Pinning information

6.1 Pinning

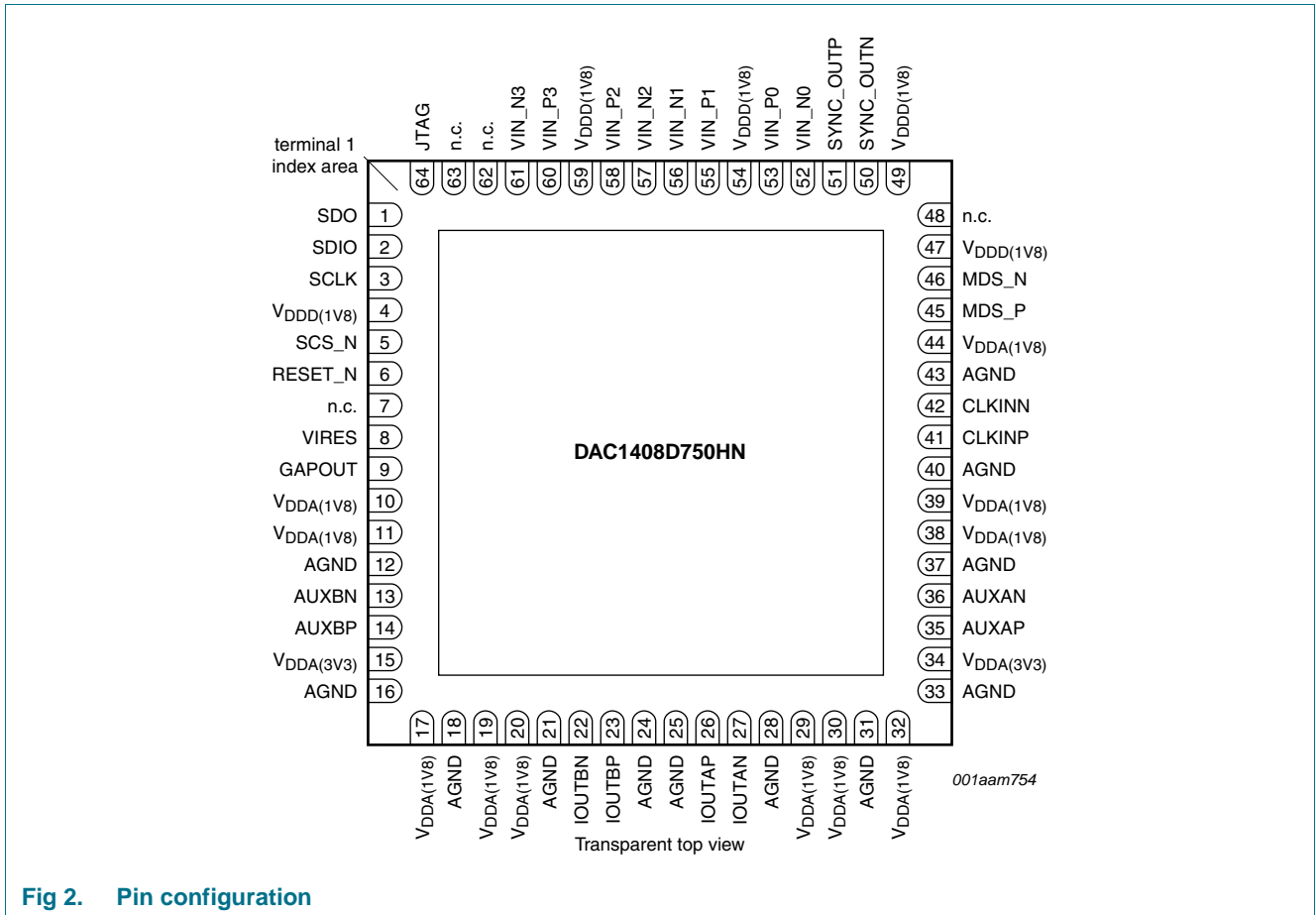


Fig 2. Pin configuration

6.2 Pin description

Table 2. Pin description

| Symbol | Pin | Type ^[1] | Description |
|------------------------|-----|---------------------|-------------------------------|
| SDO | 1 | O | SPI data output |
| SDIO | 2 | I/O | SPI data input/output |
| SCLK | 3 | I | SPI clock |
| V _{DD} (1V8) | 4 | P | digital supply voltage 1.8 V |
| SCS_N | 5 | I | SPI chip select (active LOW) |
| RESET_N | 6 | I | general reset (active LOW) |
| n.c. | 7 | - | not connected |
| VIRES | 8 | I/O | DAC biasing resistor |
| GAPOUT | 9 | I/O | band gap input/output voltage |
| V _{DDA} (1V8) | 10 | P | analog supply voltage 1.8 V |
| V _{DDA} (1V8) | 11 | P | analog supply voltage 1.8 V |

Table 2. Pin description ...continued

| Symbol | Pin | Type ^[1] | Description |
|-----------------------|-----|---------------------|--|
| AGND | 12 | G | analog ground |
| AUXBN | 13 | O | complementary auxiliary DAC B output |
| AUXBP | 14 | O | auxiliary DAC B output |
| V _{DDA(3V3)} | 15 | P | analog supply voltage 3.3 V |
| AGND | 16 | G | analog ground |
| V _{DDA(1V8)} | 17 | P | analog supply voltage 1.8 V |
| AGND | 18 | G | analog ground |
| V _{DDA(1V8)} | 19 | P | analog supply voltage 1.8 V |
| V _{DDA(1V8)} | 20 | P | analog supply voltage 1.8 V |
| AGND | 21 | G | analog ground |
| IOUTBN | 22 | O | complementary DAC B output current |
| IOUTBP | 23 | O | DAC B output current |
| AGND | 24 | G | analog ground |
| AGND | 25 | G | analog ground |
| IOUTAP | 26 | O | DAC A output current |
| IOUTAN | 27 | O | complementary DAC A output current |
| AGND | 28 | G | analog ground |
| V _{DDA(1V8)} | 29 | P | analog supply voltage 1.8 V |
| V _{DDA(1V8)} | 30 | P | analog supply voltage 1.8 V |
| AGND | 31 | G | analog ground |
| V _{DDA(1V8)} | 32 | P | analog supply voltage 1.8 V |
| AGND | 33 | G | analog ground |
| V _{DDA(3V3)} | 34 | P | analog supply voltage 3.3 V |
| AUXAP | 35 | O | auxiliary DAC A output current |
| AUXAN | 36 | O | complementary auxiliary DAC A output current |
| AGND | 37 | G | analog ground |
| V _{DDA(1V8)} | 38 | P | analog supply voltage 1.8 V |
| V _{DDA(1V8)} | 39 | P | analog supply voltage 1.8 V |
| AGND | 40 | G | analog ground |
| CLKINP | 41 | I | clock input |
| CLKINN | 42 | I | complementary clock input |
| AGND | 43 | G | analog ground |
| V _{DDA(1V8)} | 44 | P | analog supply voltage 1.8 V |
| MDS_P | 45 | I/O | multi-device synchronization |
| MDS_N | 46 | I/O | complementary multi-device synchronization |
| V _{DDD(1V8)} | 47 | P | digital supply voltage 1.8 V |
| n.c. | 48 | - | not connected |
| V _{DDD(1V8)} | 49 | P | digital supply voltage 1.8 V |
| SYNC_OUTN | 50 | O | synchronization request to transmitter, complementary output |
| SYNC_OUTP | 51 | O | synchronization request to transmitter |

Table 2. Pin description ...continued

| Symbol | Pin | Type ^[1] | Description |
|----------------------|------------------|---------------------|--|
| VIN_N0 | 52 | I | serial interface lane 0 negative input |
| VIN_P0 | 53 | I | serial interface lane 0 positive input |
| V _{DD(1V8)} | 54 | P | digital supply voltage 1.8 V |
| VIN_P1 | 55 | I | serial interface lane 1 positive input |
| VIN_N1 | 56 | I | serial interface lane 1 negative input |
| VIN_N2 | 57 | I | serial interface lane 2 negative input |
| VIN_P2 | 58 | I | serial interface lane 2 positive input |
| V _{DD(1V8)} | 59 | P | digital supply voltage 1.8 V |
| VIN_P3 | 60 | I | serial interface lane 3 positive input |
| VIN_N3 | 61 | I | serial interface lane 3 negative input |
| n.c. | 62 | - | not connected |
| n.c. | 63 | - | not connected |
| JTAG | 64 | I | JTAG test mode select (must be grounded) |
| GND | H ^[2] | G | ground |

[1] P: power supply; G: ground; I: input; O: output.

[2] H = heatsink (exposed die pad to be soldered to GND. A minimum of 81 thermal vias are required).

7. Limiting values

Table 3. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|---------------------|-------------------------------|------------|------|------|------|
| V _{D(3V3)} | analog supply voltage (3.3 V) | | -0.5 | +4.6 | V |
| V _{D(1V8)} | analog supply voltage (1.8 V) | | -0.5 | +2.5 | V |
| V _{DD} | digital supply voltage | | -0.5 | +2.5 | V |
| T _{stg} | storage temperature | | -55 | +150 | °C |
| T _{amb} | ambient temperature | | -40 | +85 | °C |
| T _j | junction temperature | | -40 | +125 | °C |

8. Thermal characteristics

Table 4. Thermal characteristics

| Symbol | Parameter | Conditions | Typ | Unit |
|----------------------|---|------------|---------------------|------|
| R _{th(j-a)} | thermal resistance from junction to ambient | | ^[1] 18.7 | K/W |
| R _{th(j-c)} | thermal resistance from junction to case | | ^[1] 6.7 | K/W |

[1] Complies with JEDEC test board, in free air.

9. Characteristics

Table 5. Characteristics

$V_{DDA(1V8)} = V_{DDD} = 1.7\text{ V to }1.9\text{ V}$; $V_{DDA(3V3)} = 3.13\text{ V to }3.47\text{ V}$; AGND and GND are shorted together; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; typical values measured at $V_{DDA(1V8)} = V_{DDD} = 1.8\text{ V}$; $V_{DDA(3V3)} = 3.3\text{ V}$; $T_{amb} = +25\text{ °C}$; $R_L = 50\text{ }\Omega$; $I_{O(fs)} = 20\text{ mA}$; maximum sample rate; PLL off unless otherwise specified.

| Symbol | Parameter | Conditions | Test ^[1] | Min | Typ | Max | Unit | |
|-----------------------------|-----------------------------------|---|---------------------|------|------|------|------|--|
| $V_{DDA(3V3)}$ | analog supply voltage (3.3 V) | | I | 3.13 | 3.3 | 3.47 | V | |
| $V_{DDD(1V8)}$ | digital supply voltage (1.8 V) | | I | 1.7 | 1.8 | 1.9 | V | |
| $V_{DDA(1V8)}$ | analog supply voltage (1.8 V) | | I | 1.7 | 1.8 | 1.9 | V | |
| $I_{DDA(3V3)}$ | analog supply current (3.3 V) | $f_o = 19\text{ MHz}$; $f_s = 740\text{ Msps}$; 4× interpolation; NCO on | I | - | 42 | - | mA | |
| $I_{DDD(1V8)}$ | digital supply current, (1.8 V) | $f_o = 19\text{ MHz}$; $f_s = 740\text{ Msps}$; 4× interpolation; NCO on | I | - | 353 | - | mA | |
| $I_{DDA(1V8)}$ | analog supply current, (1.8 V) | $f_o = 19\text{ MHz}$; $f_s = 740\text{ Msps}$; 4× interpolation; NCO on | I | - | 435 | - | mA | |
| ΔI_{DDD} | digital supply current difference | x/sin x function on; $f_s = 740\text{ Msps}$ | I | - | 59 | - | mA | |
| P_{tot} | total power dissipation | $f_s = 740\text{ Msps}$; 4× interpolation; NCO off; DAC Q off | C | - | 0.84 | - | W | |
| | | $f_s = 740\text{ Msps}$; 4× interpolation; NCO off | C | - | 1.28 | - | W | |
| | | $f_s = 740\text{ Msps}$; 4× interpolation; NCO on | C | - | 1.58 | - | W | |
| | | $f_s = 625\text{ Msps}$; 2× interpolation; NCO off | C | - | 1.33 | - | W | |
| | | $f_s = 625\text{ Msps}$; 2× interpolation; NCO on | C | - | 1.51 | - | W | |
| | | Power-down mode; $f_o = 19\text{ MHz}$; $f_s = 740\text{ Msps}$; 4× interpolation; NCO on | | | | | | |
| | | complete device; Power-down mode | I | - | 0.04 | - | W | |
| | | DAC A and DAC B; Power-down mode | I | - | 0.65 | - | W | |
| DAC A and DAC B; Sleep mode | I | - | 0.87 | - | W | | | |

Timing specifications

| | | | | | | | |
|------------------|---------------------|---------------------------|---|-----|-----|---|----|
| $t_{d(startup)}$ | start-up delay time | from full Power-down mode | D | - | 20 | - | ms |
| $t_{d(restart)}$ | restart delay time | from Sleep mode | D | - | 300 | - | ns |
| t_{lock} | lock time | maximum input rate | D | [2] | 11 | - | μs |

Clock inputs (CLKINN, CLKINP)^[3]

| | | | | | | | |
|-------|---------------|--|---|-----|---|------|----|
| V_i | input voltage | range: CLK+ or CLK- $ V_{gpd} < 50\text{ mV}$ ^[4] | C | 825 | - | 1575 | mV |
|-------|---------------|--|---|-----|---|------|----|

Table 5. Characteristics ...continued

$V_{DDA(1V8)} = V_{DDD} = 1.7\text{ V to }1.9\text{ V}$; $V_{DDA(3V3)} = 3.13\text{ V to }3.47\text{ V}$; AGND and GND are shorted together; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; typical values measured at $V_{DDA(1V8)} = V_{DDD} = 1.8\text{ V}$; $V_{DDA(3V3)} = 3.3\text{ V}$; $T_{amb} = +25\text{ °C}$; $R_L = 50\ \Omega$; $I_{O(fs)} = 20\text{ mA}$; maximum sample rate; PLL off unless otherwise specified.

| Symbol | Parameter | Conditions | Test ^[1] | Min | Typ | Max | Unit |
|--|--|---|---------------------|--------------|------|--------------|---------------|
| V_{idth} | input differential threshold voltage | $ V_{gpd} < 50\text{ mV}$ ^[4] | C | -100 | - | +100 | mV |
| R_i | input resistance | | D | - | 10 | - | M Ω |
| C_i | input capacitance | | D | - | 0.5 | - | pF |
| Digital inputs (SDO, SDIO, SCLK, SCS_N, RESET_N) | | | | | | | |
| V_{IL} | LOW-level input voltage | | C | GND | - | $0.3V_{DDD}$ | V |
| V_{IH} | HIGH-level input voltage | | C | $0.7V_{DDD}$ | - | V_{DDD} | V |
| I_{IL} | LOW-level input current | $V_{IL} = 0.3V_{DDD}\text{ V}$ | I | - | 1 | - | μA |
| I_{IH} | HIGH-level input current | $V_{IH} = 0.7V_{DDD}\text{ V}$ | I | - | 1 | - | μA |
| Digital outputs (SDO, SDIO) | | | | | | | |
| V_{OL} | LOW-level output voltage | $I_{load} = 2\text{ mA}$ | C | GND | - | 0.13 | V |
| V_{OH} | HIGH-level output voltage | $I_{load} = 2\text{ mA}$ | C | 1.65 | - | V_{DDD} | V |
| Digital inputs (V_{in_p}/V_{in_n})^[5] | | | | | | | |
| $V_{I(cm)}$ | common-mode input voltage | | D | - | 0.78 | - | V |
| $V_{I(dif)(p-p)}$ | peak-to-peak differential input voltage | | D | 175 | - | 1000 | mV |
| Z_{tt} | V_{tt} source impedance | | D | - | 0.7 | - | Ω |
| ΔZ_i | differential input impedance | | D | - | 100 | - | Ω |
| Digital outputs (SYNC_OUTN/SYNC_OUTP)^[6] | | | | | | | |
| $V_{O(cm)}$ | common-mode output voltage | | C | - | 1.18 | - | V |
| $V_{O(dif)(p-p)}$ | peak-to-peak differential output voltage | | C | - | 0.45 | - | V |
| Digital inputs/outputs (MDS_N/MDS_P) | | | | | | | |
| $V_{O(dif)(p-p)}$ | peak-to-peak differential output voltage | | D | - | 600 | - | mV |
| $C_{O(L)}$ | Output load capacitance | between pins GND and MDS_N or MDS_P | D | - | - | 10 | pF |
| C_i | Input capacitance | between pins GND and MDS_N or MDS_P | D | - | 0.3 | - | pF |

Table 5. Characteristics ...continued

$V_{DDA(1V8)} = V_{DDD} = 1.7\text{ V to }1.9\text{ V}$; $V_{DDA(3V3)} = 3.13\text{ V to }3.47\text{ V}$; AGND and GND are shorted together; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; typical values measured at $V_{DDA(1V8)} = V_{DDD} = 1.8\text{ V}$; $V_{DDA(3V3)} = 3.3\text{ V}$; $T_{amb} = +25\text{ °C}$; $R_L = 50\ \Omega$; $I_{O(fs)} = 20\text{ mA}$; maximum sample rate; PLL off unless otherwise specified.

| Symbol | Parameter | Conditions | Test ^[1] | Min | Typ | Max | Unit |
|--|------------------------------------|---|---------------------|------|-------|----------------|------------|
| Analog outputs (IOUTAP, IOUTAN, IOUTBP, IOUTBN) | | | | | | | |
| $I_{O(fs)}$ | full-scale output current | register value = 00h (see Table 13 and Table 14) | D | - | 1.6 | - | mA |
| | | register = default value (see Table 13 and Table 14) | | - | 20 | - | mA |
| V_O | output voltage | compliance range | D | 1.8 | - | $V_{DDA(3V3)}$ | V |
| R_o | output resistance | | D | - | 250 | - | k Ω |
| C_o | output capacitance | | D | - | 3 | - | pF |
| ΔE_O | offset error variation | | D | - | 6 | - | ppm/°C |
| ΔE_G | gain error variation | | D | - | 18 | - | ppm/°C |
| Reference voltage output (GAPOUT) | | | | | | | |
| $V_{O(ref)}$ | reference output voltage | | C | 1.20 | 1.25 | 1.29 | V |
| $I_{O(ref)}$ | reference output current | external voltage 1.2 V | C | - | 40 | - | μ A |
| $\Delta V_{O(ref)}$ | reference output voltage variation | | C | - | 117 | - | ppm/°C |
| Analog auxiliary outputs (AUXAP, AUXAN, AUXBP and AUXBN) | | | | | | | |
| $I_{O(aux)}$ | auxiliary output current | differential outputs | I | - | 2.2 | - | mA |
| $V_{O(aux)}$ | auxiliary output voltage | compliance range | D | 0 | - | 2 | V |
| $N_{DAC(aux)mono}$ | auxiliary DAC monotonicity | guaranteed | D | - | 10 | - | bits |
| Input timing (Vin_p/Vin_n) | | | | | | | |
| f_{data} | data rate | 2× interpolation | D | - | - | 312.5 | MspS |
| | | 4× interpolation | D | - | - | 187.5 | MspS |
| | | 8× interpolation | D | - | - | 93.75 | MspS |
| f_{bit} | bit rate | serial input | D | 0.7 | - | 3.125 | Gbps |
| Output timing (IOUTAP, IOUTAN, IOUTBP, IOUTBN) | | | | | | | |
| f_s | sampling rate | | D | - | - | 750 | MspS |
| t_s | settling time | up to 0.5 LSB | D | - | 20 | - | ns |
| NCO frequency range; $f_s = 750\text{ MspS}$ | | | | | | | |
| f_{NCO} | NCO frequency | register value = 00000000h (see Table 21 to Table 24) | D | - | 0 | - | MHz |
| | | register value = FFFFFFFFh (see Table 21 to Table 24) | D | - | 750 | - | MHz |
| f_{step} | step frequency | | D | - | 0.175 | - | Hz |
| Low power NCO frequency range; $f_s = 750\text{ MspS}$ | | | | | | | |
| f_{NCO} | NCO frequency | reg value = 00000000h (see Table 21 to Table 24) | D | - | 0 | - | MHz |
| | | reg value = F8000000h (see Table 21 to Table 24) | D | - | 726.4 | - | MHz |

Table 5. Characteristics ...continued

$V_{DDA(1V8)} = V_{DDD} = 1.7\text{ V to }1.9\text{ V}$; $V_{DDA(3V3)} = 3.13\text{ V to }3.47\text{ V}$; AGND and GND are shorted together; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; typical values measured at $V_{DDA(1V8)} = V_{DDD} = 1.8\text{ V}$; $V_{DDA(3V3)} = 3.3\text{ V}$; $T_{amb} = +25\text{ °C}$; $R_L = 50\ \Omega$; $I_{O(fs)} = 20\text{ mA}$; maximum sample rate; PLL off unless otherwise specified.

| Symbol | Parameter | Conditions | Test ^[1] | Min | Typ | Max | Unit | |
|-----------------------------|--|--|---------------------|-----|------|------|------|-----|
| f_{step} | step frequency | | D | - | 23.4 | - | MHz | |
| Dynamic performances | | | | | | | | |
| SFDR | spurious-free dynamic range | $f_{data} = 92.16\text{ Msps}$; $f_s = 737.28\text{ Msps}$; 8×; BW = $f_{data} / 2$; PLL on | [7] | | | | | |
| | | $f_o = 4\text{ MHz at }-1\text{ dBFS}$ | C | - | 77 | - | dBc | |
| | | $f_{data} = 184.32\text{ Msps}$; $f_s = 737.28\text{ Msps}$; 4×; BW = $f_{data} / 2$ | [7] | | | | | |
| | | $f_o = 19\text{ MHz at }-1\text{ dBFS}$ | C | - | 74.5 | - | dBc | |
| | | $f_{data} = 312.5\text{ Msps}$; $f_s = 625\text{ Msps}$; 2×; BW = $f_{data} / 2$ | [7] | | | | | |
| | $f_o = 19\text{ MHz at }-1\text{ dBFS}$ | I | - | 75 | - | dBc | | |
| SFDR _{RBW} | restricted bandwidth spurious-free dynamic range | $f_s = 737.28\text{ Msps}$; 4× interpolation; $f_o = 153.6\text{ MHz at }-1\text{ dBFS}$; BW = 100 MHz | I | [7] | - | 81.5 | - | dBc |
| | | $f_s = 737.28\text{ Msps}$; 4× interpolation; $f_o = 153.6\text{ MHz at }-1\text{ dBFS}$; BW = 20 MHz | C | [7] | - | 84 | - | dBc |
| IMD3 | third-order intermodulation distortion | $f_{o1} = 95\text{ MHz}$; $f_{o2} = 97\text{ MHz}$; $f_s = 737.28\text{ Msps}$; 4× interpolation | C | [7] | - | 76 | - | dBc |
| | | $f_{o1} = 153.1\text{ MHz}$; $f_{o2} = 154.1\text{ MHz}$; $f_s = 737.28\text{ Msps}$; 4× interpolation | I | [7] | - | 81 | - | dBc |
| | | $f_{o1} = 137\text{ MHz}$; $f_{o2} = 143\text{ MHz}$; $f_s = 737.28\text{ Msps}$; 4× interpolation | C | [7] | - | 80 | - | dBc |
| ACPR | adjacent channel power ratio | NCO on; 4× interpolation; $f_s = 737.28\text{ Msps}$; $f_o = 96\text{ MHz}$ | [7] | | | | | |
| | | 1 carrier; BW = 5 MHz | C | - | 75 | - | dBc | |
| | | 2 carriers; BW = 10 MHz | C | - | 72 | - | dBc | |
| | | 4 carriers; BW = 20 MHz | C | - | 69 | - | dBc | |
| | | NCO on; 4× interpolation; $f_s = 737.28\text{ Msps}$; $f_o = 153.6\text{ MHz}$ | [7] | | | | | |
| | | 1 carrier; BW = 5 MHz | C | - | 75 | - | dBc | |
| | | 2 carriers; BW = 10 MHz | C | - | 71 | - | dBc | |
| 4 carriers; BW = 20 MHz | C | - | 68 | - | dBc | | | |

Table 5. Characteristics ...continued

$V_{DDA(1V8)} = V_{DDD} = 1.7\text{ V to }1.9\text{ V}$; $V_{DDA(3V3)} = 3.13\text{ V to }3.47\text{ V}$; AGND and GND are shorted together; $T_{amb} = -40\text{ °C to }+85\text{ °C}$; typical values measured at $V_{DDA(1V8)} = V_{DDD} = 1.8\text{ V}$; $V_{DDA(3V3)} = 3.3\text{ V}$; $T_{amb} = +25\text{ °C}$; $R_L = 50\ \Omega$; $I_{O(fs)} = 20\text{ mA}$; maximum sample rate; PLL off unless otherwise specified.

| Symbol | Parameter | Conditions | Test ^[1] | Min | Typ | Max | Unit | |
|--------|------------------------|--|---------------------|-----|-----|------|------|--------|
| NSD | noise spectral density | $f_s = 737.28\text{ Msps}$; 4× interpolation; $f_o = 153.6\text{ MHz at }0\text{ dBFS}$ | I | [7] | - | -155 | - | dBm/Hz |

- [1] D = guaranteed by design; C = guaranteed by characterization; I = 100 % industrially tested.
- [2] Delay between the deassertion of bits FORCE_RESET_FCLK and FORCE_RESET_DCLK and the deassertion of the sync signal. It reflects the delay required by DAC1408D750 to lock to a JESD204A stream. It supposes that the TX is already transmitting K28.5 characters in error free conditions.
- [3] CLKINP/CLKINN inputs are at differential LVDS levels. An external termination resistor with a value of between 80 Ω and 120 Ω (see [Figure 15](#)) should be connected across the pins.
- [4] $|V_{gpd}|$ represents the ground potential difference voltage. This is the voltage that results from current flowing through the finite resistance and the inductance between the receiver and the driver circuit ground voltage.
- [5] Vin_p and Vin_n inputs are differential CML inputs. They are terminated internally to V_{tt} via 50 Ω (see [Figure 4](#)).
- [6] SYNC_OUTP/SYNC_OUTN outputs are differential LVDS outputs. They must be terminated by a resistor with a value of between 80 Ω and 120 Ω .
- [7] Optimum performances at high sampling rate (> 650 Msps) are achieved with $V_{DDA(1V8)} = 1.8\text{ V} \pm 2\%$.
- [8] IMD3 rejection with -6 dBFS/tone.

10. Application information

10.1 General description

The DAC1408D750 is a dual 14-bit DAC operating up to 750 Msps. With a maximum input data rate of up to 312.5 Msps and a maximum output sampling rate of 750 Msps, the DAC1408D750 allows more flexibility for wide bandwidth and multi-carrier systems. Combined with its quadrature modulator and 32-bit NCO, the DAC1408D750 simplifies the frequency selection of the system. This is also possible because of the 2×, 4× or 8× interpolation filters which remove undesired images.

DAC1408D750 supports the following JESD204A key features:

- 10-bit/8-bit decoding
- Code group synchronization
- inter-lane alignment
- $1 + x^{14} + x^{15}$ scrambling polynomial
- Character replacement
- TX/RX synchronization management via sync signals
- Multiple Converter Device Alignment-Multiple Lanes (MCDA-ML) device

DAC1408D750 can be interfaced with any logic device that features high speed SERDES functionality. This macro is now widely available in FPGA from different vendors. Standalone SERDES ICs can also be used.

To enhance the intrinsic board layout simplification of the JESD204A standard, NXP includes polarity swapping for each of the lanes and additionally offers lane swapping. Each physical lane can be configured logically as lane0, lane1, lane2 or lane3.

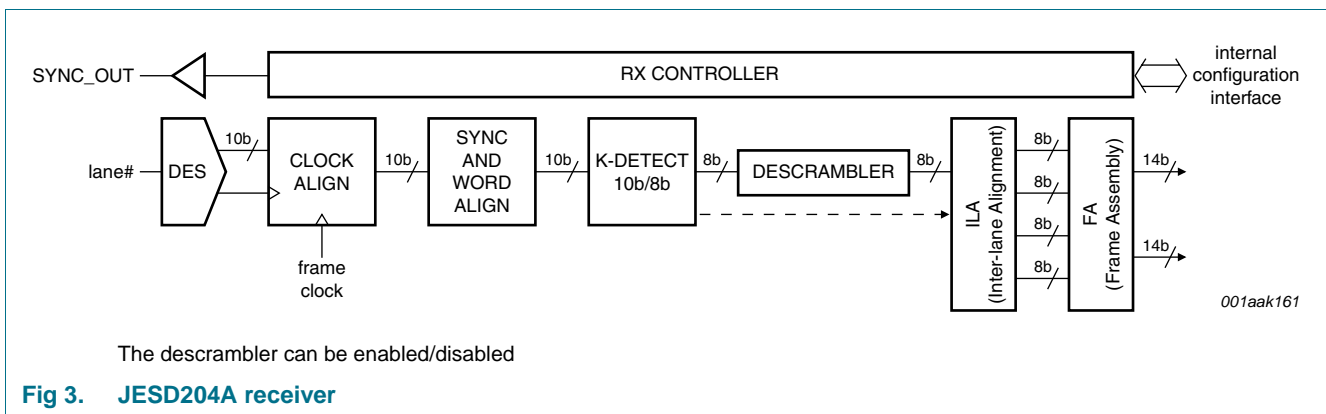
This device is MCDA-ML compliant, offering inter-lane alignment between several devices. Samples alignment between devices is maintained up to output level because of an NXP proprietary mechanism. One device is configured as the master and all the others are configured as slaves. These align their output samples automatically to the master ones. Therefore, a system with several DAC1408D750s can produce data with a guaranteed alignment of less than 1 DAC output clock period.

Each DAC generates two complementary current outputs on pins IOUTAP/IOUTAN and IOUTBP/IOUTBN. This provides a full-scale output current of up to 20 mA. An internal reference is available for the reference current which is externally adjustable using pin VIRES.

The DAC1408D750 must be configured before operating. Therefore, it features an SPI slave interface to access internal registers. Some of these registers also provide information about the JESD204A interface status.

The DAC1408D750 requires supplies of both 3.3 V and 1.8 V. The 1.8 V supply has separate digital and analog power supply pins. The clock input is LVDS compliant.

10.2 JESD204A receiver



The JEDEC204A defines the following parameters:

- L is the number of lanes per link
- M is the number of converters per device
- F is the number of bytes per frame clock period

The DAC1408D750 supports both LMF = 421 and LMF = 211. The current setting is configurable via the SPI registers interface.

The complete Digital Layer Processing (DLP) adds a variable delay on each lane path. This is mainly because of the inter-lane alignment.

Table 6. Digital Layer Processing Latency

| Symbol | Parameter | Conditions | Test ^[1] | Min | Typ | Max | Unit |
|----------------|------------|--------------------------------|---------------------|-----|-----|-----|----------------------|
| t _d | delay time | digital layer processing delay | D | 13 | - | 28 | cycle ^[2] |

[1] D = guaranteed by design.

[2] Frame clock cycle.

10.2.1 Lane input

Each lane is CML compliant. It is terminated to a common voltage with an integrated 50 Ω resistor.

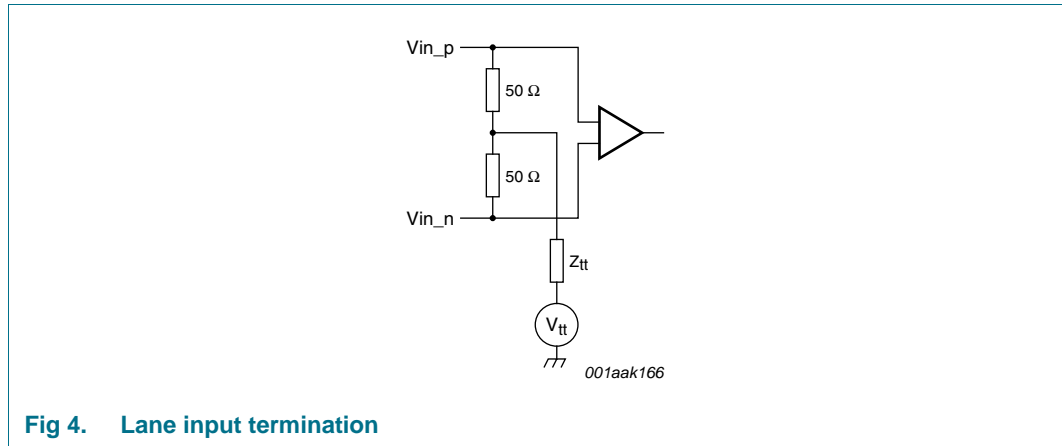


Fig 4. Lane input termination

The common-mode voltage is programmable by the SET_VCM_VOLTAGE register as shown in [Table 75 on page 55](#).

DC coupling is only possible if both the DAC and the transmitter have the same common-mode voltage. If this is not the case, AC coupling is required.

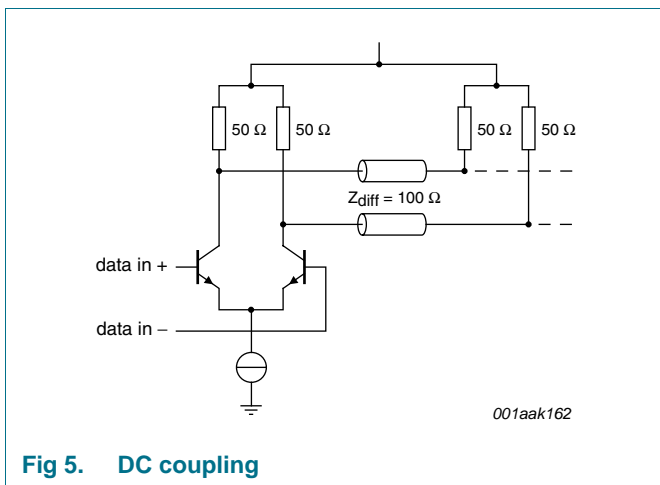


Fig 5. DC coupling

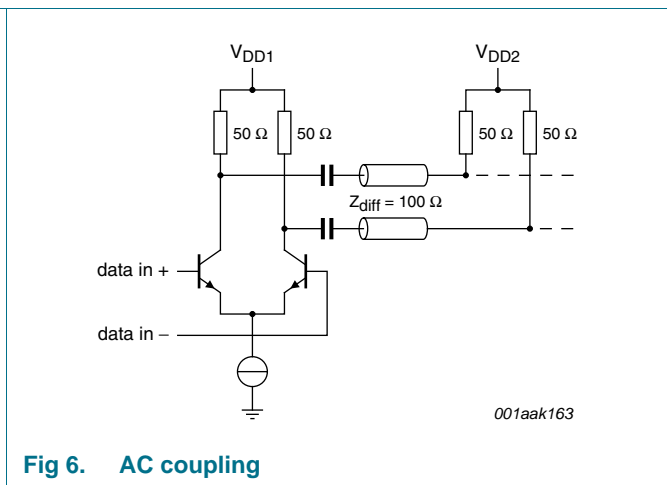


Fig 6. AC coupling

The deserializer performs the incoming data clock recovery and also the serial to parallel conversion. Therefore, each lane includes its own PLL that must first lock.

The clock alignment module transfers the data from the regenerated clock to the frame clock domain. The frequency of both clocks is the same but the phase relationship between the clocks is unknown.

10.2.2 Sync and word align

As stated in JESD204A, the transmitter and the receiver first have to synchronize. This is achieved through the SYNC_OUT signals and a sync pattern (K28.5 symbol). The receiver (i.e. DAC1408D750) first drives its SYNC_OUT outputs. The sync pattern is continuously sent until the receiver de-asserts the SYNC_OUT signal.

The lane processing makes use of the sync patterns to synchronize the data stream, determine the initial running disparity and extract the 10-bit word from the incoming data stream (word-alignment).

The SYNC_OUT signal is also used during normal operation by the DAC1408D750 to request a link reinitialization. This occurs when the 10b/8b module loses synchronization.

The SYNC_OUT signal conforms to LVDS signaling. Its common-mode voltage and its single-ended peak amplitude can be programmed using SET_SYNC_LEVEL bits in the SET_SYNC registers (see [Table 77 on page 55](#)).

SYNC_OUT is asynchronous with the frame clock. There is no timing specification with respect to the CLKINP and CLKINN inputs.

10.2.3 Comma detection and word align

This stage monitors the data stream for code characters (comma detection), decodes the words to bytes (octets) and performs optional character replacement as part of frame/lane alignment monitoring and correction. This module provides the required control signals to the RX controller and ILA.

This module decodes the 10-bit words into 8-bit words (octets). The decoding table is specified in the IEEE 802.3-2005 specification. During decoding, the disparity is calculated according to the disparity rules mentioned in the same specification IEEE 802.3-2005. When the disparity counter is more than +2 or less than -2, an error is generated.

The following comma symbols are detected during data transmission irrespective of the running disparity:

/K/ = K28.5

/F/ = K28.7

/A/ = K28.3

/R/ = K28.0

/Q/ = K28.4

A flag is sent to the control interface to reflect detected commas in registers.

The following flags are also triggered according to the following definitions:

- VALID: a code group that is found in the column of the 10b/8b decoding tables according to the current running disparity.
- DISPARITY ERROR: The received code group exists in the 10b/8b decoding table, but is not found in the proper column according to the current running disparity.
- NOT-IN-TABLE (NIT) ERROR: The received code group is not found in the 10b/8b decoding table for either disparity.
- INVALID: a code group that either shows a disparity error or that does not exist in the 10b/8b decoding table.

DAC1408D750 supports character replacement whatever the state of the descrambler. When scrambling is not active, the received K28.3 /A/ or K28.7 /F/ is replaced by the previous sample. When scrambling is active, the corresponding data octet D28.3 (0xC) or D28.7 (0xFC) is used.

10.2.4 Descrambler

The descrambler is a 16-bit parallel self-synchronous descrambler based on the polynomial $1 + x^{14} + x^{15}$. This processing can be turned off.

10.2.5 inter-lane alignment

This feature removes strict PCB design skew compensation between the lanes.

10.2.5.1 Single device operation

This module handles the alignment of the four data streams. Because of inter-lane skew and each PLL per lane concept, these alignment characters may be received at different times by the receivers. After the synchronization period, the lock signal is HIGH. This enables the receipt of K28.3 /A/ characters.

The /A/ characters provided in the initial alignment sequence are used to align the four data streams. The ILA_CNTRL register's SEL_ILA[1:0] bits select which K28.3 /A/ symbol triggers the initial lane alignment: "00" = 1st /A/ symbol, "01" = 2nd /A/ symbol, "10" = 3rd /A/ symbol, "11" = 4th /A/ symbol; [Table 86 on page 61](#). When all receivers have received their first selected /A/, they start propagating the received data to the frame assembly module at the same point in time.

This module can compensate up to ± 7 frame clock period misalignments between the lanes.

When initial lane alignment is not supported, the manual alignment mode can be used.

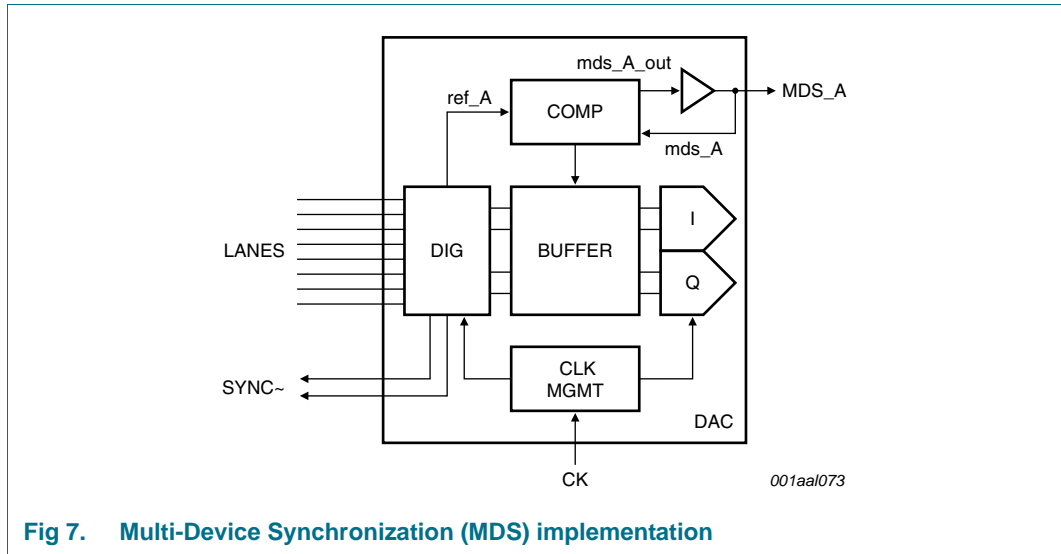
After the initial ILA sequence, the lane alignment monitoring starts. If the received user data contains a K28.3 /A/ symbol:

- its position is compared to the value of the alignment monitor counter
- if two successive K28.3 /A/ symbols have been received at a wrong position, a realignment takes place
- if the buffers are empty or overflow, this is indicated by the registers ILA_BUF_ERR_LN0 to ILA_BUF_ERR_LN3

10.2.5.2 Multi-device operation

DAC1408D750 implements a multi-device inter-lane alignment that guarantees a skew of less than one output period between them.

Two modes are available: master/slave and all slave. Both make use of the MDS_P and MDS_N pins.



Each DAC device of the system generates its own reference (ref_A in [Figure 7](#)).

If configured as a slave, an early-late comparator compares the internal reference with the external reference provided by the MDS pins. The comparator controls an internal buffer that is used to delay the samples.

10.2.5.3 Master/slave mode

The external reference is provided by one of the DACs (the master DAC), which has to be configured to do this. The others are set to slave mode.

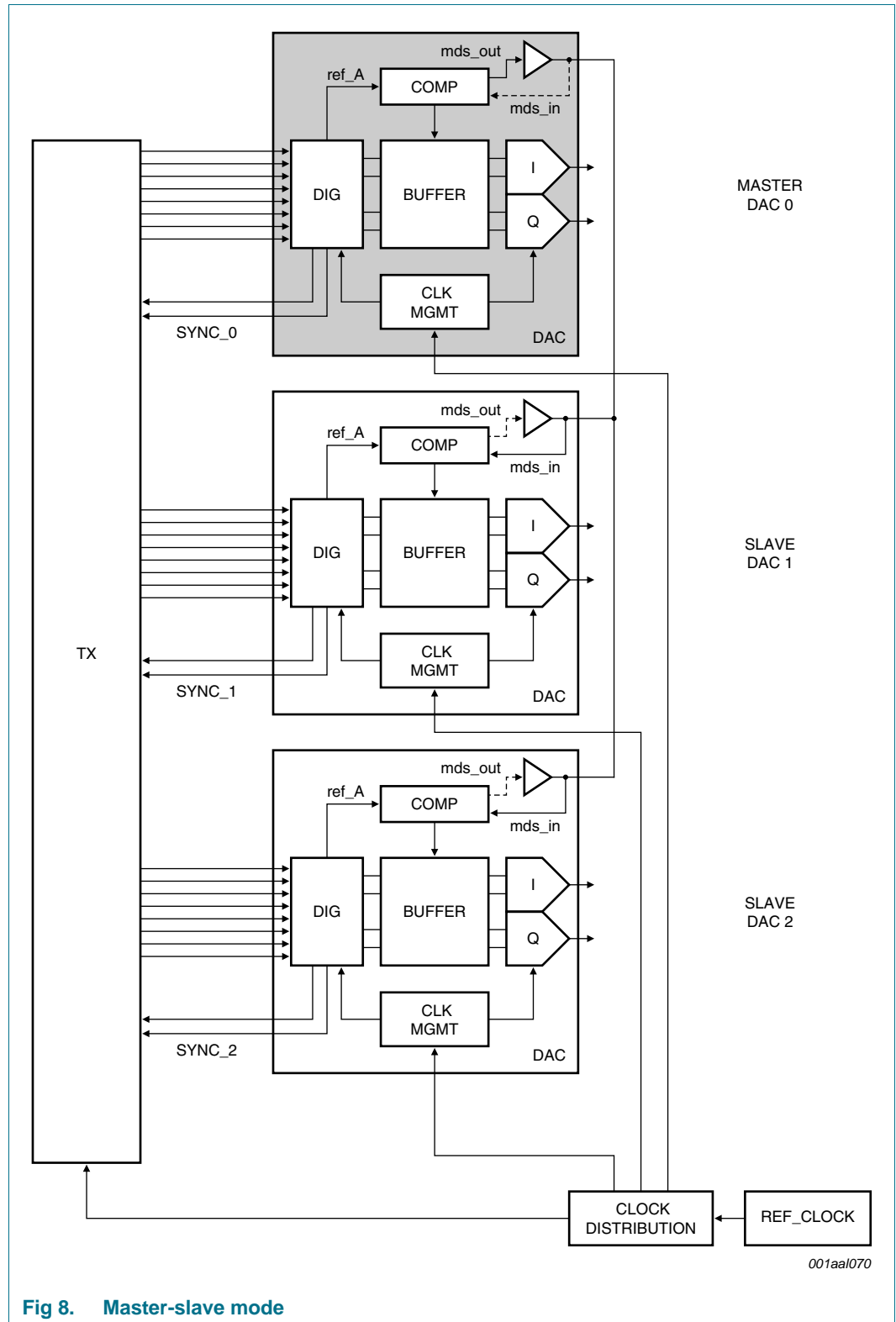


Fig 8. Master-slave mode

001aa1070

The MDS signal generated by the master DAC must reach all slaves within one DAC output clock period. This induces PCB layout constraints for the MDS signal and also for the clock distribution. Because trace lengths differ, the clock edges reach each of the DACs at different times.

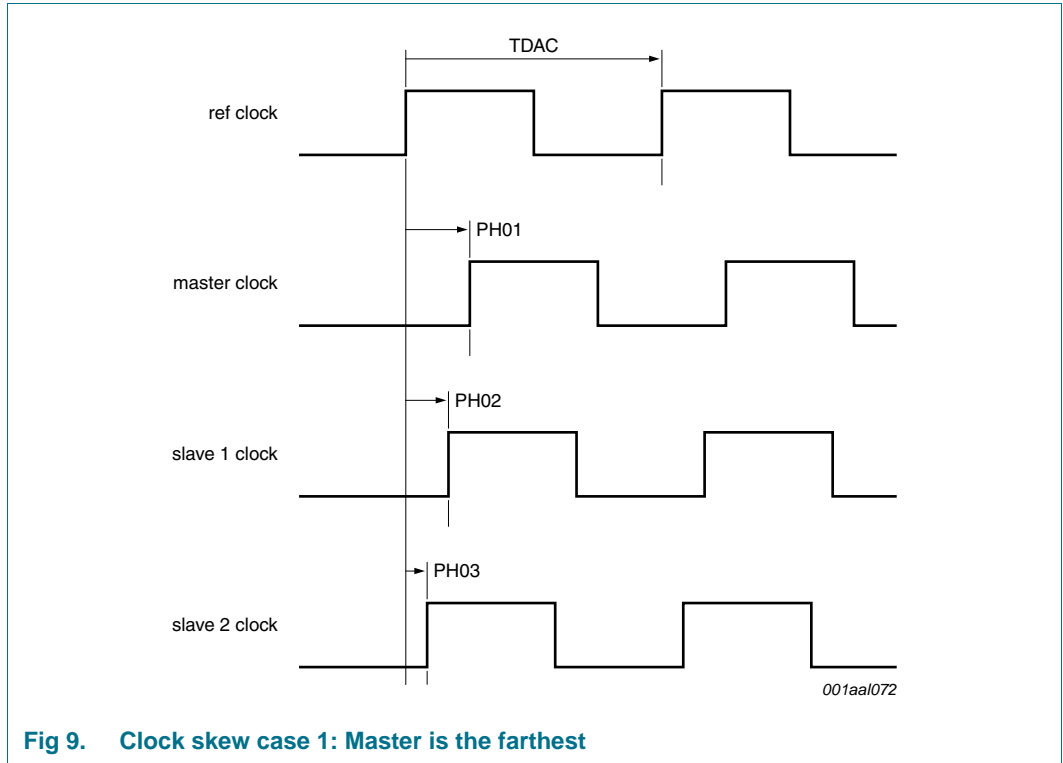


Fig 9. Clock skew case 1: Master is the farthest

The worst case clock skew is given by $\delta t_1 = PH01 - PH03$, where $PH0x$ represents the sum of the trace delay and the clock skew at the output of the clock generator.

The maximum allowable trace delay for the MDS signal is given by $\Delta t = TDAC - \delta t_1$.

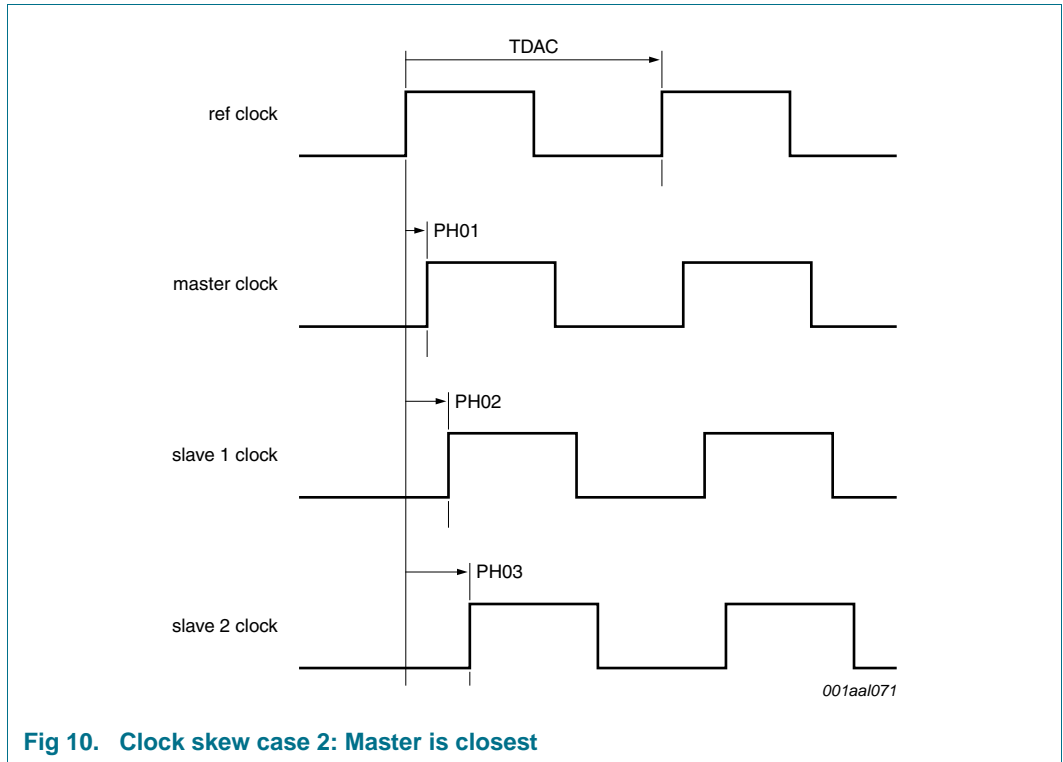


Fig 10. Clock skew case 2: Master is closest

The worst case clock skew is given by $\delta t_2 = PH03 - PH01$.

The minimum allowable trace delay for the MDS signal is given by $\Delta t = \delta t_2$.

In real applications, the master DAC can be anywhere and both conditions must be satisfied: $\delta t_2 < \Delta t_{m\text{ds}} < TDAC - \delta t_1$.

Example:

- clock generator skew = ± 80 ps
- FR4 substrate $\Rightarrow 15$ cm/ns delay
- clock trace length difference = 3 cm and 4 cm
- Output sampling rate = 750 Msps

$$\Rightarrow 200 \text{ ps} + 80 \text{ ps} < \Delta t_{m\text{ds}} < 1333 \text{ ps} - (266 \text{ ps} + 80 \text{ ps})$$

$$\Rightarrow 280 \text{ ps} < \Delta t_{m\text{ds}} < 987 \text{ ps}$$

$$\Rightarrow 4.2 \text{ cm} < L_{m\text{ds}} < 14.8 \text{ cm}$$

10.2.5.4 All slave mode

The external reference is provided by the JESD204A transmitter. All DACs are configured in slave mode.

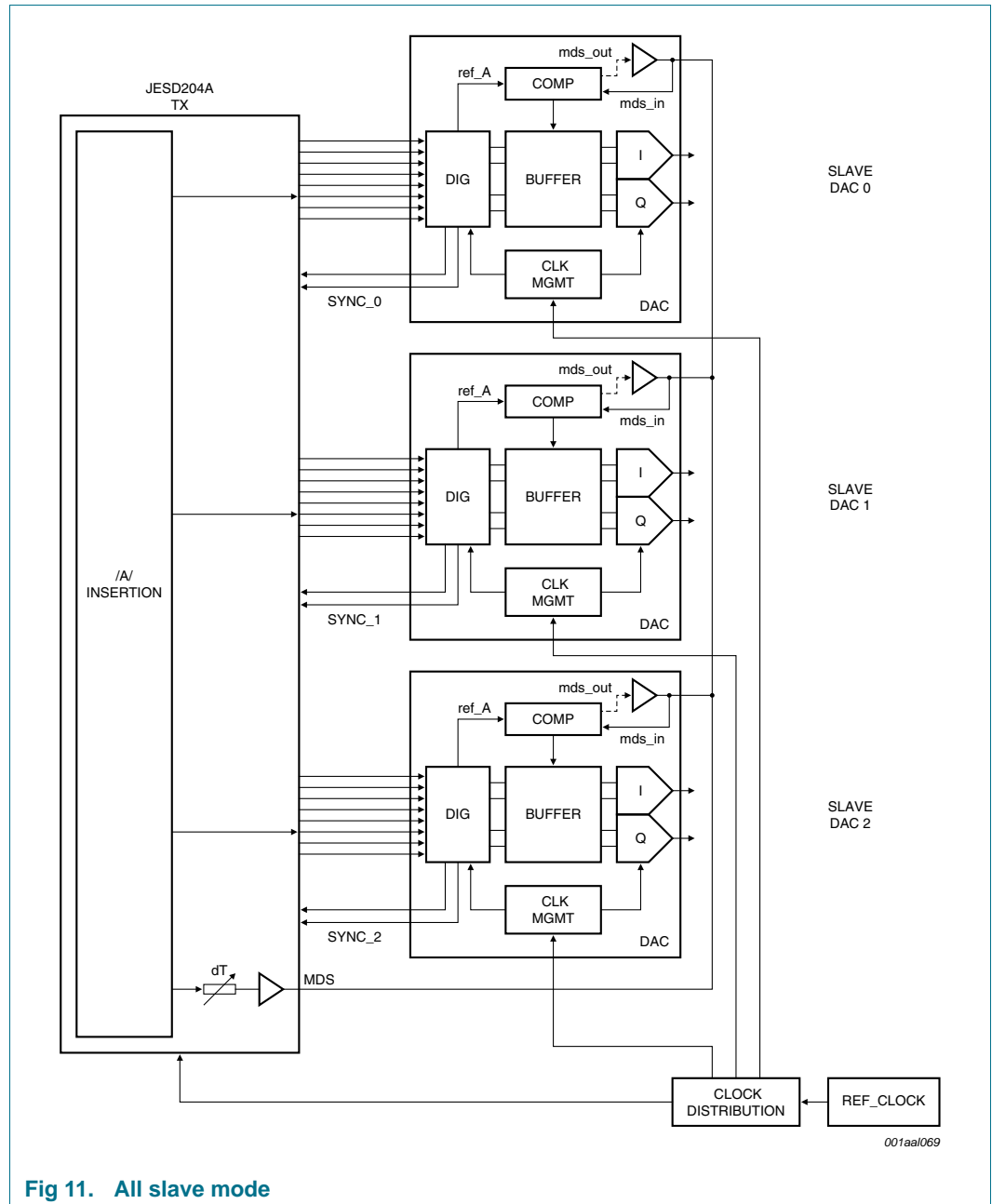


Fig 11. All slave mode

The MDS signal is now driven from the transmitter. It is generated at the end of the inter-lane alignment phase (see the JESD204A standard for details).

The transmitter must also compensate for the DAC latency. Although the DAC has an internal samples delay line, it cannot handle large delays.

In this mode, PCB layout is also important. The following delay equation applies: $\delta t < \Delta t_{m_{ds}} < TDAC - \delta t$, where δt is the clock skew considered close to DAC pins.

10.2.6 Frame assembly

DAC1408D750 supports only $/F/ = 1$, which means that every frame clock period carries one byte per lane. Frame assembly combines the octet of lane_0 with the six MSB bits of lane_1 and reassembles the original 14-bit sample. The same is done for lane_2 and lane_3. Tail bits are dropped.

The frame assembler also handles previously triggered errors.

If scrambling is enabled:

If a nit_err (not-in-table error) or kout_unexp (unexpected control character) occurs in lane_0 and/or lane_1, the previous 14-bit sample is repeated twice for I (lane_0, lane_1). The same is done for Q (lane_2, lane_3).

If scrambling is disabled:

If a nit_err (not-in-table error) or kout_unexp (unexpected control character) occurs in lane_0 and/or lane_1, the previous 14-bit sample is repeated once for I (lane_0, lane_1). The same is done for Q (lane_2, lane_3).

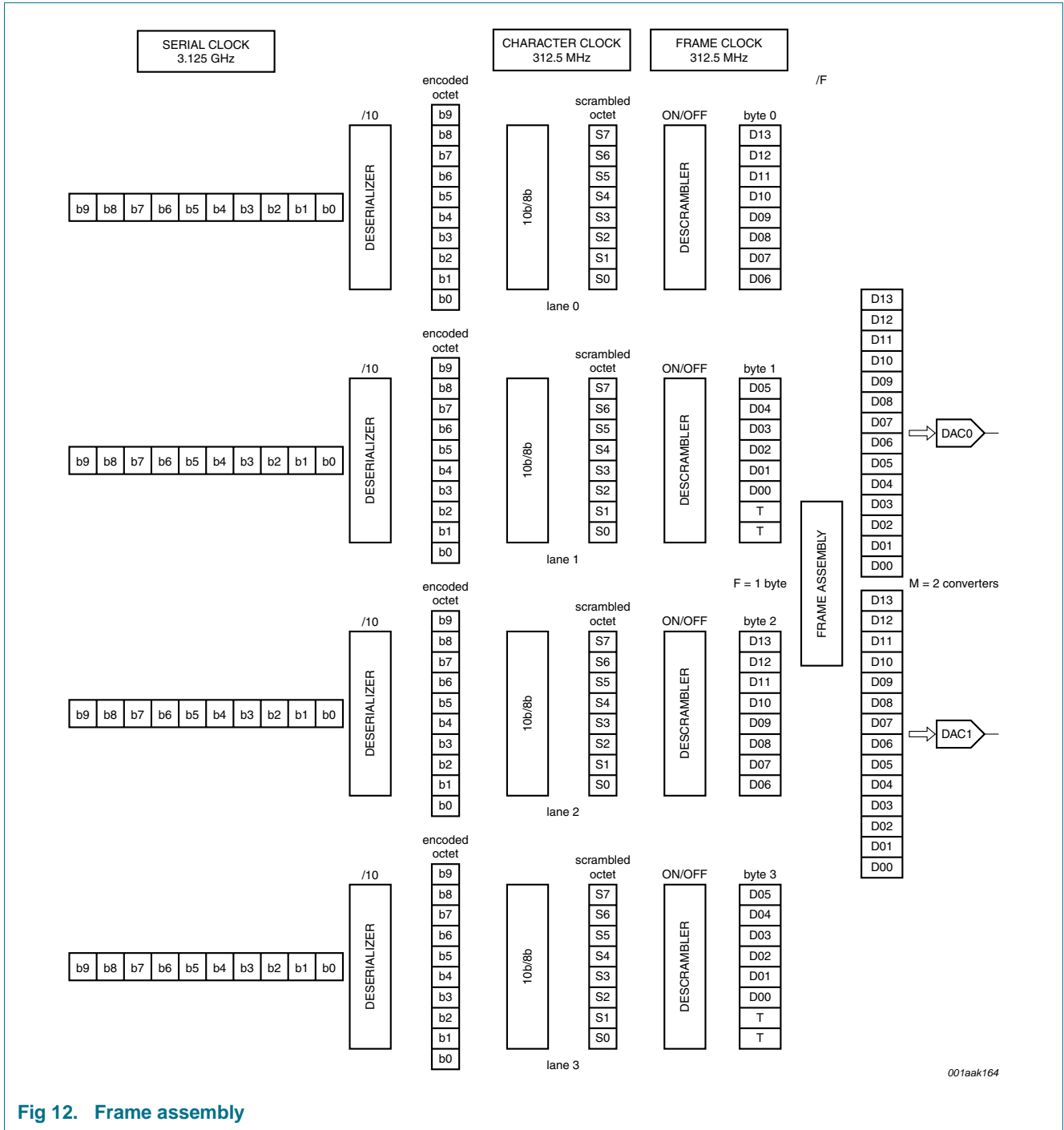


Fig 12. Frame assembly

10.3 Serial Peripheral Interface (SPI)

10.3.1 Protocol description

The DAC1408D750 serial interface is a synchronous serial communication port allowing easy interfacing with many industry microprocessors. It provides access to the registers that define the operating modes of the chip in both Write mode and Read mode.

This interface can be configured as a 3-wire type (SDIO as bidirectional pin) or a 4-wire type (SDIO and SDO as unidirectional pin, input and output port respectively). In both configurations, SCLK acts as the serial clock and SCS_N acts as the serial chip select bar.

Each read/write operation is sequenced by the SCS_N signal and enabled by a LOW assertion to drive the chip with two bytes to five bytes, depending on the content of the instruction byte (see [Table 8](#)).

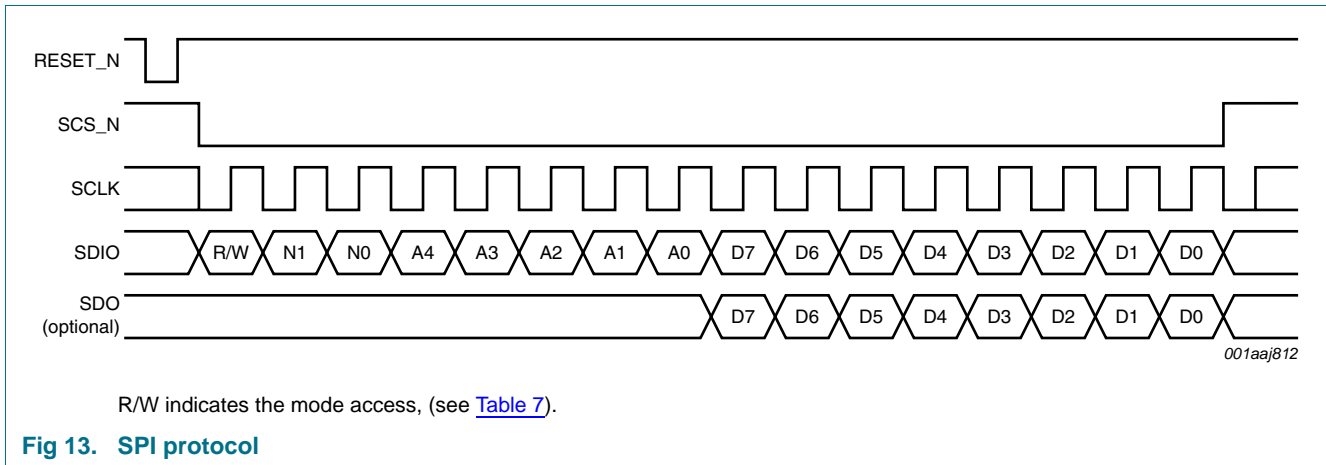


Table 7. Read or Write mode access description

| R/W | Description |
|-----|----------------------|
| 0 | Write mode operation |
| 1 | Read mode operation |

In [Table 8](#) below, N1 and N0 indicate the number of bytes transferred after the instruction byte.

Table 8. Number of bytes to be transferred

| N1 | N0 | Number of bytes transferred |
|----|----|-----------------------------|
| 0 | 0 | 1 |
| 0 | 1 | 2 |
| 1 | 0 | 3 |
| 1 | 1 | 4 |

A[4:0] indicates which register is being addressed. In the case of a multiple transfer, this address points to the first register to be accessed. The address is then internally decreased after each following data phase.

10.3.2 SPI timing description

The SPI interface can operate at a frequency of up to 15 MHz. The SPI timing is shown in [Figure 14](#).

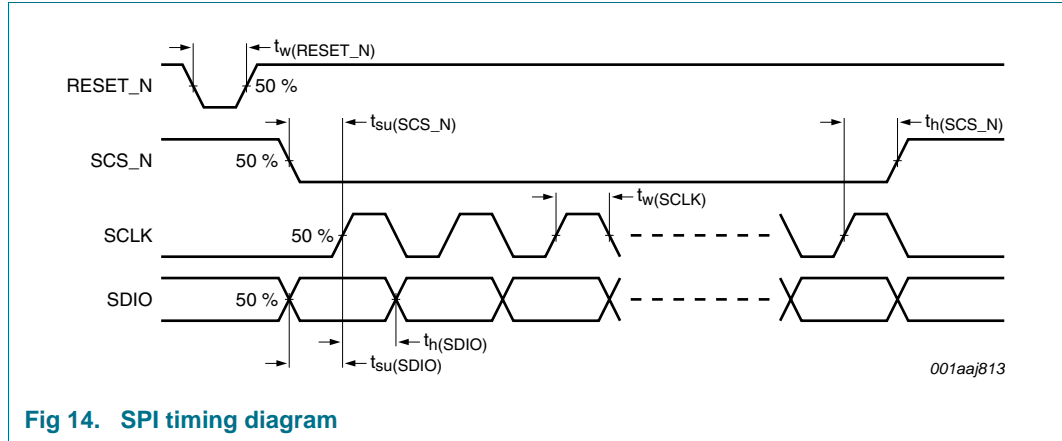


Fig 14. SPI timing diagram

The SPI timing characteristics are given in [Table 9](#).

Table 9. SPI timing characteristics

| Symbol | Parameter | Min | Typ | Max | Unit |
|-------------------------|---------------------|-----|-----|-----|------|
| f_{SCLK} | SCLK frequency | - | - | 15 | MHz |
| $t_w(\text{SCLK})$ | SCLK pulse width | 30 | - | - | ns |
| $t_{su}(\text{SCS_N})$ | SCS_N set-up time | 20 | - | - | ns |
| $t_h(\text{SCS_N})$ | SCS_N hold time | 20 | - | - | ns |
| $t_{su}(\text{SDIO})$ | SDIO set-up time | 10 | - | - | ns |
| $t_h(\text{SDIO})$ | SDIO hold time | 5 | - | - | ns |
| $t_w(\text{RESET_N})$ | RESET_N pulse width | 30 | - | - | ns |

10.4 Clock input

The DAC1408D750 has one differential clock input, CLKINN/CLKINP.

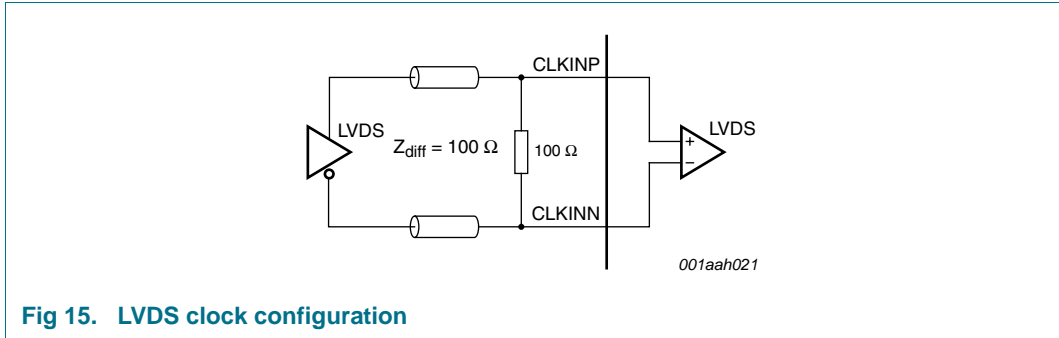


Fig 15. LVDS clock configuration

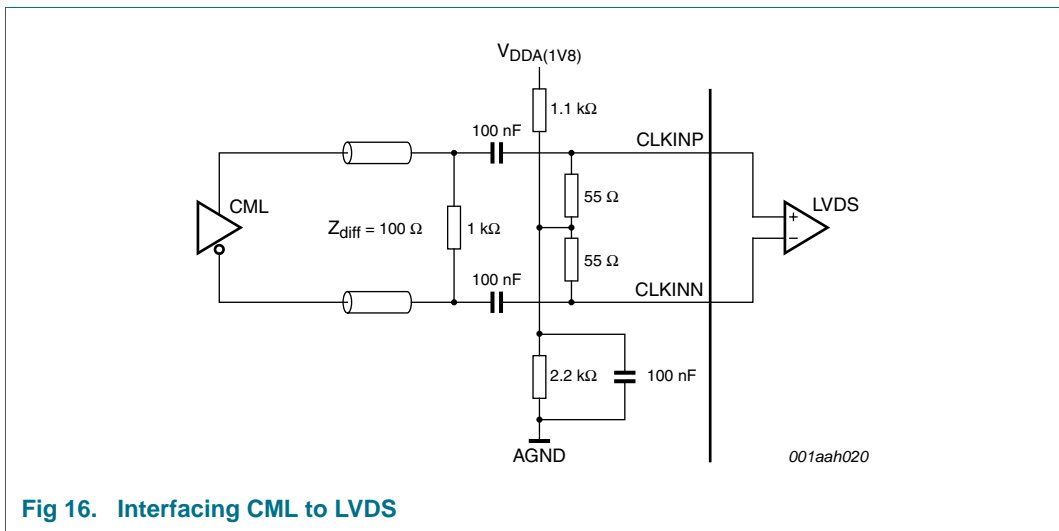


Fig 16. Interfacing CML to LVDS

The DAC1408D750 can operate with a clock frequency up to 312.5 MHz or up to 750 MHz if the internal PLL is bypassed. The clock input can be LVDS (see Figure 15) but it can also be interfaced with CML (see Figure 16). Error free data transition from one internal clock domain to another one is handled by Clock Domain Interface logic.

During the reset phase (RESET_N asserted), the clock must be stable and running. This ensures a proper reset of the complete device.

The device has no embedded power-on-reset feature. Driving the RESET_N pin to set the device to its default state is mandatory.

10.5 FIR filters

The three interpolation FIR filters have a stop band attenuation of at least 80 dBc and a pass band ripple of less than 0,0005 dB.

Table 10. Interpolation filter coefficients

| First interpolation filter | | | Second interpolation filter | | | Third interpolation filter | | |
|----------------------------|-------|-------|-----------------------------|-------|-------|----------------------------|-------|-------|
| Lower | Upper | Value | Lower | Upper | Value | Lower | Upper | Value |
| H(1) | H(55) | -4 | H(1) | H(23) | -2 | H(1) | H(15) | -39 |
| H(2) | H(54) | 0 | H(2) | H(22) | 0 | H(2) | H(14) | 0 |
| H(3) | H(53) | 13 | H(3) | H(21) | 17 | H(3) | H(13) | 273 |
| H(4) | H(52) | 0 | H(4) | H(20) | 0 | H(4) | H(12) | 0 |
| H(5) | H(51) | -34 | H(5) | H(19) | -75 | H(5) | H(11) | -1102 |
| H(6) | H(50) | 0 | H(6) | H(18) | 0 | H(6) | H(10) | 0 |
| H(7) | H(49) | 72 | H(7) | H(17) | 238 | H(7) | H(9) | 4964 |
| H(8) | H(48) | 0 | H(8) | H(16) | 0 | H(8) | - | 8192 |
| H(9) | H(47) | -138 | H(9) | H(15) | -660 | - | - | - |
| H(10) | H(46) | 0 | H(10) | H(14) | 0 | - | - | - |
| H(11) | H(45) | 245 | H(11) | H(13) | 2530 | - | - | - |
| H(12) | H(44) | 0 | H(12) | - | 4096 | - | - | - |
| H(13) | H(43) | -408 | - | - | - | - | - | - |
| H(14) | H(42) | 0 | - | - | - | - | - | - |
| H(15) | H(41) | 650 | - | - | - | - | - | - |
| H(16) | H(40) | 0 | - | - | - | - | - | - |
| H(17) | H(39) | -1003 | - | - | - | - | - | - |
| H(18) | H(38) | 0 | - | - | - | - | - | - |
| H(19) | H(37) | 1521 | - | - | - | - | - | - |
| H(20) | H(36) | 0 | - | - | - | - | - | - |
| H(21) | H(35) | -2315 | - | - | - | - | - | - |
| H(22) | H(34) | 0 | - | - | - | - | - | - |
| H(23) | H(33) | 3671 | - | - | - | - | - | - |
| H(24) | H(32) | 0 | - | - | - | - | - | - |
| H(25) | H(31) | -6642 | - | - | - | - | - | - |
| H(26) | H(30) | 0 | - | - | - | - | - | - |
| H(27) | H(29) | 20756 | - | - | - | - | - | - |
| H(28) | - | 32768 | - | - | - | - | - | - |

10.6 Quadrature modulator and Numerically Controlled Oscillator (NCO)

The quadrature modulator allows the 14-bit I and Q data to be mixed with the carrier signal generated by the NCO.

The frequency of the NCO is programmed over 32 bits and the sign of the sine component can be inverted in order to operate positive or negative, lower or upper single sideband up-conversion.

10.6.1 NCO in 32-bit

When using the NCO, the frequency can be set by the four registers `FREQNCO_LSB`, `FREQNCO_LISB`, `FREQNCO_UI SB` and `FREQNCO_MSB` over 32 bits.

The frequency for the NCO in 32-bit is calculated as follows:

$$f_{NCO} = \frac{M \times f_s}{2^{32}} \quad (1)$$

where M is the decimal representation of `FREQ_NCO[31:0]`.

The phase of the NCO can be set from 0° to 360° by both registers `PHINCO_LSB` and `PHINCO_MSB` over 16 bits.

The default setting is $f_{NCO} = 96$ MHz when $f_s = 640$ Msp/s and the default phase is 0°.

10.6.2 Low-power NCO

When using the low-power NCO, the frequency can be set by the five MSBs of register `FREQNCO_MSB`.

The frequency for the low-power NCO is calculated as follows:

$$f_{NCO} = \frac{M \times f_s}{2^5} \quad (2)$$

where M is the decimal representation of `FREQ_NCO[31:27]`.

The phase of the low-power NCO can be set by the five MSBs of the register `PHINCO_MSB`.

10.6.3 Minus_3dB

During normal use, a full-scale pattern is also full-scale at the output of the DAC. Nevertheless, when the I and Q data are simultaneously close to full-scale, some clipping can occur and the `minus_3dB` function can be used to reduce the gain in the modulator by 3 dB. This is to keep a full-scale range at the output of the DAC without added interferers.

10.7 x / (sin x)

The roll-off effect of the DAC causes a selectable FIR filter to be inserted to compensate for the $(\sin x) / x$ effect. This filter introduces a DC loss of 3.4 dB. The coefficients are represented in [Table 11](#).

Table 11. Inversion filter coefficients

| First interpolation filter | | |
|----------------------------|-------|-------|
| Lower | Upper | Value |
| H(1) | H(9) | 2 |
| H(2) | H(8) | -4 |
| H(3) | H(7) | 10 |
| H(4) | H(6) | -35 |
| H(5) | - | 401 |

10.8 DAC transfer function

The full-scale output current for each DAC is the sum of the two complementary current outputs:

$$I_{O(fs)} = I_{IOUTP} + I_{IOUTN} \tag{3}$$

The output current depends on the digital input data:

$$I_{IOUTP} = I_{O(fs)} \times \left(\frac{DATA}{16383}\right) \tag{4}$$

$$I_{IOUTN} = I_{O(fs)} \times \left(\frac{16383 - DATA}{16383}\right) \tag{5}$$

The setting applied to register COMMON bit DF (register 00h[2]; see [Table 17 “Page 0 register allocation map”](#)) defines whether the DAC1408D750 operates with a binary input or a two’s complement input.

[Table 12](#) shows the output current as a function of the input data, when $I_{O(fs)} = 20$ mA.

Table 12. DAC transfer function

| Data | I13/Q13 to I0/Q0 | | IOUTnP | IOUTnN |
|------|-------------------|-------------------|--------|--------|
| | Binary | Two’s complement | | |
| 0 | 00 0000 0000 0000 | 10 0000 0000 0000 | 0 mA | 20 mA |
| ... | ... | ... | ... | ... |
| 2048 | 10 0000 0000 0000 | 00 0000 0000 0000 | 10 mA | 10 mA |
| ... | ... | ... | ... | ... |
| 4095 | 11 1111 1111 1111 | 01 1111 1111 1111 | 20 mA | 0 mA |

10.9 Full-scale current

10.9.1 Regulation

The DAC1408D750 reference circuitry integrates an internal band gap reference voltage which delivers a 1.25 V reference to the GAPOUT pin. It is recommended to decouple pin GAPOUT using a 100 nF capacitor.

The reference current is generated via an external resistor of $909\ \Omega$ (1 %) connected to pin VIRES. A control amplifier sets the appropriate full-scale current ($I_{O(fs)}$) for both DACs (see [Figure 17](#)).

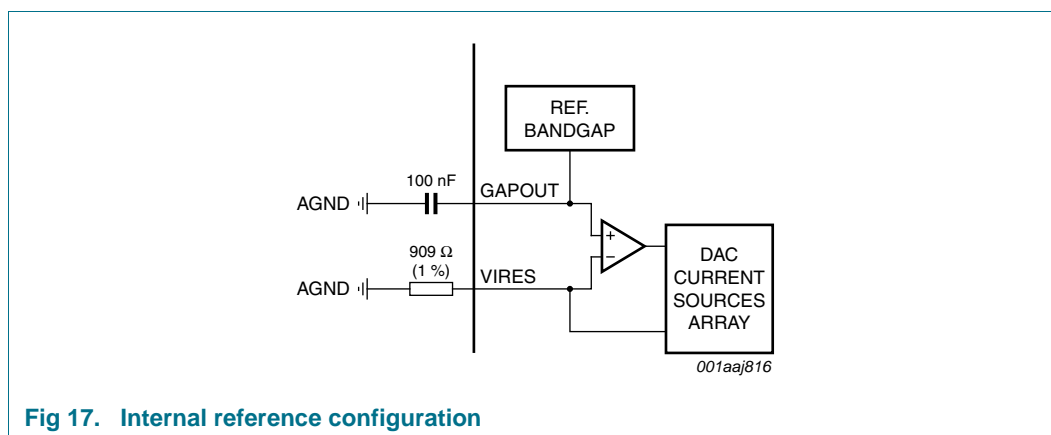


Fig 17. Internal reference configuration

This configuration is optimum for temperature drift compensation because the band gap reference voltage can be matched to the voltage across the feedback resistor.

10.9.1.1 External regulation

The DAC current can also be set by applying an external reference voltage to the non-inverting input pin GAPOUT and disabling the internal band gap reference voltage with bit GAP_PD (register 00h[0]; see [Table 18 “COMMON register \(address 00h\) bit description”](#)).

10.9.2 Full-scale current adjustment

The default full-scale current ($I_{O(fs)}$) is 20 mA but further adjustments can be made by the user to both DACs independently using the serial interface from 1.6 mA to 22 mA, $\pm 10\%$.

The settings applied to DAC_A_GAIN_COARSE[3:0] (register 0Ah; see [Table 28 “DAC_A_CFG_2 register \(address 0Ah\) bit description”](#) and register 0Bh; see [Table 29 “DAC_A_CFG_3 register \(address 0Bh\) bit description”](#)) and DAC_B_GAIN_COARSE[3:0] (register 0Dh; see [Table 31 “DAC_B_CFG_2 register \(address 0Dh\) bit description”](#) and register 0Eh; see [Table 32 “DAC_B_CFG_3 register \(address 0Eh\) bit description”](#)) define the coarse variation of the full-scale current (see [Table 13](#)).

Table 13. $I_{O(fs)}$ coarse adjustment

Default settings are shown highlighted.

| DAC_GAIN_COARSE[3:0] | | $I_{O(fs)}$ (mA) |
|----------------------|-------------|------------------|
| Decimal | Binary | |
| 0 | 0000 | 1.6 |
| 1 | 0001 | 3.0 |
| 2 | 0010 | 4.4 |
| 3 | 0011 | 5.8 |
| 4 | 0100 | 7.2 |
| 5 | 0101 | 8.6 |
| 6 | 0110 | 10.0 |
| 7 | 0111 | 11.4 |
| 8 | 1000 | 12.8 |
| 9 | 1001 | 14.2 |
| 10 | 1010 | 15.6 |
| 11 | 1011 | 17.0 |
| 12 | 1100 | 18.5 |
| 13 | 1101 | 20.0 |
| 14 | 1110 | 21.0 |
| 15 | 1111 | 22.0 |

The settings applied to DAC_A_GAIN_FINE[5:0] (register 0Ah; see [Table 28](#) “DAC_A_CFG_2 register (address 0Ah) bit description”) and to DAC_B_GAIN_FINE[5:0] (register 0Dh; see [Table 31](#) “DAC_B_CFG_2 register (address 0Dh) bit description”) define the fine variation of the full-scale current (see [Table 14](#)).

Table 14. $I_{O(fs)}$ fine adjustment

Default settings are shown highlighted.

| DAC_GAIN_FINE[5:0] | | Delta $I_{O(fs)}$ |
|--------------------|------------------|-------------------|
| Decimal | Two's complement | |
| -32 | 10 0000 | -10 % |
| ... | ... | ... |
| 0 | 00 0000 | 0 |
| ... | ... | ... |
| 31 | 01 1111 | +10 % |

The coding of the fine gain adjustment is two's complement.

10.10 Digital offset correction

When the DAC1408D750 analog output is DC connected to the next stage, the digital offset correction can be used to adjust the common-mode level at the output of the DAC. It adds an offset at the end of the digital part, just before the DAC.

The settings applied to DAC_A_OFFSET[11:0] (register 09h; see [Table 27](#) “DAC_A_CFG_1 register (address 09h) bit description”) and register 0Bh; see [Table 29](#) “DAC_A_CFG_3 register (address 0Bh) bit description”) and to “DAC_B_OFFSET[11:0]”

(register 0Ch; see [Table 30 “DAC_B_CFG_1 register \(address 0Ch\) bit description”](#) and register 0Eh; see [Table 32 “DAC_B_CFG_3 register \(address 0Eh\) bit description”](#)) define the range of variation of the digital offset (see [Table 15](#)).

Table 15. Digital offset adjustment
 Default settings are shown highlighted.

| DAC_OFFSET[11:0] | | Offset applied |
|------------------|-----------------------|----------------|
| Decimal | Two's complement | |
| -2048 | 1000 0000 0000 | -4096 |
| -2047 | 1000 0000 0001 | -4094 |
| ... | ... | ... |
| -1 | 1111 1111 1111 | -2 |
| 0 | 0000 0000 0000 | 0 |
| +1 | 0000 0000 0001 | +2 |
| ... | ... | ... |
| 2046 | 0111 1111 1110 | +4092 |
| 2047 | 0111 1111 1111 | +4094 |

10.11 Analog output

The DAC1408D750 has two output channels each of which produces two complementary current outputs. These allow the even-order harmonics and noise to be reduced. The pins are IOUTAP/IOUTAN and IOUTBP/IOUTBN respectively and need to be connected via a load resistor R_L to the 3.3 V analog power supply ($V_{DDA(3V3)}$).

The equivalent analog output circuit of one DAC is shown in [Figure 18](#). This circuit consists of a parallel combination of NMOS current sources and their associated switches for each segment.

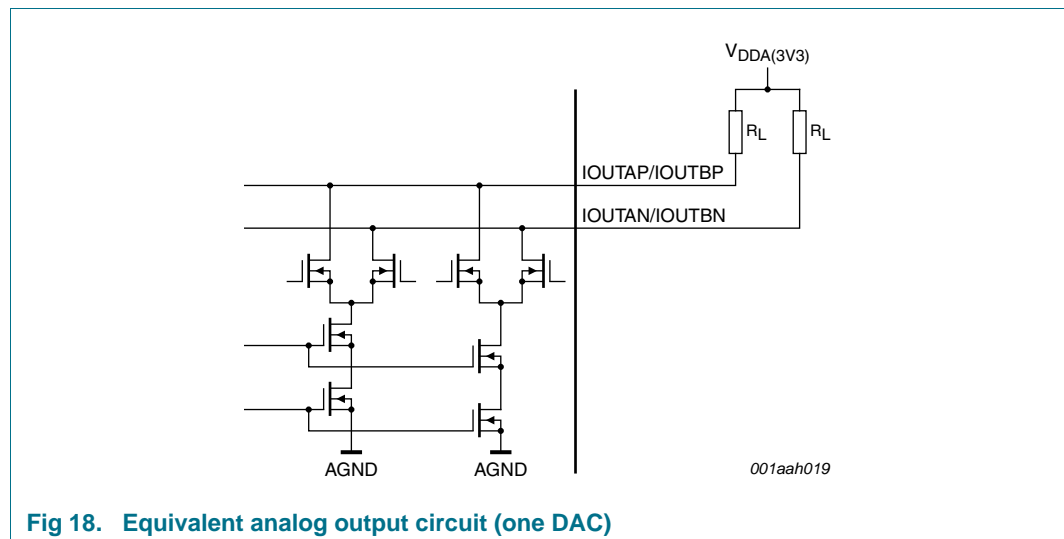


Fig 18. Equivalent analog output circuit (one DAC)

The cascode source configuration increases the output impedance of the source, thus improving the dynamic performance of the DAC by introducing less distortion.

The device can provide an output level ($V_{o(p-p)}$) of up to 2 V, depending on the application, the following stages and the targeted performances.

10.12 Auxiliary DACs

The DAC1408D750 integrates two auxiliary DACs that can be used to compensate for any offset between the DAC and the next stage in the transmission path.

Both auxiliary DACs have a 10-bit resolution and are current sources (referenced to ground).

$$I_{O(AUX)} = I_{AUXP} + I_{AUXN} \tag{6}$$

The output current depends on the auxiliary DAC data:

$$AUXP = I_{O(AUX)} \times \left(\frac{AUX[9:0]}{1023} \right) \tag{7}$$

$$AUXN = I_{O(AUX)} \times \left(\frac{(1023 - AUX[9:0])}{1023} \right) \tag{8}$$

[Table 16](#) shows the output current as a function of the auxiliary DAC data.

Table 16. Auxiliary DAC transfer function

Default settings are shown highlighted.

| Data | AUX[9:0] (binary) | I _{AUXP} | I _{AUXN} |
|------------|---------------------|-------------------|-------------------|
| 0 | 00 0000 0000 | 0 mA | 2.2 mA |
| ... | ... | ... | ... |
| 512 | 10 0000 0000 | 1.1 mA | 1.1 mA |
| ... | ... | ... | ... |
| 1023 | 11 1111 1111 | 2.2 mA | 0 mA |

10.13 Output configuration

10.13.1 Basic output configuration

The use of a differentially-coupled transformer output provides optimum distortion performance (see [Figure 19](#)). In addition, it helps to match the impedance and provides electrical isolation.

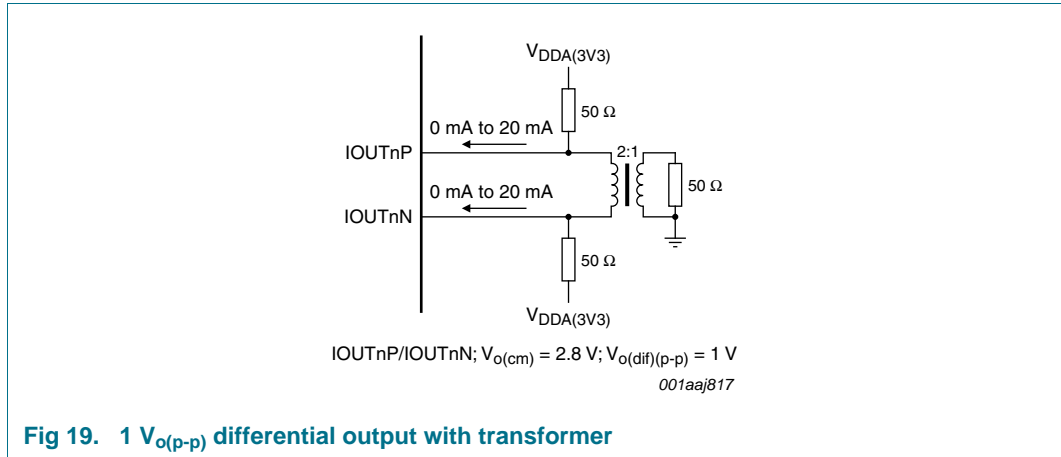


Fig 19. 1 $V_{O(p-p)}$ differential output with transformer

The DAC1408D750 can operate at a $V_{O(p-p)}$ of 2 V differential outputs. In this configuration, it is recommended to connect the center tap of the transformer to a 62 Ω resistor connected to the 3.3 V analog power supply in order to adjust the DC common-mode to approximately 2.7 V (see [Figure 20](#)).

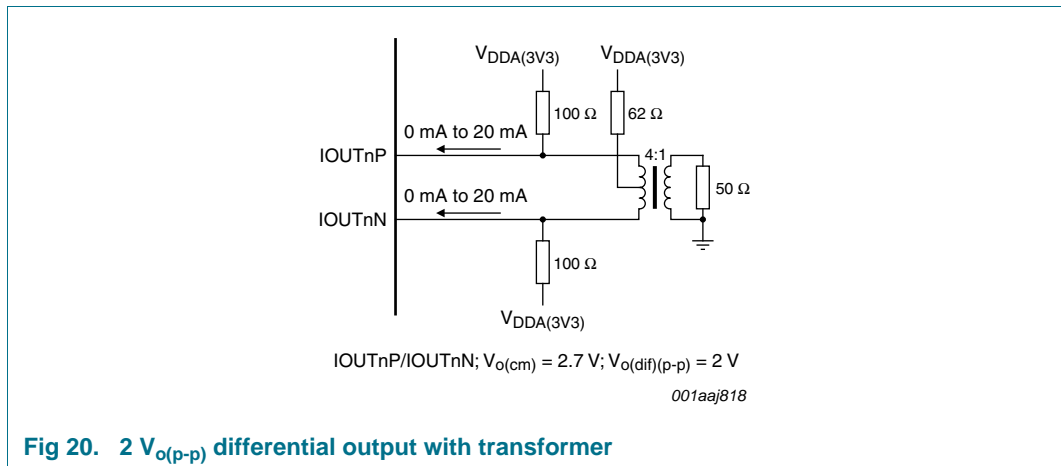


Fig 20. 2 $V_{O(p-p)}$ differential output with transformer

10.13.2 DC interface to an Analog Quadrature Modulator (AQM)

When the system operation requires to keep the DC component of the spectrum, the DAC1408D750 must use a DC interface to connect to an AQM. In this case, the offset compensation for LO cancellation can be made with the use of the digital offset control in the DAC.

Figure 21 is an example of a connection to an AQM with a common-mode input level ($V_{i(cm)}$) of 1.7 V.

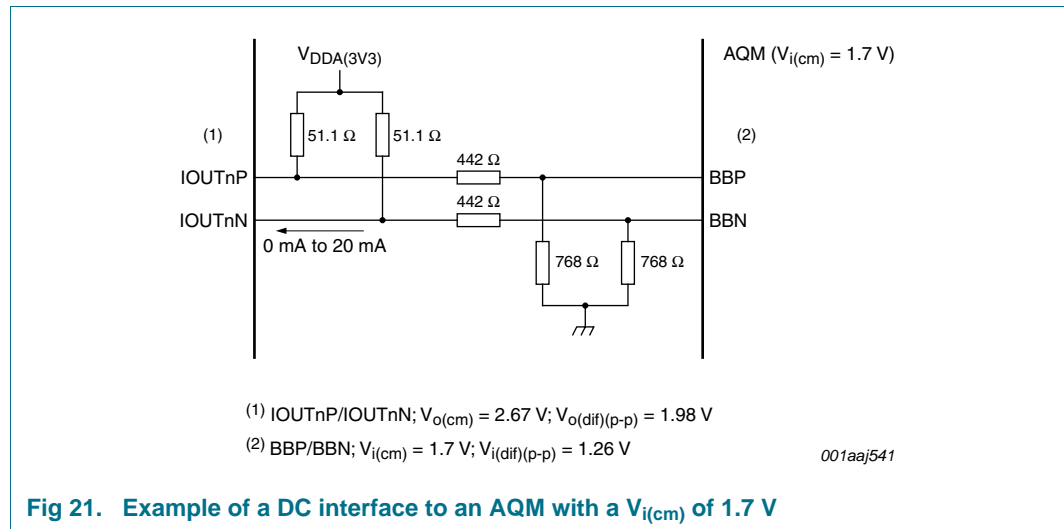


Fig 21. Example of a DC interface to an AQM with a $V_{i(cm)}$ of 1.7 V

Figure 22 is an example of a connection to an AQM with a common-mode input level ($V_{i(cm)}$) of 3.3 V.

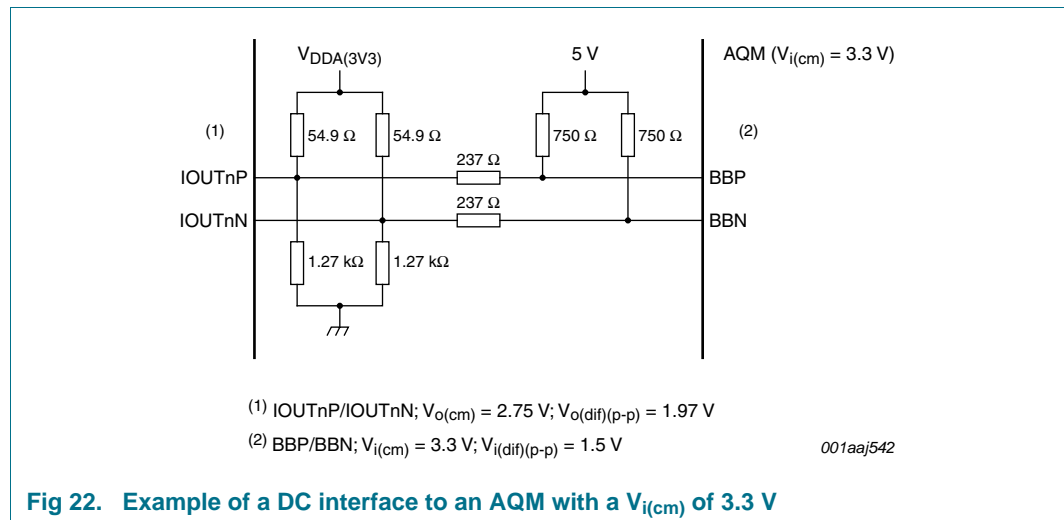


Fig 22. Example of a DC interface to an AQM with a $V_{i(cm)}$ of 3.3 V

The auxiliary DACs can be used to control the offset in a precise range or with precise steps.

Figure 23 is an example of a DC interface connected to an AQM with a common-mode input level ($V_{i(cm)}$) of 1.7 V when using auxiliary DACs.

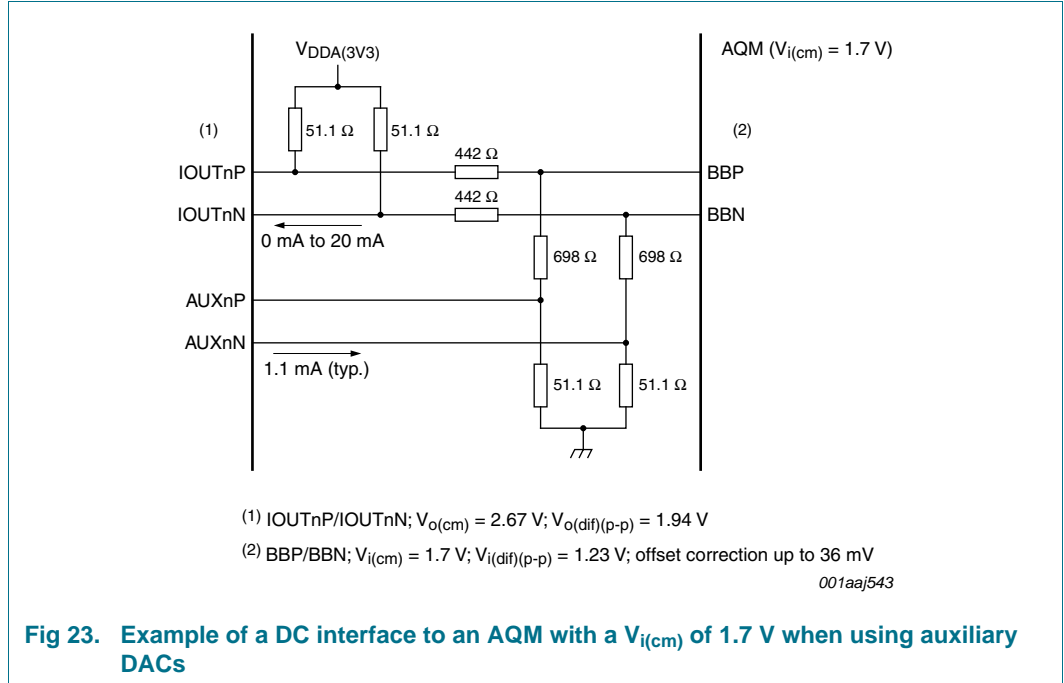
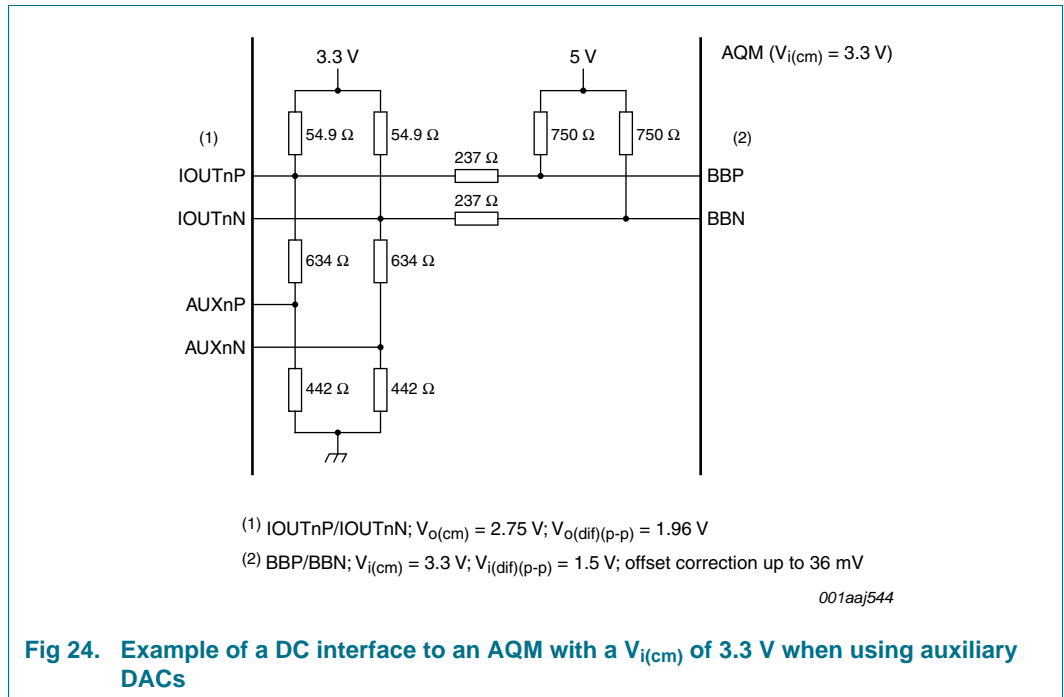


Figure 24 is an example of a DC interface connected to an AQM with a common-mode input level ($V_{i(cm)}$) of 3.3 V when using auxiliary DACs.



The constraints to adjusting the interface are the output compliance range of the DAC and the auxiliary DACs, the input common-mode level of the AQM, and the range of offset correction.

10.13.3 AC interface to an Analog Quadrature Modulator (AQM)

When the AQM common-mode voltage is close to ground, the DAC1408D750 must be AC-coupled and the auxiliary DACs are needed for offset correction.

Figure 25 is an example of a connection to an AQM with a common-mode input level ($V_{i(cm)}$) of 0.5 V when using auxiliary DACs.

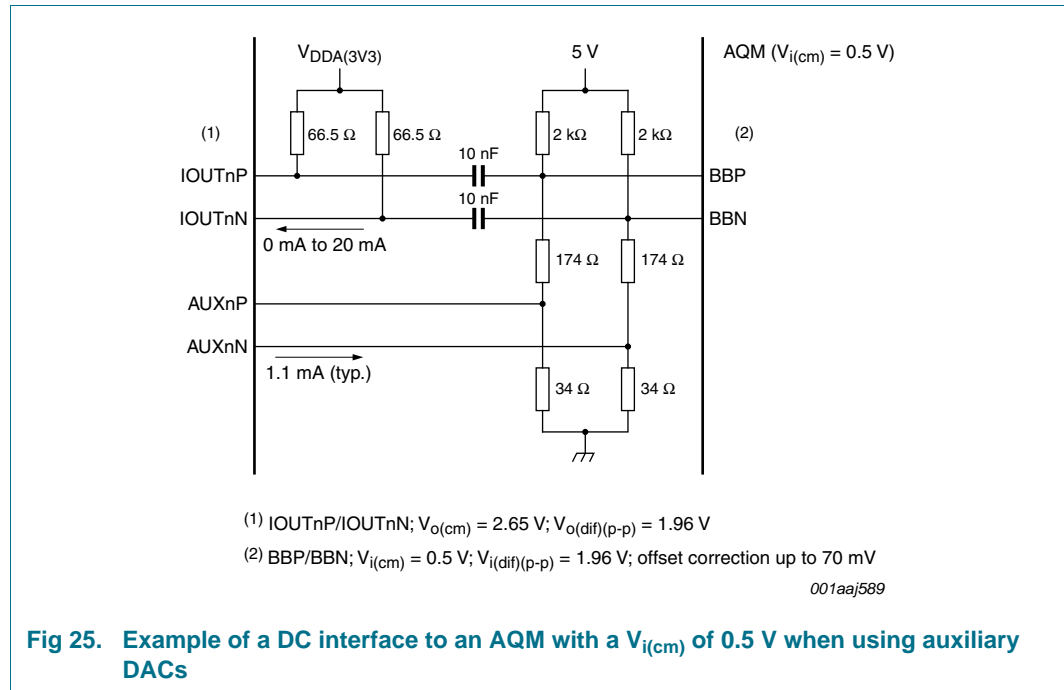


Fig 25. Example of a DC interface to an AQM with a $V_{i(cm)}$ of 0.5 V when using auxiliary DACs

10.13.4 Phase correction

The Analog Quadrature Modulator which follows the DACs may have a phase imbalance which results in undesired sidebands. By adjusting the phase between the I and Q channels, the spur can be reduced.

Without compensation the I and Q have a phase difference of $\Pi / 2$ (90°). The registers PHASECORR_CNTRL0 and PHASECORR_CNTRL1 located in register page 0 allow a phase variation from 75.7° to 104.3° . The two registers define a signed value that ranges from -512 to $+511$. The resulting phase compensation (in radians) is given by the equation: $\text{PHASE_CORR}[9:0] / 2048$.

10.14 Power and grounding

The power supplies should be decoupled with the following ground pins to optimize the decoupling:

- $V_{\text{DDA}(1V8)}$: pin 38 with pin 37; pin 44 with pin 43; pin 11 with pin 12; pin 17 with pin 18; pin 32 with pin 31

10.15 Configuration interface

10.15.1 Register description

DAC1408D750 implements indirect addressing using a page access method. The page-address is located at address 0x1F and is by default 0x00, which selects page 0 as the default page. For example, to access registers which configure the deserializer, one must first activate page 4 by writing 0x04 to the page-address 0x1F.

The DAC1408D750 contains six different pages.

The device has no embedded power-on-reset feature. Driving the RESET_N pin to set the device to its default state is mandatory.

10.15.2 Detailed descriptions of registers

The register information has been provided in page form accompanied by a detailed description for each bit in the tables following the register allocation map of each page.

10.15.2.1 Page 0 allocation map description

Table 17. Page 0 register allocation map

| Address | Register name | R/W | Bit definition | | | | | | | | | Default | | |
|---------|---------------|------------------|----------------|------------------------|-------------|-------------------|----------------------|-------------------|----------------|------------------|--------------|----------|----------|-----|
| | | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Bin | Hex | | |
| 0 | 00h | COMMON | R/W | SPI_3W | SPI_RST | - | - | - | DF | PD_ALL | PD_GAP | 10000100 | 84h | |
| 1 | 01h | TXCFG | R/W | NCO_EN | NCO_LP_SEL | INV_SINE_EN | MODE[2:0] | | | INT_FIR[1:0] | | 00000001 | 01h | |
| 2 | 02h | PLLCFG | R/W | PLL_PD | - | - | PLL_DIV[1:0] | | PLL_PHASE[1:0] | PLL_POL | 00000000 | 00h | | |
| 3 | 03h | FREQNCO_LSB | R/W | FREQ_NCO[7:0] | | | | | | | | | 01100110 | 66h |
| 4 | 04h | FREQNCO_LISB | R/W | FREQ_NCO[15:8] | | | | | | | | | 01100110 | 66h |
| 5 | 05h | FREQNCO_UISB | R/W | FREQ_NCO[23:16] | | | | | | | | | 01100110 | 66h |
| 6 | 06h | FREQNCO_MSB | R/W | FREQ_NCO[31:24] | | | | | | | | | 00100110 | 26h |
| 7 | 07h | PHINCO_LSB | R/W | PH_NCO[7:0] | | | | | | | | | 00000000 | 00h |
| 8 | 08h | PHINCO_MSB | R/W | PH_NCO[15:8] | | | | | | | | | 00000000 | 00h |
| 9 | 09h | DAC_A_CFG_1 | R/W | DAC_A_PD | DAC_A_SLEEP | DAC_A_OFFSET[5:0] | | | | | | 00000000 | 00h | |
| 10 | 0Ah | DAC_A_CFG_2 | R/W | DAC_A_GAIN_COARSE[1:0] | | | DAC_A_GAIN_FINE[5:0] | | | | | | 01000000 | 40h |
| 11 | 0Bh | DAC_A_CFG_3 | R/W | DAC_A_GAIN_COARSE[3:2] | | | DAC_A_OFFSET[11:6] | | | | | | 11000000 | C0h |
| 12 | 0Ch | DAC_B_CFG_1 | R/W | DAC_B_PD | DAC_B_SLEEP | DAC_B_OFFSET[5:0] | | | | | | 00000000 | 00h | |
| 13 | 0Dh | DAC_B_CFG_2 | R/W | DAC_B_GAIN_COARSE[1:0] | | | DAC_B_GAIN_FINE[5:0] | | | | | | 01000000 | 40h |
| 14 | 0Eh | DAC_B_CFG_3 | R/W | DAC_B_GAIN_COARSE[3:2] | | | DAC_B_OFFSET[11:6] | | | | | | 11000000 | C0h |
| 15 | 0Fh | DAC_CFG | R/W | - | - | - | - | - | - | MINUS_3DB | NOISE_SHAPER | 00000000 | 00h | |
| 17 | 11h | DAC_CURRENT_0 | R/W | - | - | - | - | DAC_DIG_BIAS[2:0] | | | - | 00000110 | 06h | |
| 18 | 12h | DAC_CURRENT_1 | R/W | - | - | - | - | DAC_MST_BIAS[2:0] | | | - | 00000110 | 06h | |
| 19 | 13h | DAC_CURRENT_2 | R/W | DAC_DRV_BIAS[2:0] | | | - | DAC_SLV_BIAS[2:0] | | | - | 01100110 | 66h | |
| 20 | 14h | DAC_CURRENT_3 | R/W | DAC_CK_BIAS[2:0] | | | - | DAC_CAS_BIAS[2:0] | | | - | 01100110 | 66h | |
| 21 | 15h | DAC_SEL_PH_FINE | R/W | - | - | - | - | - | - | SEL_PH_FINE[1:0] | | 00000010 | 02h | |
| 22 | 16h | PHASECORR_CNTRL0 | R/W | PHASE_CORR[7:0] | | | | | | | | | 00000000 | 00h |
| 23 | 17h | PHASECORR_CNTRL1 | R/W | PHASE_CORR_ENABLE | - | - | - | - | - | PHASE_CORR[9:8] | | 00000000 | 00h | |
| 26 | 1Ah | DAC_A_AUX_MSB | R/W | AUX_A[9:2] | | | | | | | | | 10000000 | 80h |
| 27 | 1Bh | DAC_A_AUX_LSB | R/W | AUX_A_PD | - | - | - | - | - | AUX_A[1:0] | | 00000000 | 00h | |

Table 17. Page 0 register allocation map ...continued

| Address | Register name | R/W | Bit definition | | | | | | | | Default | | |
|---------|---------------|---------------|----------------|------------|----|----|----|----|-----------|------------|----------|----------|-----|
| | | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Bin | Hex | |
| 28 | 1Ch | DAC_B_AUX_MSB | R/W | AUX_B[9:2] | | | | | | | | 10000000 | 80h |
| 29 | 1Dh | DAC_B_AUX_LSB | R/W | AUX_B_PD | - | - | - | - | - | AUX_B[1:0] | | 00000000 | 00h |
| 31 | 1Fh | PAGE_ADDRESS | R/W | - | - | - | - | - | PAGE[2:0] | | 00000000 | 00h | |

10.15.2.2 Page 0 bit definition detailed description

Please refer to [Table 17](#) for a register overview for page 0. In the following tables, all the values emphasized in bold are the default values.

Table 18. COMMON register (address 00h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|---------|--------|----------|--|
| 7 | SPI_3W | R/W | | serial interface bus type |
| | | | 0 | 4 wire SPI |
| | | | 1 | 3 wire SPI |
| 6 | SPI_RST | R/W | | serial interface reset |
| | | | 0 | no reset |
| | | | 1 | performs a reset on all registers except 0x00 |
| 2 | DF | R/W | | data format |
| | | | 0 | signed (two's compliment) format |
| | | | 1 | unsigned format |
| 1 | PD_ALL | R/W | | power-down |
| | | | 0 | no action |
| | | | 1 | all circuits (digital and analog) are switched off |
| 0 | GAP_PD | R/W | | internal band gap power-down |
| | | | 0 | no action |
| | | | 1 | internal band gap references are switched off |

Table 19. TXCFG register (address 01h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------|--------|------------|--|
| 7 | NCO_EN | R/W | | NCO |
| | | | 0 | disabled (the NCO phase is reset to 0) |
| | | | 1 | enabled |
| 6 | NCO_LP_SEL | R/W | | low-power NCO |
| | | | 0 | NCO may use all 32 bits |
| | | | 1 | NCO frequency and phase given by the five MSBs of the registers 06h and 08h respectively |
| 5 | INV_SINE_EN | R/W | | $x / (\sin x)$ function |
| | | | 0 | disabled |
| | | | 1 | enabled |
| 4 to 2 | MODE[2:0] | R/W | | modulation |
| | | | 000 | dual DAC: no modulation |
| | | | 001 | positive upper single sideband up-conversion |
| | | | 010 | positive lower single sideband up-conversion |
| | | | 011 | negative upper single sideband up-conversion |
| | | | 100 | negative lower single sideband up-conversion |

Table 19. TXCFG register (address 01h) bit description ...continued

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------|--------|-----------|------------------|
| 1 to 0 | INT_FIR[1:0] | R/W | | interpolation |
| | | | 00 | no interpolation |
| | | | 01 | 2× |
| | | | 10 | 4× |
| | | | 11 | 8× |

Table 20. PLLCFG register (address 02h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------|--------|-----------|-----------------------------|
| 7 | PLL_PD | R/W | | PLL |
| | | | 0 | switched on |
| | | | 1 | switched off |
| 6 | - | R/W | 0 | undefined |
| 5 | - | R/W | 0 | must be written with '0' |
| 4 to 3 | PLL_DIV[1:0] | R/W | | PLL divider factor |
| | | | 00 | 2 |
| | | | 01 | 4 |
| | | | 10 | 8 |
| 2 to 1 | PLL_PHASE[1:0] | R/W | | PLL phase shift of f_s |
| | | | 00 | 0° |
| | | | 01 | 120° |
| | | | 10 | 240° |
| | | | 11 | undefined |
| 0 | PLL_POL | R/W | | clock edge of DAC (f_s) |
| | | | 0 | normal |
| | | | 1 | inverted |

Table 21. FREQNCO_LSB register (address 03h) bit description

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-------|--|
| 7 to 0 | FREQ_NCO[7:0] | R/W | 66h | lower 8 bits for the NCO frequency setting |

Table 22. FREQNCO_LISB register (address 04h) bit description

| Bit | Symbol | Access | Value | Description |
|--------|----------------|--------|-------|---|
| 7 to 0 | FREQ_NCO[15:8] | R/W | 66h | lower intermediate 8 bits for the NCO frequency setting |

Table 23. FREQNCO_UISB register (address 05h) bit description

| Bit | Symbol | Access | Value | Description |
|--------|-----------------|--------|-------|---|
| 7 to 0 | FREQ_NCO[23:16] | R/W | 66h | upper intermediate 8 bits for the NCO frequency setting |

Table 24. FREQNCO_MSB register (address 06h) bit description

| Bit | Symbol | Access | Value | Description |
|--------|-----------------|--------|-------|---|
| 7 to 0 | FREQ_NCO[31:24] | R/W | 26h | most significant 8 bits for the NCO frequency setting |

Table 25. PHINCO_LSB register (address 07h) bit description

| Bit | Symbol | Access | Value | Description |
|--------|-------------|--------|-------|--|
| 7 to 0 | PH_NCO[7:0] | R/W | 00h | lower 8 bits for the NCO phase setting |

Table 26. PHINCO_MSB register (address 08h) bit description

| Bit | Symbol | Access | Value | Description |
|--------|--------------|--------|-------|---|
| 7 to 0 | PH_NCO[15:8] | R/W | 00h | most significant 8 bits for the NCO phase setting |

Table 27. DAC_A_CFG_1 register (address 09h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|----------|-----------------------------------|
| 7 | DAC_A_PD | R/W | | DAC A power |
| | | | 0 | on |
| | | | 1 | off |
| 6 | DAC_A_SLEEP | R/W | | DAC A Sleep mode |
| | | | 0 | disabled |
| | | | 1 | enabled |
| 5 to 0 | DAC_A_OFFSET[5:0] | R/W | 00h | lower 6 bits for the DAC A offset |

Table 28. DAC_A_CFG_2 register (address 0Ah) bit description

| Bit | Symbol | Access | Value | Description |
|--------|------------------------|--------|-------|---|
| 7 to 6 | DAC_A_GAIN_COARSE[1:0] | R/W | 1h | least significant 2 bits for the DAC A gain setting for coarse adjustment |
| 5 to 0 | DAC_A_GAIN_FINE[5:0] | R/W | 00h | the 6 bits for the DAC A gain setting for fine adjustment |

Table 29. DAC_A_CFG_3 register (address 0Bh) bit description

| Bit | Symbol | Access | Value | Description |
|--------|------------------------|--------|-------|--|
| 7 to 6 | DAC_A_GAIN_COARSE[3:2] | R/W | 3h | most significant 2 bits for the DAC A gain setting for coarse adjustment |
| 5 to 0 | DAC_A_OFFSET[11:6] | R/W | 00h | most significant 6 bits for the DAC A offset |

Table 30. DAC_B_CFG_1 register (address 0Ch) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|----------|-----------------------------------|
| 7 | DAC_B_PD | R/W | | DAC B power |
| | | | 0 | on |
| | | | 1 | off |
| 6 | DAC_B_SLEEP | R/W | | DAC B Sleep mode |
| | | | 0 | disabled |
| | | | 1 | enabled |
| 5 to 0 | DAC_B_OFFSET[5:0] | R/W | 00h | lower 6 bits for the DAC B offset |

Table 31. DAC_B_CFG_2 register (address 0Dh) bit description

| Bit | Symbol | Access | Value | Description |
|--------|------------------------|--------|-------|---|
| 7 to 6 | DAC_B_GAIN_COARSE[1:0] | R/W | 1h | least significant 2 bits for the DAC B gain setting for coarse adjustment |
| 5 to 0 | DAC_B_GAIN_FINE[5:0] | R/W | 00h | the 6 bits for the DAC B gain setting for fine adjustment |

Table 32. DAC_B_CFG_3 register (address 0Eh) bit description

| Bit | Symbol | Access | Value | Description |
|--------|------------------------|--------|-------|--|
| 7 to 6 | DAC_B_GAIN_COARSE[3:2] | R/W | 3h | most significant 2 bits for the DAC B gain setting for coarse adjustment |
| 5 to 0 | DAC_B_OFFSET[11:6] | R/W | 00h | most significant 6 bits for the DAC B offset |

Table 33. DAC_CFG register (address 0Fh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|--------------|--------|----------|-----------------|
| 1 | MINUS_3DB | R/W | | NCO gain |
| | | | 0 | unity |
| | | | 1 | -3 dB |
| 0 | NOISE_SHAPER | R/W | | noise shaper |
| | | | 0 | disabled |
| | | | 1 | enabled |

Table 34. DAC_CURRENT_0 register (address 11h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|-------|--|
| 3 to 1 | DAC_DIG_BIAS[2:0] | R/W | 3h | bias current control (see Table 46) |

Table 35. DAC_CURRENT_1 register (address 12h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|-------|--|
| 3 to 1 | DAC_MST_BIAS[2:0] | R/W | 3h | bias current control (see Table 46) |

Table 36. DAC_CURRENT_2 register (address 13h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|-------|--|
| 7 to 5 | DAC_DRV_BIAS[2:0] | R/W | 3h | bias current control (see Table 46) |
| 3 to 1 | DAC_SLV_BIAS[2:0] | R/W | 3h | bias current control (see Table 46) |

Table 37. DAC_CURRENT_3 register (address 14h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|-------|--|
| 7 to 5 | DAC_CK_BIAS[2:0] | R/W | 3h | bias current control (see Table 46) |
| 3 to 1 | DAC_CAS_BIAS[2:0] | R/W | 3h | bias current control (see Table 46) |

Table 38. DAC_SEL_PH_FINE register (address 15h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------|--------|-------|--------------------------|
| 1 to 0 | SEL_PH_FINE[1:0] | R/W | 2h | fine DAC phase selection |

Table 39. PHASECORR_CNTRL0 register (address 16h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------------|--------|-------|-----------------------------|
| 7 to 0 | PHASE_CORR[7:0] | R/W | 00h | LSB phase correction factor |

Table 40. PHASECORR_CNTRL1 register (address 17h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|----------|-----------------------------|
| 7 | PHASE_CORR_ENABLE | R/W | | phase correction |
| | | | 0 | disabled |
| | | | 1 | enabled |
| 1 to 0 | PHASE_CORR[9:8] | R/W | 0h | MSB phase correction factor |

Table 41. DAC_A_AUX_MSB register (address 1Ah) bit description

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|---|
| 7 to 0 | AUX_A[9:2] | R/W | 80h | most significant 8 bits for auxiliary DAC A |

Table 42. DAC_A_AUX_LSB register (address 1Bh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|----------|----------------------------------|
| 7 | AUX_A_PD | R/W | | auxiliary DAC A power |
| | | | 0 | on |
| | | | 1 | off |
| 1 to 0 | AUX_A[1:0] | R/W | 0h | lower 2 bits for auxiliary DAC A |

Table 43. DAC_B_AUX_MSB register (address 1Ch) bit description

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|---|
| 7 to 0 | AUX_B[9:2] | R/W | 80h | most significant 8 bits for auxiliary DAC B |

Table 44. DAC_B_AUX_LSB register (address 1Dh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|----------|----------------------------------|
| 7 | AUX_B_PD | R/W | | auxiliary DAC B power |
| | | | 0 | on |
| | | | 1 | off |
| 1 to 0 | AUX_B[1:0] | R/W | 0h | lower 2 bits for auxiliary DAC B |

Table 45. DAC_B_AUX_LSB register (address 1Dh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------|--------|-------|--------------|
| 2 to 0 | PAGE[2:0] | R/W | 0h | page address |

Table 46. Bias current control table

Default settings are shown highlighted.

| BIAS[2:0] | Deviation from nominal current |
|-----------|--------------------------------|
| 000 | -30 % |
| 001 | ... |
| 010 | ... |
| 011 | 0 % |
| 100 | ... |
| 101 | ... |
| 110 | ... |
| 111 | +30 % |

10.15.2.3 Page 1 allocation map description

Table 47. Page 1 register allocation map

| Address | Register name | R/W | Bit definition | | | | | | | | | Default ^[1] | |
|---------|---------------|-------------------|----------------|-----------------------|------------------------|-------------|--------------|---------------------|---------------------|-------------|------------|------------------------|-----|
| | | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Bin | Hex | |
| 0 | 00h | MDS_MAIN | R/W | MDS_EQCHECK[1:0] | MDS_RUN | MDS_NCO | MDS_SEL_LN23 | MDS_32T_ENA | MDS_MASTER | MDS_ENA | 00000100 | 04h | |
| 1 | 01h | MDS_WIN_PERIOD_A | R/W | MDS_WIN_PERIOD_A[7:0] | | | | | | | | 10000000 | 80h |
| 2 | 02h | MDS_WIN_PERIOD_B | R/W | MDS_WIN_PERIOD_B[7:0] | | | | | | | | 01000000 | 40h |
| 3 | 03h | MDS_MISCCNTRL0 | R/W | - | - | - | MDS_EVAL_ENA | MDS_PRERUN_ENA | MDS_PULSEWIDTH[2:0] | | | 00010000 | 10h |
| 4 | 04h | MDS_MAN_ADJUSTDLY | R/W | MDS_MAN | MDS_MAN_ADJUSTDLY[6:0] | | | | | | 01000000 | 40h | |
| 5 | 05h | MDS_AUTO_CYCLES | R/W | MDS_AUTO_CYCLES[7:0] | | | | | | | | 10000000 | 80h |
| 6 | 06h | MDS_MISCCNTRL1 | R/W | MDS_SR_CKEN | MDS_SR_LOCKOUT | MDS_SR_LOCK | MDS_RELOCK | MDS_LOCK_DELAY[3:0] | | | | 00001111 | 0Fh |
| 8 | 08h | MDS_ADJDELAY | R | - | MDS_ADJDELAY[6:0] | | | | | | uuuuuuuu | uuh | |
| 9 | 09h | MDS_STATUS0 | R | EARLY | LATE | EQUAL | MDS_LOCK | EARLY_ERROR | LATE_ERROR | EQUAL_FOUND | MDS_ACTIVE | uuuuuuuu | uuh |
| 10 | 0Ah | MDS_STATUS1 | R | - | - | - | - | JD_ODD | MDS_PRERUN | MDS_LOCKOUT | MDS_LOCK | uuuuuuuu | uuh |
| 31 | 1Fh | PAGE_ADDRESS | R/W | - | - | - | - | - | PAGE[2:0] | | | 00000000 | 00h |

[1] u = undefined at power-up or after reset.

10.15.2.4 Page 1 bit definition detailed description

Please refer to [Table 47](#) for a register overview and their default values. In the following tables, all the values emphasized in bold are the default values.

Table 48. MDS_MAIN register (address 00h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------|--------|-----------|---|
| 7 to 6 | MDS_EQCHECK[1:0] | R/W | | lock mode |
| | | | 00 | lock when (early = 1 and late = 1) |
| | | | 01 | lock when (early = 1 and late = 1 and equal = 1) |
| | | | 10 | lock when equal = 1 |
| | | | 11 | force_lock (equal-check = 1) |
| 5 | MDS_RUN | R/W | | evaluation restart |
| | | | 0 | no action |
| | | | 1 | transition from 0 to 1 restarts evaluation_counter |
| 4 | MDS_NCO | R/W | | NCO synchronization |
| | | | 0 | no action |
| | | | 1 | NCO synchronization enabled |
| 3 | MDS_SEL_LN23 | R/W | | synchronization reference |
| | | | 0 | use lane 1 enable as reference for synchronization |
| | | | 1 | use lane 2/lane 3 enable as reference for synchronization |
| 2 | MDS_32T_ENA | R/W | | maximum delay |
| | | | 0 | maximum coarse delay is 16T_dclk |
| | | | 1 | maximum coarse delay is 32T_dclk |
| 1 | MDS_MASTER | R/W | | MDS mode |
| | | | 0 | slave mode |
| | | | 1 | master mode |
| 0 | MDS_ENA | R/W | | MDS function |
| | | | 0 | disable MDS function |
| | | | 1 | enable MDS function |

Table 49. MDS_WIN_PERIOD_A register (address 01h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------------------|--------|-------|--------------------------------|
| 7 to 0 | MDS_WIN_PERIOD_A[7:0] | R/W | 80h | determines MDS window LOW-time |

Table 50. MDS_WIN_PERIOD_B register (address 02h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------------------|--------|-------|---------------------------------|
| 7 to 0 | MDS_WIN_PERIOD_B[7:0] | R/W | 40h | determines MDS window HIGH-time |

Table 51. MDS_MISCCNTRL0 register (address 03h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------------|--------|------------|---|
| 4 | MDS_EVAL_ENA | R/W | | MDS evaluation |
| | | | 0 | disabled |
| | | | 1 | enabled |
| 3 | MDS_PRERUN_ENA | R/W | | automatic MDS start-up |
| | | | 0 | no mds_win/mds_ref generation in advance |
| | | | 1 | mds_win/mds_ref run-in before MDS evaluation |
| 2 to 0 | MDS_PULSEWIDTH[2:0] | R/W | | width of MDS (in output clk-periods) |
| | | | 000 | 1T |
| | | | 001 | 2T |
| | | | 010 to 111 | $(\text{MDS_pulsewidth} - 1) \times 4T$ |

Table 52. MDS_MAN_ADJUSTDLY register (address 04h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------------|--------|-------|--|
| 7 | MDS_MAN | R/W | | adjustment delay mode |
| | | | 0 | auto-control adjustment delays |
| | | | 1 | manual control adjustment delays |
| 6 to 0 | MDS_MAN_ADJUSTDLY[6:0] | R/W | | adjustment delay value |
| | | | 40h | if MDS_MAN = 0 then initial value adjustment delay |
| | | | - | if MDS_MAN = 1 then controls adjustment delay |

Table 53. MDS_AUTO_CYCLES register (address 05h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------------|--------|-------|---|
| 7 to 0 | MDS_AUTO_CYCLES[7:0] | R/W | 80h | number of evaluation cycles applied for MDS |

Table 54. MDS_MISCCNTRL1 register (address 06h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|----------------|--------|-------|------------------------------|
| 7 | MDS_SR_CKEN | R/W | | lock mode |
| | | | 0 | free-running mds_cken |
| | | | 1 | MDS_cken forced LOW |
| 6 | MDS_SR_LOCKOUT | R/W | | lockout detector soft reset |
| | | | 0 | mds_lockout in use |
| | | | 1 | MDS_lockout forced LOW |
| 5 | MDS_SR_LOCK | R/W | | lock detector soft reset |
| | | | 0 | MDS_lock in use |
| | | | 1 | MDS_lock forced LOW |

Table 54. MDS_MISCCNTRL1 register (address 06h) bit description ...continued

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------------|--------|-------|--|
| 4 | MDS_RELOCK | R/W | | relock mode |
| | | | 0 | no action |
| | | | 1 | relock when lockout occurs |
| 3 to 0 | MDS_LOCK_DELAY[3:0] | R/W | Fh | number of succeeding 'equal'-detections until lock |

Table 55. MDS_ADJDELAY register (address 08h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|-------|-------------------------------|
| 6 to 0 | MDS_ADJDELAY[6:0] | R | - | actual value adjustment delay |

Table 56. MDS_STATUS0 register (address 09h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|-------------|--------|-------|---|
| 7 | EARLY | R | | early signal (sampled) from early-late detector |
| | | | 0 | false |
| | | | 1 | true |
| 6 | LATE | R | | late signal (sampled) from early-late detector |
| | | | 0 | false |
| | | | 1 | true |
| 5 | EQUAL | R | | equal signal (sampled) from early-late detector |
| | | | 0 | false |
| | | | 1 | true |
| 4 | MDS_LOCK | R | | result equal check |
| | | | 0 | false |
| | | | 1 | true |
| 3 | EARLY_ERROR | R | | adjustment delay maximum value stops the search |
| | | | 0 | false |
| | | | 1 | true |
| 2 | LATE_ERROR | R | | adjustment delay minimum value stops the search |
| | | | 0 | false |
| | | | 1 | true |
| 1 | EQUAL_FOUND | R | | evaluation logic has detected equal condition |
| | | | 0 | false |
| | | | 1 | true |
| 0 | MDS_ACTIVE | R | | evaluation logic active |
| | | | 0 | false |
| | | | 1 | true |

Table 57. MDS_STATUS1 register (address 0Ah) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|-----|-------------|--------|-------|---|
| 3 | JD_ODD | R | | MDS start mode |
| | | | 0 | MDS start aligned to cdi-even sample |
| | | | 1 | MDS start aligned to cdi-odd sample (only for ^2) |
| 2 | MDS_PRERUN | R | | MDS pre-run phase active flag |
| | | | 0 | false |
| | | | 1 | true |
| 1 | MDS_LOCKOUT | R | | MDS lockout detected flag |
| | | | 0 | false |
| | | | 1 | true |
| 0 | MDS_LOCK | R | | MDS lock flag |
| | | | 0 | false |
| | | | 1 | true |

Table 58. PAGE_ADDRESS register (address 1Fh) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|-----------|--------|-------|--------------|
| 2 to 0 | PAGE[2:0] | R/W | 0h | page address |

10.15.2.5 Page 2 allocation map description

Table 59. Page 2 register allocation map

| Address | | Register name | R/W | Bit definition | | | | | | | | Default | |
|---------|-----|-----------------|-----|-------------------------|--------------------|---------------|-----------------|--------------|---------------------|------------------|------------------|----------|-----|
| | | | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Bin | Hex |
| 0 | 00h | MAINCONTROL | R/W | - | - | FULL_RE_INIT | SYNC_INIT_LEVEL | 0 | 0 | FORCE_RESET_DCLK | FORCE_RESET_FCLK | 00000011 | 03h |
| 3 | 03h | JCLK_CNTRL | R/W | SR_CDI | - | CDI_MODE[1:0] | | - | FCLK_POL | FCLK_SEL[1:0] | | 00000000 | 00h |
| 4 | 04h | RST_EXT_FCLK | R/W | RST_EXT_FCLK_TIME[7:0] | | | | | | | | 00111111 | 3Fh |
| 5 | 05h | RST_EXT_DCLK | R/W | RST_EXT_DCLK_TIME[7:0] | | | | | | | | 00100000 | 20h |
| 6 | 06h | DCSMU_PREDIVCNT | R/W | DCSMU_PREDIVIDER[7:0] | | | | | | | | 00011110 | 1Eh |
| 7 | 07h | PLL_CHARGETIME | R/W | PLL_CHARGE_TIME[7:0] | | | | | | | | 00110010 | 32h |
| 8 | 08h | PLL_RUN_IN_TIME | R/W | PLL_RUNIN_TIME[7:0] | | | | | | | | 00110010 | 32h |
| 9 | 09h | CA_RUN_IN_TIME | R/W | CA_RUNIN_TIME[7:0] | | | | | | | | 00000100 | 04h |
| 22 | 16h | SET_VCM_VOLTAGE | R/W | - | - | - | - | SET_VCM[3:0] | | | 00000010 | 02h | |
| 23 | 17h | SET_SYNC | R/W | - | SET_SYNC_VCOM[2:0] | | | - | SET_SYNC_LEVEL[2:0] | | 01000011 | 43h | |
| 27 | 1Bh | TYPE_ID | R | DAC | FRONTEND[1:0] | | DUAL | DSP | | BIT_RES[1:0] | | 11011101 | DDh |
| 28 | 1Ch | DAC_VERSION | R | DAC_VERSION_ID[7:0] | | | | | | | | 00000001 | 01h |
| 29 | 1Dh | DIG_VERSION | R | DIG_VERSION_ID[7:0] | | | | | | | | 00000010 | 02h |
| 30 | 1Eh | JRX_ANA_VERSION | R | JRX_ANA_VERSION_ID[7:0] | | | | | | | | 00000010 | 02h |
| 31 | 1Fh | PAGE_ADDRESS | R/W | - | - | - | - | - | PAGE[2:0] | | | 00000000 | 00h |

10.15.2.6 Page 2 bit definition detailed description

Please refer to [Table 59](#) for a register overview and their default values. In the following tables, all the values emphasized in bold are the default values.

Table 60. MAINCONTROL register (address 00h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|------------------|--------|----------|--|
| 5 | FULL_RE_INIT | R/W | | initialization |
| | | | 0 | quick reinitialization |
| | | | 1 | full reinitialization |
| 4 | SYNC_INIT_LEVEL | R/W | | synchronization |
| | | | 0 | synchronization starts with '0' |
| | | | 1 | synchronization starts with '1' |
| 3 | - | R/W | | must be written with '0' |
| 2 | - | R/W | | must be written with '0' |
| 1 | FORCE_RESET_DCLK | R/W | | reset_dclk |
| | | | 0 | release reset_dclk |
| | | | 1 | force reset_dclk |
| 0 | FORCE_RESET_FCLK | R/W | | reset_fclk |
| | | | 0 | release reset_fclk |
| | | | 1 | force reset_fclk |

Table 61. JCLK_CNTRL register (address 03h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-----------|------------------------------------|
| 7 | SR_CDI | R/W | | cdi reset |
| | | | 0 | no action |
| | | | 1 | soft reset cdi |
| 5 to 4 | CDI_MODE[1:0] | R/W | | cdi mode |
| | | | 00 | cdi_mode 0 (^2 modes) |
| | | | 01 | cdi_mode 1 (^4 modes) |
| | | | 10 | cdi_mode 2 (^8 modes) |
| | | | 11 | reserved |
| 2 | FCLK_POL | R/W | | f _{clk} polarity |
| | | | 0 | no action |
| | | | 1 | invert polarity |
| 1 to 0 | FCLK_SEL[1:0] | R/W | | f _{clk} clock source |
| | | | 00 | dclk × 2 |
| | | | 01 | dclk |
| | | | 10 | dclk_div2; running |
| | | | 11 | dclk_div2; reset dclk_div2 divider |

Table 62. RST_EXT_FCLK register (address 04h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------------|--------|-------|--|
| 7 to 0 | RST_EXT_FCLK_TIME[7:0] | R/W | 3Fh | specifies extension time reset_fclk in f_{clk} periods |

Table 63. RST_EXT_DCLK register (address 05h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------------|--------|-------|---|
| 7 to 0 | RST_EXT_DCLK_TIME[7:0] | R/W | 20h | specifies extension time reset_dclk (in dclk-periods) |

Table 64. DCSMU_PREDIVCNT register (address 06h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------------------|--------|-------|--|
| 7 to 0 | DCSMU_PREDIVIDER[7:0] | R/W | 1Eh | value used by dcsmu predivider (at f_{clk}) |

Table 65. PLL_CHARGETIME register (address 07h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------------|--------|-------|---|
| 7 to 0 | PLL_CHARGE_TIME[7:0] | R/W | 32h | PLL charge time (at $f_{clk}/DCSMU_PREDIVIDER[7:0]$) |

Table 66. PLL_RUN_IN_TIME register (address 08h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------------|--------|-------|--|
| 7 to 0 | PLL_RUNIN_TIME[7:0] | R/W | 32h | PLL run in time (at $f_{clk}/DCSMU_PREDIVIDER[7:0]$) |

Table 67. CA_RUN_IN_TIME register (address 09h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------------|--------|-------|---|
| 7 to 0 | CA_RUNIN_TIME[7:0] | R/W | 04h | clock alignment run in time (at $f_{clk}/DCSMU_PREDIVIDER[7:0]$) |

Table 68. SET_VCM_VOLTAGE register (address 16h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------|--------|-------|--|
| 3 to 0 | SET_VCM[3:0] | R/W | 02h | set lane common-mode voltage (see Table 75) |

Table 69. SET_SYNC register (address 17h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------------|--------|-------|---|
| 6 to 4 | SET_SYNC_VCOM[2:0] | R/W | 4h | set synchronization transmitter common-mode level (see Table 76) |
| 2 to 0 | SET_SYNC_LEVEL[2:0] | R/W | 3h | set synchronization transmitter output level swing (see Table 77) |

Table 70. TYPE_ID register (address 1Bh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------|--------|-----------|---|
| 7 | DAC | R | | part type |
| | | | 0 | ADC |
| | | | 1 | DAC |
| 6 to 5 | FRONTEND [1:0] | R | | input format |
| | | | 00 | CMOS |
| | | | 01 | LVDS |
| | | | 10 | JESD204A |
| | | | 11 | reserved |
| 4 | DUAL | R | | converter structure |
| | | | 0 | single |
| | | | 1 | dual |
| 3 to 2 | DSP | R | | digital processing |
| | | | 00 | none |
| | | | 01 | upsampling filters |
| | | | 10 | single sideband modulator |
| | | | 11 | upsampling filters + single sideband modulator |
| 1 to 0 | BIT_RES[1:0] | R | | resolution |
| | | | 00 | 16 bits |
| | | | 01 | 14 bits |
| | | | 10 | 12 bits |
| | | | 11 | 10 bits |

Table 71. DAC_VERSION register (address 1Ch) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------------|--------|-------|-----------------------|
| 7 to 0 | DAC_VERSION_ID[7:0] | R | 01h | dual DAC core version |

Table 72. DIG_VERSION register (address 1Dh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------------|--------|-------|-----------------|
| 7 to 0 | DIG_VERSION_ID[7:0] | R | 02h | digital version |

Table 73. JRX_ANA_VERSION register (address 1Eh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------------|--------|-------|-----------------------------|
| 7 to 0 | JRX_ANA_VERSION_ID[7:0] | R | 02h | analog deserializer version |

Table 74. PAGE_ADDRESS register (address 1Fh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------|--------|-------|--------------|
| 2 to 0 | PAGE[2:0] | R/W | 0h | page address |

Table 75. Lane common-mode voltage adjustment

| Register 16h: SET_VCM_VOLTAGE | | |
|-------------------------------|-----------------|----------------------|
| Decimal | SET_VCM_VOLTAGE | V _{com} (V) |
| 15 | 1111 | 1.40 |
| 14 | 1110 | 1.36 |
| 13 | 1101 | 1.31 |
| 12 | 1100 | 1.26 |
| 11 | 1011 | 1.21 |
| 10 | 1010 | 1.16 |
| 9 | 1001 | 1.12 |
| 8 | 1000 | 1.07 |
| 7 | 0111 | 1.02 |
| 6 | 0110 | 0.97 |
| 5 | 0101 | 0.92 |
| 4 | 0100 | 0.87 |
| 3 | 0011 | 0.82 |
| 2 | 0010 | 0.78 |
| 1 | 0001 | 0.73 |
| 0 | 0000 | 0.68 |

Table 76. SYNC common-mode voltage adjustment

| Register 17h: SET_SYNC | | |
|------------------------|--------------------|----------------------|
| Decimal | SET_SYNC_VCOM[2:0] | V _{com} (V) |
| 7 | 111 | 1.46 |
| 6 | 110 | 1.36 |
| 5 | 101 | 1.27 |
| 4 | 100 | 1.17 |
| 3 | 011 | 1.07 |
| 2 | 010 | 0.98 |
| 1 | 001 | 0.88 |
| 0 | 000 | 0.79 |

Table 77. SYNC swing voltage adjustment

| Register 17h: SET_SYNC | | |
|------------------------|---------------------|---------------------------------|
| Decimal | SET_SYNC_LEVEL[2:0] | Single-ended output voltage (V) |
| 7 | 111 | 0.48 |
| 6 | 110 | 0.42 |
| 5 | 101 | 0.36 |
| 4 | 100 | 0.30 |
| 3 | 011 | 0.24 |
| 2 | 010 | 0.18 |
| 1 | 001 | 0.12 |
| 0 | 000 | 0.06 |

10.15.2.7 Page 4 allocation map description

Table 78. Page 4 register allocation map

| Address | Register name | R/W | Bit definition | | | | | | | | | Default | |
|---------|---------------|----------------------|----------------|----------------------------|----------------|--------------------------|----------------|-----------------------|-------------------|-----------------------|-------------------|----------|-----|
| | | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Bin | Hex | |
| 0 | 00h | SR_DLP_0 | R/W | SR_SWA_LN3 | SR_SWA_LN2 | SR_SWA_LN1 | SR_SWA_LN0 | SR_CA_LN3 | SR_CA_LN2 | SR_CA_LN1 | SR_CA_LN0 | 00000000 | 00h |
| 1 | 01h | SR_DLP_1 | R/W | SR_CNTRL_LN3 | SR_CNTRL_LN2 | SR_CNTRL_LN1 | SR_CNTRL_LN0 | SR_DEC_LN3 | SR_DEC_LN2 | SR_DEC_LN1 | SR_DEC_LN0 | 00000000 | 00h |
| 2 | 02h | FORCE_LOCK | R/W | FORCE_LOCK_LN3 | FORCE_LOCK_LN2 | FORCE_LOCK_LN1 | FORCE_LOCK_LN0 | - | - | - | SR_ILA | 00000000 | 00h |
| 3 | 03h | MAN_LOCK_LN_1_0 | R/W | MAN_LOCK_LN1[3:0] | | | | MAN_LOCK_LN0[3:0] | | | | 00000000 | 00h |
| 4 | 04h | MAN_LOCK_2_0 | R/W | MAN_LOCK_LN3[3:0] | | | | MAN_LOCK_LN2[3:0] | | | | 00000000 | 00h |
| 5 | 05h | CA_CNTRL | R/W | WORD_SWAP_LN3 | WORD_SWAP_LN2 | WORD_SWAP_LN1 | WORD_SWAP_LN0 | SELECT_RF_F10_LN3 | SELECT_RF_F10_LN2 | SELECT_RF_F10_LN1 | SELECT_RF_F10_LN0 | 00000000 | 00h |
| 6 | 06h | SCR_CNTRL | R/W | MAN_SCR_LN3 | MAN_SCR_LN2 | MAN_SCR_LN1 | MAN_SCR_LN0 | FORCE_SCR_LN3 | FORCE_SCR_LN2 | FORCE_SCR_LN1 | FORCE_SCR_LN0 | 00000000 | 00h |
| 7 | 07h | ILA_CNTRL | R/W | SEL_421_211 | SEL_ILA[1:0] | | SEL_LOCK[2:0] | | | SUP_LANE_SYN | EN_SCR | 10000011 | 83h |
| 8 | 08h | FORCE_ALIGN | R/W | - | - | - | - | - | - | DYN_ALIGN_ENA | FORCE_ALIGN | 00000000 | 00h |
| 9 | 09h | MAN_ALIGN_LN_0_1 | R/W | MAN_ALIGN_LN1[3:0] | | | | MAN_ALIGN_LN0[3:0] | | | | 00000000 | 00h |
| 10 | 0Ah | MAN_ALIGN_LN_2_3 | R/W | MAN_ALIGN_LN3[3:0] | | | | MAN_ALIGN_LN2[3:0] | | | | 00000000 | 00h |
| 11 | 0Bh | FA_ERR_HANDLING | R/W | SEL_KOUT_UNEXP_LN23[1:0] | | SEL_KOUT_UNEXP_LN10[1:0] | | SEL_NIT_ERR_LN23[1:0] | | SEL_NIT_ERR_LN10[1:0] | | 00000000 | 00h |
| 12 | 0Ch | SYNCOUT_MODE | R/W | SEL_RE_INIT[2:0] | | | SYNC_POL | SEL_SYNC[3:0] | | | | 00000000 | 00h |
| 13 | 0Dh | LANE_POLARITY | R/W | - | - | - | - | POL_LN3 | POL_LN2 | POL_LN1 | POL_LN0 | 00000000 | 00h |
| 14 | 0Eh | LANE_SELECT | R/W | LANE_SEL_LN3[1:0] | | LANE_SEL_LN2[1:0] | | LANE_SEL_LN1[1:0] | | LANE_SEL_LN0[1:0] | | 11100100 | E4h |
| 16 | 10h | SOFT_RESET_SCRAMBLER | R/W | - | - | - | - | SR_SCR_LN3 | SR_SCR_LN2 | SR_SCR_LN1 | SR_SCR_LN0 | 00000000 | 00h |
| 17 | 11h | INIT_SCR_S15T8_LN0 | R/W | INIT_VALUE_S15_S8_LN0[7:0] | | | | | | | | 00000000 | 00h |

Table 78. Page 4 register allocation map ...continued

| Address | | Register name | R/W | Bit definition | | | | | | | | Default | | |
|---------|-----|----------------------|-----|----------------------------|---------------------------|----------------|----------------|--------------------------|----------------|----------------|----------------|----------|----------|-----|
| | | | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Bin | Hex | |
| 18 | 12h | INIT_SCR_S7T1_LN0 | R/W | - | INIT_VALUE_S7_S1_LN0[6:0] | | | | | | | | 00000000 | 00h |
| 19 | 13h | INIT_SCR_S15T8_LN1 | R/W | INIT_VALUE_S15_S8_LN1[7:0] | | | | | | | | 00000000 | 00h | |
| 20 | 14h | INIT_SCR_S7T1_LN1 | R/W | - | INIT_VALUE_S7_S1_LN1[6:0] | | | | | | | | 00000000 | 00h |
| 21 | 15h | INIT_SCR_S15T8_LN2 | R/W | INIT_VALUE_S15_S8_LN2[7:0] | | | | | | | | 00000000 | 00h | |
| 22 | 16h | INIT_SCR_S7T1_LN2 | R/W | - | INIT_VALUE_S7_S1_LN2[6:0] | | | | | | | | 00000000 | 00h |
| 23 | 17h | INIT_SCR_S15T8_LN3 | R/W | INIT_VALUE_S15_S8_LN3[7:0] | | | | | | | | 00000000 | 00h | |
| 24 | 18h | INIT_SCR_S7T1_LN3 | R/W | - | INIT_VALUE_S7_S1_LN3[6:0] | | | | | | | | 00000000 | 00h |
| 25 | 19h | INIT_ILA_BUFPTR_LN01 | R/W | INIT_ILA_BUFPTR_LN1[3:0] | | | | INIT_ILA_BUFPTR_LN0[3:0] | | | | 10001000 | 88h | |
| 26 | 1Ah | INIT_ILA_BUFPTR_LN23 | R/W | INIT_ILA_BUFPTR_LN3[3:0] | | | | INIT_ILA_BUFPTR_LN2[3:0] | | | | 10001000 | 88h | |
| 27 | 1Bh | ERROR_HANDLING | R/W | - | NAD_ERR_CORR | KUX_CORR | NAD_CORR | CORR_MODE[1:0] | | IMPL_ALT | IGNORE_ERR | 00000000 | 00h | |
| 28 | 1Ch | REINIT_CNTRL | R/W | REINIT_ILA_LN3 | REINIT_ILA_LN2 | REINIT_ILA_LN1 | REINIT_ILA_LN0 | RESYNC_O_L_LN3 | RESYNC_O_L_LN2 | RESYNC_O_L_LN1 | RESYNC_O_L_LN0 | 00000000 | 00h | |
| 31 | 1Fh | PAGE_ADDRESS | R/W | - | - | - | - | - | PAGE[2:0] | | | 00000000 | 00h | |

10.15.2.8 Page 4 bit definition detailed description

Please refer to [Table 78](#) for a register overview and their default values. In the following tables, all the values emphasized in bold are the default values.

Table 79. SR_DLP_0 register (address 00h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|------------|--------|-------|---------------------------------------|
| 7 | SR_SWA_LN3 | R/W | 0 | soft reset sync_word_alignment lane 3 |
| 6 | SR_SWA_LN2 | R/W | 0 | soft reset sync_word_alignment lane 2 |
| 5 | SR_SWA_LN1 | R/W | 0 | soft reset sync_word_alignment lane 1 |
| 4 | SR_SWA_LN0 | R/W | 0 | soft reset sync_word_alignment lane 0 |
| 3 | SR_CA_LN3 | R/W | 0 | soft reset clock_alignment lane 3 |
| 2 | SR_CA_LN2 | R/W | 0 | soft reset clock_alignment lane 2 |
| 1 | SR_CA_LN1 | R/W | 0 | soft reset clock_alignment lane 1 |
| 0 | SR_CA_LN0 | R/W | 0 | soft reset clock_alignment lane 0 |

Table 80. SR_DLP_1 register (address 01h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|--------------|--------|-------|---------------------------------|
| 7 | SR_CNTRL_LN3 | R/W | 0 | soft reset controller lane 3 |
| 6 | SR_CNTRL_LN2 | R/W | 0 | soft reset controller lane 2 |
| 5 | SR_CNTRL_LN1 | R/W | 0 | soft reset controller lane 1 |
| 4 | SR_CNTRL_LN0 | R/W | 0 | soft reset controller lane 0 |
| 3 | SR_DEC_LN3 | R/W | 0 | soft reset decoder_10b8b lane 3 |
| 2 | SR_DEC_LN2 | R/W | 0 | soft reset decoder_10b8b lane 2 |
| 1 | SR_DEC_LN1 | R/W | 0 | soft reset decoder_10b8b lane 1 |
| 0 | SR_DEC_LN0 | R/W | 0 | soft reset decoder_10b8b lane 0 |

Table 81. FORCE_LOCK register (address 02h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|----------------|--------|-------|--|
| 7 | FORCE_LOCK_LN3 | R/W | | lane 3 lock mode |
| | | | 0 | automatic lock sync_word_alignment lane 3 |
| 6 | FORCE_LOCK_LN2 | R/W | 1 | manual lock sync_word_alignment lane 3 |
| | | | 0 | automatic lock sync_word_alignment lane 2 |
| 5 | FORCE_LOCK_LN1 | R/W | 1 | manual lock sync_word_alignment lane 2 |
| | | | 0 | automatic lock sync_word_alignment lane 1 |
| 4 | FORCE_LOCK_LN0 | R/W | 1 | manual lock sync_word_alignment lane 1 |
| | | | 0 | automatic lock sync_word_alignment lane 0 |
| | | | 1 | manual lock sync_word_alignment lane 0 |
| | | | 0 | automatic lock sync_word_alignment lane 0 |

Table 81. FORCE_LOCK register (address 02h) bit description ...continued

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|--------|--------|-------|--------------------------------|
| 0 | SR_ILA | R/W | | soft reset interlane alignment |
| | | | 0 | no action |
| | | | 1 | reset |

Table 82. MAN_LOCK_LN_1_0 register (address 03h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|-------|---|
| 7 to 4 | MAN_LOCK_LN1[3:0] | R/W | 0h | manual lock setting synchronization word alignment lane 1 |
| 3 to 0 | MAN_LOCK_LN0[3:0] | R/W | 0h | manual lock setting synchronization word alignment lane 0 |

Table 83. MAN_LOCK_2_0 register (address 04h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|-------|---|
| 7 to 4 | MAN_LOCK_LN3[3:0] | R/W | 0h | manual lock setting synchronization word alignment lane 3 |
| 3 to 0 | MAN_LOCK_LN2[3:0] | R/W | 0h | manual lock setting synchronization word alignment lane 2 |

Table 84. CA_CNTRL register (address 05h) bit description

| Bit | Symbol | Access | Value | Description |
|-----|-------------------|--------|-------|---|
| 7 | WORD_SWAP_LN3 | R/W | | lane 3 bit swapping |
| | | | 0 | dout_ca_ln3[7:0] = din_ca_ln3[7:0] |
| | | | 1 | dout_ca_ln3[7:0] = din_ca_ln3[0:7] |
| 6 | WORD_SWAP_LN2 | R/W | | lane 2 bit swapping |
| | | | 0 | dout_ca_ln2[7:0] = din_ca_ln2[7:0] |
| | | | 1 | dout_ca_ln2[7:0] = din_ca_ln2[0:7] |
| 5 | WORD_SWAP_LN1 | R/W | | lane 1 bit swapping |
| | | | 0 | dout_ca_ln1[7:0] = din_ca_ln1[7:0] |
| | | | 1 | dout_ca_ln1[7:0] = din_ca_ln1[0:7] |
| 4 | WORD_SWAP_LN0 | R/W | | lane 0 bit swapping |
| | | | 0 | dout_ca_ln0[7:0] = din_ca_ln0[7:0] |
| | | | 1 | dout_ca_ln0[7:0] = din_ca_ln0[0:7] |
| 3 | SELECT_RF_F10_LN3 | R/W | | lane 3 sampling mode |
| | | | 0 | din_ca_ln3 sampled at falling edge f10_ln3 |
| | | | 1 | din_ca_ln3 sampled at rising edge f10_ln3 |
| 2 | SELECT_RF_F10_LN2 | R/W | | lane 2 sampling mode |
| | | | 0 | din_ca_ln2 sampled at falling edge f10_ln2 |
| | | | 1 | din_ca_ln2 sampled at rising edge f10_ln2 |

Table 84. CA_CNTRL register (address 05h) bit description ...continued

| Bit | Symbol | Access | Value | Description |
|-----|-------------------|--------|-------|---|
| 1 | SELECT_RF_F10_LN1 | R/W | | lane 1 sampling mode |
| | | | 0 | din_ca_In1 sampled at falling edge f10_In1 |
| | | | 1 | din_ca_In1 sampled at rising edge f10_In1 |
| 0 | SELECT_RF_F10_LN0 | R/W | | lane 0 sampling mode |
| | | | 0 | din_ca_In0 sampled at falling edge f10_In0 |
| | | | 1 | din_ca_In0 sampled at rising edge f10_In0 |

Table 85. SCR_CNTRL register (address 06h) bit description

| Bit | Symbol | Access | Value | Description |
|-----|---------------|--------|-------|---|
| 7 | MAN_SCR_LN3 | R/W | | lane 3 manual scrambling |
| | | | 0 | scrambling lane 3 off (when force_scr_In3 = 1) |
| | | | 1 | scrambling lane 3 on (when force_scr_In3 = 1) |
| 6 | MAN_SCR_LN2 | R/W | | lane 2 manual scrambling |
| | | | 0 | scrambling lane 2 off (when force_scr_In2 = 1) |
| | | | 1 | scrambling lane 2 on (when force_scr_In2 = 1) |
| 5 | MAN_SCR_LN1 | R/W | | lane 1 manual scrambling |
| | | | 0 | scrambling lane 1 off (when force_scr_In1 = 1) |
| | | | 1 | scrambling lane 1 on (when force_scr_In1 = 1) |
| 4 | MAN_SCR_LN0 | R/W | | lane 0 manual scrambling |
| | | | 0 | scrambling lane 0 off (when force_scr_In0 = 1) |
| | | | 1 | scrambling lane 0 on (when force_scr_In0 = 1) |
| 3 | FORCE_SCR_LN3 | R/W | | lane 3 scrambling mode |
| | | | 0 | scrambling lane 3 depends on lock_In3 and en_scr |
| | | | 1 | scrambling lane 3 depends on man_scr_In3 |
| 2 | FORCE_SCR_LN2 | R/W | | lane 2 scrambling mode |
| | | | 0 | scrambling lane 2 depends on lock_In2 and en_scr |
| | | | 1 | scrambling lane 2 depends on man_scr_In2 |
| 1 | FORCE_SCR_LN1 | R/W | | lane 1 scrambling mode |
| | | | 0 | scrambling lane 1 depends on lock_In1 and en_scr |
| | | | 1 | scrambling lane 1 depends on man_scr_In1 |
| 0 | FORCE_SCR_LN0 | R/W | | lane 0 scrambling mode |
| | | | 0 | scrambling lane 0 depends on lock_In0 and en_scr |
| | | | 1 | scrambling lane 0 depends on man_scr_In0 |

Table 86. ILA_CNTRL register (address 07h) bit description

| Bit | Symbol | Access | Value | Description |
|----------|---|--------|------------|---|
| 7 | SEL_421_211 | R/W | | inter-lane alignment mode |
| | | | 0 | inter-lane alignment based on lane 3 : lane 2 and/or lane 1 : lane 0 |
| | | | 1 | inter-lane alignment based on In3 : In0 |
| 6 to 5 | SEL_ILA[1:0] | R/W | | inter-lane alignment trigger mode |
| | | | 00 | inter-lane alignment is done after receiving 1 /A/-symbol |
| | | | 01 | inter-lane alignment is done after receiving 2 /A/-symbols |
| | | | 10 | inter-lane alignment is done after receiving 3 /A/-symbols |
| | | | 11 | inter-lane alignment is done after receiving 4 /A/-symbols |
| 4 to 2 | SEL_LOCK[2:0] | R/W | | inter-lane alignment start mode |
| | | | 000 | inter-lane alignment may start only if all (4 or 2) lanes are locked |
| | | | 001 | inter-lane alignment may start if one of the (4 or 2) lanes are locked |
| | | | 010 | inter-lane alignment may start if lane 0 is locked |
| | | | 011 | inter-lane alignment may start if lane 1 is locked |
| | | | 100 | inter-lane alignment may start if lane 2 is locked |
| | | | 101 | inter-lane alignment may start if lane 3 is locked |
| | | | 1 | SUP_LANE_SYN |
| 0 | inter-lane alignment synchronization disabled | | | |
| 1 | inter-lane alignment synchronization enabled | | | |
| 0 | EN_SCR | R/W | | data descrambling |
| | | | 0 | disabled |
| | | | 1 | enabled |

Table 87. FORCE_ALIGN register (address 08h) bit description

| Bit | Symbol | Access | Value | Description |
|-----|---------------|--------|----------|--|
| 1 | DYN_ALIGN_ENA | R/W | | dynamic re-alignment mode |
| | | | 0 | no dynamic re-alignment |
| | | | 1 | dynamic re-alignment (and monitoring) enabled |
| 0 | FORCE_ALIGN | R/W | | lane alignment mode |
| | | | 0 | automatic lane alignment based on /A/ symbols |
| | | | 1 | manual lane alignment based on man_align_Inx |

Table 88. MAN_ALIGN_LN_0_1 register (address 09h) bit description

| Bit | Symbol | Access | Value | Description |
|--------|--------------------|--------|-------|---|
| 7 to 4 | MAN_ALIGN_LN1[3:0] | R/W | 0h | indicates alignment data-delay for lane 1 [1..15] |
| 3 to 0 | MAN_ALIGN_LN0[3:0] | R/W | 0h | indicates alignment data-delay for lane 0 [1..15] |

Table 89. MAN_ALIGN_LN_2_3 register (address 0Ah) bit description

| Bit | Symbol | Access | Value | Description |
|--------|--------------------|--------|-------|---|
| 7 to 4 | MAN_ALIGN_LN3[3:0] | R/W | 0h | indicates alignment data-delay for lane 3 [1..15] |
| 3 to 0 | MAN_ALIGN_LN2[3:0] | R/W | 0h | indicates alignment data-delay for lane 2 [1..15] |

Table 90. FA_ERR_HANDLING register (address 0Bh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------------------|--------|-----------|--|
| 7 to 6 | SEL_KOUT_UNEXP_LN23[1:0] | R/W | | lane 2/lane 3 unexpected /K/ error handling |
| | | | 00 | unexpected /K/ in lane 2 or lane 3 error_handling |
| | | | 01 | unexpected /K/ in lane 2 and lane 3 error_handling |
| | | | 10 | unexpected /K/ in lane 2 error_handling |
| | | | 11 | unexpected /K/ in lane 3 error_handling |
| 5 to 4 | SEL_KOUT_UNEXP_LN10[1:0] | R/W | | lane 0/lane 1 unexpected /K/ error handling |
| | | | 00 | unexpected /K/ in lane 0 or lane 1 error_handling |
| | | | 01 | unexpected /K/ in lane 0 and lane 1 error_handling |
| | | | 10 | unexpected /K/ in lane 0 error_handling |
| | | | 11 | unexpected /K/ in lane 1 error_handling |
| 3 to 2 | SEL_NIT_ERR_LN23[1:0] | R/W | | lane 2/lane 3 nit-error handling |
| | | | 00 | nit-errors in lane 2 or lane 3 error_handling |
| | | | 01 | not-in-table errors lane 2 and lane 3 error_handling |
| | | | 10 | not-in-table errors in lane 2 error_handling |
| | | | 11 | not-in-table errors in lane 3 error_handling |
| 1 to 0 | SEL_NIT_ERR_LN10[1:0] | R/W | | lane 0/lane 1 nit-error handling |
| | | | 00 | nit-errors in lane 0 or lane 1 error_handling |
| | | | 01 | not-in-table errors lane 0 and lane 1 error_handling |
| | | | 10 | not-in-table errors in lane 0 error_handling |
| | | | 11 | not-in-table errors in lane 1 error_handling |

Table 91. SYNCOUT_MODE register (address 0Ch) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description | | | |
|--------|------------------------------|--------|-------------|---|-----|----------|------------------------------------|
| 7 to 5 | SEL_RE_INIT[2:0] | R/W | | reinitialization mode | | | |
| | | | 000 | i_re_init when 1 of the lane_rst's is active | | | |
| | | | 001 | i_re_init when rst_In0 or rst_In1 is active | | | |
| | | | 010 | i_re_init when rst_In2 or rst_In3 is active | | | |
| | | | 011 | i_re_init when rst_In0 is active | | | |
| | | | 100 | i_re_init when rst_In1 is active | | | |
| | | | 101 | i_re_init when rst_In2 is active | | | |
| | | | 110 | i_re_init when rst_In3 is active | | | |
| | | | 111 | i_re_init remains '0' | | | |
| | | | 4 | SYNC_POL | R/W | | synchronization polarity |
| | | | | | | 0 | sync_out is active when LOW |
| 1 | sync_out is active when HIGH | | | | | | |
| 3 to 0 | SEL_SYNC[3:0] | R/W | | synchronization mode | | | |
| | | | 0000 | sync when one of the four lane_syncs is active | | | |
| | | | 0001 | sync when all four lane_syncs are active | | | |
| | | | 0010 | sync when sync_In0 or sync_In1 is active | | | |
| | | | 0011 | sync when both sync_In0 and sync_In1 are active | | | |
| | | | 0100 | sync when sync_In2 or sync_In3 is active | | | |
| | | | 0101 | sync when both sync_In2 and sync_In3 are active | | | |
| | | | 0110 | sync when sync_In0 is active | | | |
| | | | 0111 | sync when sync_In1 is active | | | |
| | | | 1000 | sync when sync_In2 is active | | | |
| | | | 1001 | sync when sync_In3 is active | | | |
| | | | 1010 | sync remains fixed '1' | | | |
| | | | other | sync remains fixed '0' | | | |

Table 92. LANE_POLARITY register (address 0Dh) bit description

| Bit | Symbol | Access | Value | Description |
|-----|---------|--------|----------|---------------------------------|
| 3 | POL_LN3 | R/W | | lane 3 data polarity |
| | | | 0 | no action |
| | | | 1 | invert all data bits of lane 3 |
| 2 | POL_LN2 | R/W | | lane 2 data polarity |
| | | | 0 | no action |
| | | | 1 | invert all data bits of lane 2 |
| 1 | POL_LN1 | R/W | | lane 1 data polarity |
| | | | 0 | no action |
| | | | 1 | invert all data bits of lane 1] |
| 0 | POL_LN0 | R/W | | lane 0 data polarity |
| | | | 0 | no action |
| | | | 1 | invert all data bits of lane 0 |

Table 93. LANE_SELECT register (address 0Eh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|-----------|--|
| 7 to 6 | LANE_SEL_LN3[1:0] | R/W | | lane 3 data mapping |
| | | | 00 | ila_in_ln3 = lane_ln0 (dout and controls) |
| | | | 01 | ila_in_ln3 = lane_ln1 (dout and controls) |
| | | | 10 | ila_in_ln3 = lane_ln2 (dout and controls) |
| | | | 11 | ila_in_ln3 = lane_ln3 (dout and controls) |
| 5 to 4 | LANE_SEL_LN2[1:0] | R/W | | lane 2 data mapping |
| | | | 00 | ila_in_ln2 = lane_ln0 (dout and controls) |
| | | | 01 | ila_in_ln2 = lane_ln1 (dout and controls) |
| | | | 10 | ila_in_ln2 = lane_ln2 (dout and controls) |
| | | | 11 | ila_in_ln2 = lane_ln3 (dout and controls) |
| 3 to 2 | LANE_SEL_LN1[1:0] | R/W | | lane 1 data mapping |
| | | | 00 | ila_in_ln1 = lane_ln0 (dout and controls) |
| | | | 01 | ila_in_ln1 = lane_ln1 (dout and controls) |
| | | | 10 | ila_in_ln1 = lane_ln2 (dout and controls) |
| | | | 11 | ila_in_ln1 = lane_ln3 (dout and controls) |
| 1 to 0 | LANE_SEL_LN0[1:0] | R/W | | lane 0 data mapping |
| | | | 00 | ila_in_ln0 = lane_ln0 (dout and controls) |
| | | | 01 | ila_in_ln0 = lane_ln1 (dout and controls) |
| | | | 10 | ila_in_ln0 = lane_ln2 (dout and controls) |
| | | | 11 | ila_in_ln0 = lane_ln3 (dout and controls) |

Table 94. SOFT_RESET_SCRAMBLER register (address 10h) bit description

| Bit | Symbol | Access | Value | Description |
|-----|------------|--------|----------|--------------------------------|
| 3 | SR_SCR_LN3 | R/W | | lane 3 scrambler reset |
| | | | 0 | no action |
| | | | 1 | soft_reset scrambler of lane 3 |
| 2 | SR_SCR_LN2 | R/W | | lane 2 scrambler reset |
| | | | 0 | no action |
| | | | 1 | soft_reset scrambler of lane 2 |
| 1 | SR_SCR_LN1 | R/W | | lane 1 scrambler reset |
| | | | 0 | no action |
| | | | 1 | soft_reset scrambler of lane 1 |
| 0 | SR_SCR_LN0 | R/W | | lane 0 scrambler reset |
| | | | 0 | no action |
| | | | 1 | soft_reset scrambler of lane 0 |

Table 95. INIT_SCR_S15T8_LN0 register (address 11h) bit description

| Bit | Symbol | Access | Value | Description |
|--------|----------------------------|--------|-------|---|
| 7 to 0 | INIT_VALUE_S15_S8_LN0[7:0] | R/W | 00h | initialization value for lane 0 descrambler bits s15 : s8 |

Table 96. INIT_SCR_S7T1_LN0 (address 12h) bit description

| Bit | Symbol | Access | Value | Description |
|--------|---------------------------|--------|-------|--|
| 6 to 0 | INIT_VALUE_S7_S1_LN0[6:0] | R/W | 00h | initialization value for lane 0 descrambler bits s7 : s1 |

Table 97. INIT_SCR_S15T8_LN1 register (address 13h) bit description

| Bit | Symbol | Access | Value | Description |
|--------|----------------------------|--------|-------|---|
| 7 to 0 | INIT_VALUE_S15_S8_LN1[7:0] | R/W | 00h | initialization value for lane 1 descrambler bits s15 : s8 |

Table 98. INIT_SCR_S7T1_LN1 register (address 14h) bit description

| Bit | Symbol | Access | Value | Description |
|--------|---------------------------|--------|-------|--|
| 6 to 0 | INIT_VALUE_S7_S1_LN1[6:0] | R/W | 00h | initialization value for lane 1 descrambler bits s7 : s1 |

Table 99. INIT_SCR_S15T8_LN2 register (address 15h) bit description

| Bit | Symbol | Access | Value | Description |
|--------|----------------------------|--------|-------|---|
| 7 to 0 | INIT_VALUE_S15_S8_LN2[7:0] | R/W | 00h | initialization value for lane 2 descrambler bits s15 : s8 |

Table 100. INIT_SCR_S7T1_LN2 register (address 16h) bit description

| Bit | Symbol | Access | Value | Description |
|--------|---------------------------|--------|-------|--|
| 6 to 0 | INIT_VALUE_S7_S1_LN2[6:0] | R/W | 00h | initialization value for lane 2 descrambler bits s7 : s1 |

Table 101. INIT_SCR_S15T8_LN3 register (address 17h) bit description

| Bit | Symbol | Access | Value | Description |
|--------|----------------------------|--------|-------|---|
| 7 to 0 | INIT_VALUE_S15_S8_LN3[7:0] | R/W | 00h | initialization value for lane 3 descrambler bits s15 : s8 |

Table 102. INIT_SCR_S7T1_LN3 register (address 18h) bit description

| Bit | Symbol | Access | Value | Description |
|--------|---------------------------|--------|-------|--|
| 6 to 0 | INIT_VALUE_S7_S1_LN3[6:0] | R/W | 00h | initialization value for lane 3 descrambler bits s7 : s1 |

Table 103. INIT_ILA_BUFPTR_LN01 register (address 19h) bit description

| Bit | Symbol | Access | Value | Description |
|--------|--------------------------|--------|-------|--|
| 7 to 4 | INIT_ILA_BUFPTR_LN1[3:0] | R/W | 8h | initialization value for lane 1 ILA buffer pointer |
| 3 to 0 | INIT_ILA_BUFPTR_LN0[3:0] | R/W | 8h | initialization value for lane 0 ILA buffer pointer |

Table 104. INIT_ILA_BUFPTR_LN23 register (address 1Ah) bit description

| Bit | Symbol | Access | Value | Description |
|--------|--------------------------|--------|-------|--|
| 7 to 4 | INIT_ILA_BUFPTR_LN3[3:0] | R/W | 8h | initialization value for lane 3 ILA buffer pointer |
| 3 to 0 | INIT_ILA_BUFPTR_LN2[3:0] | R/W | 8h | initialization value for lane 2 ILA buffer pointer |

Table 105. ERROR_HANDLING register (address 1Bh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------|--------|-----------|---|
| 6 | NAD_ERR_CORR | R/W | | frame assembler (fa) |
| | | | 0 | not-in-table errors passed to fa |
| | | | 1 | nad (nit and disparity) errors passed to fa |
| 5 | KUX_CORR | R/W | | K-character error mode |
| | | | 0 | unexpected K-character errors ignored (at fa) |
| | | | 1 | unexpected K-character errors concealment (at fa) |
| 4 | NAD_CORR | R/W | | nad error mode |
| | | | 0 | nad-errors ignored (at fa) |
| | | | 1 | nad-errors concealment (at fa) |
| 3 to 2 | CORR_MODE[1:0] | R/W | | conceal mode |
| | | | 00 | conceal 1 period at fa |
| | | | 01 | conceal 2 periods at fa |
| | | | 10 | conceal 3 periods at fa |
| | | | 11 | conceal 4 periods at fa |
| 1 | IMPL_ALT | R/W | | disparity error detection configuration |
| | | | 0 | default disparity error detection (table mode) |
| 0 | IGNORE_ERR | R/W | | general error mode |
| | | | 0 | no action |
| | | | 1 | ignore disparity/nit-errors at lane-controller |

Table 106. REINIT_CNTRL register (address 1Ch) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|----------------|--------|----------|---|
| 7 | REINIT_ILA_LN3 | R/W | | lane 3, ila-buffer out-of-range check |
| | | | 0 | no action |
| | | | 1 | lane 3 ila-buffer out-of-range_error activates reinitialization |
| 6 | REINIT_ILA_LN2 | R/W | | lane 2, ila-buffer out-of-range check |
| | | | 0 | no action |
| | | | 1 | lane 2 ila-buffer out-of-range_error activates reinitialization |
| 5 | REINIT_ILA_LN1 | R/W | | lane 1, ila-buffer out-of-range check |
| | | | 0 | no action |
| | | | 1 | lane 1 ila-buffer out-of-range_error activates reinitialization |
| 4 | REINIT_ILA_LN0 | R/W | | lane 0, ila-buffer out-of-range check |
| | | | 0 | no action |
| | | | 1 | lane 0 ila-buffer out-of-range_error activates reinitialization |

Table 106. REINIT_CNTRL register (address 1Ch) bit description ...continued*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|-----|----------------|--------|----------|---|
| 3 | RESYNC_O_L_LN3 | R/W | | lane 3, resync over link |
| | | | 0 | no action |
| | | | 1 | lane 3 lane controller checks for K28.5 /K/ symbols |
| 2 | RESYNC_O_L_LN2 | R/W | | lane 2, resync over link |
| | | | 0 | no action |
| | | | 1 | lane 2 lane controller checks for K28.5 /K/ symbols |
| 1 | RESYNC_O_L_LN1 | R/W | | lane 1, resync over link |
| | | | 0 | no action |
| | | | 1 | lane 1 lane controller checks for K28.5 /K/ symbols |
| 0 | RESYNC_O_L_LN0 | R/W | | lane 0, resync over link |
| | | | 0 | no action |
| | | | 1 | lane 0 controller checks for K28.5 /K/ symbols |

Table 107. PAGE_ADDRESS register (address 1Fh) bit description

| Bit | Symbol | Access | Value | Description |
|--------|-----------|--------|-------|--------------|
| 2 to 0 | PAGE[2:0] | R/W | 0h | page_address |

10.15.2.9 Page 5 allocation map description

Table 108. Page 5 register allocation map

| Address | Register name | R/W | Bit definition | | | | | | | | Default ^[1] | | |
|---------|---------------|----------------------|----------------|-----------------------|----------------------|----------------------|----------------------|-----------------------|----------------------|----------------------|------------------------|----------|-----|
| | | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Bin | Hex | |
| 0 | 00h | ILA_MON_1_0 | R | ILA_MON_LN1[3:0] | | | | ILA_MON_LN0[3:0] | | | | uuuuuuuu | uuh |
| 1 | 01h | ILA_MON_3_2 | R | ILA_MON_LN3[3:0] | | | | ILA_MON_LN2[3:0] | | | | uuuuuuuu | uuh |
| 2 | 02h | ILA_BUF_ERR | R | - | - | - | - | ILA_BUF_ERR_LN3 | ILA_BUF_ERR_LN2 | ILA_BUF_ERR_LN1 | ILA_BUF_ERR_LN0 | uuuuuuuu | uuh |
| 3 | 03h | CA_MON | R | CA_MON_LN3[1:0] | | CA_MON_LN2[1:0] | | CA_MON_LN1[1:0] | | CA_MON_LN0[1:0] | | uuuuuuuu | uuh |
| 4 | 04h | DEC_FLAGS | R | DEC_NIT_ERR_LN3 | DEC_NIT_ERR_LN2 | DEC_NIT_ERR_LN1 | DEC_NIT_ERR_LN0 | DEC_DISP_ERR_LN3 | DEC_DISP_ERR_LN2 | DEC_DISP_ERR_LN1 | DEC_DISP_ERR_LN0 | uuuuuuuu | uuh |
| 5 | 05h | KOUT_FLAG | R | - | - | - | - | DEC_KOUT_LN3 | DEC_KOUT_LN2 | DEC_KOUT_LN1 | DEC_KOUT_LN0 | uuuuuuuu | uuh |
| 6 | 06h | K28_LN0_FLAG | R | - | - | - | K28_7_LN0 | K28_5_LN0 | K28_4_LN0 | K28_3_LN0 | K28_0_LN0 | uuuuuuuu | uuh |
| 7 | 07h | K28_LN1_FLAG | R | - | - | - | K28_7_LN1 | K28_5_LN1 | K28_4_LN1 | K28_3_LN1 | K28_0_LN1 | uuuuuuuu | uuh |
| 8 | 08h | K28_LN2_FLAG | R | - | - | - | K28_7_LN2 | K28_5_LN2 | K28_4_LN2 | K28_3_LN2 | K28_0_LN2 | uuuuuuuu | uuh |
| 9 | 09h | K28_LN3_FLAG | R | - | - | - | K28_7_LN3 | K28_5_LN3 | K28_4_LN3 | K28_3_LN3 | K28_0_LN3 | uuuuuuuu | uuh |
| 10 | 0Ah | KOUT_UNEXPECTED_FLAG | R | - | - | - | - | DEC_KOUT_UNEXP_LN3 | DEC_KOUT_UNEXP_LN2 | DEC_KOUT_UNEXP_LN1 | DEC_KOUT_UNEXP_LN0 | uuuuuuuu | uuh |
| 11 | 0Bh | LOCK_CNT_MON_LN01 | R | LOCK_CNT_MON_LN1[3:0] | | | | LOCK_CNT_MON_LN0[3:0] | | | | uuuuuuuu | uuh |
| 12 | 0Ch | LOCK_CNT_MON_LN23 | R | LOCK_CNT_MON_LN3[3:0] | | | | LOCK_CNT_MON_LN2[3:0] | | | | uuuuuuuu | uuh |
| 13 | 0Dh | CS_STATE_LNX | R | CS_STATE_LN3[1:0] | | CS_STATE_LN2[1:0] | | CS_STATE_LN1[1:0] | | CS_STATE_LN0[1:0] | | uuuuuuuu | uuh |
| 14 | 0Eh | RST_BUF_ERR_FLAGS | R/W | RST_BUF_ERR_FLAGS | - | - | - | - | - | - | - | 00000000 | 00h |
| 15 | 0Fh | INTR_MISC_ENA | R/W | INTR_ENA_CS_INIT_LN3 | INTR_ENA_CS_INIT_LN2 | INTR_ENA_CS_INIT_LN1 | INTR_ENA_CS_INIT_LN0 | INTR_ENA_BUF_ERR_LN3 | INTR_ENA_BUF_ERR_LN2 | INTR_ENA_BUF_ERR_LN1 | INTR_ENA_BUF_ERR_LN0 | 00000000 | 00h |
| 16 | 10h | FLAG_CNT_LSB_LN0 | R | FLAG_CNT_LN0[7:0] | | | | | | | | uuuuuuuu | uuh |

Table 108. Page 5 register allocation map ...continued

| Address | | Register name | R/W | Bit definition | | | | | | | | Default ^[1] | |
|---------|-----|--------------------|-----|--------------------|--------------------|----------------|---------------------------|-------------------|-------------------|-------------------|-------------------|------------------------|-----|
| | | | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Bin | Hex |
| 17 | 11h | FLAG_CNT_MSB_LN0 | R | FLAG_CNT_LN0[15:8] | | | | | | | | uuuuuuuu | uuh |
| 18 | 12h | FLAG_CNT_LSB_LN1 | R | FLAG_CNT_LN1[7:0] | | | | | | | | uuuuuuuu | uuh |
| 19 | 13h | FLAG_CNT_MSB_LN1 | R | FLAG_CNT_LN1[15:8] | | | | | | | | uuuuuuuu | uuh |
| 20 | 14h | FLAG_CNT_LSB_LN2 | R | FLAG_CNT_LN2[7:0] | | | | | | | | uuuuuuuu | uuh |
| 21 | 15h | FLAG_CNT_MSB_LN2 | R | FLAG_CNT_LN2[15:8] | | | | | | | | uuuuuuuu | uuh |
| 22 | 16h | FLAG_CNT_LSB_LN3 | R | FLAG_CNT_LN3[7:0] | | | | | | | | uuuuuuuu | uuh |
| 23 | 17h | FLAG_CNT_MSB_LN3 | R | FLAG_CNT_LN3[15:8] | | | | | | | | uuuuuuuu | uuh |
| 24 | 18h | BER_LEVEL_LSB | R/W | BER_LEVEL[7:0] | | | | | | | | 00000000 | 00h |
| 25 | 19h | BER_LEVEL_MSB | R/W | BER_LEVEL[15:8] | | | | | | | | 00000000 | 00h |
| 26 | 1Ah | INTR_ENA | R/W | INTR_ENA_NIT | INTR_ENA_DISP | INTR_ENA_KOUT | INTR_ENA_KOUT_UNEXP | INTR_ENA_K28_7 | INTR_ENA_K28_5 | INTR_ENA_K28_3 | INTR_ENA_MISC | 00000000 | 00h |
| 27 | 1Bh | CNTRL_FLAGCNT_LN01 | R/W | RST_CFC_LN1 | SEL_CFC_LN1[2:0] | | | RST_CFC_LN0 | SEL_CFC_LN0[2:0] | | | 01010101 | 55h |
| 28 | 1Ch | CNTRL_FLAGCNT_LN23 | R/W | RST_CFC_LN3 | SEL_CFC_LN3[2:0] | | | RST_CFC_LN2 | SEL_CFC_LN2[2:0] | | | 01010101 | 55h |
| 29 | 1Dh | MON_FLAGS_RESET | R/W | RST_NIT_ERR_FLAGS | RST_DISP_ERR_FLAGS | RST_KOUT_FLAGS | RST_KOUT_UNEXPECTED_FLAGS | RST_K28_LN3_FLAGS | RST_K28_LN2_FLAGS | RST_K28_LN1_FLAGS | RST_K28_LN0_FLAGS | 00000000 | 00h |
| 30 | 1Eh | DBG_CNTRL | R/W | BER_MODE | INTR_CLEAR | INTR_MODE[2:0] | | | - | - | - | 00000000 | 00h |
| 31 | 1Fh | PAGE_ADDRESS | R/W | - | - | - | - | - | PAGE[2:0] | | | 00000000 | 00h |

[1] u = undefined at power-up or after reset.

10.15.2.10 Page 5 bit definition detailed description

Please refer to [Table 108](#) for a register overview and their default values. In the following tables, all the values emphasized in bold are the default values.

Table 109. ILA_MON_1_0 register (address 00h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------|--------|-------|---------------------|
| 7 to 4 | ILA_MON_LN1[3:0] | R | - | ila_buf_In1 pointer |
| 3 to 0 | ILA_MON_LN0[3:0] | R | - | ila_buf_In0 pointer |

Table 110. ILA_MON_3_2 register (address 01h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------|--------|-------|---------------------|
| 7 to 4 | ILA_MON_LN3[3:0] | R | - | ila_buf_In3 pointer |
| 3 to 0 | ILA_MON_LN2[3:0] | R | - | ila_buf_In2 pointer |

Table 111. ILA_BUF_ERR register (address 02h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|-----------------|--------|-------|-------------------------------------|
| 3 | ILA_BUF_ERR_LN3 | R | | lane 3 ila buffer error |
| | | | 0 | ila_buf_In3 pointer is in range |
| | | | 1 | ila_buf_In3 pointer is out of range |
| 2 | ILA_BUF_ERR_LN2 | R | | lane 2 ila buffer error |
| | | | 0 | ila_buf_In2 pointer is in range |
| | | | 1 | ila_buf_In2 pointer is out of range |
| 1 | ILA_BUF_ERR_LN1 | R | | lane 1 ila buffer error |
| | | | 0 | ila_buf_In1 pointer is in range |
| | | | 1 | ila_buf_In1 pointer is out of range |
| 0 | ILA_BUF_ERR_LN0 | R | | lane 0 ila buffer error |
| | | | 0 | ila_buf_In0 pointer is in range |
| | | | 1 | ila_buf_In0 pointer is out of range |

Table 112. CA_MON register (address 03h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------------|--------|-------|--------------------------------------|
| 7 to 6 | CA_MON_LN3[1:0] | R | - | clock alignment phase monitor lane 3 |
| 5 to 4 | CA_MON_LN2[1:0] | R | - | clock alignment phase monitor lane 2 |
| 3 to 2 | CA_MON_LN1[1:0] | R | - | clock alignment phase monitor lane 1 |
| 1 to 0 | CA_MON_LN0[1:0] | R | - | clock alignment phase monitor lane 0 |

Table 113. DEC_FLAGS register (address 04h) bit description

| Bit | Symbol | Access | Value | Description |
|-----|------------------|--------|-------|--------------------------------|
| 7 | DEC_NIT_ERR_LN3 | R | - | not-in-table error flag lane 3 |
| 6 | DEC_NIT_ERR_LN2 | R | - | not-in-table error flag lane 2 |
| 5 | DEC_NIT_ERR_LN1 | R | - | not-in-table error flag lane 1 |
| 4 | DEC_NIT_ERR_LN0 | R | - | not-in-table error flag lane 0 |
| 3 | DEC_DISP_ERR_LN3 | R | - | disparity error flag lane 3 |
| 2 | DEC_DISP_ERR_LN2 | R | - | disparity error flag lane 2 |
| 1 | DEC_DISP_ERR_LN1 | R | - | disparity error flag lane 1 |
| 0 | DEC_DISP_ERR_LN0 | R | - | disparity error flag lane 0 |

Table 114. KOUT_FLAG register (address 05h) bit description

| Bit | Symbol | Access | Value | Description |
|-----|--------------|--------|-------|-----------------------------|
| 3 | DEC_KOUT_LN3 | R | - | /K/ symbols found in lane 3 |
| 2 | DEC_KOUT_LN2 | R | - | /K/ symbols found in lane 2 |
| 1 | DEC_KOUT_LN1 | R | - | /K/ symbols found in lane 1 |
| 0 | DEC_KOUT_LN0 | R | - | /K/ symbols found in lane 0 |

Table 115. K28_LN0_FLAG register (address 06h) bit description

| Bit | Symbol | Access | Value | Description |
|-----|-----------|--------|-------|-----------------------------------|
| 4 | K28_7_LN0 | R | - | K28_7 /F/ symbols found in lane 0 |
| 3 | K28_5_LN0 | R | - | K28_5 /K/ symbols found in lane 0 |
| 2 | K28_4_LN0 | R | - | K28_4 /Q/ symbols found in lane 0 |
| 1 | K28_3_LN0 | R | - | K28_3 /A/ symbols found in lane 0 |
| 0 | K28_0_LN0 | R | - | K28_0 /R/ symbols found in lane 0 |

Table 116. K28_LN1_FLAG register (address 07h) bit description

| Bit | Symbol | Access | Value | Description |
|-----|-----------|--------|-------|-----------------------------------|
| 4 | K28_7_LN1 | R | - | K28_7 /F/ symbols found in lane 1 |
| 3 | K28_5_LN1 | R | - | K28_5 /K/ symbols found in lane 1 |
| 2 | K28_4_LN1 | R | - | K28_4 /Q/ symbols found in lane 1 |
| 1 | K28_3_LN1 | R | - | K28_3 /A/ symbols found in lane 1 |
| 0 | K28_0_LN1 | R | - | K28_0 /R/ symbols found in lane 1 |

Table 117. K28_LN2_FLAG register (address 08h) bit description

| Bit | Symbol | Access | Value | Description |
|-----|-----------|--------|-------|-----------------------------------|
| 4 | K28_7_LN2 | R | - | K28_7 /F/ symbols found in lane 2 |
| 3 | K28_5_LN2 | R | - | K28_5 /K/ symbols found in lane 2 |
| 2 | K28_4_LN2 | R | - | K28_4 /Q/ symbols found in lane 2 |
| 1 | K28_3_LN2 | R | - | K28_3 /A/ symbols found in lane 2 |
| 0 | K28_0_LN2 | R | - | K28_0 /R/ symbols found in lane 2 |

Table 118. K28_LN3_FLAG register (address 09h) bit description

| Bit | Symbol | Access | Value | Description |
|-----|-----------|--------|-------|-----------------------------------|
| 4 | K28_7_LN3 | R | - | K28_7 /F/ symbols found in lane 3 |
| 3 | K28_5_LN3 | R | - | K28_5 /K/ symbols found in lane 3 |
| 2 | K28_4_LN3 | R | - | K28_4 /Q/ symbols found in lane 3 |
| 1 | K28_3_LN3 | R | - | K28_3 /A/ symbols found in lane 3 |
| 0 | K28_0_LN3 | R | - | K28_0 /R/ symbols found in lane 3 |

Table 119. KOUT_UNEXPECTED_FLAG register (address 0Ah) bit description

| Bit | Symbol | Access | Value | Description |
|-----|--------------------|--------|-------|--|
| 3 | DEC_KOUT_UNEXP_LN3 | R | - | unexpected /K/ symbols found in lane 3 |
| 2 | DEC_KOUT_UNEXP_LN2 | R | - | unexpected /K/ symbols found in lane 2 |
| 1 | DEC_KOUT_UNEXP_LN1 | R | - | unexpected /K/ symbols found in lane 1 |
| 0 | DEC_KOUT_UNEXP_LN0 | R | - | unexpected /K/ symbols found in lane 0 |

Table 120. LOCK_CNT_MON_LN01 register (address 0Bh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------------------|--------|-------|--|
| 7 to 4 | LOCK_CNT_MON_LN1[3:0] | R | - | lock_state monitor synchronization word alignment lane 1 |
| 3 to 0 | LOCK_CNT_MON_LN0[3:0] | R | - | lock_state monitor synchronization word alignment lane 0 |

Table 121. LOCK_CNT_MON_LN23 register (address 0Ch) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------------------|--------|-------|--|
| 7 to 4 | LOCK_CNT_MON_LN3[3:0] | R | - | lock_state monitor synchronization word alignment lane 3 |
| 3 to 0 | LOCK_CNT_MON_LN2[3:0] | R | - | lock_state monitor synchronization word alignment lane 2 |

Table 122. CS_STATE_LNX register (address 0Dh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|-------|--|
| 7 to 6 | CS_STATE_LN3[1:0] | R | - | monitor cs_state fsm lane 3 (see Table 142) |
| 5 to 4 | CS_STATE_LN2[1:0] | R | - | monitor cs_state fsm lane 2 (see Table 142) |
| 3 to 2 | CS_STATE_LN1[1:0] | R | - | monitor cs_state fsm lane 1 (see Table 142) |
| 1 to 0 | CS_STATE_LN0[1:0] | R | - | monitor cs_state fsm lane 0 (see Table 142) |

Table 123. RST_BUF_ERR_FLAGS register (address 0Eh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|-------------------|--------|-------|-----------------------------|
| 7 | RST_BUF_ERR_FLAGS | R/W | 0 | reset ILA_BUF_ERR_LNn flags |

Table 124. INTR_MISC_ENA register (address 0Fh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|-----|----------------------|--------|-------|---|
| 7 | INTR_ENA_CS_INIT_LN3 | R/W | 0 | intr_misc in case cs_state_ln3 = cs_init |
| 6 | INTR_ENA_CS_INIT_LN2 | R/W | 0 | intr_misc in case cs_state_ln2 = cs_init |
| 5 | INTR_ENA_CS_INIT_LN1 | R/W | 0 | intr_misc in case cs_state_ln1 = cs_init |
| 4 | INTR_ENA_CS_INIT_LN0 | R/W | 0 | intr_misc in case cs_state_ln0 = cs_init |
| 3 | INTR_ENA_BUF_ERR_LN3 | R/W | 0 | generate interrupt if ILA_BUF_ERR_LN3 = 1 |
| 2 | INTR_ENA_BUF_ERR_LN2 | R/W | 0 | generate interrupt if ILA_BUF_ERR_LN2 = 1 |
| 1 | INTR_ENA_BUF_ERR_LN1 | R/W | 0 | generate interrupt if ILA_BUF_ERR_LN1 = 1 |
| 0 | INTR_ENA_BUF_ERR_LN0 | R/W | 0 | generate interrupt if ILA_BUF_ERR_LN0 = 1 |

Table 125. FLAG_CNT_LSB_LN0 register (address 10h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|-------|-----------------------------|
| 7 to 0 | FLAG_CNT_LN0[7:0] | R | - | LSBs of flag_counter lane 0 |

Table 126. FLAG_CNT_MSB_LN0 register (address 11h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------------|--------|-------|-----------------------------|
| 7 to 0 | FLAG_CNT_LN0[15:8] | R | - | MSBs of flag_counter lane 0 |

Table 127. FLAG_CNT_LSB_LN1 register (address 12h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|-------|-----------------------------|
| 7 to 0 | FLAG_CNT_LN1[7:0] | R | - | LSBs of flag_counter lane 1 |

Table 128. FLAG_CNT_MSB_LN1 register (address 13h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------------|--------|-------|-----------------------------|
| 7 to 0 | FLAG_CNT_LN1[15:8] | R | - | MSBs of flag_counter lane 1 |

Table 129. FLAG_CNT_LSB_LN2 register (address 14h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|-------|-----------------------------|
| 7 to 0 | FLAG_CNT_LN2[7:0] | R | - | LSBs of flag_counter lane 2 |

Table 130. FLAG_CNT_MSB_LN2 register (address 15h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------------|--------|-------|-----------------------------|
| 7 to 0 | FLAG_CNT_LN2[15:8] | R | - | MSBs of flag_counter lane 2 |

Table 131. FLAG_CNT_LSB_LN3 register (address 16h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------------|--------|-------|-----------------------------|
| 7 to 0 | FLAG_CNT_LN3[7:0] | R | - | LSBs of flag_counter lane 3 |

Table 132. FLAG_CNT_MSB_LN3 register (address 17h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------------|--------|-------|-----------------------------|
| 7 to 0 | FLAG_CNT_LN3[15:8] | R | - | MSBs of flag_counter lane 3 |

Table 133. BER_LEVEL_LSB register (address 18h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|----------------|--------|-------|---|
| 7 to 0 | BER_LEVEL[7:0] | R/W | 00h | LSBs level used for simple (DC) BER-measurement |

Table 134. BER_LEVEL_MSB register (address 19h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-----------------|--------|-------|---|
| 7 to 0 | BER_LEVEL[15:8] | R/W | 00h | MSBs level used for simple (DC) BER-measurement |

Table 135. INTR_ENA register (address 1Ah) bit description

| Bit | Symbol | Access | Value | Description |
|-----|---------------------|--------|-------|---|
| 7 | INTR_ENA_NIT | R/W | | not-in-table interrupt |
| | | | 0 | no action |
| 6 | INTR_ENA_DISP | R/W | 1 | nit-error in ln<x> affects i_ln<x> |
| | | | 0 | no action |
| 5 | INTR_ENA_KOUT | R/W | 1 | disparity-error interrupt |
| | | | 0 | no action |
| 4 | INTR_ENA_KOUT_UNEXP | R/W | 1 | disparity-error in ln<x> affects i_ln<x> |
| | | | 0 | no action |
| 3 | INTR_ENA_K28_7 | R/W | 1 | K-character interrupt |
| | | | 0 | no action |
| 2 | INTR_ENA_K28_5 | R/W | 1 | detection k-control character in ln<x> affects i_ln<x> |
| | | | 0 | no action |
| 1 | INTR_ENA_K28_3 | R/W | 1 | detection unexpected K-character in ln<x> affects i_ln<x> |
| | | | 0 | no action |
| 0 | INTR_ENA_MISC | R/W | 1 | K28_7 interrupt |
| | | | 0 | no action |
| | | | 1 | detection K28_7 in ln<x> affects i_ln<x> |
| | | | 0 | no action |
| | | | 1 | K28_5 interrupt |
| | | | 0 | no action |
| | | | 1 | detection K28_5 in ln<x> affects i_ln<x> |
| | | | 0 | no action |
| | | | 1 | K28_3 interrupt |
| | | | 0 | no action |
| | | | 1 | detection K28_3 in ln<x> affects i_ln<x> |
| | | | 0 | no action |
| | | | 1 | miscellaneous interrupt |
| | | | 0 | no action |
| | | | 1 | detection depends on intr_misc_ena (see Table 124) |
| | | | 0 | no action |

Table 136. CNTRL_FLAGCNT_LN01 register (address 1Bh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------|--------|-------|---|
| 7 | RST_CFC_LN1 | R/W | 0 | reset FLAG_CNT_LN1 |
| 6 to 4 | SEL_CFC_LN1[2:0] | R/W | 5h | select FLAG_CNT_LN1 source (see Table 141) |
| 3 | RST_CFC_LN0 | R/W | 0 | reset FLAG_CNT_LN0 |
| 2 to 0 | SEL_CFC_LN0[2:0] | R/W | 5h | select FLAG_CNT_LN0 source (see Table 141) |

Table 137. CNTRL_FLAGCNT_LN23 register (address 1Ch) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------------|--------|-------|---|
| 7 | RST_CFC_LN3 | R/W | 0 | reset FLAG_CNT_LN3 |
| 6 to 4 | SEL_CFC_LN3[2:0] | R/W | 5h | select FLAG_CNT_LN3 source (see Table 141) |
| 3 | RST_CFC_LN2 | R/W | 0 | reset FLAG_CNT_LN2 |
| 2 to 0 | SEL_CFC_LN2[2:0] | R/W | 5h | select FLAG_CNT_LN2 source (see Table 141) |

Table 138. MON_FLAGS_RESET register (address 1Dh) bit description

| Bit | Symbol | Access | Value | Description |
|-----|---------------------------|--------|-------|--|
| 7 | RST_NIT_ERR_FLAGS | R/W | 0 | reset nit-error monitor flags |
| 6 | RST_DISP_ERR_FLAGS | R/W | 0 | reset disparity monitor flags |
| 5 | RST_KOUT_FLAGS | R/W | 0 | reset K symbols monitor flags |
| 4 | RST_KOUT_UNEXPECTED_FLAGS | R/W | 0 | reset unexpected K symbols monitor flags |
| 3 | RST_K28_LN3_FLAGS | R/W | 0 | reset K28_x monitor flags for lane 3 |
| 2 | RST_K28_LN2_FLAGS | R/W | 0 | reset K28_x monitor flags for lane 2 |
| 1 | RST_K28_LN1_FLAGS | R/W | 0 | reset K28_x monitor flags for lane 1 |
| 0 | RST_K28_LN0_FLAGS | R/W | 0 | reset K28_x monitor flags for lane 0 |

Table 139. DBG_CNTRL register (address 1Eh) bit description

| Bit | Symbol | Access | Value | Description |
|--------|----------------|--------|------------|--|
| 7 | BER_MODE | R/W | | simple BER-measurement |
| | | | 0 | no action |
| | | | 1 | simple BER-measurement enabled |
| 6 | INTR_CLEAR | R/W | | interrupts clear |
| | | | 0 | no action |
| | | | 1 | clear interrupts (to '1') |
| 5 to 3 | INTR_MODE[2:0] | R/W | | interrupt settings |
| | | | 000 | global interrupt depends on lane 0 |
| | | | 001 | global interrupt depends on lane 1 |
| | | | 010 | global interrupt depends on lane 2 |
| | | | 011 | global interrupt depends on lane 3 |
| | | | 100 | global interrupt depends on lane 0 or lane 1 |
| | | | 101 | global interrupt depends on lane 2 or lane 3 |
| | | | 110 | global interrupt depends on lane 0 or lane 1 or lane 2 or lane 3 |
| | | | 111 | no interrupt |

Table 140. PAGE_ADDRESS register (address 1Fh) bit description

| Bit | Symbol | Access | Value | Description |
|--------|-----------|--------|-------|--------------|
| 2 to 0 | PAGE[2:0] | R/W | 0h | page_address |

Table 141. Counter source

Default settings are shown highlighted.

| SEL_CFC_LNn[2:0] | Source |
|------------------|---------------------------|
| 000 | not-in-table error |
| 001 | disparity error |
| 010 | K symbol found |
| 011 | unexpected K symbol found |
| 100 | K28_7 (/F) symbol found |
| 101 | K28_5 (/K) symbol found |
| 110 | K28_3 (/A) symbol found |
| 111 | K28_0 (/R) symbol found |

Table 142. Code group synchronization state machine

| CS_STATE_LNn[1:0] | Definition |
|-------------------|--|
| 00 | looking for K28_5 (/K) symbol |
| 01 | four consecutive K28_5 (/K) symbols have been received |
| 10 | code group synchronization achieved |
| 11 | not applicable |

10.15.2.11 Page 6 allocation map description

Table 143. Page 6 register allocation map

| Address | Register name | R/W | Bit definition | | | | | | | | Default ^[1] | | |
|---------|---------------|------------|----------------|---------------|----|----|--------------|--------------|----|----|------------------------|----------|------|
| | | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Bin | Hex | |
| 0 | 00h | LN0_CFG_0 | R | LN0_DID[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 1 | 01h | LN0_CFG_1 | R | - | - | - | - | LN0_BID[3:0] | | | | uuuuuuuu | 0xuu |
| 2 | 02h | LN0_CFG_2 | R | - | - | - | LN0_LID[4:0] | | | | uuuuuuuu | 0xuu | |
| 3 | 03h | LN0_CFG_3 | R | LN0_SCR | - | - | LN0_L[4:0] | | | | uuuuuuuu | 0xuu | |
| 4 | 04h | LN0_CFG_4 | R | LN0_F[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 5 | 05h | LN0_CFG_5 | R | - | - | - | LN0_K[4:0] | | | | uuuuuuuu | 0xuu | |
| 6 | 06h | LN0_CFG_6 | R | LN0_M[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 7 | 07h | LN0_CFG_7 | R | LN0_CS[1:0] | | - | LN0_N[4:0] | | | | uuuuuuuu | 0xuu | |
| 8 | 08h | LN0_CFG_8 | R | - | - | - | LN0_N'[4:0] | | | | uuuuuuuu | 0xuu | |
| 9 | 09h | LN0_CFG_9 | R | - | - | - | LN0_S[4:0] | | | | uuuuuuuu | 0xuu | |
| 10 | 0Ah | LN0_CFG_10 | R | LN0_HD | - | - | LN0_CF[4:0] | | | | uuuuuuuu | 0xuu | |
| 11 | 0Bh | LN0_CFG_11 | R | LN0_RES1[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 12 | 0Ch | LN0_CFG_12 | R | LN0_RES2[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 13 | 0Dh | LN0_CFG_13 | R | LN0_FCHK[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 16 | 10h | LN1_CFG_0 | R | LN1_DID[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 17 | 11h | LN1_CFG_1 | R | - | - | - | - | LN1_BID[3:0] | | | | uuuuuuuu | 0xuu |
| 18 | 12h | LN1_CFG_2 | R | - | - | - | LN1_LID[4:0] | | | | uuuuuuuu | 0xuu | |
| 19 | 13h | LN1_CFG_3 | R | LN1_SCR | - | - | LN1_L[4:0] | | | | uuuuuuuu | 0xuu | |
| 20 | 14h | LN1_CFG_4 | R | LN1_F[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 21 | 15h | LN1_CFG_5 | R | - | - | - | LN1_K[4:0] | | | | uuuuuuuu | 0xuu | |
| 22 | 16h | LN1_CFG_6 | R | LN1_M[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 23 | 17h | LN1_CFG_7 | R | LN1_CS[1:0] | | - | LN1_N[4:0] | | | | uuuuuuuu | 0xuu | |
| 24 | 18h | LN1_CFG_8 | R | - | - | - | LN1_N'[4:0] | | | | uuuuuuuu | 0xuu | |
| 25 | 19h | LN1_CFG_9 | R | - | - | - | LN1_S[4:0] | | | | uuuuuuuu | 0xuu | |
| 26 | 1Ah | LN1_CFG_10 | R | LN1_HD | - | - | LN1_CF[4:0] | | | | uuuuuuuu | 0xuu | |
| 27 | 1Bh | LN1_CFG_11 | R | LN1_RES1[7:0] | | | | | | | | uuuuuuuu | 0xuu |

Table 143. Page 6 register allocation map ...continued

| Address | Register name | R/W | Bit definition | | | | | | | | Default ^[1] | | |
|---------|---------------|--------------|----------------|---------------|----|----|----|----|-----------|----|------------------------|----------|------|
| | | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Bin | Hex | |
| 28 | 1Ch | LN1_CFG_12 | R | LN1_RES2[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 29 | 1Dh | LN1_CFG_13 | R | LN1_FCHK[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 31 | 1Fh | PAGE_ADDRESS | R/W | - | - | - | - | - | PAGE[2:0] | | 00000000 | 00h | |

[1] u = undefined at power-up or after reset.

10.15.2.12 Page 6 bit definition detailed description

Please refer to [Table 143](#) for a register overview and their default values. In the following tables, all the values emphasized in bold are the default values.

Table 144. LN0_CFG_0 register (address 00h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------|--------|-------|------------------|
| 7 to 0 | LN0_DID[7:0] | R | - | lane 0 device ID |

Table 145. LN0_CFG_1 register (address 01h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------|--------|-------|----------------|
| 3 to 0 | LN0_BID[3:0] | R | - | lane 0 bank ID |

Table 146. LN0_CFG_2 register (address 02h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------|--------|-------|----------------|
| 4 to 0 | LN0_LID[4:0] | R | - | lane 0 lane ID |

Table 147. LN0_CFG_3 register (address 03h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|-------------------------|
| 7 | LN0_SCR | R | - | scrambling on |
| 4 to 0 | LN0_L[4:0] | R | - | number of lanes minus 1 |

Table 148. LN0_CFG_4 register (address 04h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|------------------------------------|
| 7 to 0 | LN0_F[7:0] | R | - | number of octets per frame minus 1 |

Table 149. LN0_CFG_5 register (address 05h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|--|
| 4 to 0 | LN0_K[4:0] | R | - | number of frames per multi-frame minus 1 |

Table 150. LN0_CFG_6 register (address 06h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|---|
| 7 to 0 | LN0_M[7:0] | R | - | number of converters per device minus 1 |

Table 151. LN0_CFG_7 register (address 07h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------|--------|-------|------------------------------|
| 7 to 6 | LN0_CS[1:0] | R | - | number of control bits |
| 4 to 0 | LN0_N[4:0] | R | - | converter resolution minus 1 |

Table 152. LN0_CFG_8 register (address 08h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------|--------|-------|-----------------------------------|
| 4 to 0 | LN0_N'[4:0] | R | - | number of bits per sample minus 1 |

Table 153. LN0_CFG_9 register (address 09h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|---|
| 4 to 0 | LN0_S[4:0] | R | - | number of samples per converter per frame cycle minus 1 |

Table 154. LN0_CFG_10 register (address 0Ah) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------|--------|-------|---|
| 7 | LN0_HD | R | - | high density |
| 4 to 0 | LN0_CF[4:0] | R | - | number of control words per frame cycle |

Table 155. LN0_CFG_11 register (address 0Bh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-------|-----------------------|
| 7 to 0 | LN0_RES1[7:0] | R | - | lane 0 reserved field |

Table 156. LN0_CFG_12 register (address 0Ch) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-------|-----------------------|
| 7 to 0 | LN0_RES2[7:0] | R | - | lane 0 reserved field |

Table 157. LN0_CFG_13 register (address 0Dh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-------|-----------------|
| 7 to 0 | LN0_FCHK[7:0] | R | - | lane 0 checksum |

Table 158. LN1_CFG_0 register (address 10h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------|--------|-------|------------------|
| 7 to 0 | LN1_DID[7:0] | R | - | lane 1 device ID |

Table 159. LN1_CFG_1 register (address 11h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------|--------|-------|----------------|
| 3 to 0 | LN1_BID[3:0] | R | - | lane 1 bank ID |

Table 160. LN1_CFG_2 register (address 12h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------|--------|-------|----------------|
| 4 to 0 | LN1_LID[4:0] | R | - | lane 1 lane ID |

Table 161. LN1_CFG_3 register (address 13h) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|-------------------------|
| 7 | LN1_SCR | R | - | scrambling on |
| 4 to 0 | LN1_L[4:0] | R | - | number of lanes minus 1 |

Table 162. LN1_CFG_4 register (address 14h) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|------------------------------------|
| 7 to 0 | LN1_F[7:0] | R | - | number of octets per frame minus 1 |

Table 163. LN1_CFG_5 register (address 15h) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|---|
| 4 to 0 | LN1_K[4:0] | R | - | number of frames per multiframe minus 1 |

Table 164. LN1_CFG_6 register (address 16h) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|---|
| 7 to 0 | LN1_M[7:0] | R | - | number of converters per device minus 1 |

Table 165. LN1_CFG_7 register (address 17h) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|-------------|--------|-------|------------------------------|
| 7 to 6 | LN1_CS[1:0] | R | - | number of control bits |
| 4 to 0 | LN1_N[4:0] | R | - | converter resolution minus 1 |

Table 166. LN1_CFG_8 register (address 18h) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|-------------|--------|-------|-----------------------------------|
| 4 to 0 | LN1_N'[4:0] | R | - | number of bits per sample minus 1 |

Table 167. LN1_CFG_9 register (address 19h) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|---|
| 4 to 0 | LN1_S[4:0] | R | - | number of samples per converter per frame cycle minus 1 |

Table 168. LN1_CFG_10 register (address 1Ah) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|-------------|--------|-------|---|
| 7 to 6 | LN1_HD | R | - | high density |
| 4 to 0 | LN1_CF[4:0] | R | - | number of control words per frame cycle |

Table 169. LN1_CFG_11 register (address 1Bh) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-------|-----------------------|
| 7 to 0 | LN1_RES1[7:0] | R | - | lane 1 reserved field |

Table 170. LN1_CFG_12 register (address 1Ch) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-------|-----------------------|
| 7 to 0 | LN1_RES2[7:0] | R | - | lane 1 reserved field |

Table 171. LN1_CFG_13 register (address 1Dh) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-------|-----------------|
| 7 to 0 | LN1_FCHK[7:0] | R | - | lane 1 checksum |

Table 172. PAGE_ADDRESS register (address 1Fh) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|-----------|--------|-------|--------------|
| 2 to 0 | PAGE[2:0] | R/W | 0h | page_address |

10.15.2.13 Page 7 allocation map description

Table 173. Page 7 register allocation map

| Address | Register name | R/W | Bit definition | | | | | | | | Default ^[1] | | |
|---------|---------------|------------|----------------|---------------|----|----|--------------|--------------|----|----|------------------------|----------|------|
| | | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Bin | Hex | |
| 0 | 00h | LN2_CFG_0 | R | LN2_DID[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 1 | 01h | LN2_CFG_1 | R | - | - | - | - | LN2_BID[3:0] | | | | uuuuuuuu | 0xuu |
| 2 | 02h | LN2_CFG_2 | R | - | - | - | LN2_LID[4:0] | | | | uuuuuuuu | 0xuu | |
| 3 | 03h | LN2_CFG_3 | R | LN2_SCR | - | - | LN2_L[4:0] | | | | uuuuuuuu | 0xuu | |
| 4 | 04h | LN2_CFG_4 | R | LN2_F[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 5 | 05h | LN2_CFG_5 | R | - | - | - | LN2_K[4:0] | | | | uuuuuuuu | 0xuu | |
| 6 | 06h | LN2_CFG_6 | R | LN2_M[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 7 | 07h | LN2_CFG_7 | R | LN2_CS[1:0] | | - | LN2_N[4:0] | | | | uuuuuuuu | 0xuu | |
| 8 | 08h | LN2_CFG_8 | R | - | - | - | LN2_N'[4:0] | | | | uuuuuuuu | 0xuu | |
| 9 | 09h | LN2_CFG_9 | R | - | - | - | LN2_S[4:0] | | | | uuuuuuuu | 0xuu | |
| 10 | 0Ah | LN2_CFG_10 | R | LN2_HD | - | - | LN2_CF[4:0] | | | | uuuuuuuu | 0xuu | |
| 11 | 0Bh | LN2_CFG_11 | R | LN2_RES1[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 12 | 0Ch | LN2_CFG_12 | R | LN2_RES2[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 13 | 0Dh | LN2_CFG_13 | R | LN2_FCHK[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 16 | 10h | LN3_CFG_0 | R | LN3_DID[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 17 | 11h | LN3_CFG_1 | R | - | - | - | - | LN3_BID[3:0] | | | | uuuuuuuu | 0xuu |
| 18 | 12h | LN3_CFG_2 | R | - | - | - | LN3_LID[4:0] | | | | uuuuuuuu | 0xuu | |
| 19 | 13h | LN3_CFG_3 | R | LN3_SCR | - | - | LN3_L[4:0] | | | | uuuuuuuu | 0xuu | |
| 20 | 14h | LN3_CFG_4 | R | LN3_F[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 21 | 15h | LN3_CFG_5 | R | - | - | - | LN3_K[4:0] | | | | uuuuuuuu | 0xuu | |
| 22 | 16h | LN3_CFG_6 | R | LN3_M[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 23 | 17h | LN3_CFG_7 | R | LN3_CS[1:0] | | - | LN3_N[4:0] | | | | uuuuuuuu | 0xuu | |
| 24 | 18h | LN3_CFG_8 | R | - | - | - | LN3_N'[4:0] | | | | uuuuuuuu | 0xuu | |
| 25 | 19h | LN3_CFG_9 | R | - | - | - | LN3_S[4:0] | | | | uuuuuuuu | 0xuu | |
| 26 | 1Ah | LN3_CFG_10 | R | LN3_HD | - | - | LN3_CF[4:0] | | | | uuuuuuuu | 0xuu | |
| 27 | 1Bh | LN3_CFG_11 | R | LN3_RES1[7:0] | | | | | | | | uuuuuuuu | 0xuu |

Table 173. Page 7 register allocation map ...continued

| Address | Register name | R/W | Bit definition | | | | | | | | Default ^[1] | | |
|---------|---------------|--------------|----------------|---------------|----|----|----|----|-----------|----|------------------------|----------|------|
| | | | b7 | b6 | b5 | b4 | b3 | b2 | b1 | b0 | Bin | Hex | |
| 28 | 1Ch | LN3_CFG_12 | R | LN3_RES2[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 29 | 1Dh | LN3_CFG_13 | R | LN3_FCHK[7:0] | | | | | | | | uuuuuuuu | 0xuu |
| 31 | 1Fh | PAGE_ADDRESS | R/W | - | - | - | - | - | PAGE[2:0] | | 00000000 | 00h | |

[1] u = undefined at power-up or after reset.

10.15.2.14 Page 7 bit definition detailed description

Please refer to [Table 173](#) for a register overview and their default values. In the following tables, all the values emphasized in bold are the default values.

Table 174. LN2_CFG_0 register (address 00h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------|--------|-------|------------------|
| 7 to 0 | LN2_DID[7:0] | R | - | lane 2 device ID |

Table 175. LN2_CFG_1 register (address 01h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------|--------|-------|----------------|
| 3 to 0 | LN2_BID[3:0] | R | - | lane 2 bank ID |

Table 176. LN2_CFG_2 register (address 02h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------|--------|-------|----------------|
| 4 to 0 | LN2_LID[4:0] | R | - | lane 2 lane ID |

Table 177. LN2_CFG_3 register (address 03h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|-------------------------|
| 7 | LN2_SCR | R | - | scrambling on |
| 4 to 0 | LN2_L[4:0] | R | - | number of lanes minus 1 |

Table 178. LN2_CFG_4 register (address 04h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|------------------------------------|
| 7 to 0 | LN2_F[7:0] | R | - | number of octets per frame minus 1 |

Table 179. LN2_CFG_5 register (address 05h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|---|
| 4 to 0 | LN2_K[4:0] | R | - | number of frames per multiframe minus 1 |

Table 180. LN2_CFG_6 register (address 06h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|---|
| 7 to 0 | LN2_M[7:0] | R | - | number of converters per device minus 1 |

Table 181. LN2_CFG_7 register (address 07h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------|--------|-------|------------------------------|
| 7 to 6 | LN2_CS[1:0] | R | - | number of control bits |
| 4 to 0 | LN2_N[4:0] | R | - | converter resolution minus 1 |

Table 182. LN2_CFG_8 register (address 08h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------|--------|-------|-----------------------------------|
| 4 to 0 | LN2_N'[4:0] | R | - | number of bits per sample minus 1 |

Table 183. LN2_CFG_9 register (address 09h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|---|
| 4 to 0 | LN2_S[4:0] | R | - | number of samples per converter per frame cycle minus 1 |

Table 184. LN2_CFG_10 register (address 0Ah) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|-------------|--------|-------|---|
| 7 | LN2_HD | R | - | high density |
| 4 to 0 | LN2_CF[4:0] | R | - | number of control words per frame cycle |

Table 185. LN2_CFG_11 register (address 0Bh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-------|-----------------------|
| 7 to 0 | LN2_RES1[7:0] | R | - | lane 2 reserved field |

Table 186. LN2_CFG_12 register (address 0Ch) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-------|-----------------------|
| 7 to 0 | LN2_RES2[7:0] | R | - | lane 2 reserved field |

Table 187. LN2_CFG_13 register (address 0Dh) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-------|-----------------|
| 7 to 0 | LN2_FCHK[7:0] | R | - | lane 2 checksum |

Table 188. LN3_CFG_0 register (address 10h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------|--------|-------|------------------|
| 7 to 0 | LN3_DID[7:0] | R | - | lane 3 device ID |

Table 189. LN3_CFG_1 register (address 11h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------|--------|-------|----------------|
| 3 to 0 | LN3_BID[3:0] | R | - | lane 3 bank ID |

Table 190. LN3_CFG_2 register (address 12h) bit description

Default settings are shown highlighted.

| Bit | Symbol | Access | Value | Description |
|--------|--------------|--------|-------|----------------|
| 4 to 0 | LN3_LID[4:0] | R | - | lane 3 lane ID |

Table 191. LN3_CFG_3 register (address 13h) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|-------------------------|
| 7 | LN3_SCR | R | - | scrambling on |
| 4 to 0 | LN3_L[4:0] | R | - | number of lanes minus 1 |

Table 192. LN3_CFG_4 register (address 14h) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|------------------------------------|
| 7 to 0 | LN3_F[7:0] | R | - | number of octets per frame minus 1 |

Table 193. LN3_CFG_5 register (address 15h) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|---|
| 4 to 0 | LN3_K[4:0] | R | - | number of frames per multiframe minus 1 |

Table 194. LN3_CFG_6 register (address 16h) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|---|
| 7 to 0 | LN3_M[7:0] | R | - | number of converters per device minus 1 |

Table 195. LN3_CFG_7 register (address 17h) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|-------------|--------|-------|------------------------------|
| 7 to 6 | LN3_CS[1:0] | R | - | number of control bits |
| 4 to 0 | LN3_N[4:0] | R | - | converter resolution minus 1 |

Table 196. LN3_CFG_8 register (address 18h) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|-------------|--------|-------|-----------------------------------|
| 4 to 0 | LN3_N'[4:0] | R | - | number of bits per sample minus 1 |

Table 197. LN3_CFG_9 register (address 19h) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|------------|--------|-------|---|
| 4 to 0 | LN3_S[4:0] | R | - | number of samples per converter per frame cycle minus 1 |

Table 198. LN3_CFG_10 register (address 1Ah) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|-------------|--------|-------|---|
| 7 | LN3_HD | R | - | high density |
| 4 to 0 | LN3_CF[4:0] | R | - | number of control words per frame cycle |

Table 199. LN3_CFG_11 register (address 1Bh) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-------|-----------------------|
| 7 to 0 | LN3_RES1[7:0] | R | - | lane 3 reserved field |

Table 200. LN3_CFG_12 register (address 1Ch) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-------|-----------------------|
| 7 to 0 | LN3_RES2[7:0] | R | - | lane 3 reserved field |

Table 201. LN3_CFG_13 register (address 1Dh) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|---------------|--------|-------|-----------------|
| 7 to 0 | LN3_FCHK[7:0] | R | - | lane 3 checksum |

Table 202. PAGE_ADDRESS register (address 1Fh) bit description*Default settings are shown highlighted.*

| Bit | Symbol | Access | Value | Description |
|--------|-----------|--------|-------|--------------|
| 2 to 0 | PAGE[2:0] | R/W | 0h | page_address |

11. Package outline

HVQFN64: plastic thermal enhanced very thin quad flat package; no leads;
64 terminals; body 9 x 9 x 0.85 mm

SOT804-3

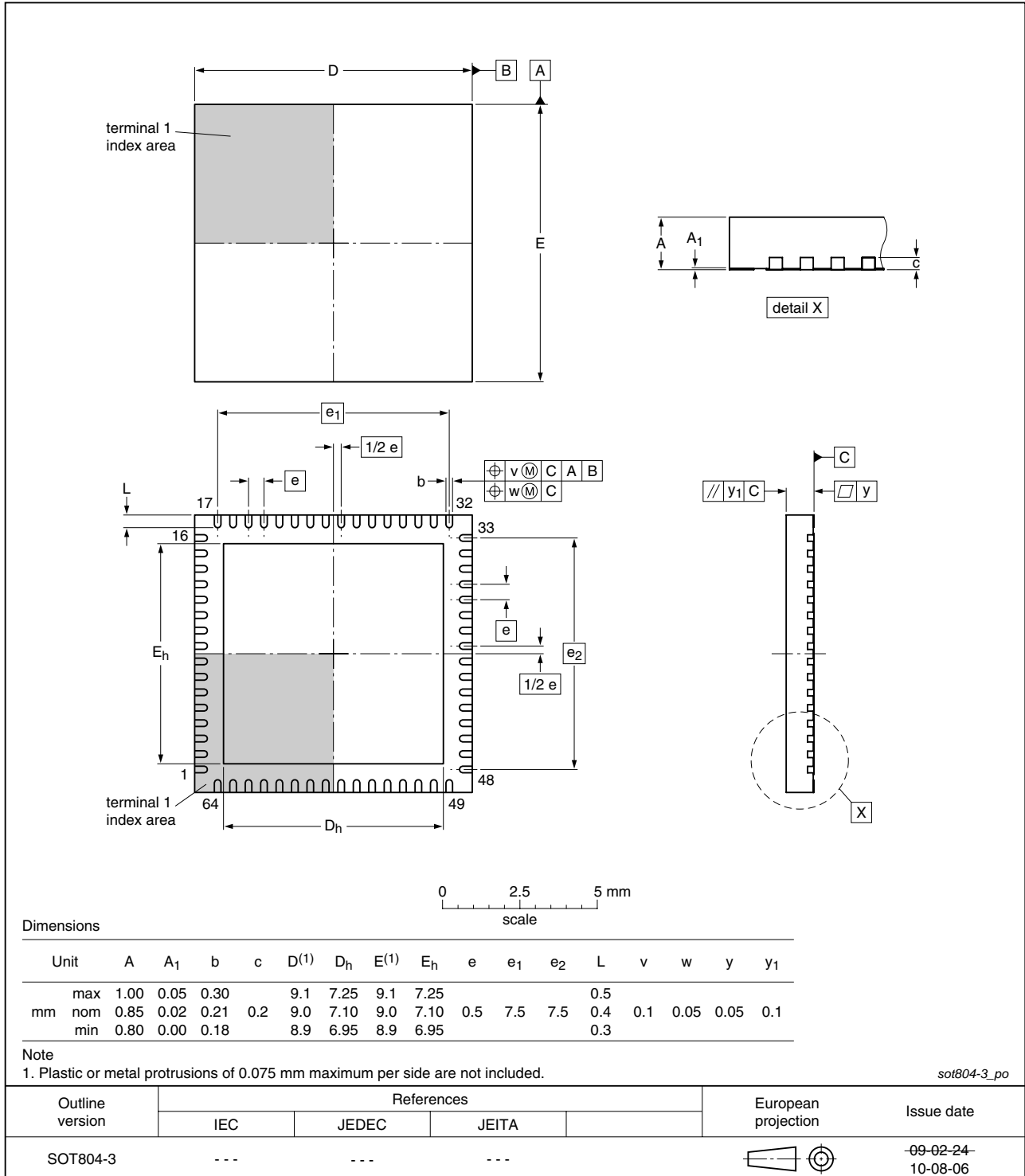


Fig 26. Package outline SOT804 (HVQFN64)

12. Abbreviations

Table 203. Abbreviations

| Acronym | Description |
|----------|---|
| AQM | Analog Quadrature Modulator |
| BER | Bit Error Rate |
| BW | BandWidth |
| CDI | Clock Domain Interface |
| CDMA | Code Division Multiple Access |
| CML | Current Mode Logic |
| CMOS | Complementary Metal Oxide Semiconductor |
| DAC | Digital-to-Analog Converter |
| DCSMU | Device Configuration Management and Start-up Unit |
| DES | DESerializer |
| EDGE | Enhanced Data rates for GSM Evolution |
| FIR | Finite Impulse Response |
| FPGA | Field Programmable Gate Array |
| GSM | Global System for Mobile communications |
| IF | Intermediate Frequency |
| ILA | Inter-Lane Alignment |
| IMD3 | third order InterMoDulation product |
| LMDS | Local Multipoint Distribution Service |
| LSB | Least Significant Bit |
| LTE | Long Term Evolution |
| LVDS | Low-Voltage Differential Signaling |
| MDS | Multipoint Distribution Service |
| MMDS | Multichannel Multipoint Distribution Service |
| MSB | Most Significant Bit |
| NCO | Numerically Controlled Oscillator |
| NMOS | Negative Metal-Oxide Semiconductor |
| PLL | Phase-Locked Loop |
| SERDES | SERializer/DESerializer |
| SFDR | Spurious Free Dynamic Range |
| SPI | Serial Peripheral Interface |
| TD-SCDMA | Time Division-Synchronous Code Division Multiple Access |
| WCDMA | Wideband Code Division Multiple Access |
| WiMax | Worldwide interoperability for Microwave Access |

13. Revision history

Table 204. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|-----------------|--------------|--|---------------|-----------------|
| DAC1408D750 v.2 | 20101202 | Product data sheet | - | DAC1408D750 v.1 |
| Modifications: | | <ul style="list-style-type: none">• Data sheet status changed from Objective to Product.• Text and drawings updated throughout entire data sheet.• Values in Table 5 “Characteristics” have been updated.• Section 10.2.2 “Sync and word align” has been updated.• Table 142 “Code group synchronization state machine” added to the data sheet. | | |
| DAC1408D750 v.1 | 20100930 | Objective data sheet | - | - |

14. Legal information

14.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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