

Dual N-Channel 30-V (D-S) MOSFET

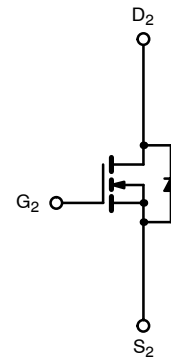
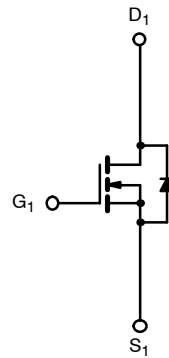
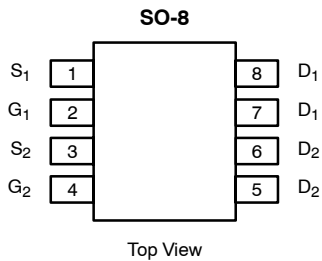
PRODUCT SUMMARY		
V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
30	0.022 @ $V_{GS} = 10$ V	7.5
	0.030 @ $V_{GS} = 4.5$ V	6.5

FEATURES

- Trench FET® Power MOSFET
- PWM Optimized
- 100% R_g Tested

APPLICATIONS

- Symmetrical Buck-Boost DC/DC Converter



Ordering Information: Si4804BDY—E3 (Lead Free)
Si4804BDY:T1—E3 (Lead Free with Tape and Reel)

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ UNLESS OTHERWISE NOTED)				
Parameter	Symbol	10 secs	Steady State	Unit
Drain-Source Voltage	V_{DS}	30		V
Gate-Source Voltage	V_{GS}	± 20		
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	7.5	A
		$T_A = 70^\circ\text{C}$	6.0	
Pulsed Drain Current	I_{DM}	30		A
Continuous Source Current (Diode Conduction) ^a	I_S	1.7	0.9	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	2.0	W
		$T_A = 70^\circ\text{C}$	1.3	
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150		$^\circ\text{C}$

THERMAL RESISTANCE RATINGS				
Parameter	Symbol	Limits		Unit
		Typ	Max	
Maximum Junction-to-Ambient ^a	R_{thJA}	$t \leq 10$ sec	52	$^\circ\text{C/W}$
		Steady-State	93	
Maximum Junction-to-Foot (Drain)	R_{thJF}	Steady-State	35	40

Notes

a. Surface Mounted on 1" x 1" FR4 Board.

MOSFET SPECIFICATIONS (T_J = 25 °C UNLESS OTHERWISE NOTED).						
Parameter	Symbol	Test Condition	Min	Typ ^a	Max	Unit
Static						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} = V _{GS} , I _D = 250 μA	0.8		3.0	V
Gate-Body Leakage	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±20 V			±100	nA
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
		V _{DS} = 30 V, V _{GS} = 0 V, T _J = 85 °C			15	
On-State Drain Current ^b	I _{D(on)}	V _{DS} = 5 V, V _{GS} = 10 V	20			A
Drain-Source On-State Resistance ^b	r _{DS(on)}	V _{GS} = 10 V, I _D = 7.5 A		0.017	0.022	Ω
		V _{GS} = 4.5 V, I _D = 6.5 A		0.024	0.030	
Forward Transconductance ^b	g _{fs}	V _{DS} = 15 V, I _D = 7.5 A		19		S
Diode Forward Voltage ^b	V _{SD}	I _S = 1 A, V _{GS} = 0 V		0.75	1.2	V
Dynamic^a						
Total Gate Charge	Q _g	V _{DS} = 15 V, V _{GS} = 4.5 V, I _D = 7.5 A		7	11	nC
Gate-Source Charge	Q _{gs}			2.9		
Gate-Drain Charge	Q _{gd}			2.5		
Gate Resistance	R _g		0.5	1.5	2.6	Ω
Turn-On Delay Time	t _{d(on)}	V _{DD} = 15 V, R _L = 15 Ω I _D = 1 A, V _{GEN} = 10 V, R _g = 6 Ω		9	15	ns
Rise Time	t _r			10	17	
Turn-Off Delay Time	t _{d(off)}			19	30	
Fall Time	t _f			9	15	
Source-Drain Reverse Recovery Time	t _{rr}	I _F = 1.7 A, di/dt = 100 A/μs	Ch-1	35	55	

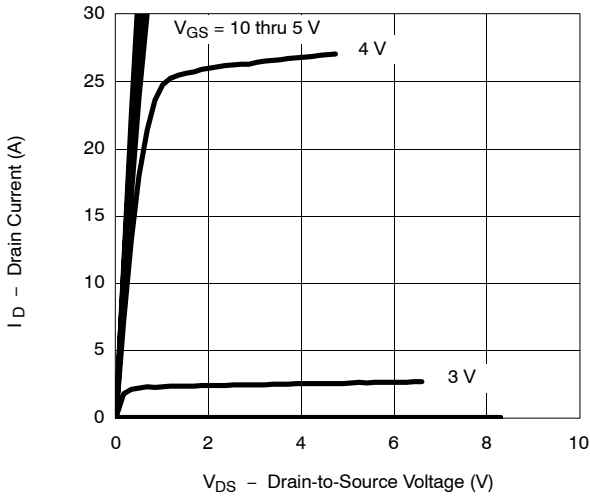
Notes

- a. Guaranteed by design, not subject to production testing.
 b. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2%.

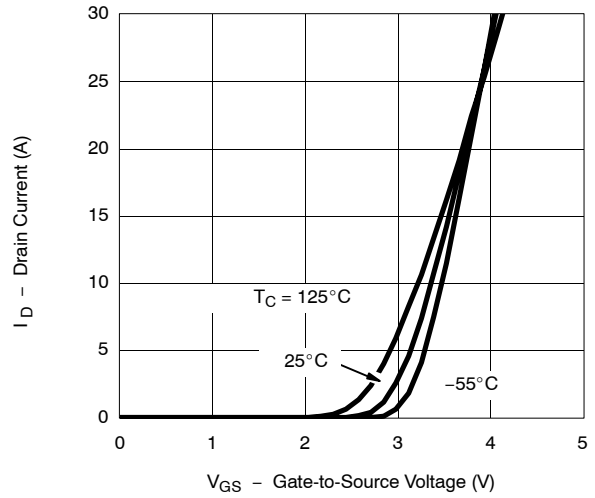


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

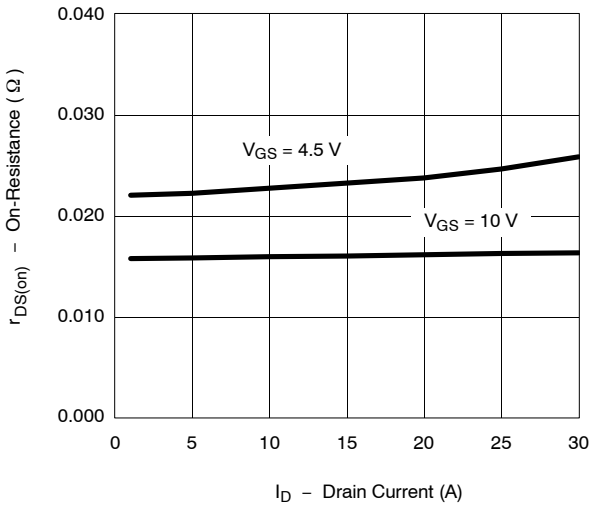
Output Characteristics



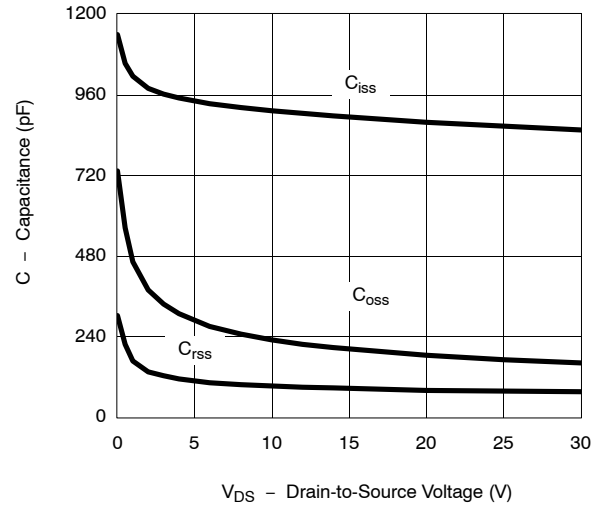
Transfer Characteristics



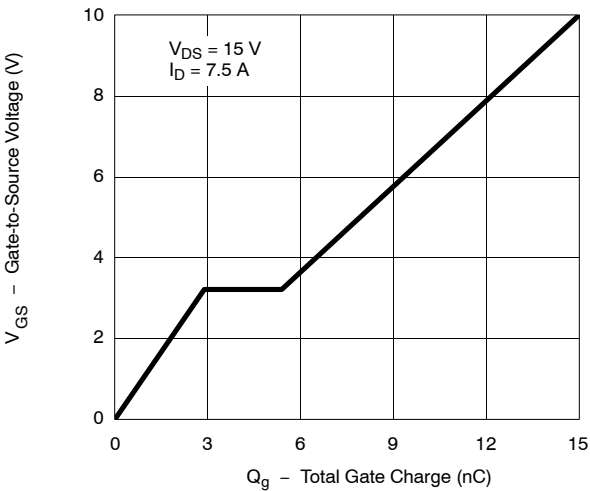
On-Resistance vs. Drain Current



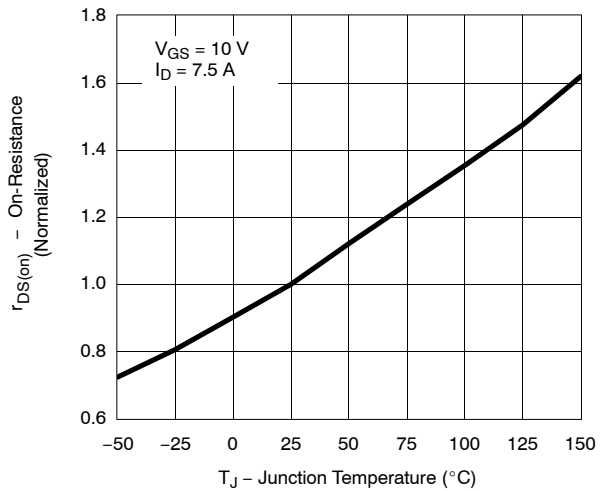
Capacitance



Gate Charge

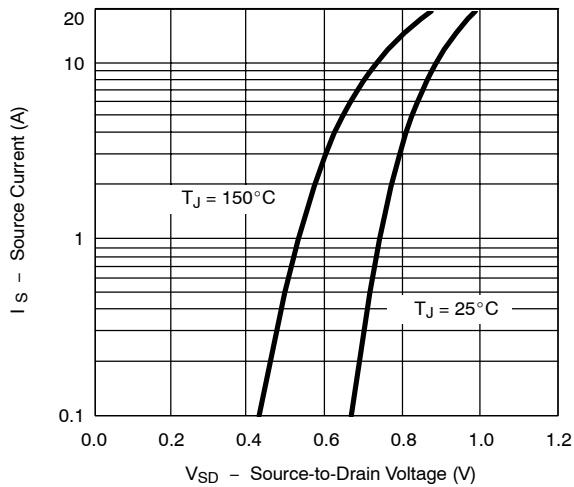


On-Resistance vs. Junction Temperature

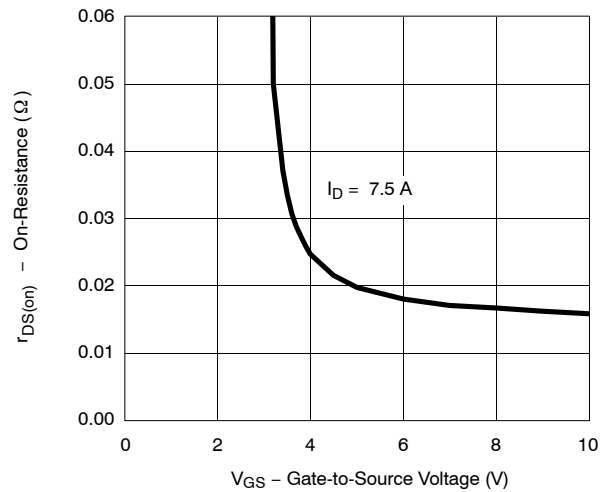


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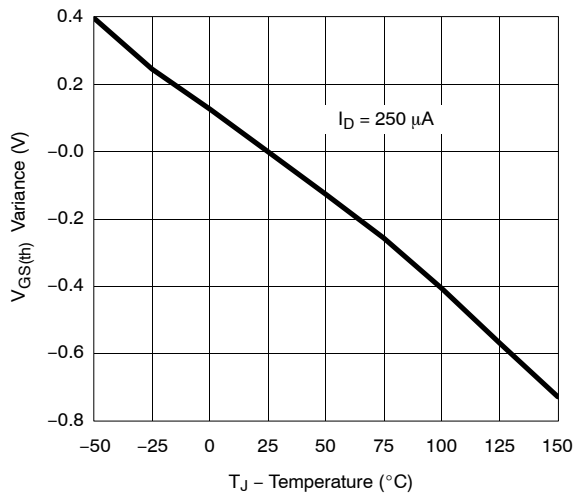
Source-Drain Diode Forward Voltage



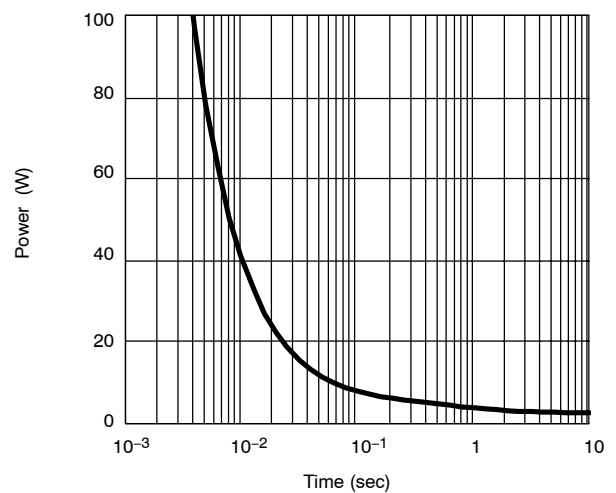
On-Resistance vs. Gate-to-Source Voltage



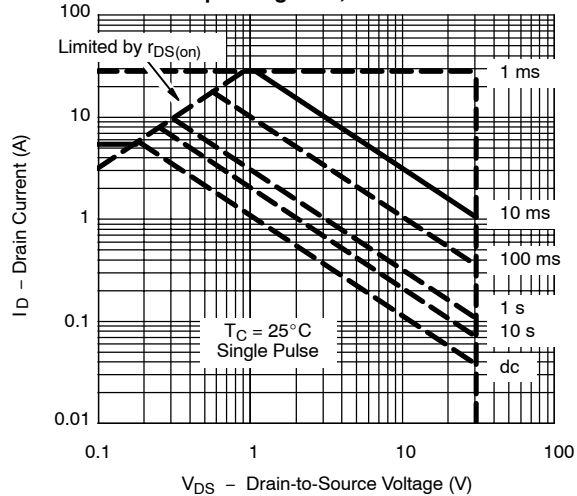
Threshold Voltage



Single Pulse Power, Junction-to-Ambient

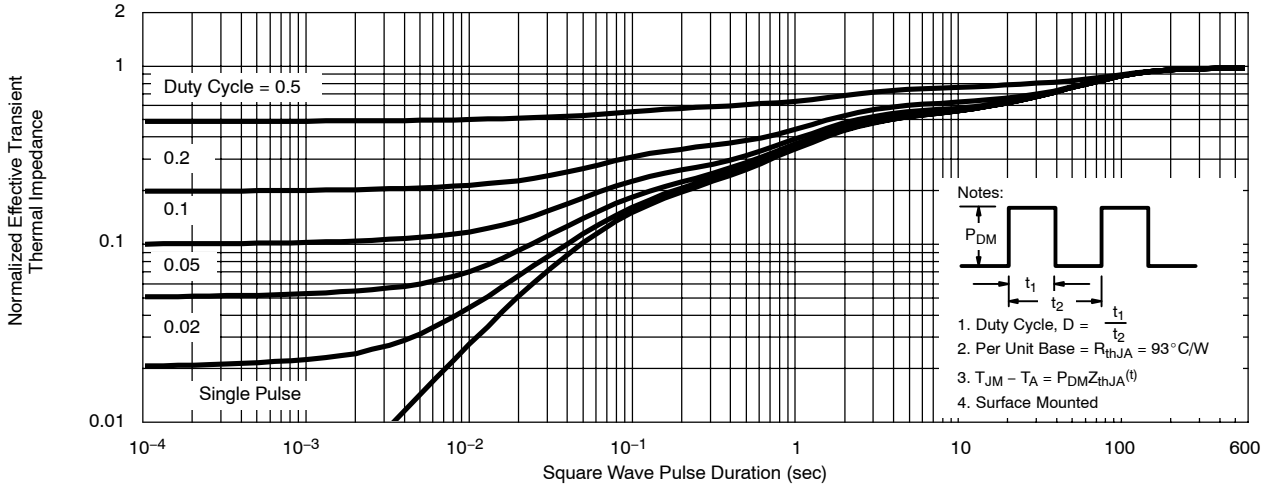


Safe Operating Area, Junction-to-Foot



TYPICAL CHARACTERISTICS (25 °C UNLESS NOTED)

Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Foot

