International IOR Rectifier

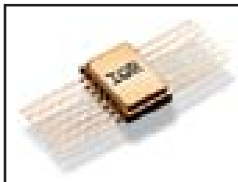
2N7620M2

RADIATION HARDENED LOGIC LEVEL POWER MOSFET THRU-HOLE (14-LEAD FLAT PACK)

IRHLA770Z4 60V, Quad N-CHANNEL R7™ TECHNOLOGY

Product Summary

Part Number	Radiation Level	$R_{DS(on)}$	I_D
IRHLA770Z4	100K Rads (Si)	0.60Ω	0.8A
IRHLA730Z4	300K Rads (Si)	0.60Ω	0.8A



14-Lead Flat Pack

International Rectifier's R7™ Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

These devices are used in applications such as current boost low signal source in PWM, voltage comparator and operational amplifiers.

Features:

- 5V CMOS and TTL Compatible
- Low $R_{DS(on)}$
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Light Weight
- Complimentary P-Channel Available - IRHLA7970Z4

Absolute Maximum Ratings (Per Die) — Pre-Irradiation

	Parameter		Units
I_D @ V_{GS} = 4.5V, T_C = 25°C	Continuous Drain Current	0.8	A
I_D @ V_{GS} = 4.5V, T_C = 100°C	Continuous Drain Current	0.5	A
I_{DM}	Pulsed Drain Current ①	3.2	A
P_D @ T_C = 25°C	Max. Power Dissipation	0.6	W
	Linear Derating Factor	0.005	W/°C
V_{GS}	Gate-to-Source Voltage	±10	V
E_{AS}	Single Pulse Avalanche Energy ②	16	mJ
I_{AR}	Avalanche Current ①	0.8	A
E_{AR}	Repetitive Avalanche Energy ①	0.06	mJ
dv/dt	Peak Diode Recovery dv/dt ③	10.2	V/ns
T_J T_{STG}	Operating Junction Storage Temperature Range	-55 to 150	°C
	Lead Temperature	300 (0.63 in./1.6 mm from case for 10s)	°C
	Weight	0.52 (Typical)	g

For footnotes refer to the last page

Electrical Characteristics For Each N-Channel Device @Tj = 25°C (Unless Otherwise specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	—	—	V	V_{GS} = 0V, I_D = 250µA
$\Delta BV_{DSS}/\Delta T_J$	Temperature Coefficient of Breakdown Voltage	—	0.067	—	V/°C	Reference to 25°C, I_D = 1.0mA
$R_{DS(on)}$	Static Drain-to-Source On-State Resistance	—	—	0.60	Ω	V_{GS} = 4.5V, I_D = 0.5A ④
$V_{GS(th)}$	Gate Threshold Voltage	1.0	—	2.0	V	V_{DS} = V_{GS}, I_D = 250µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	—	-4.7	—	mV/°C	
g_{fs}	Forward Transconductance	0.23	—	—	S	V_{DS} = 10V, I_{DS} = 0.5A ④
I_{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	µA	V_{DS}= 48V ,V_{GS}= 0V
		—	—	10		V_{DS} = 48V, V_{GS} = 0V, T_J =125°C
I_{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V_{GS} = 10V
I_{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V_{GS} = -10V
Q_g	Total Gate Charge	—	—	2.8	nC	V_{GS} = 4.5V, I_D = 0.8A
Q_{gs}	Gate-to-Source Charge	—	—	0.6		V_{DS} = 30V
Q_{gd}	Gate-to-Drain ('Miller') Charge	—	—	1.6		
$t_{d(on)}$	Turn-On Delay Time	—	—	6.5	ns	V_{DD} = 30V, I_D = 0.8A,
t_r	Rise Time	—	—	2.5		V_{GS} = 5.0V, R_G = 24Ω
$t_{d(off)}$	Turn-Off Delay Time	—	—	35		
t_f	Fall Time	—	—	13		
$L_S + L_D$	Total Inductance	—	20	—	nH	Measured from Drain lead (6mm /0.25in from pack.) to Source lead (6mm/0.25in from pack.)with Source wire internally bonded from Source pin to Drain pad
C_{iss}	Input Capacitance	—	141	—	pF	V_{GS} = 0V, V_{DS} = 25V
C_{oss}	Output Capacitance	—	38	—		f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	—	1.4	—		
R_g	Gate Resistance	—	8.0	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
I_S	Continuous Source Current (Body Diode)	—	—	0.8	A	
I_{SM}	Pulse Source Current (Body Diode) ①	—	—	3.2		
V_{SD}	Diode Forward Voltage	—	—	1.2	V	T_j = 25°C, I_S = 0.8A, V_{GS} = 0V ④
t_{rr}	Reverse Recovery Time	—	—	55	ns	T_j = 25°C, I_F = 0.8A, di/dt ≤ 100A/µs
Q_{RR}	Reverse Recovery Charge	—	—	63	nC	V_{DD} ≤ 25V ④
t_{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L_S + L_D.				

Thermal Resistance (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
R_{thJA}	Junction-to-Ambient	—	—	210	°C/W	Typical socket mount

Note: Corresponding Spice and Saber models are available International Rectifier Website.

For footnotes refer to the last page

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics For Each N-Channel Device @Tj = 25°C, Post Total Dose Irradiation ⑤⑥

	Parameter	Up to 300K Rads (Si)[1] Min	Max	Units	Test Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	60	—	V	V_{GS} = 0V, I_D = 250μA
$V_{GS(th)}$	Gate Threshold Voltage	1.0	2.0		V_{GS} = V_{DS}, I_D = 250μA
I_{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V_{GS} = 10V
I_{GSS}	Gate-to-Source Leakage Reverse	—	-100		V_{GS} = -10V
I_{DSS}	Zero Gate Voltage Drain Current	—	1.0	μA	V_{DS}= 48V, V_{GS}= 0V
$R_{DS(on)}$	Static Drain-to-Source ④ On-State Resistance (TO-39)	—	0.60	Ω	V_{GS} = 4.5V, I_D = 0.5A
$R_{DS(on)}$	Static Drain-to-Source On-state ④ Resistance (14-Lead Flat Pack)	—	0.60	Ω	V_{GS} = 4.5V, I_D = 0.5A
V_{SD}	Diode Forward Voltage ④	—	1.2	V	V_{GS} = 0V, I_D = 0.8A

1. Part numbers IRHLA770Z4, IRHLA730Z4

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area (Per Die)

Ion	LET (MeV/(mg/cm^2))	Energy (MeV)	Range (μm)	VDS (V) @VGS= 0V	@VGS= -2V	@VGS= -4V	@VGS= -5V	@VGS= -6V	@VGS= -7V	@VGS= -8V	@VGS= -10V
Br	37	305	39	60	60	60	60	60	35	30	20
I	60	370	34	60	60	60	60	60	20	15	-
Au	84	390	30	60	60	60	60	-	-	-	-

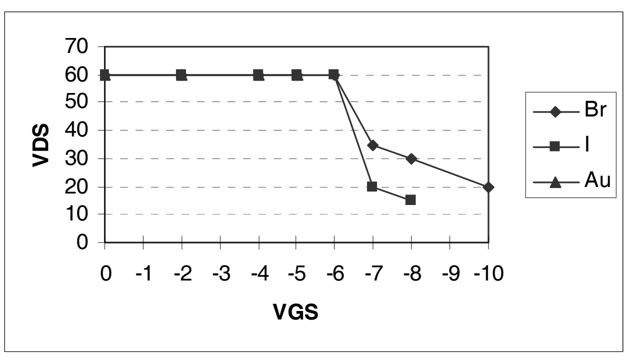


Fig a. Typical Single Event Effect, Safe Operating Area

For footnotes refer to the last page

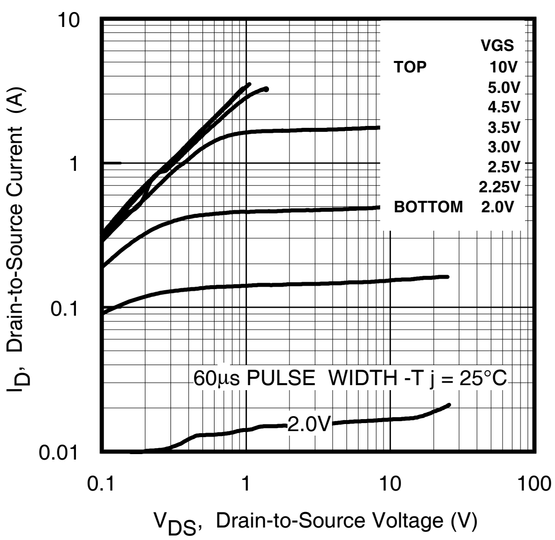


Fig 1. Typical Output Characteristics

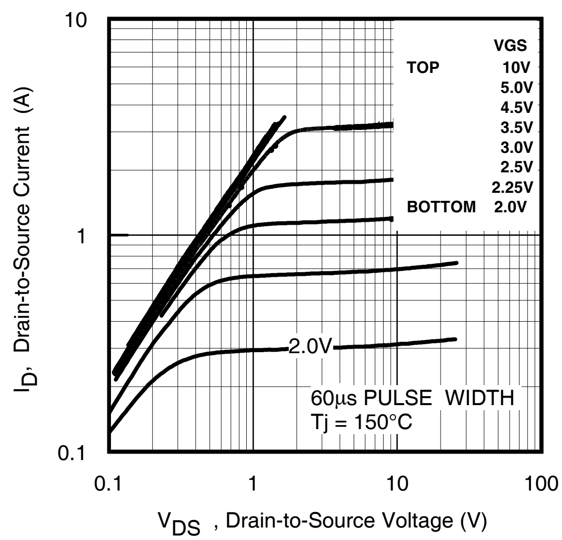


Fig 2. Typical Output Characteristics

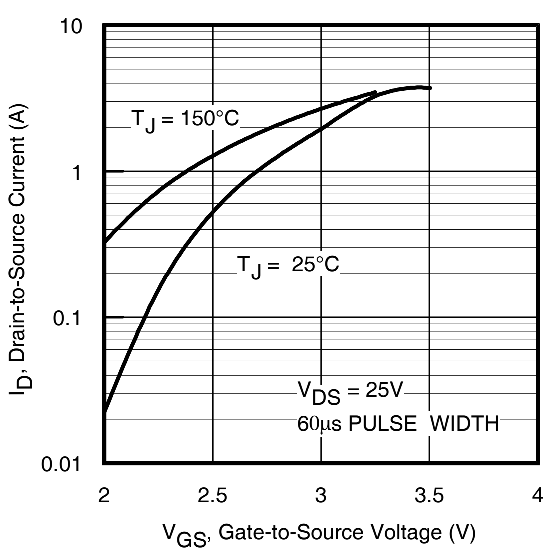


Fig 3. Typical Transfer Characteristics

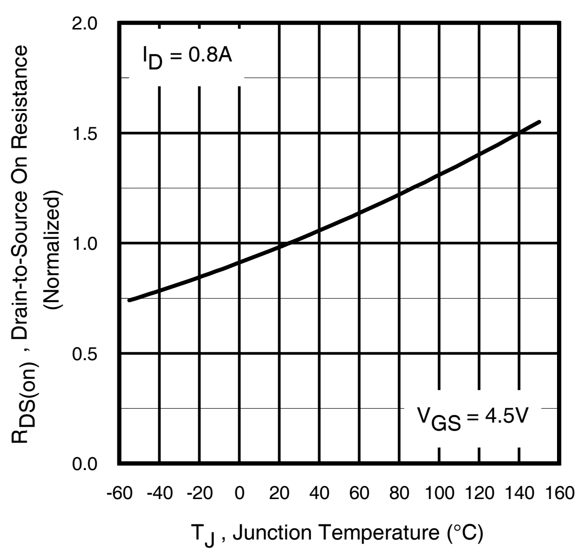


Fig 4. Normalized On-Resistance Vs. Temperature

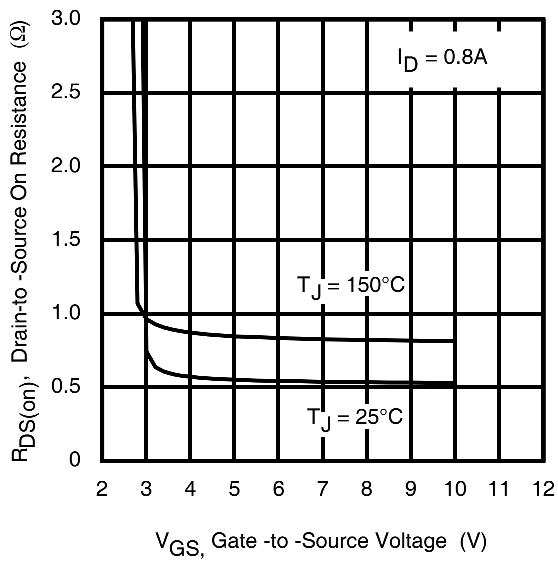


Fig 5. Typical On-Resistance Vs Gate Voltage

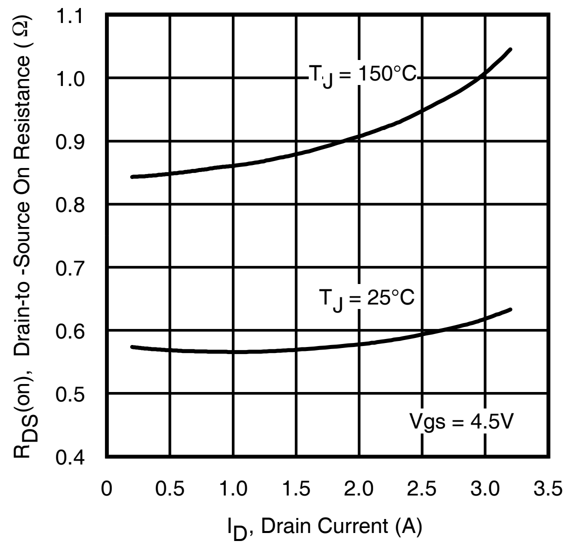


Fig 6. Typical On-Resistance Vs Drain Current

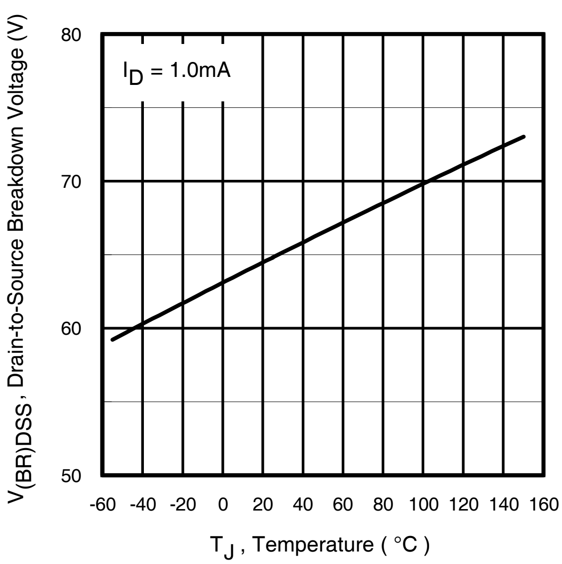


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

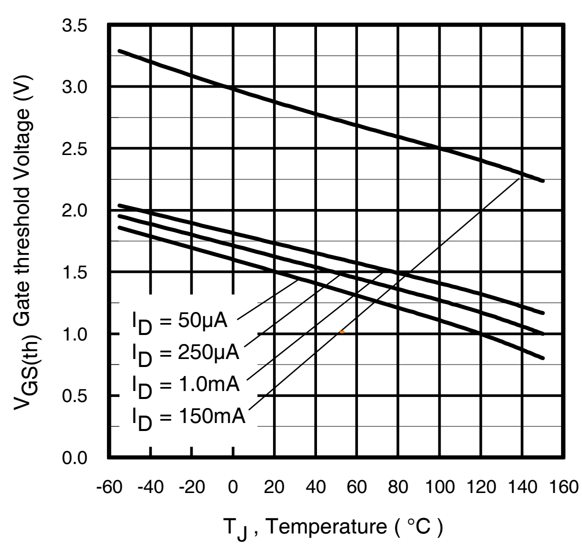


Fig 8. Typical Threshold Voltage Vs Temperature

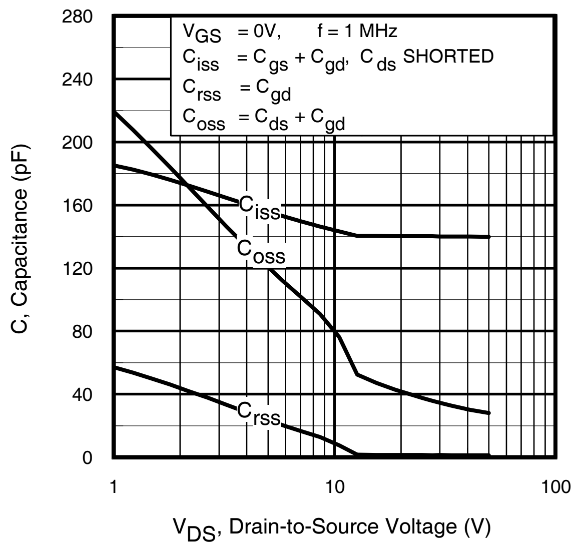


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

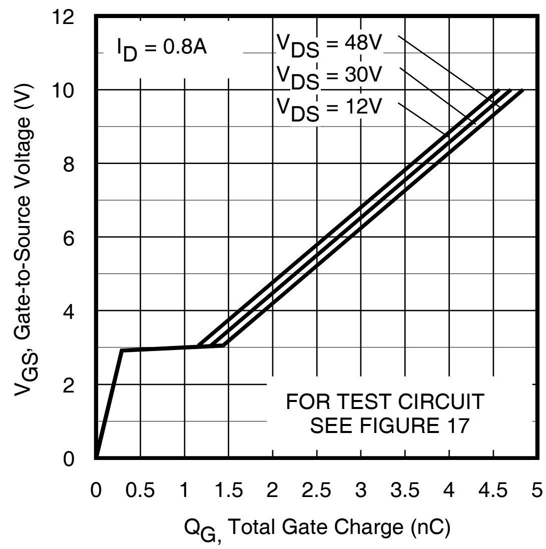


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

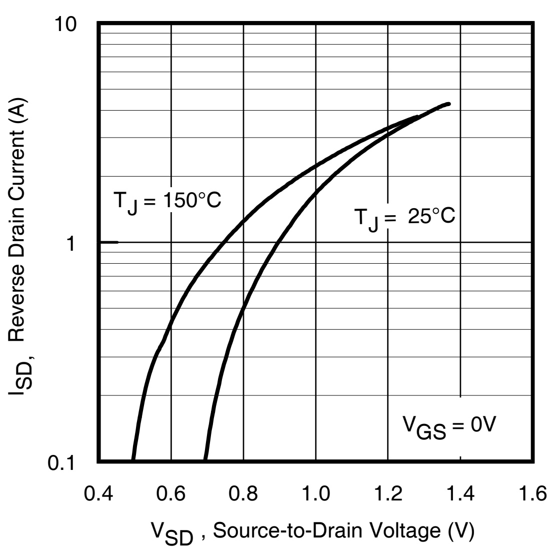


Fig 11. Typical Source-to-Drain Diode Forward Voltage

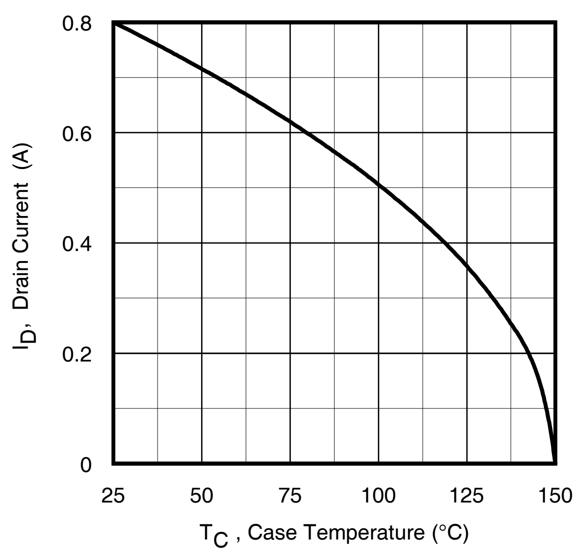


Fig 12. Maximum Drain Current Vs. Case Temperature

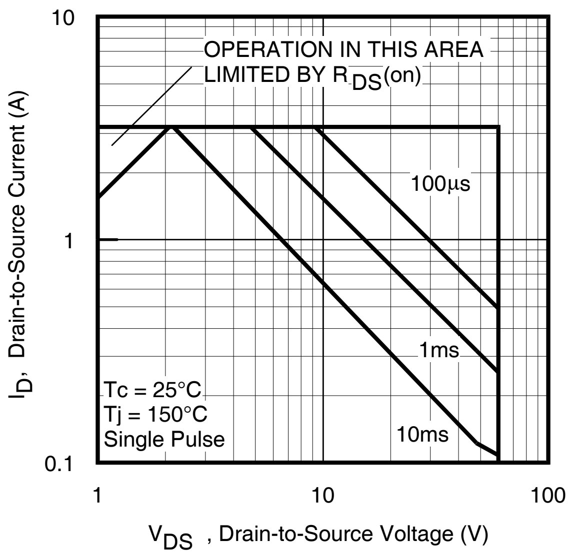


Fig 13. Maximum Safe Operating Area

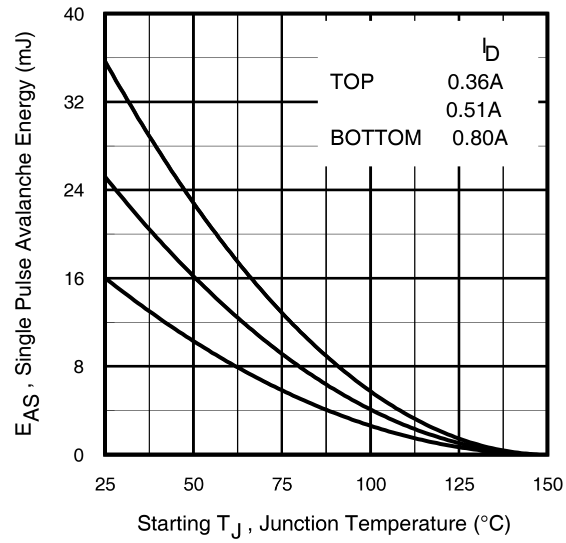


Fig 14. Maximum Avalanche Energy Vs. Drain Current

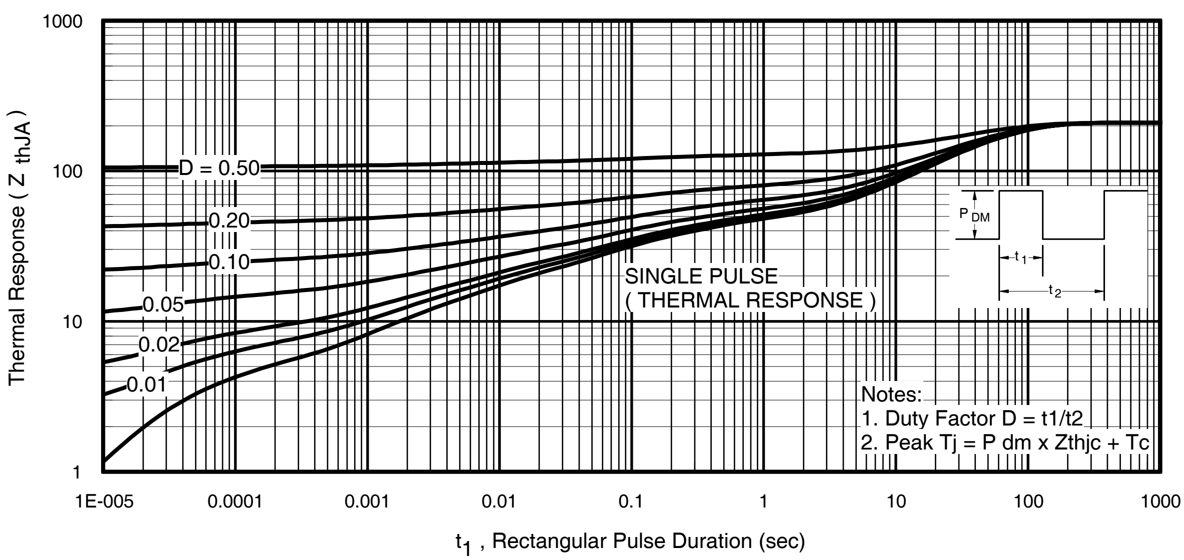


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

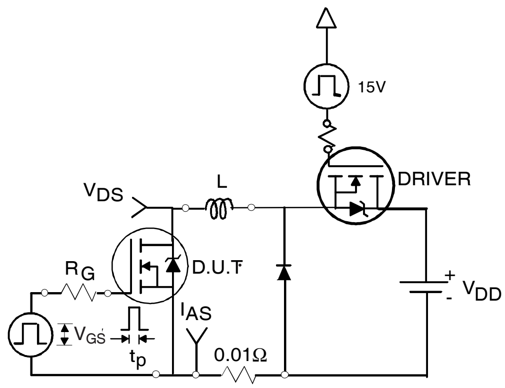


Fig 16a. Unclamped Inductive Test Circuit

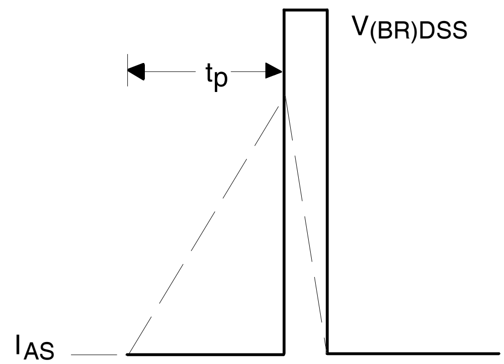


Fig 16b. Unclamped Inductive Waveforms

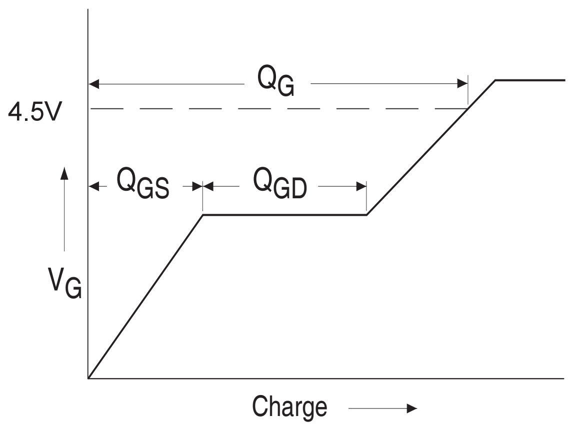


Fig 17a. Basic Gate Charge Waveform

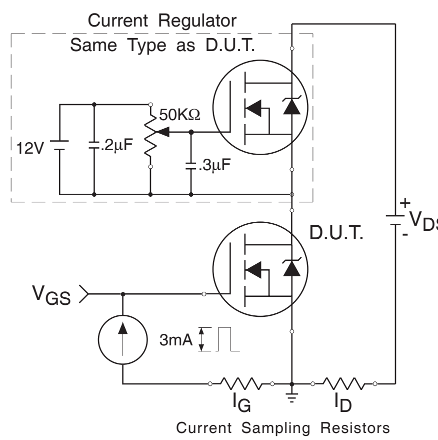


Fig 17b. Gate Charge Test Circuit

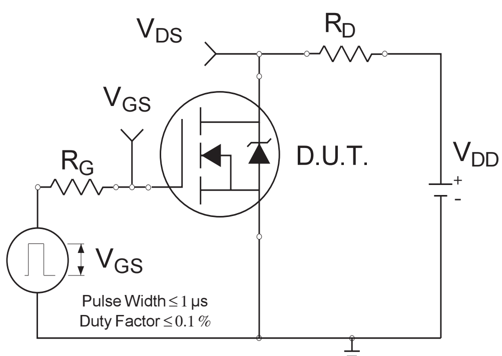


Fig 18a. Switching Time Test Circuit

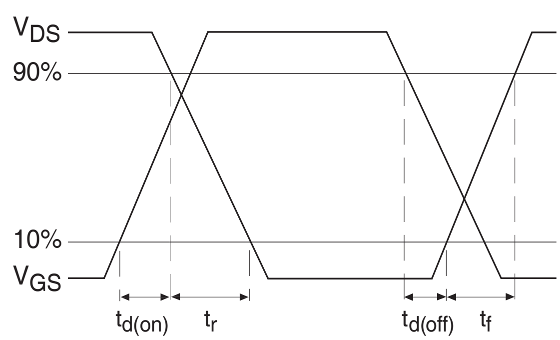


Fig 18b. Switching Time Waveforms

Footnotes:

① Repetitive Rating; Pulse width limited by maximum junction temperature.

② V_{DD} = 25V, starting T_J = 25°C, L= 50mH Peak I_L = 0.8A, V_{GS} = 10V

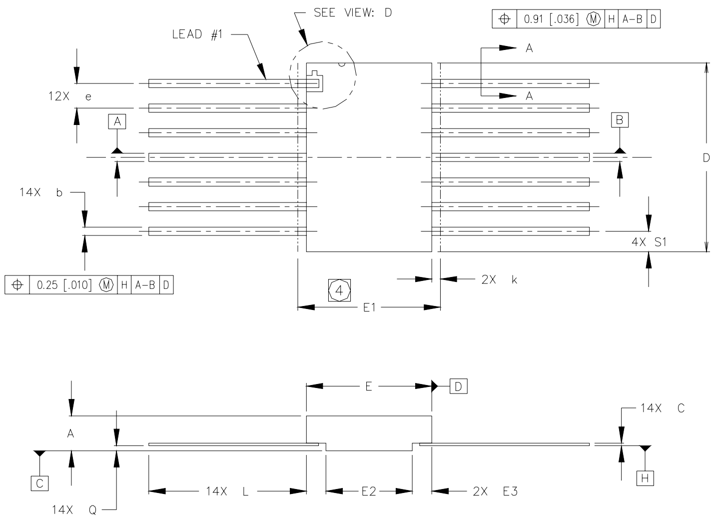
③ $I_{SD} \leq$ 0.8A, di/dt ≤ 230A/µs, $V_{DD} \leq$ 60V, $T_J \leq$ 150°C

④ Pulse width ≤ 300 µs; Duty Cycle ≤ 2%

⑤ **Total Dose Irradiation with V_{GS} Bias.** 10 volt V_{GS} applied and V_{DS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

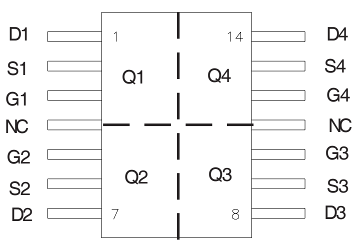
⑥ **Total Dose Irradiation with V_{DS} Bias.** 48 volt V_{DS} applied and V_{GS} = 0 during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — 14-Lead FlatPack



SYMBOL	DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	1.14	2.92	.045	.115
b	0.38	0.56	.015	.022
b1	0.38	0.48	.015	.019
c	0.10	0.23	.004	.009
c1	0.10	0.15	.004	.006
D	---	9.91	---	.390
E	5.97	6.60	.235	.260
E1	---	7.37	---	.290
E2	3.18	---	.125	---
E3	0.76	---	.030	---
e	1.27 BSC		.050 BSC	
k	0.20	0.38	.008	.015
L	6.86	9.40	.270	.370
Q	0.18	0.33	.007	.013
S1	0.13	---	005	---
M	---	0.04	---	.0015

LEAD ASSIGNMENT

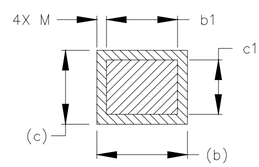


LEGEND

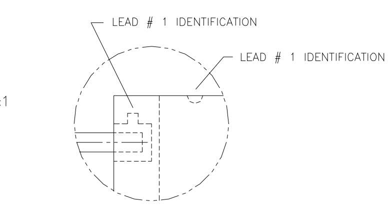
D = DRAIN, S = SOURCE , G = GATE, NC = NO CONNECTION

CHANNELS

N Channel = Q1,Q2, Q3 and Q4



SECTION A–A



VIEW D

LOCATION OF LEAD #1 IDENTIFICATION MARKS

NOTES:

1. DIMENSIONING & TOLERANCING PER ASME Y14.5M–1994.
2. CONTROLING DIMENSION: INCH
3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
4. THIS DIMENSION ALLOWS FOR OFF–CENTER LID, MENISCUS AND GLASS OVERRUN.
5. OUTLINE CONFORMS TO MIL–STD–1835C, OUTLINE CDFP3–F14 EXCEPT FOR DIMENSION Q.

International
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