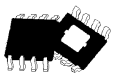
TS616

Dual wide band operational amplifier with high output current

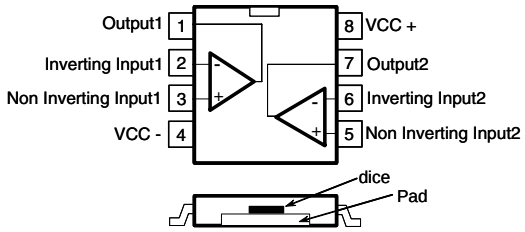
Features

- Low noise: 2.5 nV/√Hz
- High output current: 420 mA
- Very low harmonic and intermodulation distortion
- High slew rate: 420 V/µs
- -3dB bandwidth: 40 MHz @ gain = 12 dB on 25 Ω single-ended load
- 20.7 Vp-p differential output swing on 50 Ω load, 12 V power supply
- Current feedback structure
- 5 V to 12 V power supply
- Specified for 20 Ω and 50 Ω differential load



DW
SO-8 Exposed-pad
(Plastic micropackage)

Pin connections (top view)



Cross Section View Showing Exposed-Pad.
This pad must be connected to a (-Vcc) copper area on the PCB

Applications

- Line driver for xDSL
- Multiple video line driver

Description

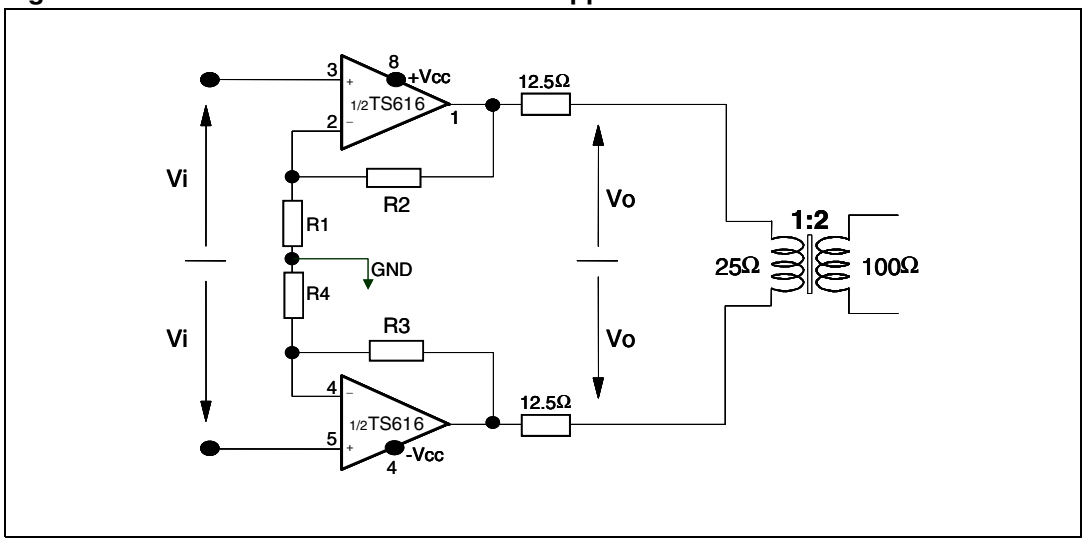
The TS616 is a dual operational amplifier featuring a high output current of 410 mA. This driver can be configured differentially for driving signals in telecommunication systems using multiple carriers. The TS616 is ideally suited for xDSL (high speed asymmetrical digital subscriber line) applications. This circuit is capable of driving a 10 Ω or 25 Ω load on a range of power supplies: ±2.5 V, 5 V, ±6 V or +12 V. The TS616 is capable of reaching a -3 dB bandwidth of 40 MHz on 25 Ω load with a 12 dB gain. This device is designed for high slew rates and demonstrates low harmonic distortion and intermodulation.

Contents

1 Typical application

Figure 1 shows a schematic of a typical xDSL application using the TS616.

Figure 1. Differential line driver for xDSL applications



2 Absolute maximum ratings and operating conditions

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	Supply voltage (1)	±7	V
V_{id}	Differential input voltage (2)	±2	V
V_{in}	Input voltage range (3)	±6	V
T_{oper}	Operating free air temperature range	-40 to + 85	°C
T_{std}	Storage temperature	-65 to +150	°C
T_j	Maximum junction temperature	150	°C
R_{thjc}	Thermal resistance junction to case	16	°C/W
R_{thja}	Thermal resistance junction to ambient area	60	°C/W
P_{max}	Maximum power dissipation (at T_{amb} = 25° C) for T_j = 150° C	2	W
ESD only pins 1, 4, 7, 8	HBM: human body model(4) MM: machine model(5) CDM: charged device model(6)	1.5 2 200	kV kV V
ESD only pins 2, 3, 5, 6	HBM: human body model(4) MM: machine model(5) CDM: charged device model(6)	1.5 2 100	kV kV V
	Output short circuit	(7)	

1. All voltage values, except differential voltage are with respect to network terminal.
2. Differential voltages are non-inverting input terminal with respect to the inverting input terminal.
3. The magnitude of input and output voltage must never exceed V_{CC} +0.3 V.
4. Human body model: a 100 pF capacitor is charged to the specified voltage, then discharged through a 1.5 kΩ resistor between two pins of the device. This is done for all couples of connected pin combinations while the other pins are floating.
5. Machine model: a 200 pF capacitor is charged to the specified voltage, then discharged directly between two pins of the device with no external series resistor (internal resistor < 5 Ω). This is done for all couples of connected pin combinations while the other pins are floating.
6. Charged device model: all pins and the package are charged together to the specified voltage and then discharged directly to the ground through only one pin. This is done for all pins.
7. An output current limitation protects the circuit from transient currents. Short-circuits can cause excessive heating. Destructive dissipation can result from short-circuits on amplifiers.

Table 2. Operating conditions

Symbol	Parameter	Value	Unit
V_{CC}	Power supply voltage	±2.5 to ±6	V
V_{icm}	Common mode input voltage	$-V_{CC}$+1.5 V to $+V_{CC}$-1.5 V	V

3 Electrical characteristics

Table 3. V_{CC} = ±6 V, R_{fb}= 910 Ω, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T_{amb}		1	3.5	mV
		$T_{min} < T_{amb} < T_{max}$		1.6		
ΔV_{io}	Differential input offset voltage	T_{amb} = 25°C			2.5	mV
I_{ib+}	Positive input bias current	T_{amb}		5	30	µA
		$T_{min} < T_{amb} < T_{max}$		7.2		
I_{ib-}	Negative input bias current	T_{amb}		3	15	µA
		$T_{min} < T_{amb} < T_{max}$		3.1		
Z_{IN+}	Input(+) impedance			82		kΩ
Z_{IN-}	Input(-) impedance			54		Ω
C_{IN+}	Input(+) capacitance			1		pF
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	ΔV_{ic} = ±4.5V	58	64		dB
		$T_{min} < T_{amb} < T_{max}$		62		
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{CC}/\Delta V_{io}$)	ΔV_{CC} = ±2.5V to ±6V	72	81		dB
		$T_{min} < T_{amb} < T_{max}$		80		
I_{CC}	Total supply current per operator	No load		13.5	17	mA
Dynamic performance and output characteristics						
R_{OL}	Open loop transimpedance	V_{out} = 7Vp-p, R_L = 25Ω	5	13.5		MΩ
		$T_{min} < T_{amb} < T_{max}$		5.7		
BW	-3dB bandwidth	Small signal V_{out} < 20mVp A_V = 12dB, R_L = 25Ω	25	40		MHz
	Full power bandwidth	Large signal V_{out} = 3Vp A_V = 12dB, R_L = 25Ω		26		
	Gain flatness @ 0.1dB	Small signal T_{amb}<20mVp A_V = 12dB, R_L = 25Ω		7		MHz
T_r	Rise time	V_{out} = 6Vp-p, A_V = 12dB, R_L = 25Ω		10.6		ns
T_f	Fall time	V_{out} = 6Vp-p, A_V = 12dB, R_L = 25Ω		12.2		ns
T_s	Settling time	V_{out} = 6Vp-p, A_V= 12dB, R_L = 25Ω		50		ns
SR	Slew rate	V_{out} = 6Vp-p, A_V = 12dB, R_L = 25Ω	330	420		V/µs
V_{OH}	High level output voltage	R_L = 25Ω connected to GND	4.8	5.05		V
V_{OL}	Low level output voltage	R_L = 25Ω Connected to GND		-5.3	-5.1	V

Table 3. V_{CC} = ±6 V, R_{fb}= 910 Ω, T_{amb} = 25° C (unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{out}	Output sink current	V_{out} = -4Vp	-320	-490		mA
		$T_{min} < T_{amb} < T_{max}$		-395		
	Output source current	V_{out} = +4Vp	330	420		
		$T_{min} < T_{amb} < T_{max}$		370		
Noise and distortion						
eN	Equivalent input noise voltage	F = 100kHz		2.5		nV/√Hz
iNp	Equivalent input noise current (+)	F = 100kHz		15		pA/√Hz
iNn	Equivalent input noise current (-)	F = 100kHz		21		pA/√Hz
HD2	2nd harmonic distortion (differential configuration)	V_{out} = 14Vp-p, A_V = 12dB F= 110kHz, R_L = 50Ω diff.		-87		dBc
HD3	3rd harmonic distortion (differential configuration)	V_{out} = 14Vp-p, A_V = 12dB F= 110kHz, R_L = 50Ω diff.		-83		dBc
IM2	2nd order intermodulation product (differential configuration)	F1= 100kHz, F2 = 110kHz V_{out} = 16Vp-p, A_V = 12dB R_L = 50Ω diff.		-76		dBc
		F1= 370kHz, F2 = 400kHz V_{out} = 16Vp-p, A_V = 12dB R_L = 50Ω diff.		-75		
IM3	3rd order intermodulation product (differential configuration)	F1 = 100kHz, F2 = 110kHz V_{out} = 16Vp-p, A_V = 12dB R_L = 50Ω diff.		-88		dBc
		F1 = 370kHz, F2 = 400kHz V_{out} = 16Vp-p, A_V = 12 B R_L = 50Ω diff.		-87		

Table 4. V_{CC} = ±2.5 V, R_{fb}= 910 Ω, T_{amb} = 25° C (unless otherwise specified)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
DC performance						
V_{io}	Input offset voltage	T_{amb}		0.2	2.5	mV
		$T_{min} < T_{amb} < T_{max}$		1		
ΔV_{io}	Differential input offset voltage	T_{amb} = 25°C			2.5	mV
I_{ib+}	Positive input bias current	T_{amb}		4	30	µA
		$T_{min} < T_{amb} < T_{max}$		7		
I_{ib-}	Negative input bias current	T_{amb}		1.1	11	µA
		$T_{min} < T_{amb} < T_{max}$		1.2		
Z_{IN+}	Input(+) impedance			71		kΩ
Z_{IN-}	Input(-) impedance			62		Ω
C_{IN+}	Input(+) capacitance			1.5		pF
CMR	Common mode rejection ratio 20 log ($\Delta V_{ic}/\Delta V_{io}$)	ΔV_{ic} = ±1V	55	61		dB
		$T_{min} < T_{amb} < T_{max}$		60		
SVR	Supply voltage rejection ratio 20 log ($\Delta V_{cc}/\Delta V_{io}$)	ΔV_{CC}= ±2V to ±2.5V	63	79		dB
		$T_{min} < T_{amb} < T_{max}$		78		
I_{CC}	Total supply current per operator	No load		11.5	15	mA
Dynamic performance and output characteristics						
R_{OL}	Open loop transimpedance	V_{out} = 2V_{p-p}, R_L = 10Ω	2	4.2		MΩ
		$T_{min} < T_{amb} < T_{max}$		1.5		
BW	-3dB bandwidth	Small signal V_{out} < 20mVp A_V = 12dB, R_L = 10Ω	20	28		MHz
	Full power bandwidth	Large signal V_{out} = 1.4V_p A_V= 12dB, R_L = 10Ω		20		
	Gain flatness @ 0.1dB	Small signal V_{out}< 20mVp A_V = 12dB, R_L = 10Ω		5.7		MHz
T_r	Rise time	V_{out} = 2.8Vp-p, A_V = 12dB R_L= 10Ω		11		ns
T_f	Fall time	V_{out} = 2.8Vp-p, A_V = 12dB R_L= 10Ω		11.5		ns
T_s	Settling time	V_{out} = 2.2Vp-p, A_V = 12dB R_L= 10Ω		39		ns
SR	Slew rate	V_{out} = 2.2Vp-p, A_V = 12dB R_L =10Ω	100	130		V/µs
V_{OH}	High level output voltage	R_L=10Ω connected to GND	1.5	1.7		V
V_{OL}	Low level output voltage	R_L=10Ω connected to GND		-1.9	-1.7	V
I_{out}	Output sink current	V_{out} = -1.25V_p	-300	-400		mA
		$T_{min} < T_{amb} < T_{max}$		-360		
	Output source current	V_{out} = +1.25V_p	200	270		
		$T_{min} < T_{amb} < T_{max}$		240		

Table 4. V_{CC} = ±2.5 V, R_{fb}= 910 Ω, T_{amb} = 25° C (unless otherwise specified) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
Noise and distorsion						
eN	Equivalent input noise voltage	F = 100kHz		2.5		nV/√Hz
iNp	Equivalent input noise current (+)	F = 100kHz		15		pA/√Hz
iNn	Equivalent input noise current (-)	F = 100kHz		21		pA/√Hz
HD2	2nd harmonic distortion (differential configuration)	V_{out} = 6V_{p-p}, A_V = 12 dB F= 110kHz, R_L = 20 Ω diff.		-97		dBc
HD3	3rd harmonic distortion (differential configuration)	V_{out} = 6V_{p-p}, A_V = 12dB F= 110 kHz, R_L = 20Ω diff.		-98		dBc
IM2	2nd order intermodulation product (differential configuration)	F1= 100 kHz, F2 = 110 kHz V_{out} = 6 V_{p-p}, A_V = 12dB R_L = 20Ω diff.		-86		dBc
		F1= 370kHz, F2 = 400kHz V_{out} = 6V_{p-p}, A_V = 12dB R_L = 20Ω diff.		-88		
IM3	3rd order intermodulation product (differential configuration)	F1 = 100kHz, F2 = 110kHz V_{out} = 6V_{p-p}, A_V = 12dB R_L = 20Ω diff.		-90		dBc
		F1 = 370kHz, F2 = 400kHz V_{out} = 6V_{p-p}, A_V = 12dB R_L = 20Ω diff.		-85		

Figure 2. Load configuration

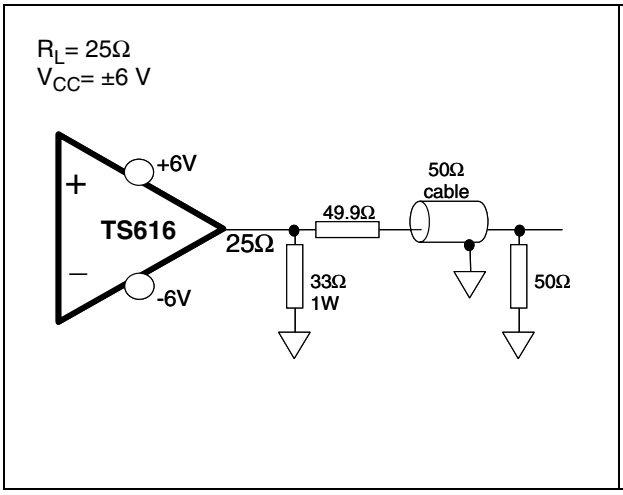


Figure 3. Load configuration

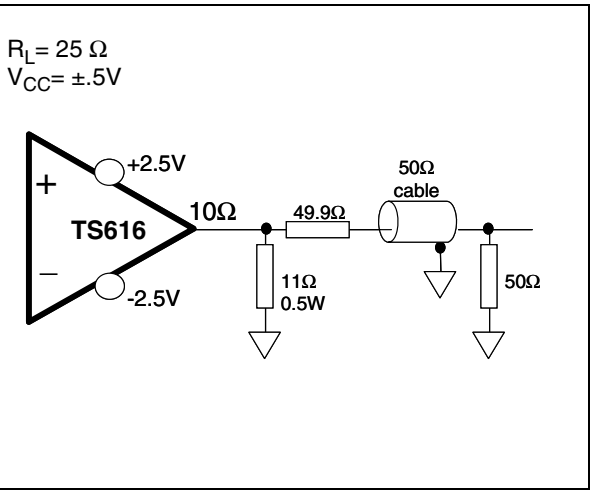


Figure 4. Closed loop gain vs. frequency

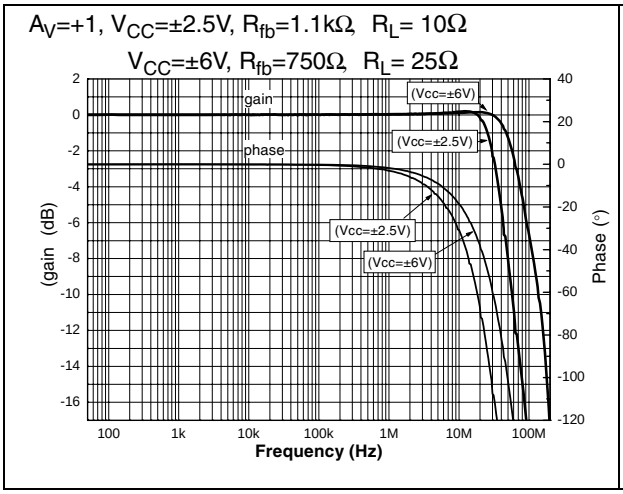


Figure 5. Closed loop gain vs. frequency

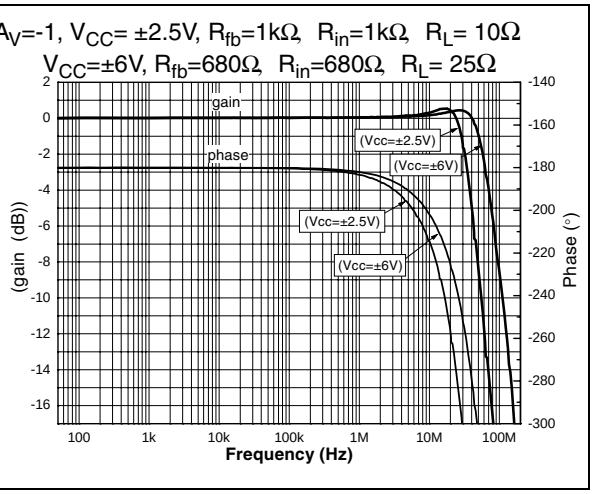


Figure 6. Closed loop gain vs. frequency

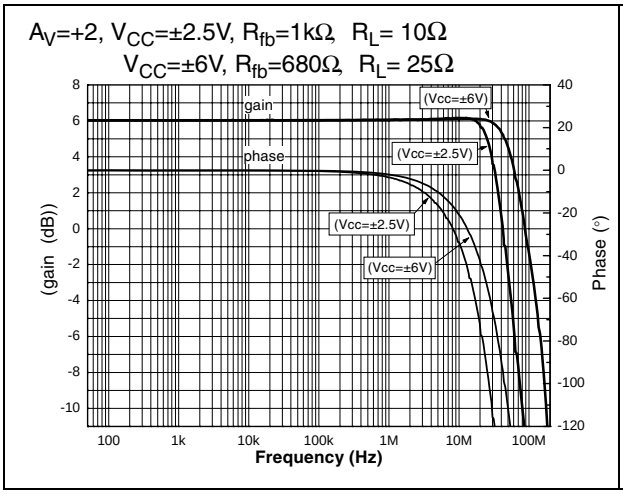


Figure 7. Closed loop gain vs. frequency

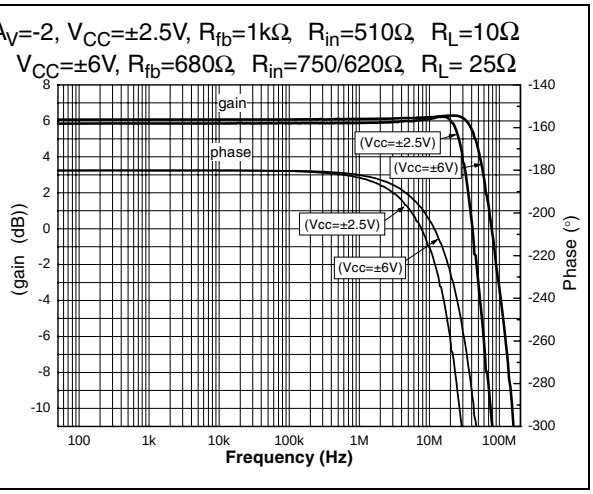


Figure 8. Closed loop gain vs. frequency

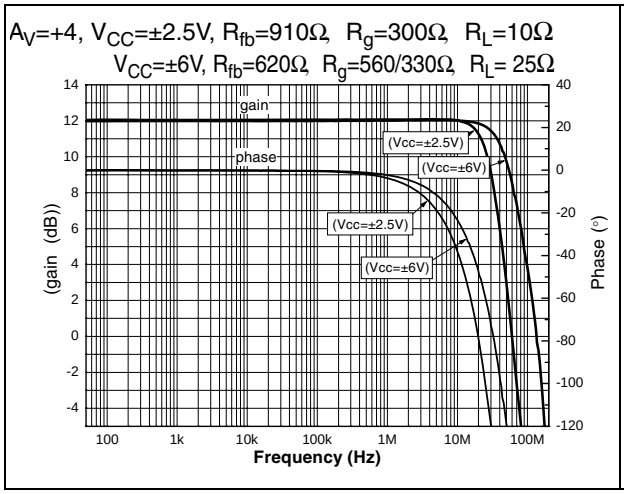


Figure 9. Closed loop gain vs. frequency

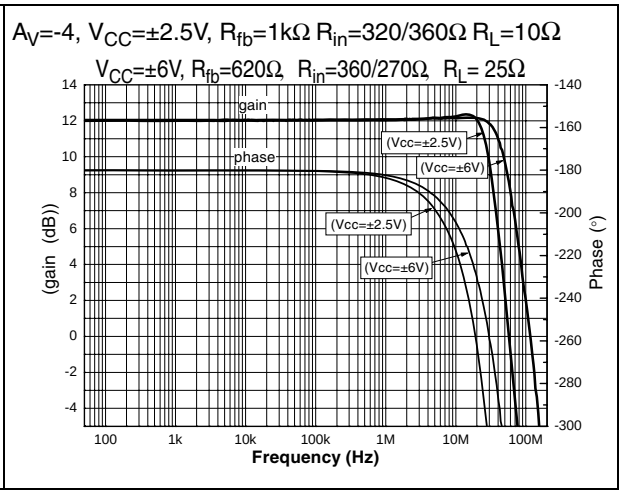


Figure 10. Closed loop gain vs. frequency

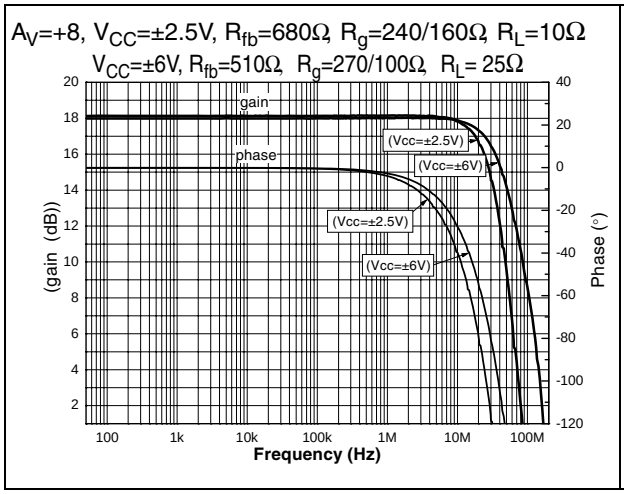


Figure 11. Closed loop gain vs. frequency

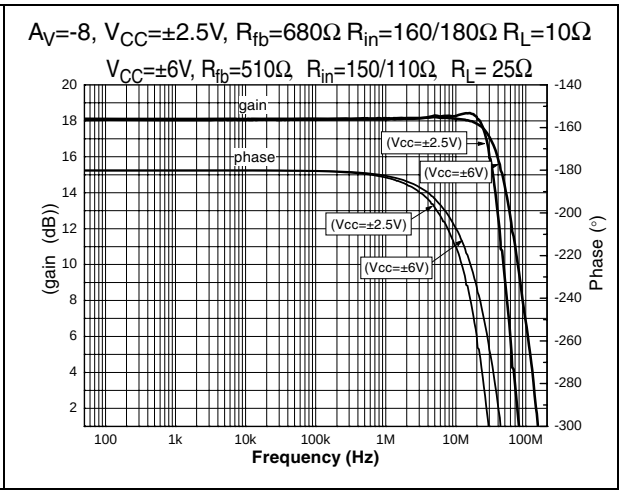


Figure 12. Positive slew rate

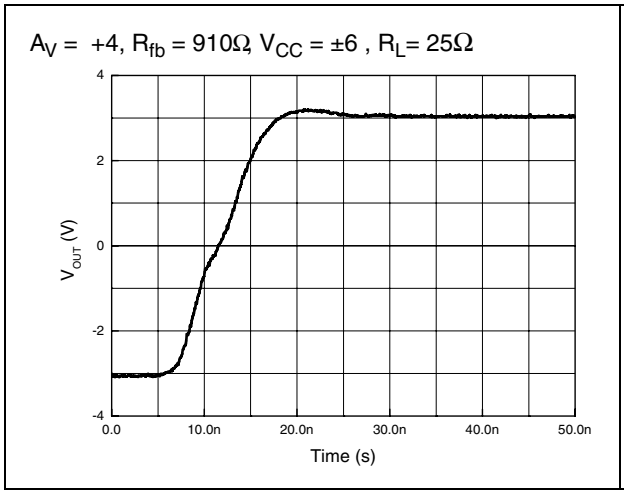


Figure 13. Positive slew rate

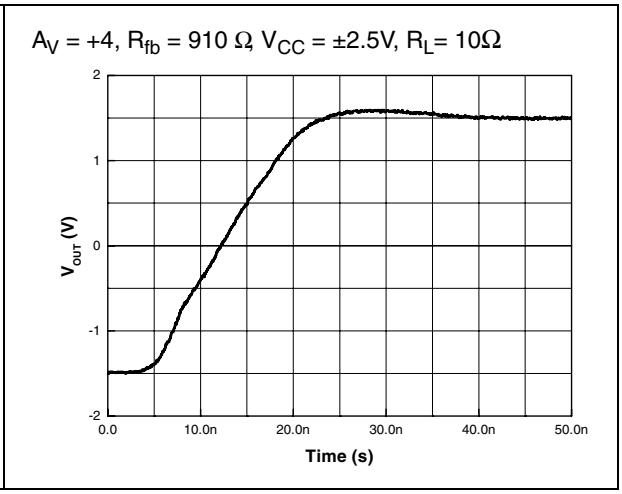


Figure 14. Positive slew rate

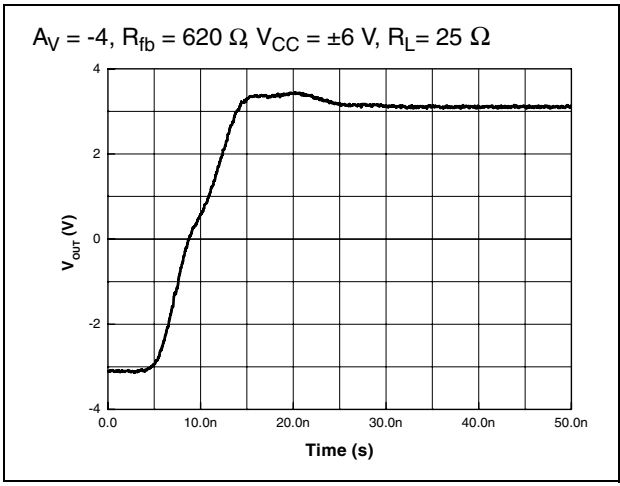


Figure 15. Positive slew rate

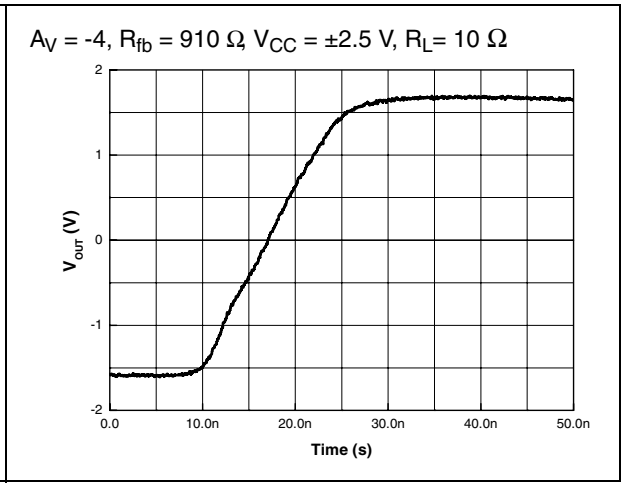


Figure 16. Negative slew rate

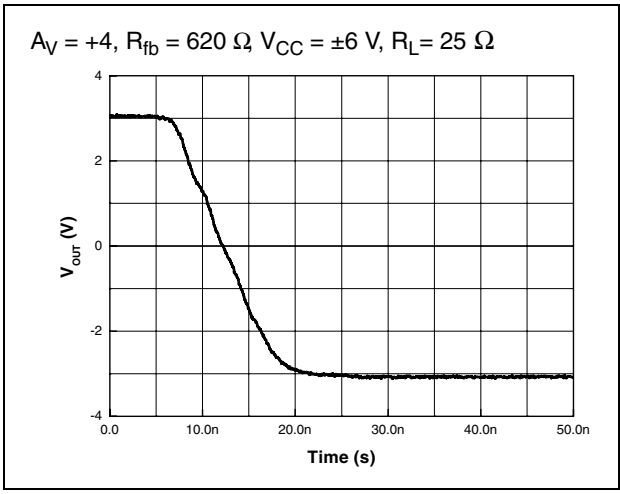


Figure 17. Negative slew rate

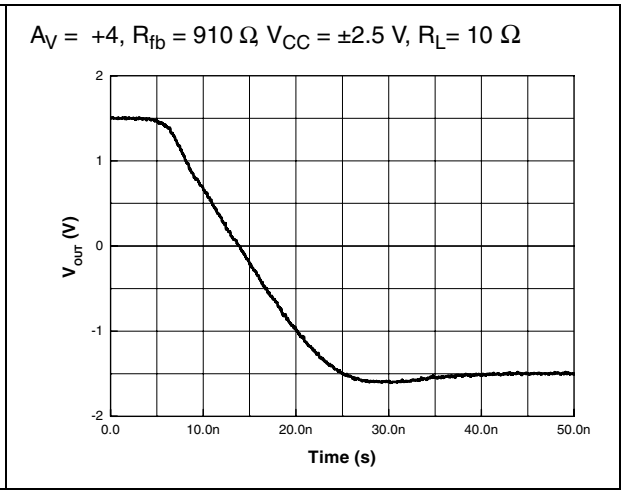


Figure 18. Negative slew rate

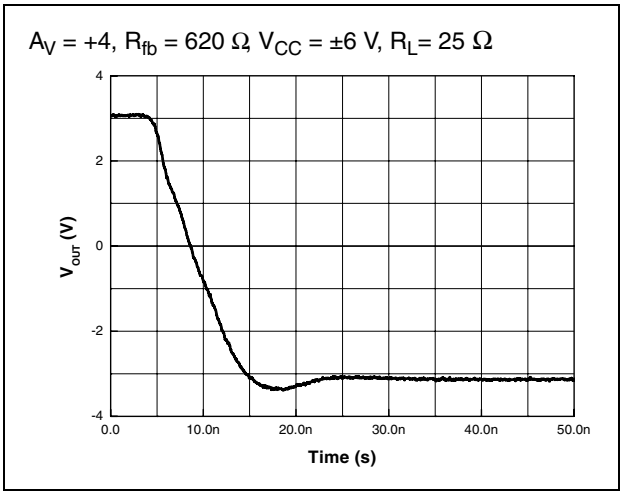


Figure 19. Negative slew rate

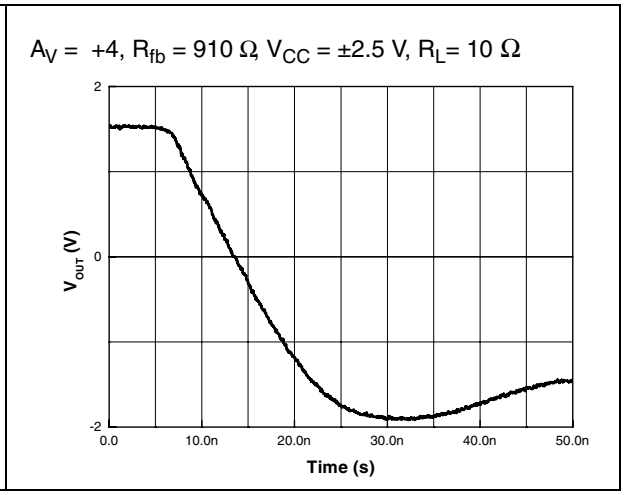


Figure 20. Input voltage noise level

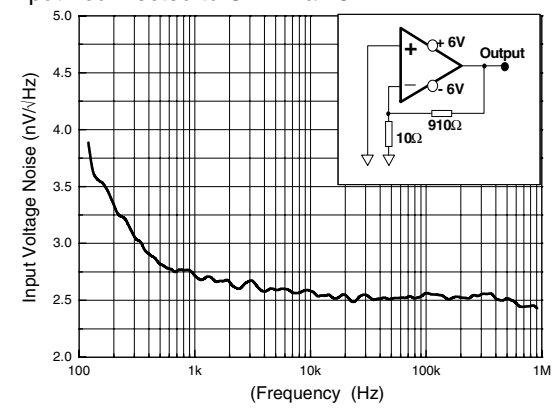


Figure 21. I_{CC} vs. power supply

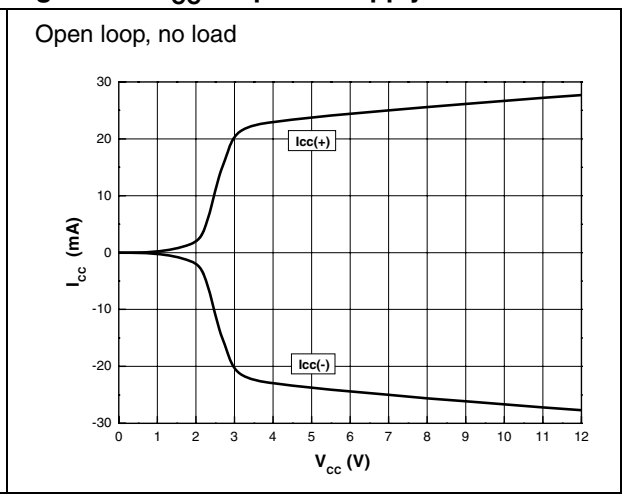


Figure 22. I_{ib} vs. power supply

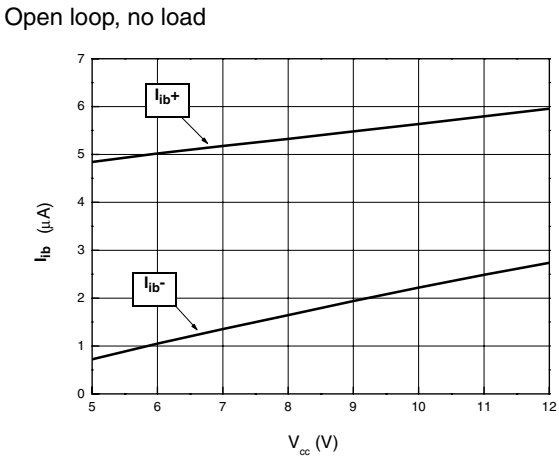


Figure 23. V_{OH} & V_{OL} vs. power supply

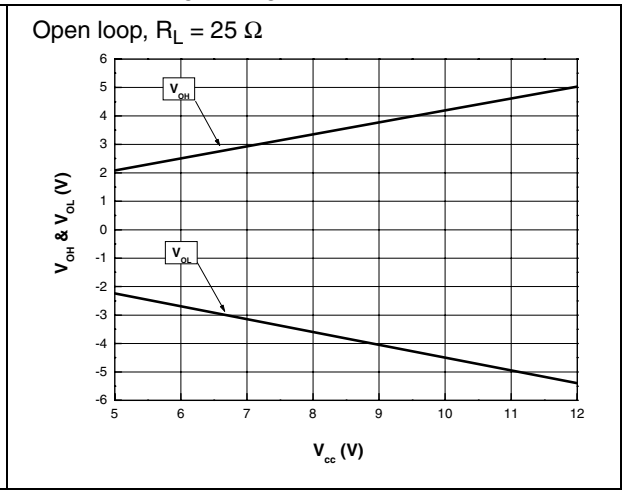


Figure 24. I_{source} vs. output amplitude

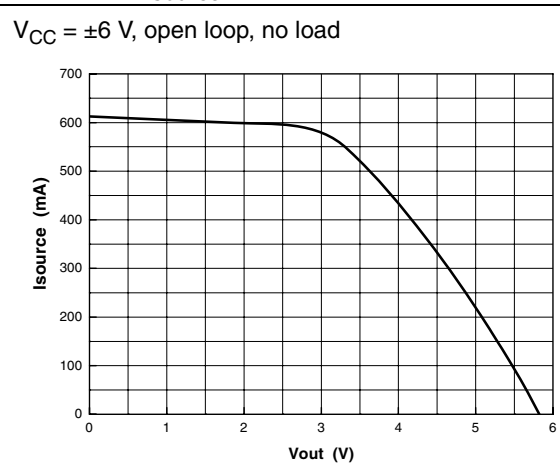


Figure 25. I_{source} vs. output amplitude

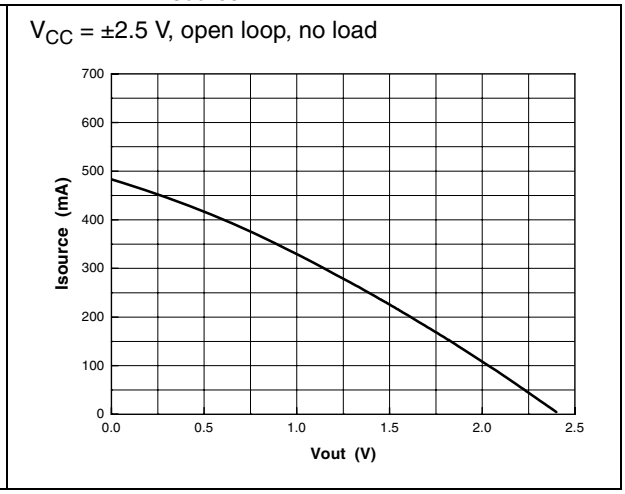


Figure 26. I_{sink} vs. output amplitude

V_{CC} = ±6 V, open loop, no load

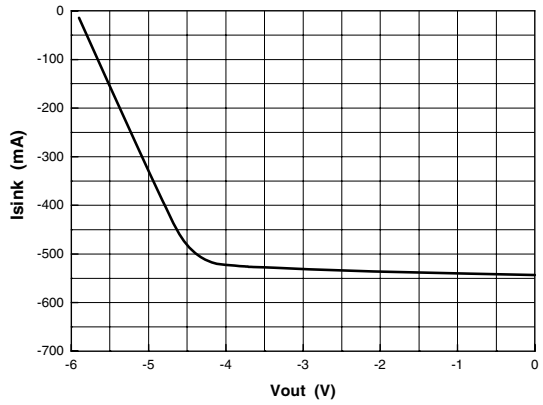


Figure 27. I_{sink} vs. output amplitude

V_{CC} = ±2.5 V, open loop, no load

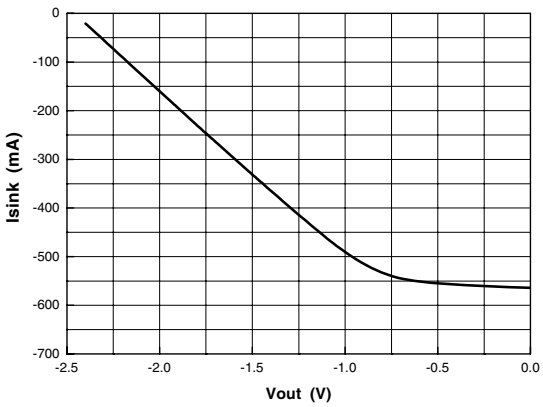


Figure 28. Maximum output amplitude vs. load

A_V = +4, R_{fb} = 620 Ω, V_{CC} = ±6 V

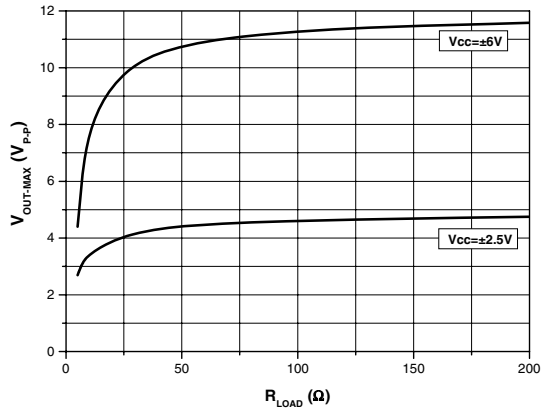


Figure 29. Bandwidth vs. temperature

A_V = +4, R_{fb} = 910 Ω

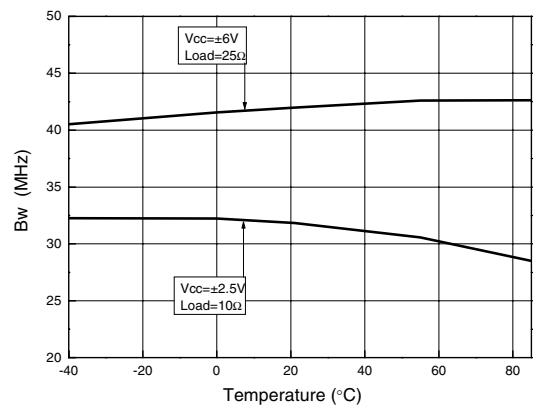


Figure 30. Transimpedance vs. temperature

Open loop

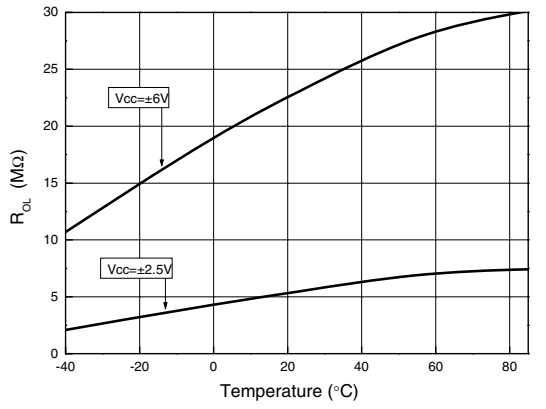


Figure 31. I_{CC} vs. temperature

Open loop, no load

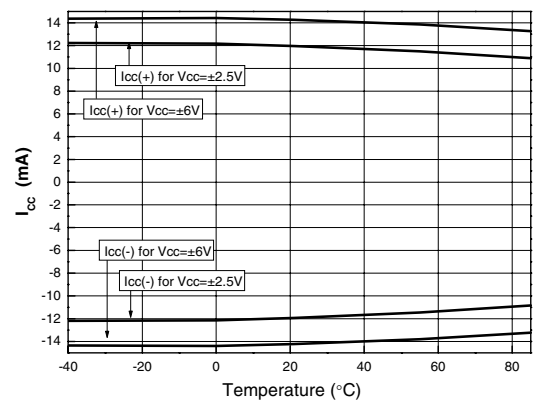


Figure 32. Slew rate vs. temperature

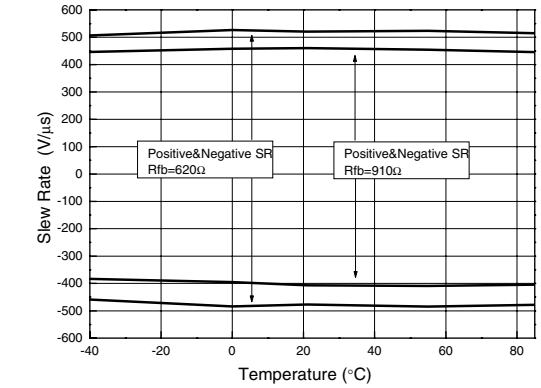


Figure 33. Slew rate vs. temperature

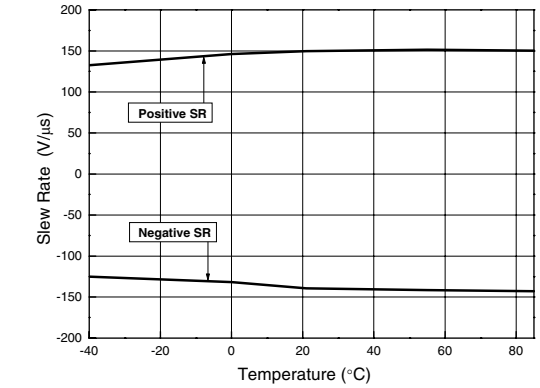


Figure 34. I_{ib}(+) vs. temperature

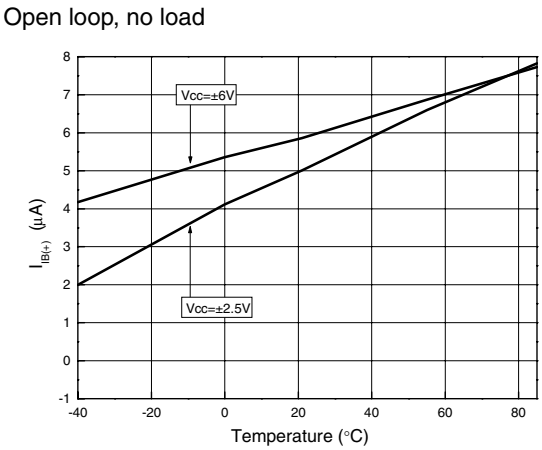


Figure 35. I_{ib}(+) vs. temperature

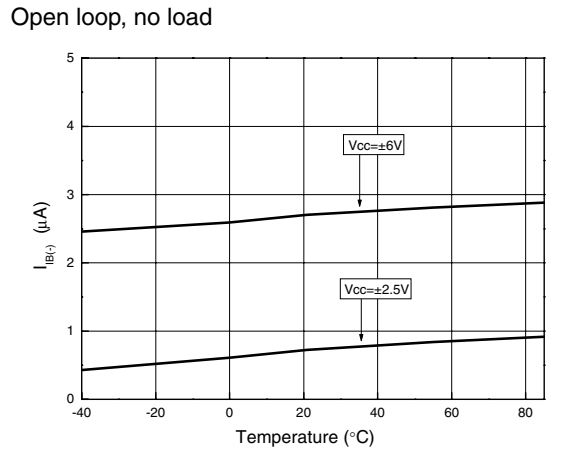


Figure 36. V_{OH} vs. temperature

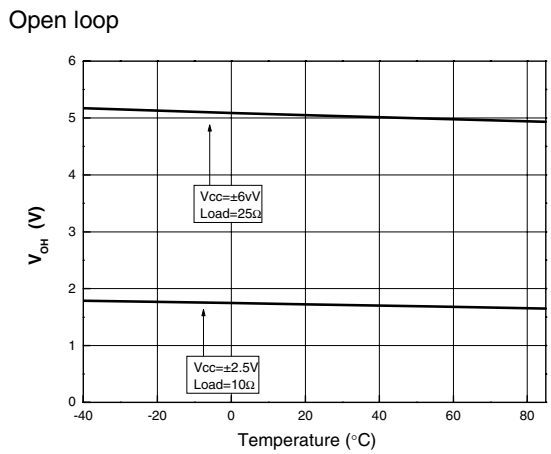


Figure 37. V_{OL} vs. temperature

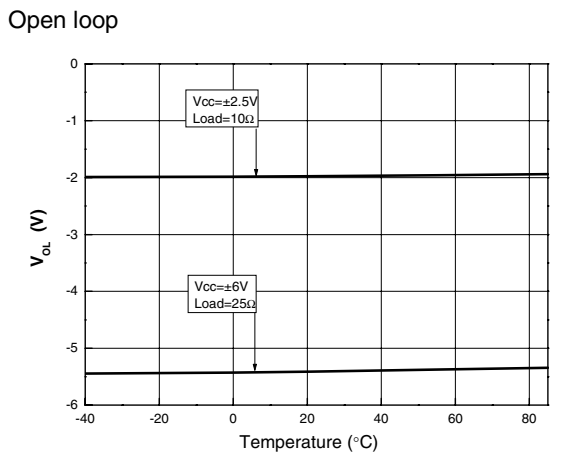


Figure 38. Differential V_{io} vs. temperature

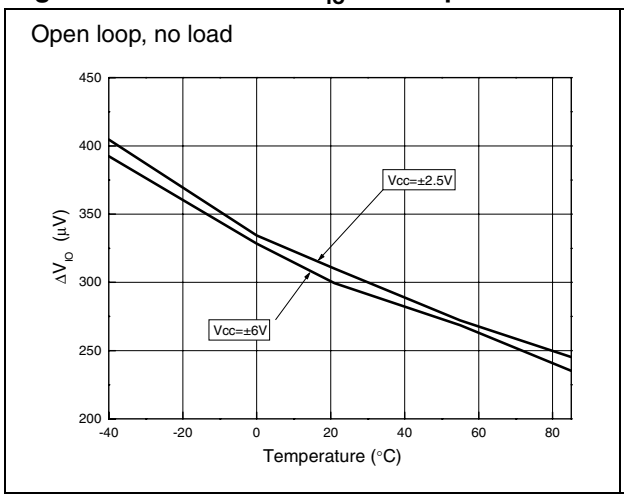


Figure 39. V_{io} vs. temperature

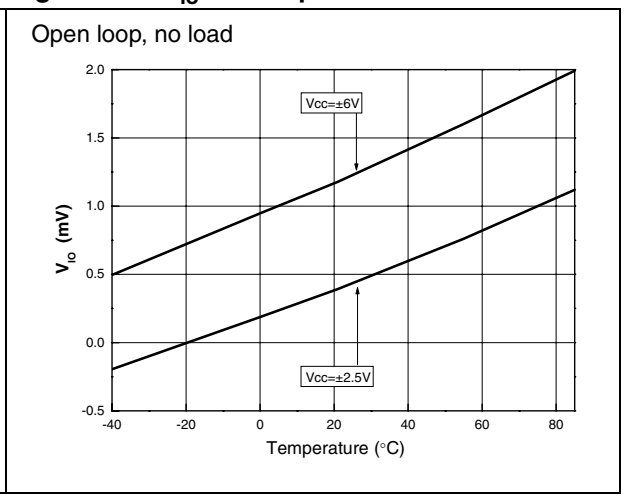


Figure 40. I_{out} vs. temperature

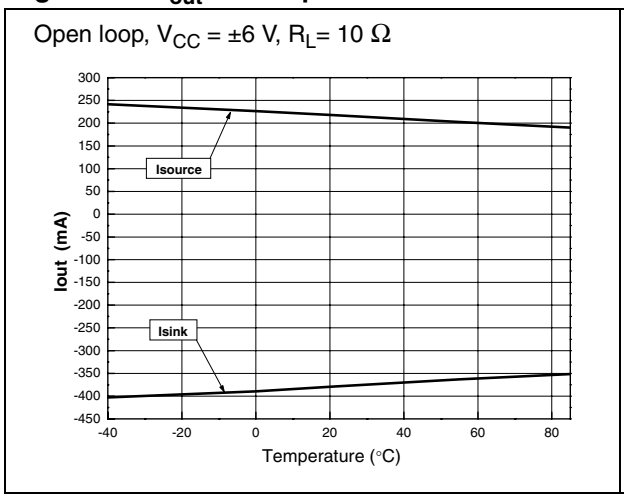


Figure 41. I_{out} vs. temperature

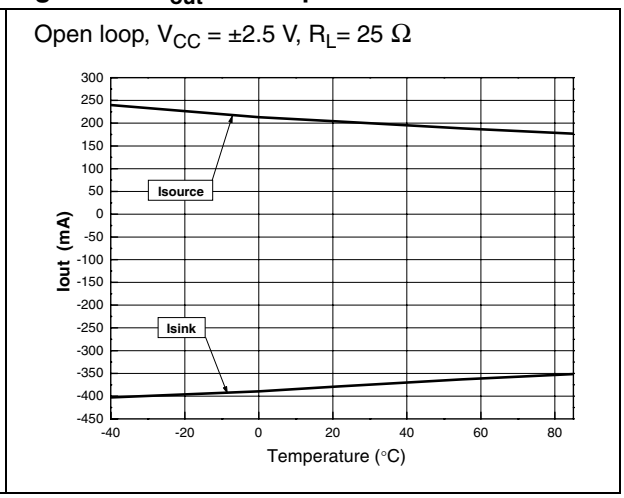


Figure 42. CMR vs. temperature

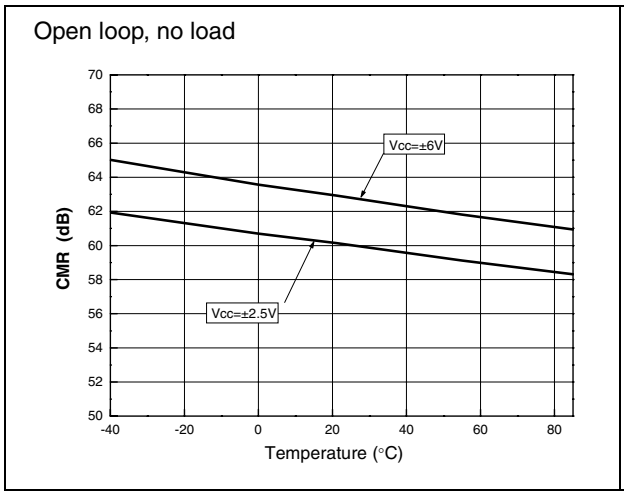
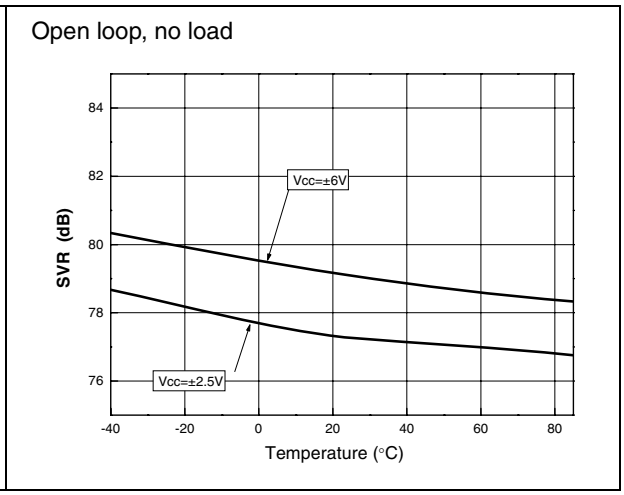


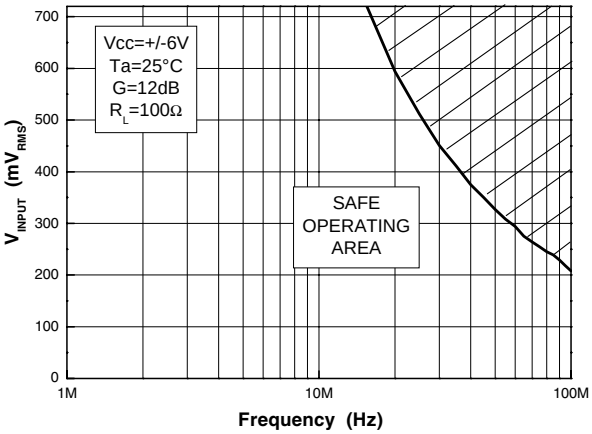
Figure 43. SVR vs. temperature



4 Safe operating area

Figure 44 shows the safe operating zone for the TS616. The curve shows the input level vs. the input frequency—a characteristic curve which must be considered in order to ensure a good application design. In the dash-lined zone, the consumption increases, and this increased consumption could do damage to the chip if the temperature increases.

Figure 44. Safe operating area



5 Intermodulation distortion product

The non-ideal output of the amplifier can be described by the following series, due to a non-linearity in the input-output amplitude transfer:

$$V_{out} = C_0 + C_1 V_{in} + C_2 V_{in}^{2} + C_n V_{in}^{n}$$

where the single-tone input is $V_{in}=A\sin\omega t$, and C_0 is the DC component, $C_1(V_{in})$ is the fundamental, C_n is the amplitude of the harmonics of the output signal V_{out}.

A one-frequency (one-tone) input signal contributes to a harmonic distortion. A two-tone input signal contributes to a harmonic distortion and an intermodulation product.

This intermodulation product, or rather, the study of the intermodulation distortion of a two-tone input signal is the first step in characterizing the amplifiers capability for driving multi-tone signals.

The two-tone input is equal to:

$$V_{in} = A\sin\omega_1 t + B\sin\omega_2 t$$

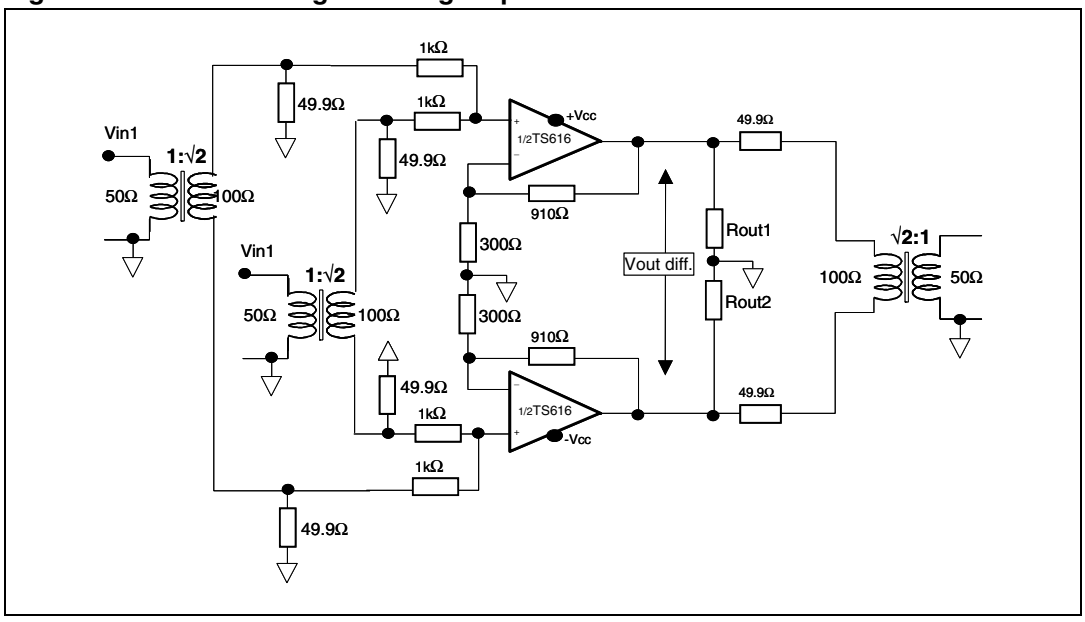
giving:

$$_t = C_0 + C_1(A\sin\omega_1 t + B\sin\omega_2 t) + C_2(A\sin\omega_1 t + B\sin\omega_2 t)^2 \ldots + C_n(A\sin\omega_1 t + B\sin\omega_2 t)^n$$

In this expression, we can extract distortion terms and intermodulation terms from a single sine wave: second-order intermodulation terms IM2 by the frequencies (ω_1 - ω_2) and (ω_1 +ω_2) with an amplitude of $C2A^2$ and third-order intermodulation terms IM3 by the frequencies ($2\omega_1$ - ω_2), ($2\omega_1$ +ω_2), ($-\omega_1$ + $2\omega_2$) and (ω_1 +$2\omega_2$) with an amplitude of $(3/4)C3A^3$.

We can measure the intermodulation product of the driver by using the driver as a mixer via a summing amplifier configuration. In doing this, the non-linearity problem of an external mixing device is avoided.

Figure 45. Non-inverting summing amplifier for intermodulation measurements



The following graphs show the IM2 and the IM3 of the amplifier in different configurations. The two-tone input signal was generated by the multisource generator Marconi 2026. Each tone has the same amplitude. The measurement was performed using a HP3585A spectrum analyzer.

Figure 46. Intermodulation vs. output amplitude

370 kHz & 400 kHz
A_V = +1.5, R_{fb} = 1kΩ, V_{CC} = ±2.5 V, R_L= 14 Ω diff.

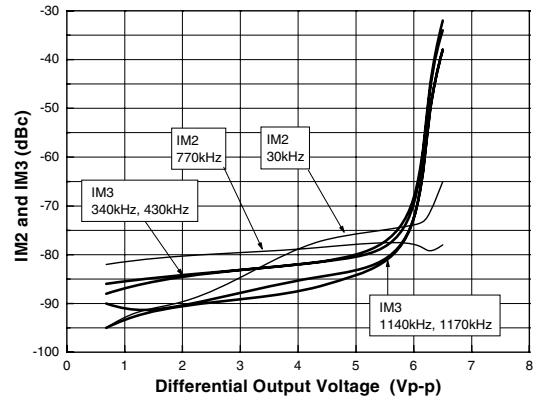


Figure 47. Intermodulation vs. output amplitude

370 kHz & 400 kHz
A_V = +1.5, R_{fb} = 1kΩ, V_{CC} = ±2.5 V, R_L= 28 Ω diff.

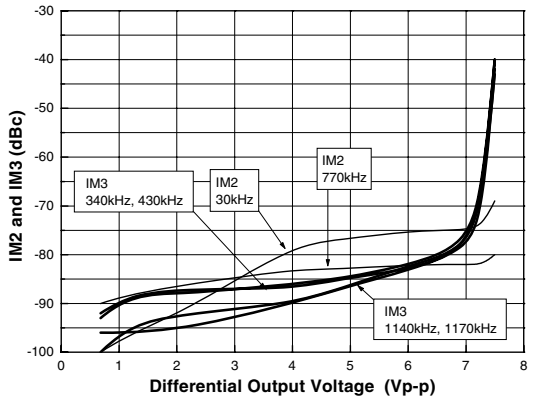


Figure 48. Intermodulation vs. gain

370 kHz & 400 kHz
V_{out}= 6 V_{pp}, V_{CC} = ±2.5 V, R_L= 20 Ω diff.

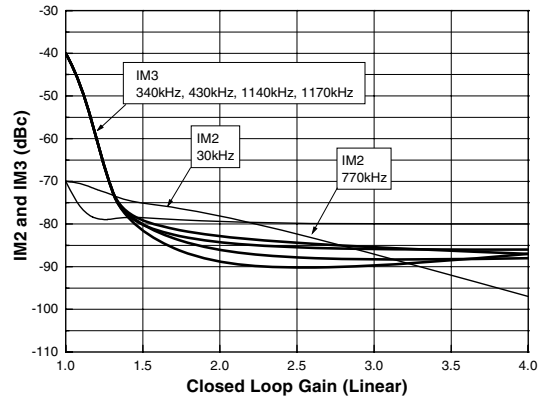


Figure 49. Intermodulation vs. load

370 kHz & 400 kHz
A_V = +1.5, R_{fb} = 1kΩ, V_{out}= .56 V_{pp}, V_{CC} = ±2.5 V

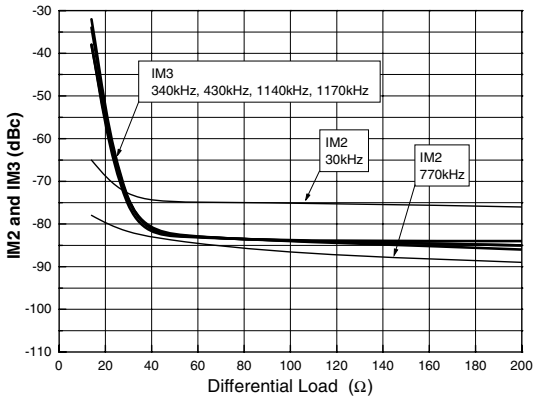


Figure 50. Intermodulation vs. output amplitude

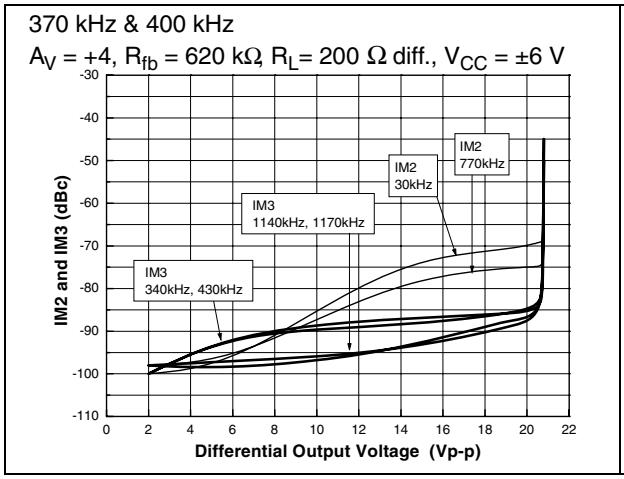


Figure 51. Intermodulation vs. output amplitude

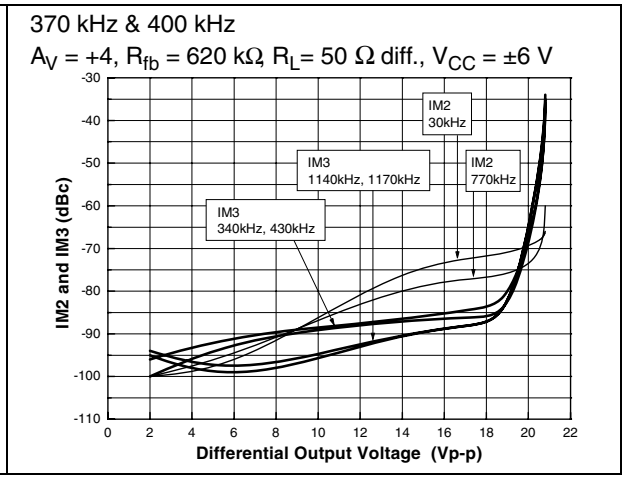


Figure 52. Intermodulation vs. output amplitude

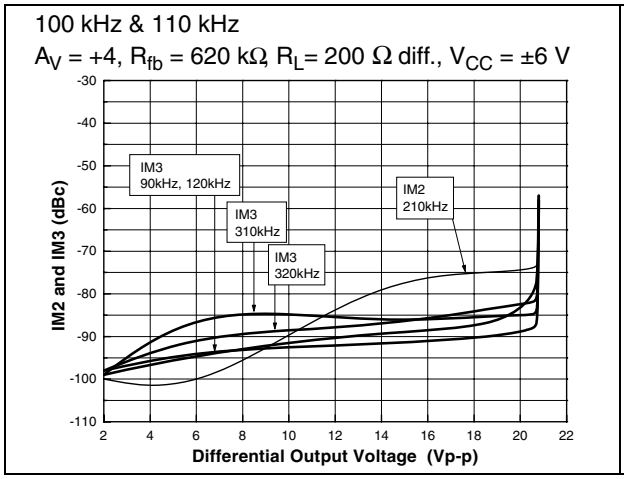


Figure 53. Intermodulation vs. output amplitude

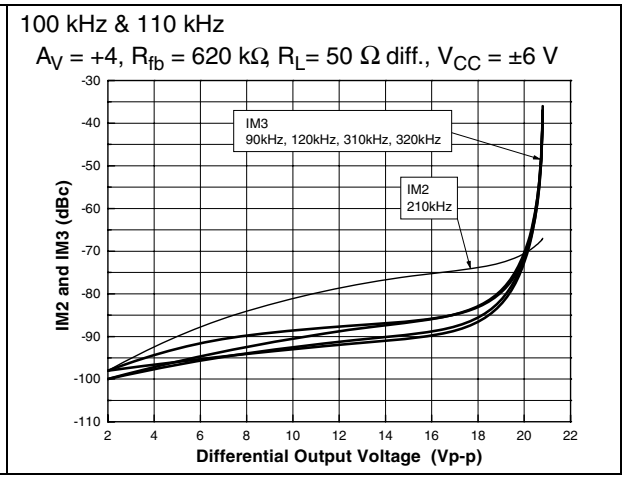
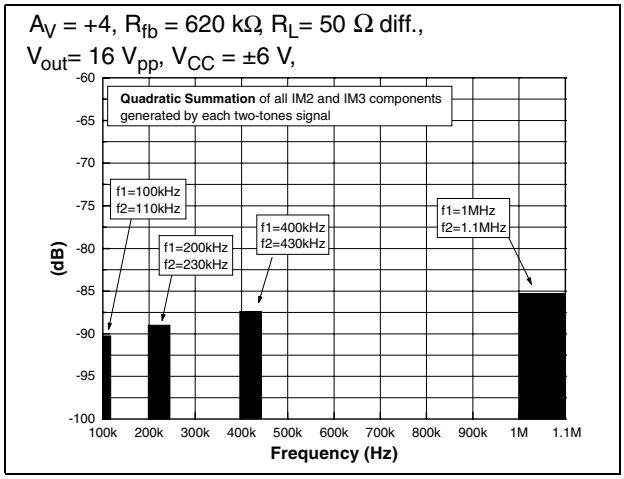


Figure 54. Intermodulation vs. frequency range



6 Printed circuit board layout considerations

In the ADSL frequency range, printed circuit board parasites can affect the closed-loop performance.

The use of a proper ground plane on both sides of the PCB is necessary to provide low inductance and a low resistance common return. The most important factors affecting gain flatness and bandwidth are stray capacitance at the output and inverting input. To minimize capacitance, the space between signal lines and ground plane should be maximized. Feedback component connections must be as short as possible in order to decrease the associated inductance which affects high-frequency gain errors. It is very important to choose the smallest possible external components—for example, surface mounted devices (SMD)—in order to minimize the size of all DC and AC connections.

6.1 Thermal information

The TS616 is housed in an exposed-pad plastic package. As described in *Figure 55*, this package has a lead frame upon which the dice is mounted. This lead frame is exposed as a thermal pad on the underside of the package. The thermal contact is direct with the dice. This thermal path provides an excellent thermal performance.

The thermal pad is electrically isolated from all pins in the package. It must be soldered to a copper area of the PCB underneath the package. Through these thermal paths within this copper area, heat can be conducted away from the package. The copper area **must** be connected to $-V_{CC}$ available on pin 4.

Figure 55. Exposed-pad package

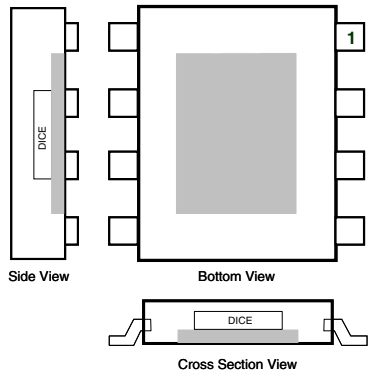


Figure 56. Evaluation board

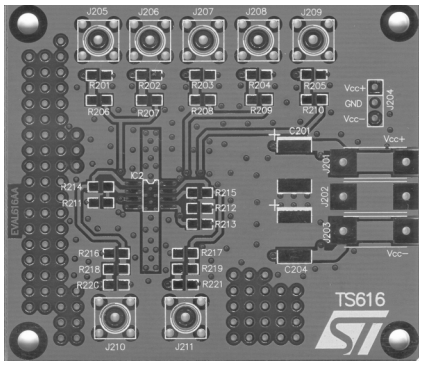


Figure 57. Schematic diagram

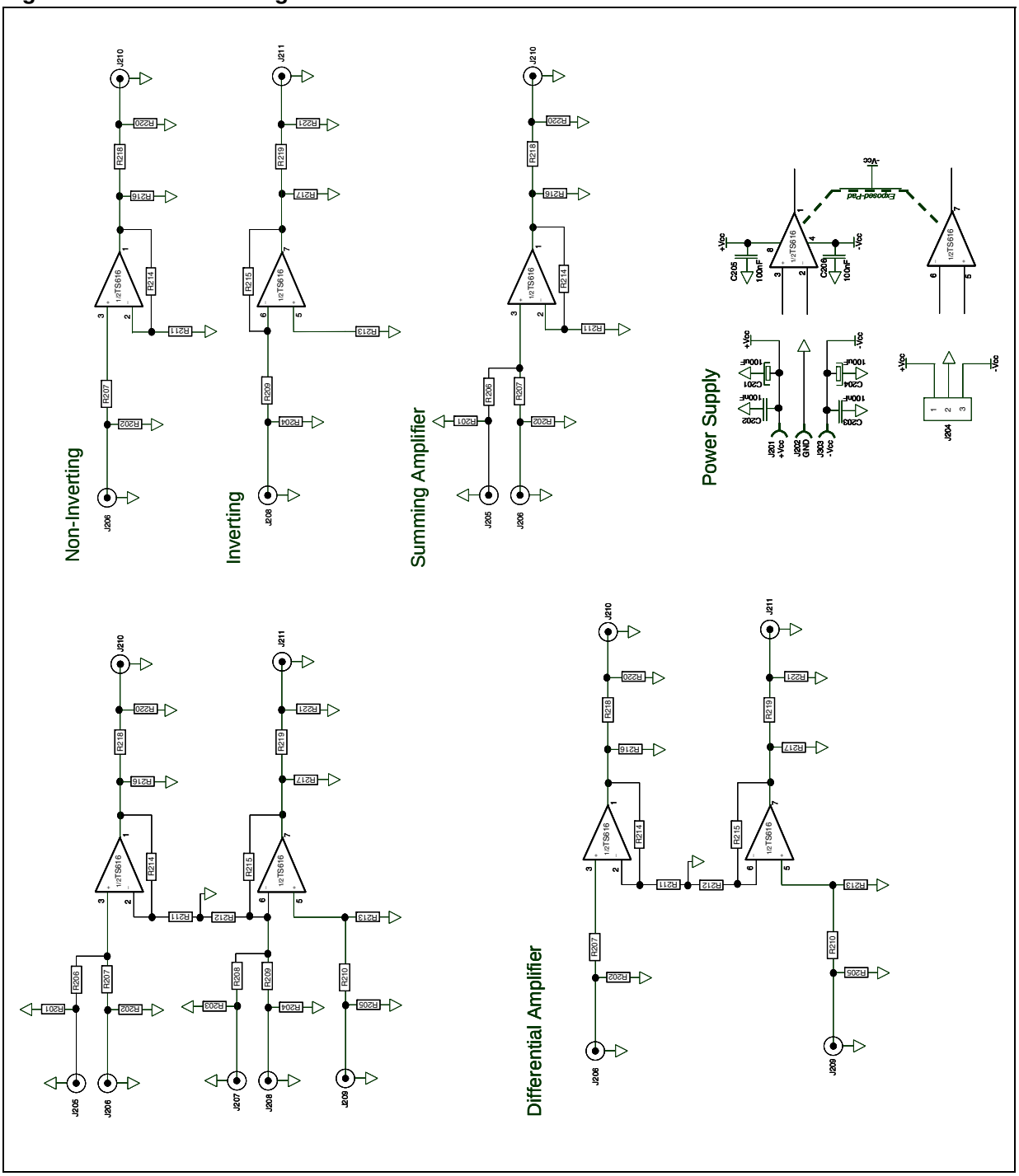


Figure 58. Component locations - top side

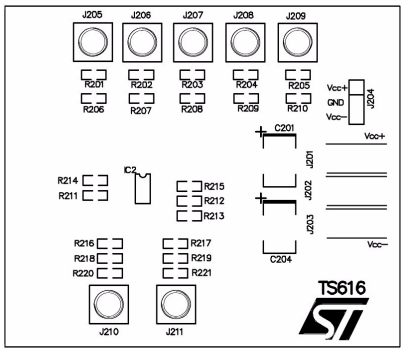


Figure 59. Component locations - bottom side

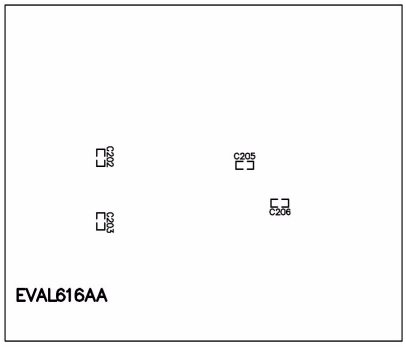


Figure 60. Top side board layout

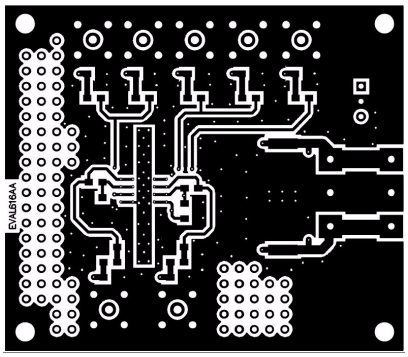
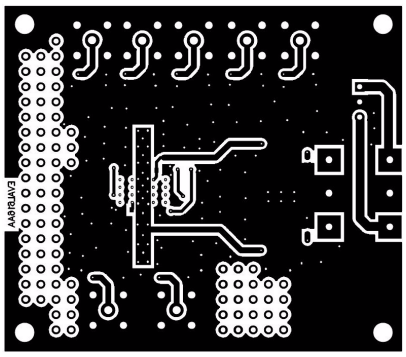


Figure 61. Bottom side board layout

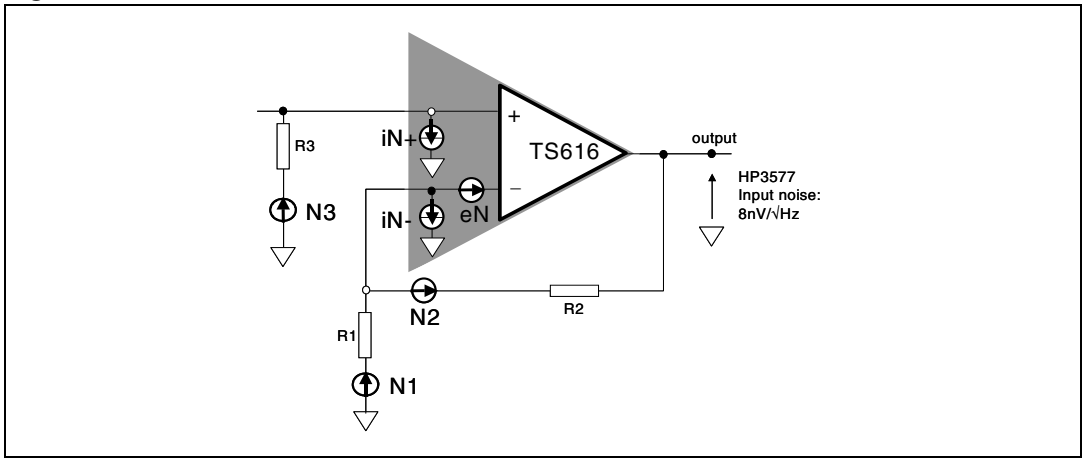


7 Noise measurements

The noise model is shown in *Figure 62*, where:

- eN: input voltage noise of the amplifier
- iNn: negative input current noise of the amplifier
- iNp: positive input current noise of the amplifier

Figure 62. Noise model



The closed loop gain is:

$$A_V = g = 1 + \frac{R_{fb}}{R_g}$$

The six noise sources are:

$$V1 = eN \times \left(1 + \frac{R2}{R1}\right)$$

$$V2 = iNn \times R2$$

$$V3 = iNp \times R3 \times \left(1 + \frac{R2}{R1}\right)$$

$$V4 = -\frac{R2}{R1} \times \sqrt{4kTR1}$$

$$V5 = \sqrt{4kTR2}$$

$$V6 = \left(1 + \frac{R2}{R1}\right)\sqrt{4kTR3}$$

We assume that the thermal noise of a resistance R is:

$$\sqrt{4kTR\Delta F}$$

where ΔF is the specified bandwidth.

On a 1 Hz bandwidth the thermal noise is reduced to:

$$\sqrt{4kTR}$$

where k is Boltzmann's constant, equal to 1374.10^{-23}J/°K. T is the temperature (°K).

The output noise eNo is calculated using the Superposition Theorem. However eNo is not the sum of all noise sources, but rather the square root of the sum of the square of each noise source, as shown in *Equation 1*.

Equation 1

$$No = \sqrt{V1^2 + V2^2 + V3^2 + V4^2 + V5^2 + V6^2}$$

Equation 2

$$No^2 = eN^2 \times g^2 + iNn^2 \times R2^2 + iNp^2 \times R3^2 \times g^2$$
$$\ldots + \left(\frac{R2}{R1}\right)^2 \times 4kTR1 + 4kTR2 + \left(1 + \frac{R2}{R1}\right)^2 \times 4kTR3$$

The input noise of the instrumentation must be extracted from the measured noise value. The real output noise value of the driver is:

Equation 3

$$eNo = \sqrt{(Measured)^2 - (instrumentation)^2}$$

The input noise is called the Equivalent Input Noise as it is not directly measured but is evaluated from the measurement of the output divided by the closed loop gain (eNo/g).

After simplification of the fourth and the fifth term of *Equation 2* we obtain:

Equation 4

$$= eN^2 \times g^2 + iNn^2 \times R2^2 + iNp^2 \times R3^2 \times g^2 \ldots + g \times 4kTR2 + \left(1 + \frac{R2}{R1}\right)^2 \times 4k$$

7.1 Measurement of *eN*

If we assume a short-circuit on the non-inverting input (R3=0), *Equation 4* becomes:

Equation 5

$$No = \sqrt{eN^2 \times g^2 + iNn^2 \times R2^2 + g \times 4kTR2}$$

In order to easily extract the value of eN, the resistance R2 will be chosen as low as possible. On the other hand, the gain must be large enough:

- R1=10 Ω, R2=910 Ω, R3=0, Gain=92
- Equivalent input noise: 2.57 nV/√Hz
- Input voltage noise: eN=2.5 nV/√Hz

7.2 Measurement of *iNn*

To measure the negative input current noise iNn, we set R3=0 and use *Equation 5*. This time the gain must be lower in order to decrease the thermal noise contribution:

- R1=100 Ω, R2=910 Ω, R3=0, gain= 10.1
- Equivalent input noise: 3.40 nV/√Hz
- Negative input current noise: iNn =21 pA/√Hz

7.3 Measurement of *iNp*

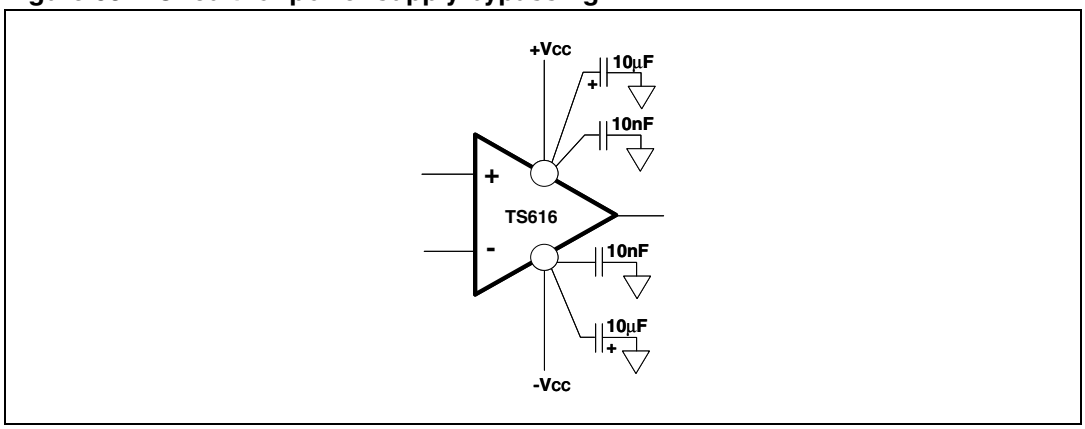
To extract iNp from *Equation 3*, a resistance R3 is connected to the non-inverting input. The value of R3 must be chosen in order to keep its thermal noise contribution as low as possible against the iNp contribution.

- R1=100 Ω, R2=910 Ω, R3=100 Ω, Gain=10.1
- Equivalent input noise: 3.93 nV/√Hz
- Positive input current noise: iNp=15 pA/√Hz
- Conditions: Frequency=100 kHz, V_{CC} = ±2.5 V
- Instrumentation: HP3585A Spectrum Analyzer (the input noise of the HP3585A is 8 nV/√Hz)

8 Power supply bypassing

Correct power supply bypassing is very important for optimizing performance in high-frequency ranges. Bypass capacitors should be placed as close as possible to the IC pins to improve high-frequency bypassing. A capacitor greater than 1 µF is necessary to minimize the distortion. For better quality bypassing, a capacitor of 10 nF is added using the same implementation conditions. Bypass capacitors must be incorporated for both the negative and the positive supply.

Figure 63. Circuit for power supply bypassing



8.1 Single power supply

The TS616 can operate with power supplies ranging from 12 V to 5 V. The power supply can either be single (12 V or 5 V referenced to ground), or dual (such as ±6 V and ±2.5 V).

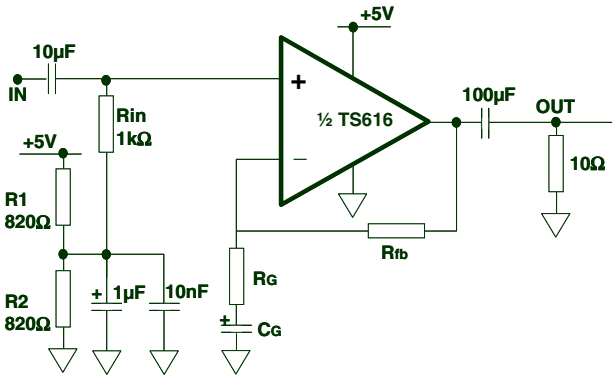
In the event that a single supply system is used, new biasing is necessary to assume a positive output dynamic range between 0 V and $+V_{CC}$ supply rails. Considering the values of V_{OH} and V_{OL}, the amplifier will provide an output dynamic from +0.5 V to 10.6 V on 25 Ω load for a 12 V supply and from 0.45 V to 3.8 V on 10 Ω load for a 5 V supply.

The amplifier must be biased with a mid-supply (nominally $+V_{CC}/2$), in order to maintain the DC component of the signal at this value. Several options are possible to provide this bias supply, such as a virtual ground using an operational amplifier or a two-resistance divider (which is the cheapest solution). A high resistance value is required to limit the current consumption. On the other hand, the current must be high enough to bias the non-inverting input of the amplifier. If we consider this bias current (30 µA max.) as the 1% of the current through the resistance divider to keep a stable mid-supply, two resistances of 2.2 kΩ can be used in the case of a 12 V power supply and two resistances of 820 Ω can be used in the case of a 5 V power supply.

The input provides a high-pass filter with a break frequency below 10 Hz which is necessary to remove the original 0 volt DC component of the input signal, and to fix it at $+V_{CC}/2$.

Figure 64 shows a schematic of a 5 V single power supply configuration.

Figure 64. Circuit for +5 V single supply

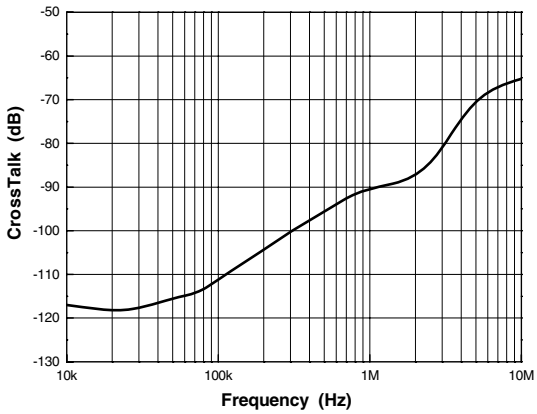


8.2 Channel separation and crosstalk

Figure 65 shows an example of crosstalk from one amplifier to a second amplifier. This phenomenon, accentuated at high frequencies, is unavoidable and intrinsic to the circuit itself.

Nevertheless, the PCB layout also has an effect on the crosstalk level. Capacitive coupling between signal wires, distance between critical signal nodes and power supply bypassing are the most significant factors.

Figure 65. Crosstalk vs. frequency: A_V=+4, R_{fb}=620 Ω, V_{CC}= ±6 V, V_{out}= 2 V_p



9 Choosing the feedback circuit

As described in *Figure 67* on page 29, the TS616 requires a 620Ω feedback resistor to optimize the bandwidth with a gain of 12 dB for a 12 V power supply. Nevertheless, due to production test constraints, the TS616 is tested with the same feedback resistor for 12 V and 5 V power supplies (910 Ω).

Table 5. Closed-loop gain - feedback components

V_{CC} (V)	Gain	R_{fb} (Ω)
±6	+1	750
	+2	680
	+4	620
	+8	510
	-1	680
	-2	680
	-4	620
	-8	510
±2.5	+1	1.1k
	+2	1k
	+4	910
	+8	680
	-1	1k
	-2	1k
	-4	910
	-8	680

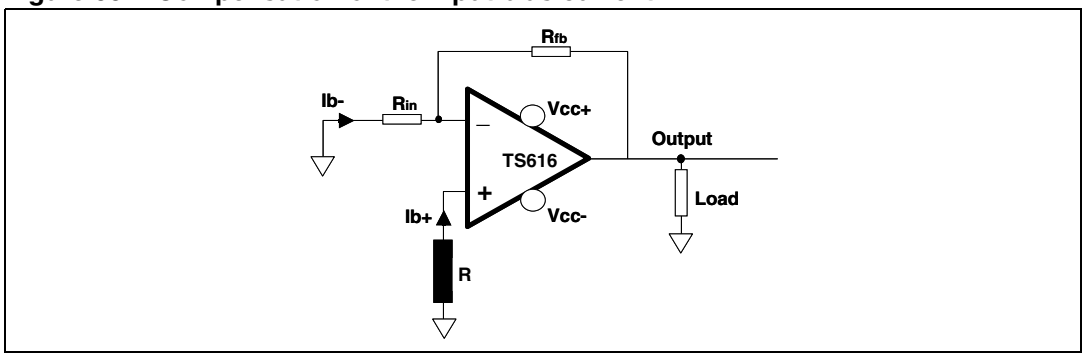
9.1 The bias of an inverting amplifier

A resistance is necessary to achieve good input biasing, such as resistance R, shown in *Figure 66*.

The magnitude of this resistance is calculated by assuming the negative and positive input bias current. The aim is to compensate for the offset bias current, which could affect the input offset voltage and the output DC component. Assuming Ib-, Ib+, R_{in}, R_{fb} and a zero volt output, the resistance R is:

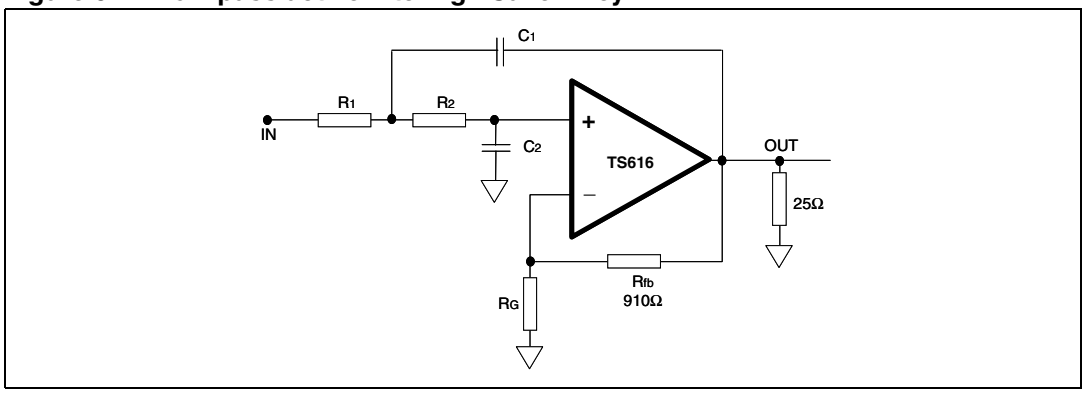
$$R = R_{in} // R_{fb}$$

Figure 66. Compensation of the input bias current



9.2 Active filtering

Figure 67. Low-pass active filtering - Sallen-Key



From the resistors R_{fb} and $R_{G,}$ we can directly calculate the gain of the filter in a classic non-inverting amplification configuration:

$$A_V = g = 1 + \frac{R_{fb}}{R_g}$$

We assume the following expression as the response of the system:

$$T_{j\omega} = \frac{Vout_{j\omega}}{Vin_{j\omega}} = \frac{g}{1 + 2\zeta\frac{j\omega}{\omega_c} + \frac{(j\omega)^2}{\omega_c^2}}$$

The cutoff frequency is not gain-dependent and so becomes:

$$\omega_c = \frac{1}{\sqrt{R1R2C1C2}}$$

The damping factor is calculated by the following expression:

$$\zeta = \frac{1}{2}\omega_c(C_1R_1 + C_1R_2 + C_2R_1 - C_1R_1g)$$

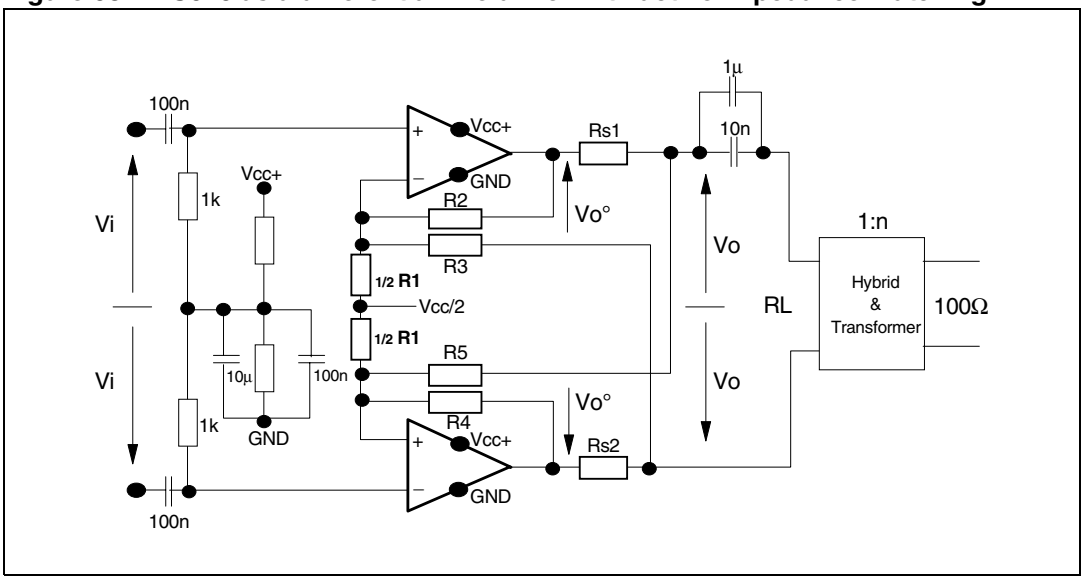
The higher the gain the more sensitive the damping factor is. When the gain is higher than 1, it is preferable to use some very stable resistor and capacitor values. In the case of R1 = R2:

$$\zeta = \frac{2C_2 - C_1\frac{R_{fb}}{R_g}}{2\sqrt{C_1C_2}}$$

10 Increasing the line level using active impedance matching

With passive matching, the output signal amplitude of the driver must be twice the amplitude on the load. To go beyond this limitation an active matching impedance can be used. With this technique, it is possible to maintain good impedance matching with an amplitude on the load higher than half of the output driver amplitude. This concept is shown in *Figure 68* for a differential line.

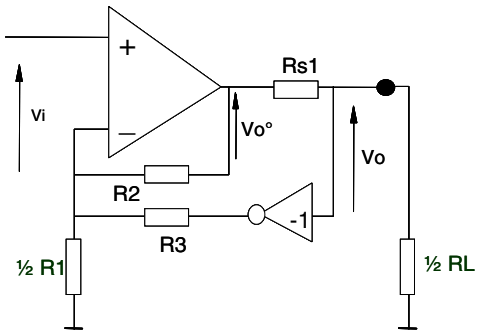
Figure 68. TS616 as a differential line driver with active impedance matching



Component calculation

Let us consider the equivalent circuit for a single-ended configuration, as shown in *Figure 69*.

Figure 69. Single-ended equivalent circuit



First let's consider the unloaded system. We can assume that the currents through R1, R2 and R3 are respectively:

$$\frac{2Vi}{R1}, \frac{(Vi - Vo^{\circ})}{R2} \text{and} \frac{(Vi + Vo)}{R3}$$

As Vo◦ equals Vo without load, the gain in this case becomes:

$$G = \frac{Vo(noload)}{Vi} = \frac{1 + \frac{2R2}{R1} + \frac{R2}{R3}}{1 - \frac{R2}{R3}}$$

The gain, for the loaded system is given by *Equation 6*:

Equation 6

$$GL = \frac{Vo(withload)}{Vi} = \frac{1}{2}\frac{1 + \frac{2R2}{R1} + \frac{R2}{R3}}{1 - \frac{R2}{R3}}$$

The system shown in *Figure 70* is an ideal generator with a synthesized impedance acting as the internal impedance of the system. From this, the output voltage becomes:

Equation 7

$$Vo = (ViG) - (Ro \cdot Iout)$$

where Ro is the synthesized impedance and Iout the output current.

On the other hand Vo can be expressed as:

Equation 8

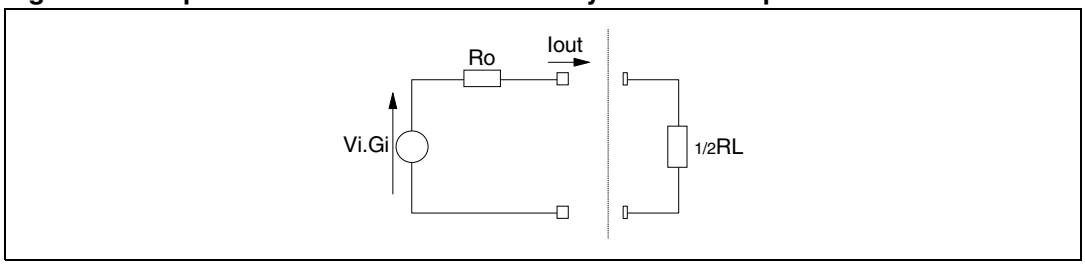
$$Vo = \frac{Vi\left(1 + \frac{2R2}{R1} + \frac{R2}{R3}\right)}{1 - \frac{R2}{R3}} - \frac{Rs1Iout}{1 - \frac{R2}{R3}}$$

By identification of both *Equation 7* and *Equation 8*, the synthesized impedance is, with Rs1 = Rs2 = Rs:

Equation 9

$$Ro = \frac{Rs}{1 - \frac{R2}{R3}}$$

Figure 70. Equivalent schematic - Ro is the synthesized impedance



Let us write Vo◦=kVo, where k is the matching factor varying between 1 and 2. If we assume that the current through R3 is negligible, we can calculate the output resistance, Ro:

$$Ro = \frac{kVoRL}{RL + 2Rs1}$$

After choosing the k factor, Rs will be equal to 1/2RL(k-1).

For a good impedance matching we assume that:

Equation 10

$$Ro = \frac{1}{2}RL$$

From *Equation 9* and *Equation 10*, we derive:

Equation 11

$$\frac{R2}{R3} = 1 - \frac{2Rs}{RL}$$

By fixing an arbitrary value of R2, *Equation 11* becomes:

$$R3 = \frac{R2}{1 - \frac{2Rs}{RL}}$$

Finally, the values of R2 and R3 allow us to extract R1 from *Equation 6*, so that:

Equation 12

$$R1 = \frac{2R2}{2\left(1 - \frac{R2}{R3}\right)GL - 1 - \frac{R2}{R3}}$$

with GL the required gain.

Table 6. Components calculation for impedance matching implementation

GL (gain for the loaded system)	GL is fixed for the application requirements GL= Vo/Vi= 0.5(1+2R2/R1+R2/R3)/(1-R2/R3)
R1	2R2/[2(1-R2/R3)GL-1-R2/R3]
R2 (= R4)	Arbitrarily fixed
R3 (= R5)	R2/(1-Rs/0.5RL)
Rs	0.5RL(k-1)
Load viewed by each driver	kRL/2

11 Package information

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: www.st.com

Figure 71. SO-8 exposed pad package mechanical drawing

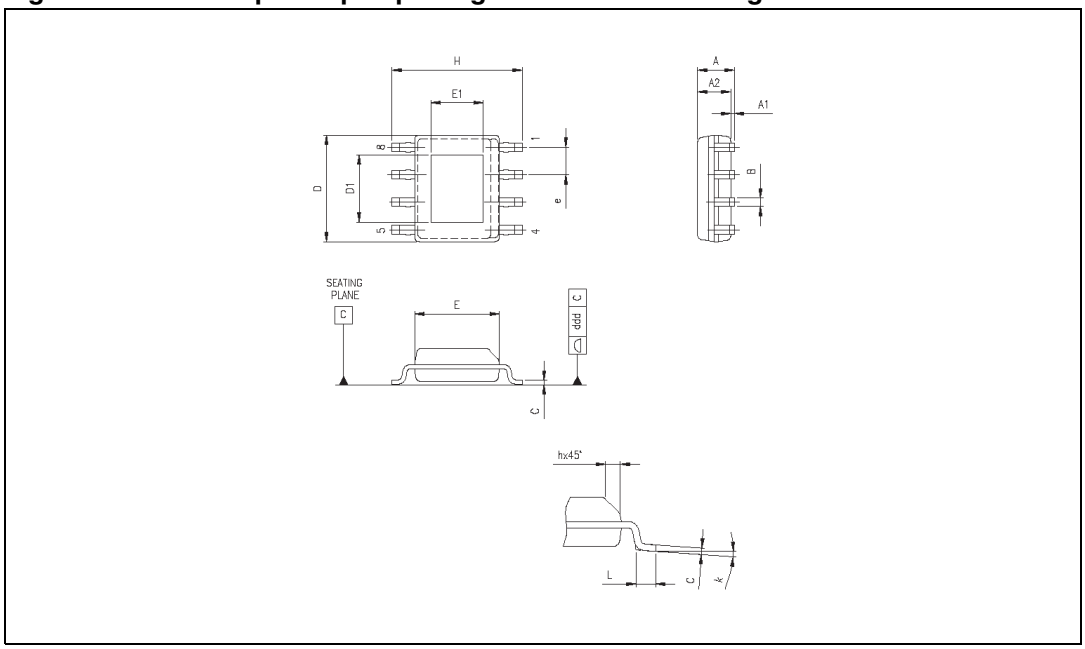


Table 7. SO-8 exposed pad package mechanical data

Dimensions						
Ref.	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.350		1.750	0.053		0.069
A1	0.000		0.150	0.001		0.0059
A2	1.100		1.650	0.043		0.065
B	0.330		0.510	0.013		0.020
C	0.190		0.250	0.007		0.010
D	4.800		5.000	0.189		0.197
D1		3.10			0.122	
E	3.800		4.000	0.150		0.157
E1		2.41			0.095	
e	1.270			0.050		
H	5.800		6.200	0.228		0.244
h	0.250		0.500	0.010		0.020
L	0.400		1.270	0.016		0.050
k	0d		8d	0d		8d
ddd			0.100			0.004

12 Ordering information

Table 8. Order codes

Part number	Temperature range	Package	Packaging	Marking
TS616IDW	-40°C to +85°C	SO-8	Tube	TS616
TS616IDWT			Tape & reel	TS616

13 Revision history

Date	Revision	Changes
1-Nov-2002	1	First release.
03-Dec-2004	2	Moved note in *Table 3* to *Section 9: Choosing the feedback circuit on page 28*. Figure 43 in Revision 1, entitled *Group Delay*, has been removed because the results presented were not technically meaningful. Simplified mathematical representations of the intermodulation product in *Section 5: Intermodulation distortion product on page 17*. In *Section 6: Printed circuit board layout considerations on page 20*, change from “The copper area *can* be connected to (-Vcc) available on pin 4.” to “The copper area **must** be connected to -Vcc available on pin 4.”. In *Section 9.1: The bias of an inverting amplifier on page 29*, change of section title, and correction of referred figure to *Figure 66*.
24-Oct-2006	3	Format update. Corrected package mechanical data for SO-8 exposed pad.
16-Apr-2007	4	Corrected package error in *Table 8: Order codes*.
26-Sep-2008	5	Corrected package error in *Table 8: Order codes*.

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