

# RJK5030DPP-M0

Silicon N Channel MOS FET  
High Speed Power Switching

R07DS0227EJ0100

Rev.1.00

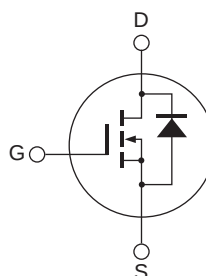
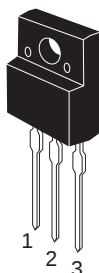
Dec 14, 2010

## Features

- Low on-state resistance  
 $R_{DS(on)} = 1.3 \Omega$  typ. (at  $I_D = 2$  A,  $V_{GS} = 10$  V,  $T_a = 25^\circ\text{C}$ )
- High speed switching

## Outline

RENESAS Package code: PRSS0003AF-A  
(Package name: TO-220FL)



1. Gate
2. Drain
3. Source

## Absolute Maximum Ratings

( $T_a = 25^\circ\text{C}$ )

| Item                              | Symbol                          | Value       | Unit               |
|-----------------------------------|---------------------------------|-------------|--------------------|
| Drain to source voltage           | $V_{DSS}$                       | 500         | V                  |
| Gate to source voltage            | $V_{GSS}$                       | $\pm 30$    | V                  |
| Drain current                     | $I_D$                           | 5           | A                  |
| Drain peak current                | $I_{D(pulse)}$ <sup>Note1</sup> | 20          | A                  |
| Avalanche current                 | $I_{AP}$ <sup>Note3</sup>       | 5           | A                  |
| Channel dissipation               | $P_{ch}$ <sup>Note 2</sup>      | 28.5        | W                  |
| Channel to case thermal Impedance | $\theta_{ch-c}$                 | 4.38        | $^\circ\text{C/W}$ |
| Channel temperature               | $T_{ch}$                        | 150         | $^\circ\text{C}$   |
| Storage temperature               | $T_{stg}$                       | -55 to +150 | $^\circ\text{C}$   |

Notes: 1. Pulse width limited by safe operating area.

2. Value at  $T_c = 25^\circ\text{C}$

3.  $ST_{ch} = 25^\circ\text{C}$ ,  $T_{ch} \leq 150^\circ\text{C}$

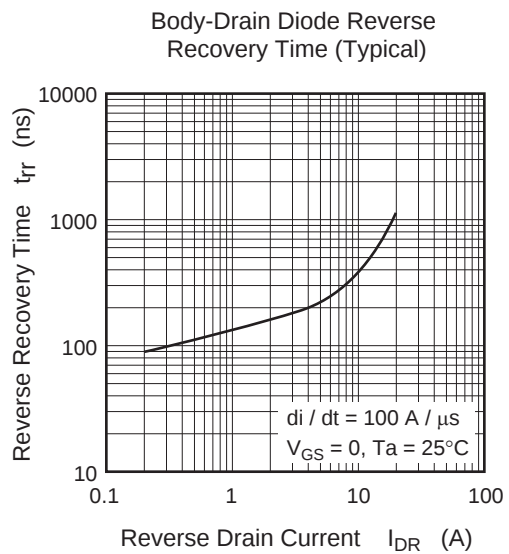
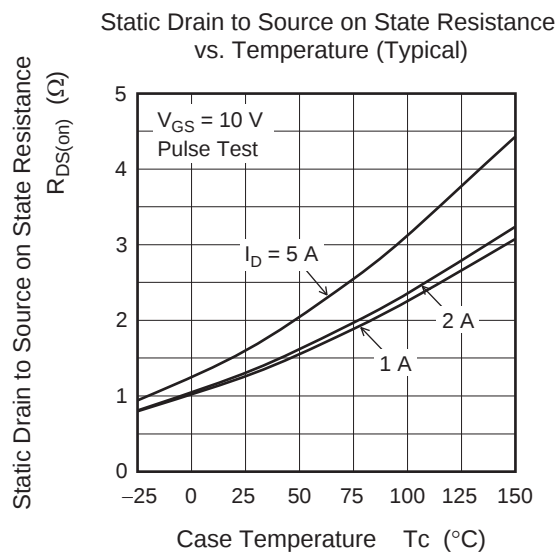
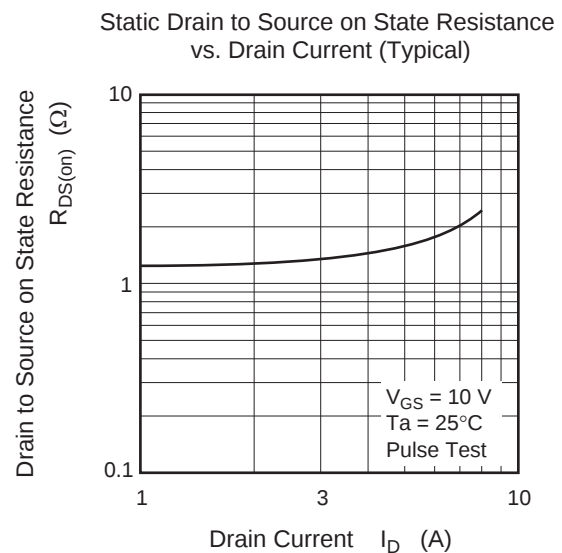
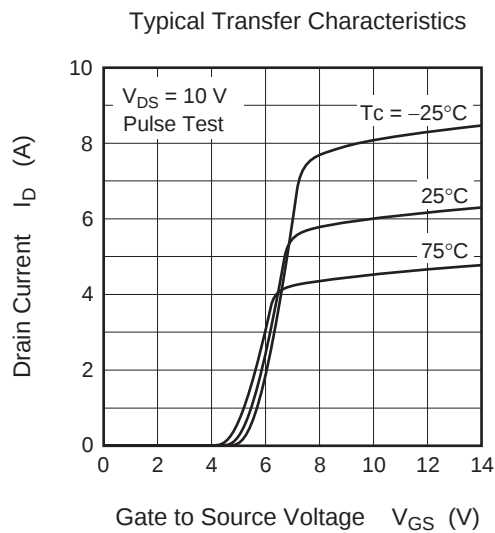
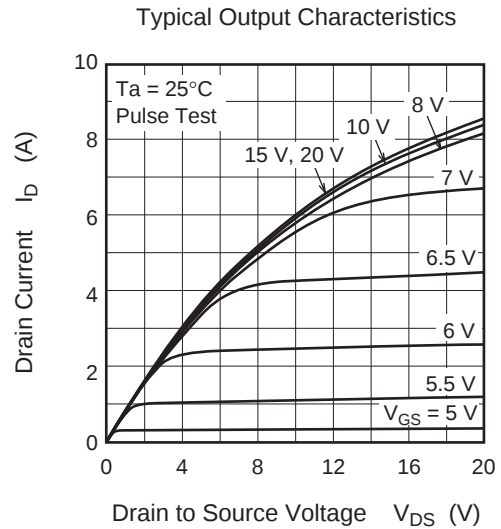
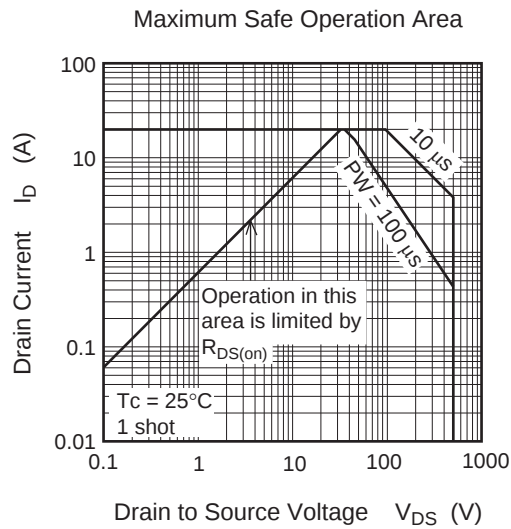
## Electrical Characteristics

(Ta = 25°C)

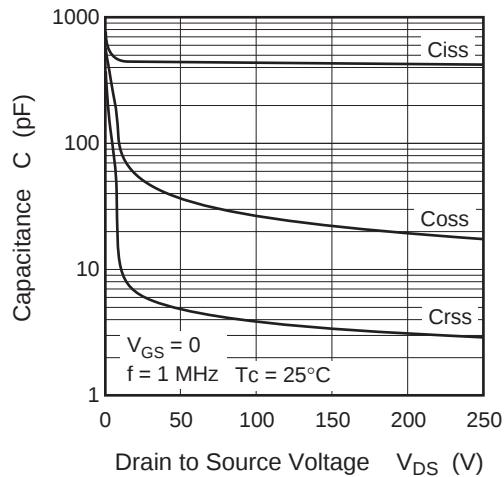
| Item                                       | Symbol        | Min | Typ | Max       | Unit          | Test Conditions                                                                                      |
|--------------------------------------------|---------------|-----|-----|-----------|---------------|------------------------------------------------------------------------------------------------------|
| Drain to source breakdown voltage          | $V_{(BR)DSS}$ | 500 | —   | —         | V             | $I_D = 1\text{ mA}$ , $V_{GS} = 0$                                                                   |
| Zero gate voltage drain current            | $I_{DSS}$     | —   | —   | 10        | $\mu\text{A}$ | $V_{DS} = 500\text{ V}$ , $V_{GS} = 0$                                                               |
| Gate to source leak current                | $I_{GSS}$     | —   | —   | $\pm 0.1$ | $\mu\text{A}$ | $V_{GS} = \pm 30\text{ V}$ , $V_{DS} = 0$                                                            |
| Gate to source cutoff voltage              | $V_{GS(off)}$ | 3.5 | —   | 4.5       | V             | $V_{DS} = 10\text{ V}$ , $I_D = 1\text{ mA}$                                                         |
| Static drain to source on state resistance | $R_{DS(on)}$  | —   | 1.3 | 1.6       | $\Omega$      | $I_D = 2\text{ A}$ , $V_{GS} = 10\text{ V}$ <sup>Note 4</sup>                                        |
| Input capacitance                          | $C_{iss}$     | —   | 550 | —         | pF            | $V_{DS} = 25\text{ V}$<br>$V_{GS} = 0$<br>$f = 1\text{ MHz}$                                         |
| Output capacitance                         | $C_{oss}$     | —   | 60  | —         | pF            |                                                                                                      |
| Reverse transfer capacitance               | $C_{rss}$     | —   | 10  | —         | pF            |                                                                                                      |
| Turn-on delay time                         | $t_{d(on)}$   | —   | 15  | —         | ns            | $V_{DD} = 200\text{ V}$<br>$I_D = 2\text{ A}$<br>$V_{GS} = 10\text{ V}$<br>$R_g = 25\text{ }\Omega$  |
| Rise time                                  | $t_r$         | —   | 20  | —         | ns            |                                                                                                      |
| Turn-off delay time                        | $t_{d(off)}$  | —   | 90  | —         | ns            |                                                                                                      |
| Fall time                                  | $t_f$         | —   | 30  | —         | ns            |                                                                                                      |
| Total gate charge                          | $Q_g$         | —   | 13  | —         | nC            | $V_{DD} = 400\text{ V}$<br>$V_{GS} = 10\text{ V}$<br>$I_D = 5\text{ A}$                              |
| Gate to source charge                      | $Q_{gs}$      | —   | 3.3 | —         | nC            |                                                                                                      |
| Gate to drain charge                       | $Q_{gd}$      | —   | 6.6 | —         | nC            |                                                                                                      |
| Body-drain diode forward voltage           | $V_{DF}$      | —   | 0.9 | 1.5       | V             | $I_F = 5\text{ A}$ , $V_{GS} = 0$ <sup>Note 4</sup>                                                  |
| Body-drain diode reverse recovery time     | $t_{rr}$      | —   | 250 | —         | ns            | $I_F = 5\text{ A}$ , $V_{GS} = 0$<br>$V_{DD} = 250\text{ V}$<br>$di_F/dt = 100\text{ A}/\mu\text{s}$ |

Note: 4. Pulse test

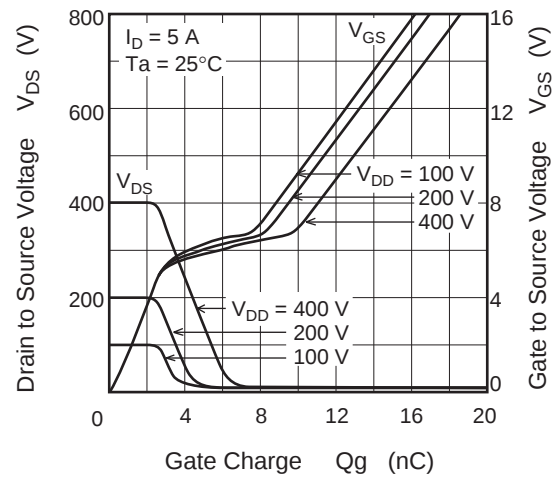
## Main Characteristics



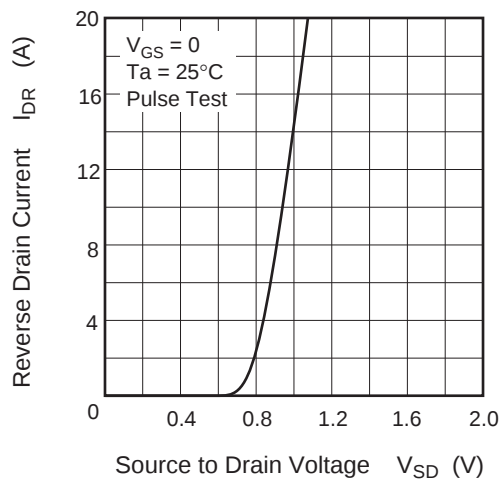
Typical Capacitance vs.  
Drain to Source Voltage



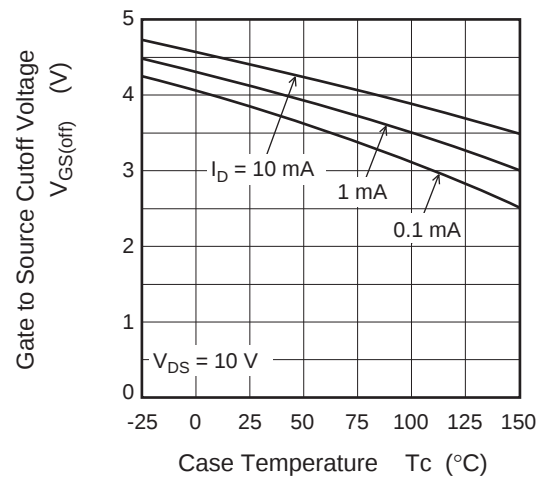
Dynamic Input Characteristics (Typical)

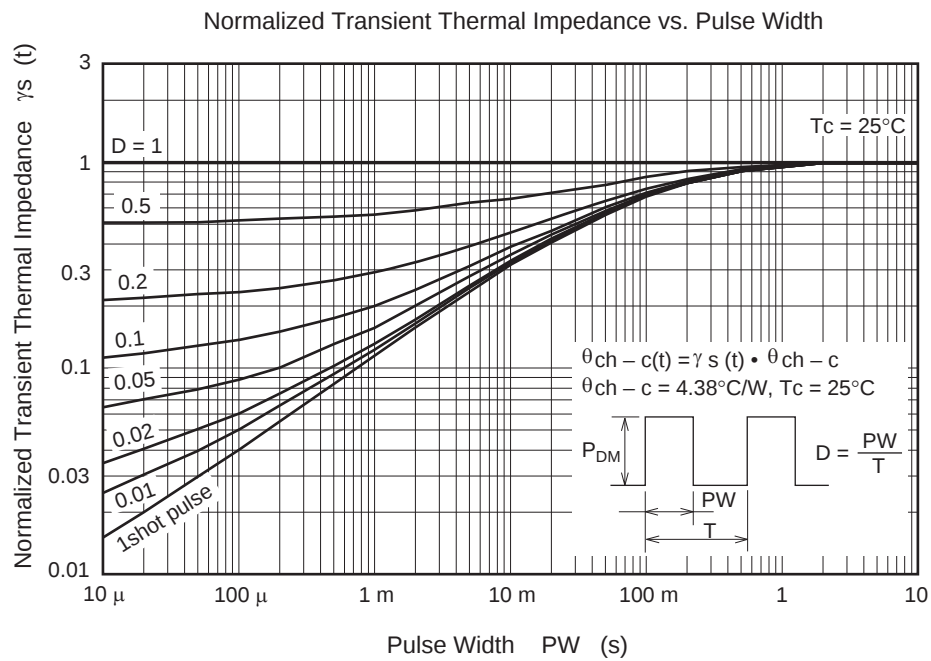


Reverse Drain Current vs.  
Source to Drain Voltage (Typical)

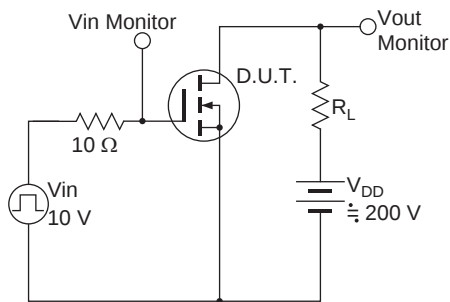


Gate to Source Cutoff Voltage  
vs. Case Temperature (Typical)

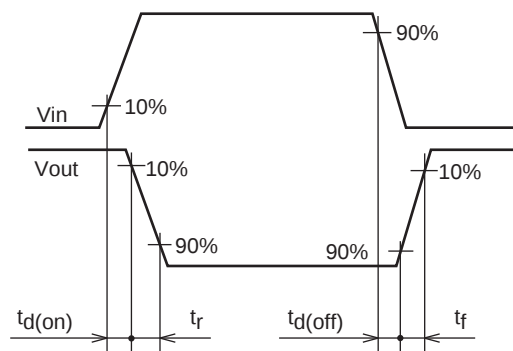




Switching Time Test Circuit



Waveform





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