Data Book

AU9254

USB Hub Controller

Technical Reference Manual

Product Specification

Official Release

Revision 1.02W

Public **Nov 2005**

Data sheet status

Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.

Revision History

Date	Revision / Model	Description
Feb 2005	1.01W	Removed the schematics. Please contact our sales if you need it.
Nov 2005	1.02W	To modified “6.0 Mechanical Information”

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1.0 Introduction

1.1 Description

The AU9254 is an integrated single chip USB hub controller designed for the emerging industry-standard Universal Serial Bus (USB). The AU9254 supports four USB downstream ports. Each downstream port has power switch control, and over-current sensing.
Single chip integration makes the AU9254 the most cost effective stand-alone USB hub solution available in the market. Downstream ports can be used to connect various USB peripheral devices, such as USB printers, modems, scanners, cameras, mice, or joysticks to the system without adding external glue logic.

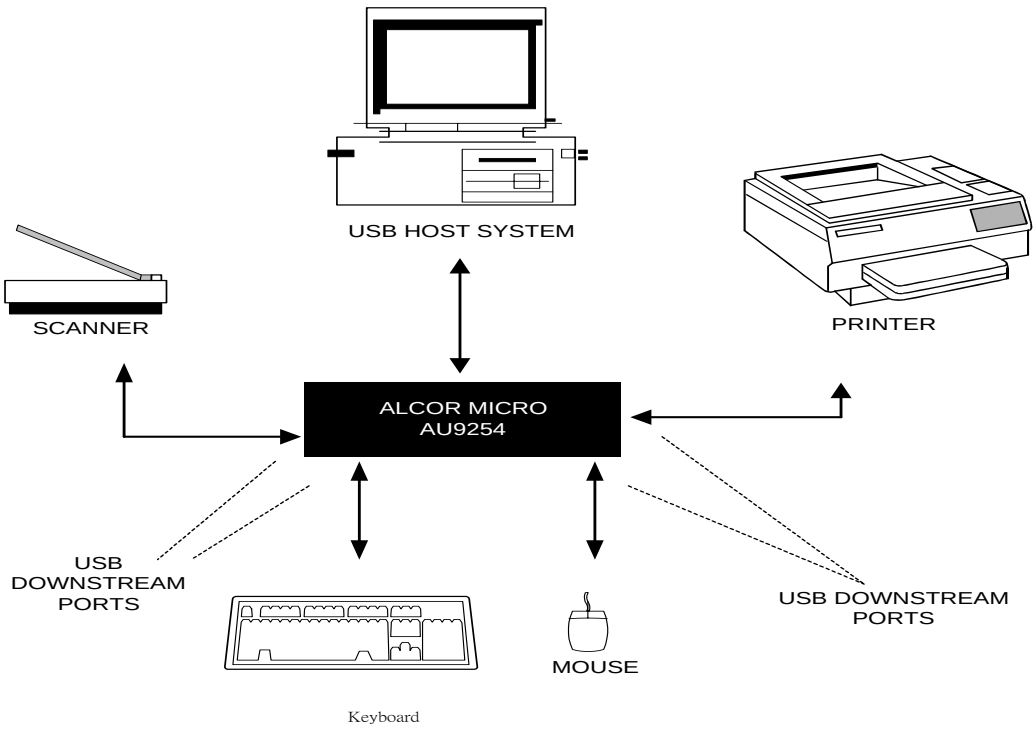
1.2 Features

- Fully compliant with the Universal Serial Bus Specification, version 1.1.
- USB hub design is compliant with Universal Serial Bus Hub Specification, revision 1.1.
- Single chip integrated USB hub controller with embedded proprietary processor.
- Supports four bus-powered/self-powered downstream ports.
- Built-in 3.3v voltage regulator allows single +5V operating voltage, resulting in reduced overall system cost.
- Runs at 12Mhz frequency.
- 28-pin SSOP package, both normal size (body size 209 mil) and smaller size (body size 150 mil) are available.

2.0 Application Block Diagram

The AU9254 is a single chip 4-port USB hub controller. The upstream port is connected to the USB system. The downstream ports can be used for a mouse, joystick, scanner, printer or other device.

Figure 2.1 Block Diagram



3.0 Pin Assignment

The AU9254 is packaged as a 28-pin shrink small outline plastic package (SSOP). The figure on the following page shows the signal names for each of the pins on the chip. Accompanying the figure is the table that describes each of the pin signals.

Figure 3.1 Pin Assignment Diagram

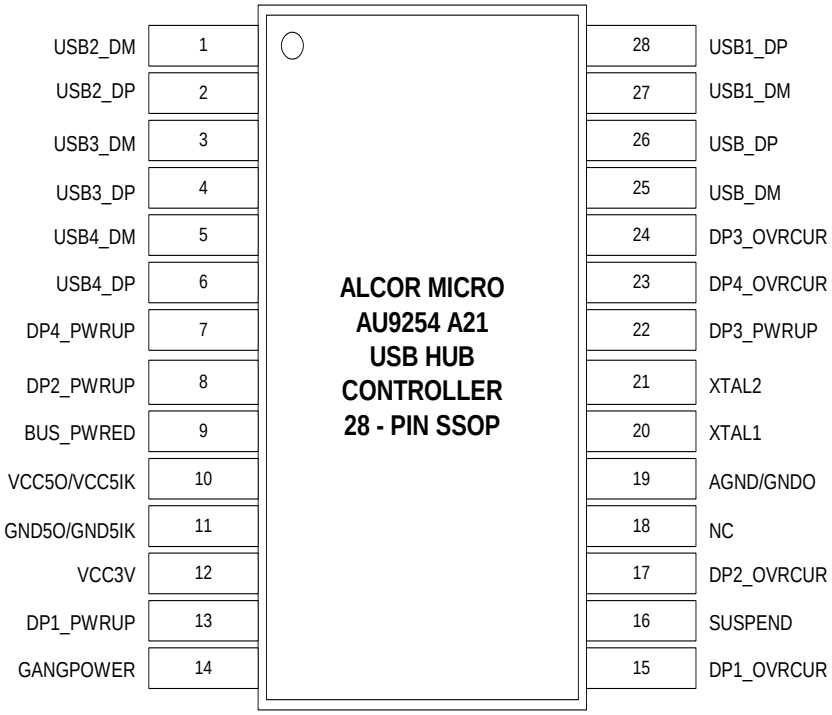


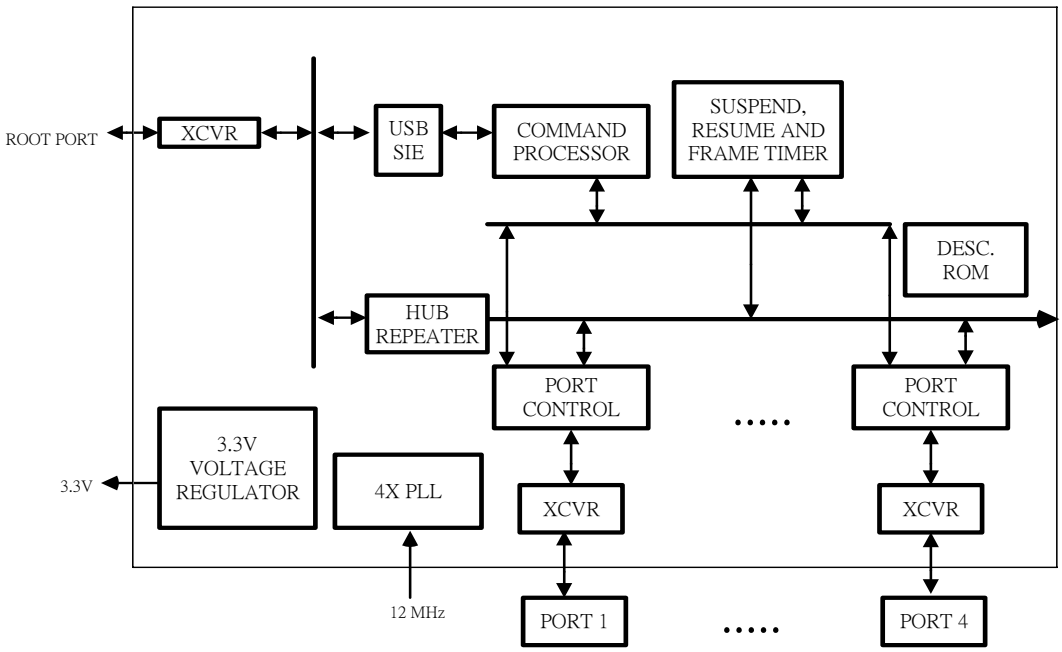
Table 3.1 Pin Descriptions of Au9254, 28-pin SSOP

Pin #	Pin Name	Input/Output	Description
1	USB_DM	Input/Output	USB D- for downstream port 2; add 15KΩ pull-down to ground.
2	USB2_DP	Input/Output	USB D+ for downstream port 2; add 15KΩ pull-down to ground.
3	USB3_DM	Input/Output	USB D- for downstream port 3; add 15KΩ pull-down to ground.
4	USB3_DP	Input/Output	USB D+ for downstream port 3; add 15KΩ pull-down to ground.
5	USB4_DM	Input/Output	USB D- for downstream port 4; add 15KΩ pull-down to ground.
6	USB4_DP	Input/Output	USB D+ for downstream port 4; add 15KΩ pull-down to ground
7	DP4_PWRUP	Output	Downstream port 4 power switch control. Active low.
8	DP2_PWRUP	Output	Downstream port 2 power switch control. Active low.
9	BUS_PWRED	Input	Bus power. Low indicates bus-powered.
10	VCC5O/VCC5IK	Power	+5 V power supply.
11	GND5O/GND5IK	Power	Ground.
12	VCC3V	Power	3.3V output for upstream D+ pull-up.
13	DP1_PWRUP	Output	Downstream port 1 power switch control. Active low.
14	GANGPOWER	Input	Ganged or individual port power selection. Add a 10k pull down for ganged power. 10k pull up for individual power.
15	DP1_OVRCUR	Input	Downstream port 1 over-current indicator. Active low.
16	SUSPEND	Output	Device is in suspended state: Active high.
17	DP2_OVRCUR	Input	Downstream port 2 over-current indicator. Active low.
18	NC		
19	AGND/GNDO	Power	Ground.
20	XTAL_1	Input	Crystal in.
21	XTAL_2	Output	Crystal out.
22	DP3_PWRUP	Output	Downstream port 3 power switch control. Active low.
23	DP4_OVRCUR	Input	Downstream port 4 over-current indicator. Active low.
24	DP3_OVRCUR	Input	Downstream port 3 over-current indicator. Active low.
25	USB_DM	Input/Output	USB D- for upstream.
26	USB_DP	Input/Output	USB D+ for upstream port. Need external 1.5KΩ pull-up to 3.3V.
27	USB1_DM	Input/Output	USB D- for downstream port 1; add 15KΩ pull-down to ground.
28	USB1_DP	Input/Output	USB D+ for downstream port 1; add 15KΩ pull-down to ground.

4.0 System Architecture and Reference Design

4.1 AU9254 Block Diagram

Figure4.1 AU9254 Block Diagram



5.0 Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1 Absolute Maximum Ratings

SYMBOL	PARAMETER	RATING	UNITS
V_{CC}	Power Supply	-0.3 to 6.0	V
V_{IN}	Input Voltage	-0.3 to VCC+0.3	V
V_{OUT}	Output Voltage	-0.3 to VCC+0.3	V
T_{STG}	Storage Temperature	-40 to 125	°C

5.2 Recommended Operating Conditions

Table 5.2 Recommended Operating Conditions

SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
V_{CC}	Power Supply	4.5	5.0	5.5	V
V_{IN}	Input Voltage	0		V_{CC}	V
T_{OPR}	Operating Temperature	-5		85	^{O}C

5.3 General DC Characteristics

Table 5.3 General DC Characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{IL}	Input low current	no pull-up or pull-down	-1		1	µA
I_{IH}	Input high current	no pull-up or pull-down	-1		1	µA
I_{OZ}	Tri-state leakage current		-10		10	µA
C_{IN}	Input capacitance			4		ρF
C_{OUT}	Output capacitance			4		ρF
C_{BID}	Bi-directional buffer capacitance			4		ρF

5.4 DC Electrical Characteristics for 5 volts operation

(Under Recommended Operating Conditions and V_{CC}=4.5v ~ 5.5v , Tj= -40°C to + 85°C)

Table 5.4 Electrical Characteristics for 5 volts operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage	TTL			0.8	V
V_{IL}	Input Low Voltage	CMOS			0.3*V_{CC}	V
V_{IL}	Schmitt input Low Voltage	TTL		1.10		V
V_{IL}	Schmitt input Low V oltage	CMOS		1.84		V
V_{IH}	Input High Voltage	TTL	2.2			V
V_{IH}	Input Hight Voltage	CMOS	0.7*V_{CC}			V
V_{IH}	Schmitt input High Voltage	TTL		1.87		V
V_{IH}	Schmitt input High Voltage	CMOS		3.22		V
V_{OL}	Output low voltage	I_{OL}=2, 4, 8, 12, 16, 24 mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=2, 4, 8, 12, 16, 24 mA	3.5			V
R_I	Input Pull-up/down resistance	Vil=0_V or Vih=V_{CC}		50		KΩ

5.5 DC Electrical Characteristics for 3.3 volts operation

(Under Recommended Operating Conditions and V_{CC}=3.0v ~ 3.6v , Tj = -40°C to +85°C)

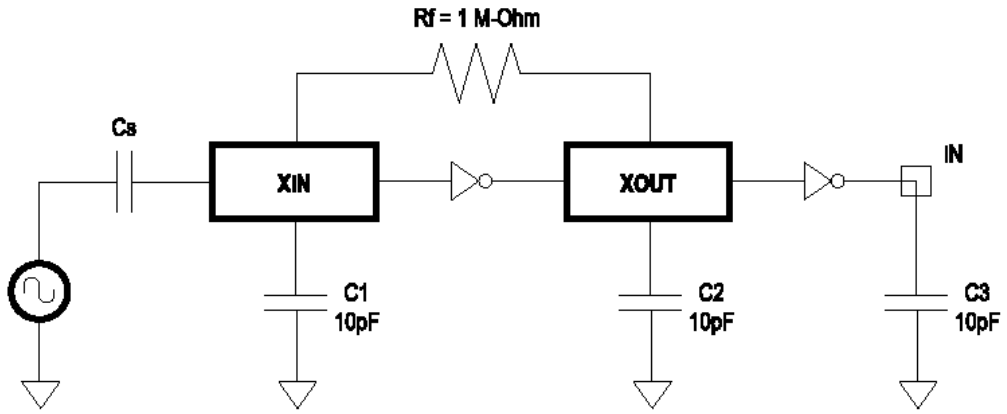
Table 5.5 DC Electrical Characteristics for 3.3 volts operation

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_{IL}	Input Low Voltage	CMOS			0.3*VCC	V
V_{IL}	Schmitt input Low Voltage	CMOS		1.22		V
V_{IH}	Input Hight Voltage	CMOS	0.7*Vcc			V
V_{IH}	Schmitt input High Voltage	CMOS		2.08		V
V_{OL}	Output low voltage	I_{OL}=2, 4, 8, 12, 16, 24 mA			0.4	V
V_{OH}	Output high voltage	I_{OH}=2, 4, 8, 12, 16, 24 mA	2.3			V
R_I	Input Pull-up/down resistance	Vil=0_V or Vih=V_{CC}		75		KΩ

5.6 Crystal Oscillator Circuit Setup for Characterization

The following setup was used to measure the open loop voltage gain for crystal oscillator circuits. The feedback resistor serves to bias the circuit at its quiescent operating point and the AC coupling capacitor, Cs, is much larger than C1 and C2.

Figure 5.1 Crystal Oscillator Circuit Setup for Characterization



5.7 USB Transceiver Characteristics

RECOMMENDED OPERATING CONDITIONS

Table 5.6 USB Transceiver Characteristics

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		3.0	3.6	V
V_I	DC input voltage range		0	5.5	V
$V_{I/O}$	DC input range for I/Os		0	V_{CC}	V
V_O	DC output voltage range		0	V_{CC}	V
T_{AMB}	Operating ambient temperature range in free air	See DC and AC characteristics for individual device	0	70	°C

ABSOLUTE MAXIMUM RATINGS (Notes 1 and 2)

In accordance with the Absolute Maximum Rating System, Voltages are referenced to GND (Ground=0v)

Table 5.7 Absolute Maximum Ratings

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
V_{CC}	DC supply voltage		-0.5	+6.5	V
I_{IK}	DC input diode current	Vi<0		-50	mA
V_I	DC input voltage	Note 3	-0.5	+5.5	V
$V_{I/O}$	DC input voltage range for I/Os		-0.5	Vcc +0.5	V
I_{OK}	DC output diode current	Vo> Vcc or Vo<0		+/-50	mA
V_O	DC output voltage	Note 3	-0.5	Vcc +0.5	V
I_O	DC output source sink current for VP/VM and RCV pins	Vo=0 to Vcc		+/-15	mA
I_O	DC output source or sink current for D+/D- pins	Vo= 0 to Vcc		+/-50	mA
I_{CC}, I_{GND}	DC Vcc or GND current			+/-100	mA
T_{STO}	Storage temperature range		-60	+150	°C
P_{TOT}	Power dissipation per package				mW

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "Recommended Operating Conditions" is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.
2. The performance capability of a high performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output voltage ratings may be exceeded if the input and output clamp current ratings are observed.

DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions. Voltages are referenced to GND (Ground=0V).

Table 5.8 DC Electrical Characteristics

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS -40°C to +85°C			UNIT
			MIN	TYP	MAX	
VHYS	Hysteresis on inputs	Vcc=3.0V to 3.6V (Note 3)	0.3	0.4	0.5	V
VIH	HIGH level input	Vcc=3.0V to 3.6V (Note 3)		1.5	2.0	V
VIL	LOW level input	Vcc=3.0V to 3.6V (Note 3)	0.8	1.1		V
RoH	Output impedance (HIGH state)	Note 2	28	34	43	ohm
RoL	Output impedance (LOW state)	Note 2	28	35	43	ohm
VOH	HIGH level output (Note 3)	Vcc=3.0V Io=6mA Vcc=3.0V Io=4mA Vcc=3.0V Io=100µA	2.2 2.4 2.8	2.7		V
VOL	LOW level output (Note 3)	Vcc=3.0V Io=6mA Vcc=3.0V Io=4mA Vcc=3.0V Io=100µA		0.3	0.7 0.4 0.2	V
IQ	Quiescent supply current	Vcc=3.6V VI=Vcc or GND Io=0		330	600	µA
Isup	Supply current in suspend	Vcc=3.6V VI=Vcc or GND Io=0			70	µA
IFS	Active supply current (Full Speed)	Vcc=3.3V		9	14	mA
ILS	Active supply current (Low Speed)	Vcc=3.3V		2		mA
ILeak	Imput leakage current	Vcc=3.6V VI=5.5V or GND, not for I/O Pins		+/-0.1	+/-0.5	µA
IOFF	3-state output OFF-state current	Vi=Vih or ViL; Vo=Vcc or GND			+/-10	µA

NOTES:

1. All typical values are at Vcc=3.3V and Tamb=25°C.
2. This value includes an external resistor of 24 ohm +/-1%. See "Load D+ and D-" diagram for testing details.
3. All signals except D+ and D-.

AC ELECTRICAL CHARACTERISTICS

GND=0V, t_R = t_F =3.0 ns; C_L =50 pF; RL=500 Ohms

Table 5.9 AC Electrical Characteristics

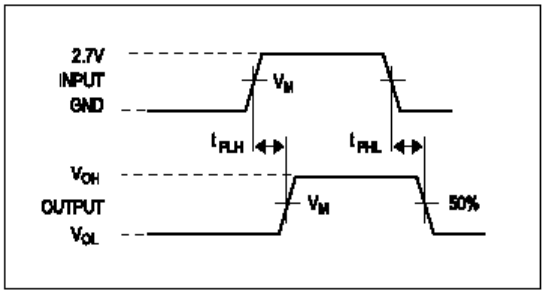
SYMBOL	PARAMETER	WAVEFORM	LIMITS (T_{AMB})					UNIT
			0°C to +25°C			0°C to +70°C		
			MIN	TYP	MAX	MIN	MAX	
tpLH tpHL	VMO/VPO to D+/D- Full Speed	1	0 0		12 12	0 0	14 14	ns
trise tfall	Rise and Fall Times Full Speed	2	4 4	9 9	20 20	4 4	20 20	ns
tRFM	Rise and Fall Time Matching Full Speed		90		110	90	110	%
tpLH tpHL	VMO/VPO to D+/D- Low Speed	1		120 120	300 300		300 300	ns
trise tfall	Rise and Fall Times Low Speed	2	75 75		300 200	75 75	300 200	ns
tRFM	Rise and Fall Time Matching Low Speed		70		130	70	130	%
tpLH tpHL	D+/D- to RCV	3		9 9	16 16		16 16	ns
tpLH tpHL	D+/D- to VP/VM	1		4 4	8 8		8 8	ns
tpHZ tpZH tpLZ tpZL	OE# to D+/D- RL = 500ohm	4			12 12 10 10		12 12 10 10	ns
tsu	Setup for SPEED	5	0					ns
Vcr	Crossover point[1]	3	1.3		2.0	1.3	2.0	V

NOTES:

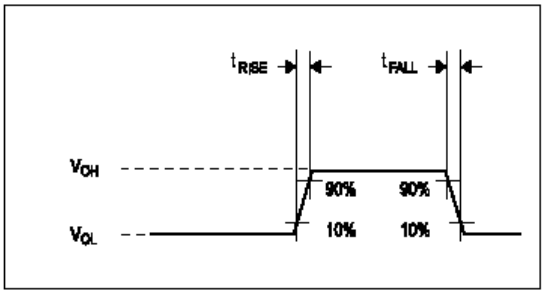
1. The crossover point is in the range of 1.3V to 2.5V for the low speed mode with a 50 pF capacitance.

Figure 5.2 Electrical Characteristics Diagram

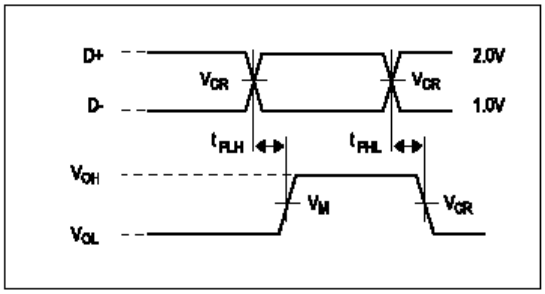
AC WAVEFORM 1.
D+/D- TO VP/VM OR VPO/VMO TO D+/D-



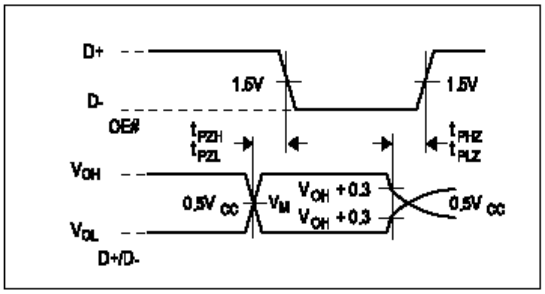
AC WAVEFORM 2.
RISE AND FALL TIMES



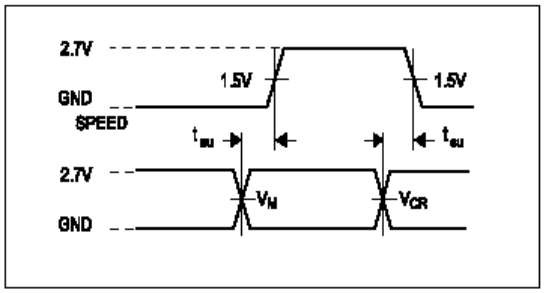
AC WAVEFORM 3.
D+/D- TO RCV



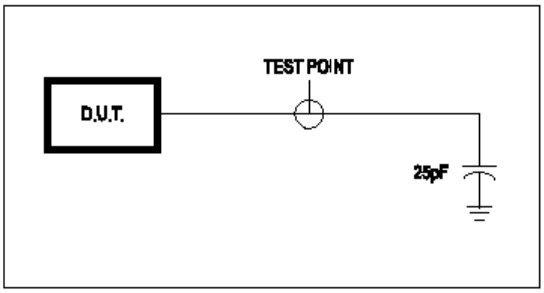
AC WAVEFORM 4.
OE# TO D/+/D-



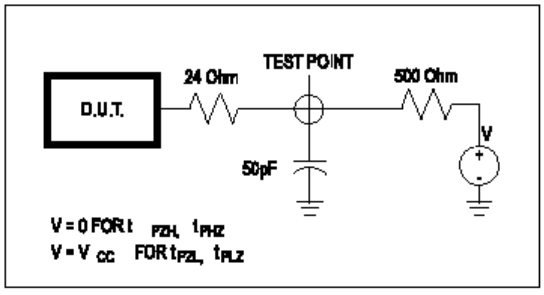
AC WAVEFORM 5.
SETUP FOR SPEED



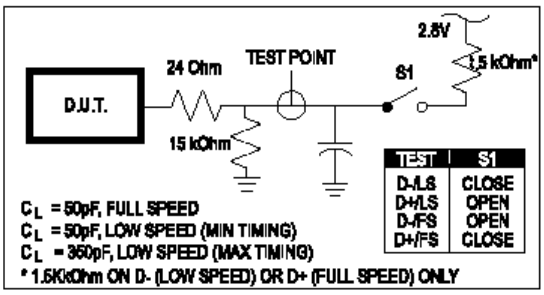
TEST CIRCUIT 1.
LOAD FOR VM/VP AND RCV



TEST CIRCUIT 2.
LOAD FOR ENABLE AND DISABLE TIMES



TEST CIRCUIT 3.
LOAD FOR D+/D-



5.8 ESD Test Results

Test Description: ESD Testing was performed on a Zapmaster system using the Human-Body-Model (HBM) and Machine-Model (MM), according to MIL-STD 883 and EIAJ IC-121 respectively.

- Human-Body-Model stresses devices by sudden application of a high voltage supplied by a 100pF capacitor through 1.5k-ohm resistance.
- Machine-Model stresses devices by sudden application of a high voltage supplied by a 200pF capacitor through very low (0 ohm) resistance.

Test Circuit & Condition

- Zap Interval: 1 second
- Number of Zaps: 3 positive and 3 negative at room temperature
- Criteria: I-V Curve Tracing

Table 5.10 ESD Data

Model	Mode	S/S	Target	Results
HBM	Vdd, Vss, I/C	15	6000V	PASS
MM	Vdd, Vss, I/C	15	200V	PASS

5.9 Latch-Up Test Results

Test Description: Latch-Up testing was performed at room ambient using an IMCS-4600 system which applies a stepped voltage to one pin per device with all other pins open except Vdd and Vss which were biased to 5Volts and ground respectively.

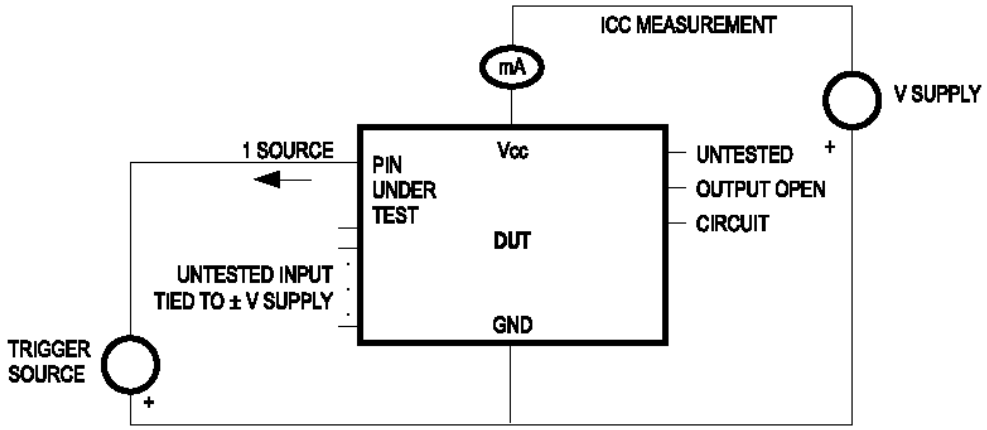
Testing was started at 5.0V (Positive) or 0V (Negative), and the DUT was biased for 0.5 seconds.

If neither the PUT current supply nor the device current supply reached the predefined limit (DUT=00mA, Icc=100mA), then the voltage was increased by 0.1Volts and the pin was tested again.

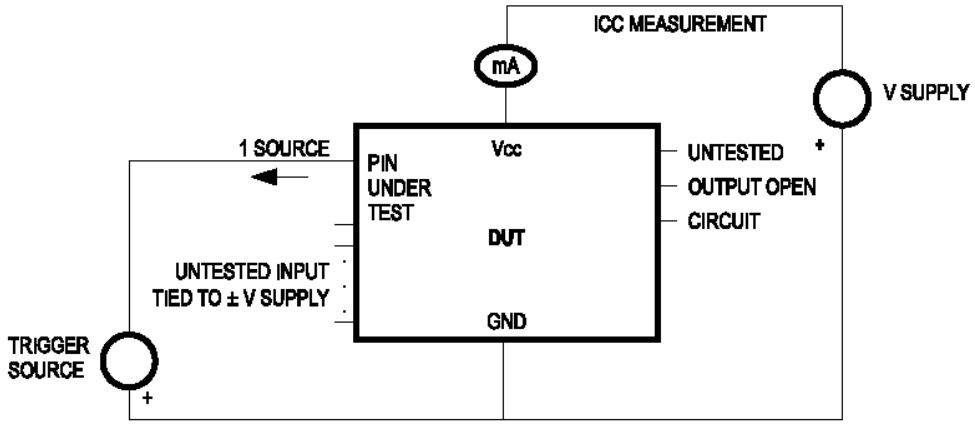
This procedure was recommended by the JEDEC JC-40.2 CMOS Logic standardization committee.

Notes:
1. DUT: The device under test.
2. PUT: The pin under test.

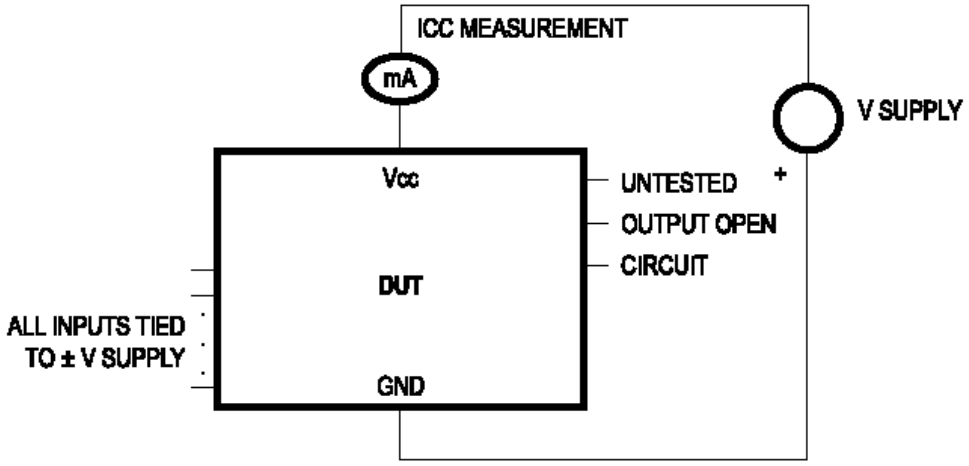
Figure 5.3 Latch-Up Test Results Diagram



Test Circuit: Positive Input/Output Overvoltage/Overcurrent



Test Circuit: Negative Input/Output Overvoltage/Overcurrent



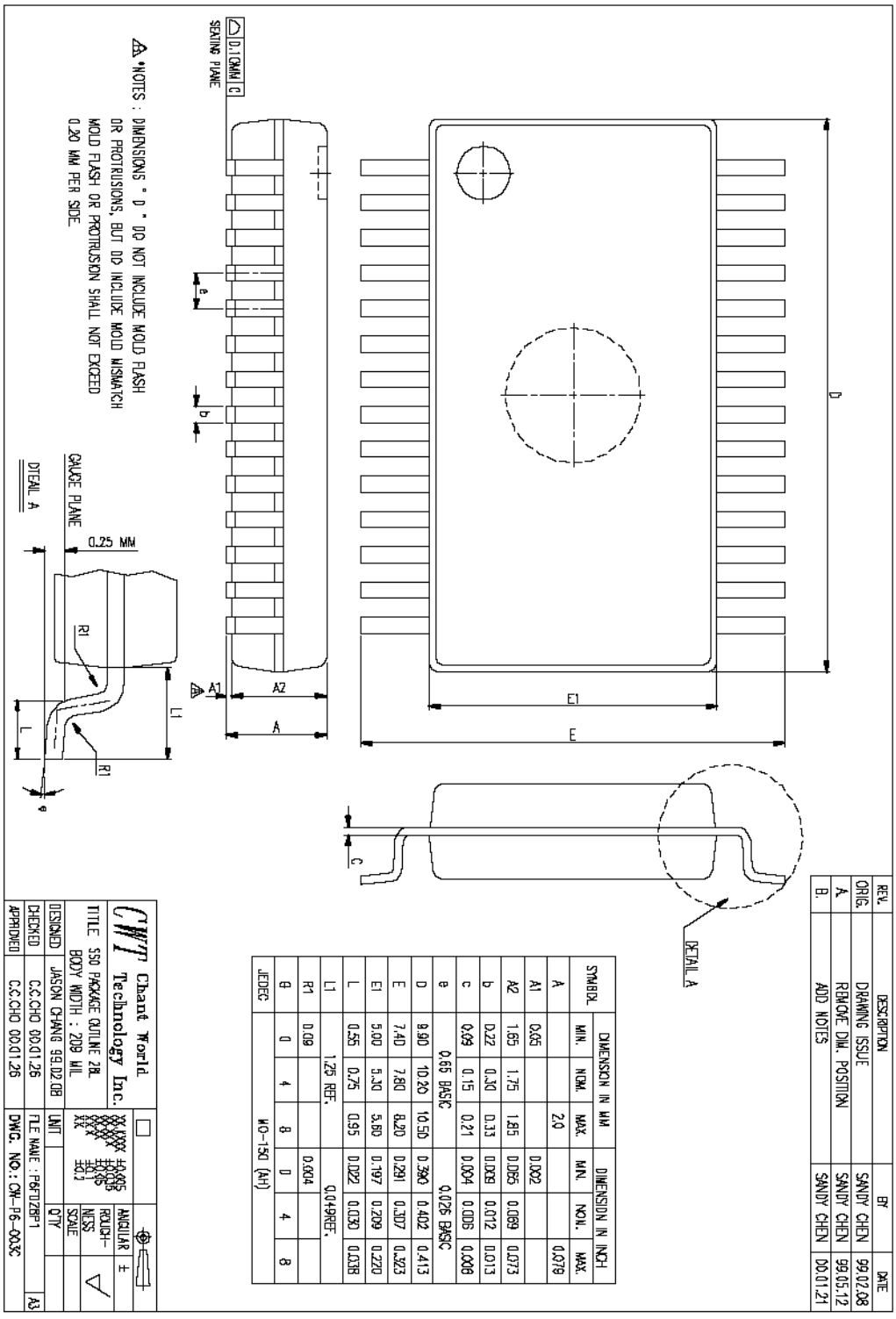
Supply Overvoltage Test

Table 5.11 Latch-Up Data

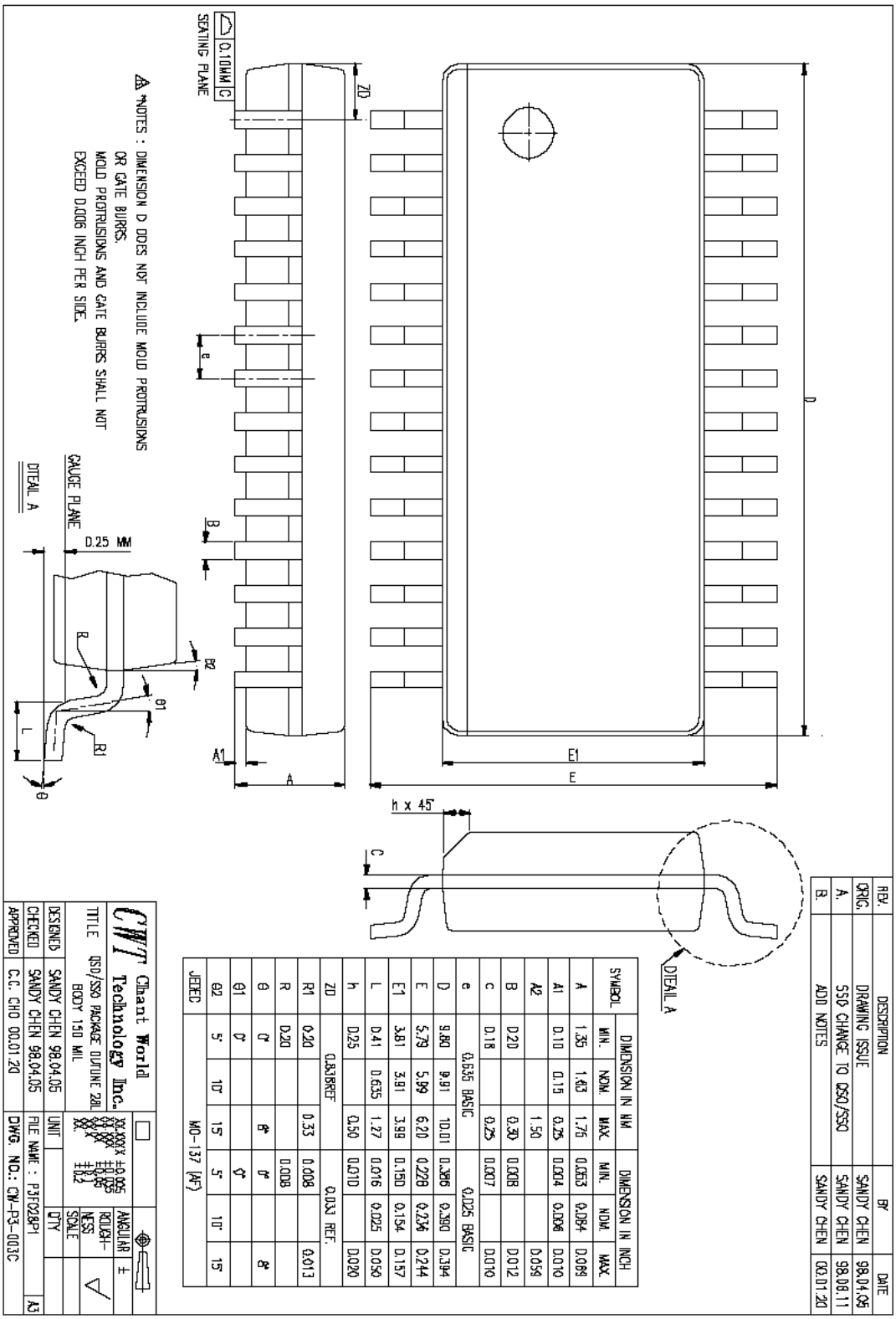
Mode		Voltage (V)/CUITENT(ma)	S/S	Results
Voltage	+	11.0	5	Pass
	-	11.0	5	Pass
Current	+	200	5	Pass
	-	200	5	Pass
Vdd - Vxx		9.0	5	Pass

6.0 Mechanical Information

6.1 Normal Size Package (Body Size 209 mil)



6.2 Small Size Package (Body Size 150 mil)



REV.	DESCRIPTION	BY	DATE
ORIG.	DRAWING ISSUE	SANDY CHEN	98.04.06
A.	SSD CHANGE TO QSO/SSO	SANDY CHEN	98.08.11
B.	ADD NOTES	SANDY CHEN	00.01.20

SYMBOL	DIMENSION IN MM			DIMENSION IN INCH		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	1.35	1.43	1.75	0.053	0.054	0.069
A1	0.10	0.15	0.25	0.004	0.006	0.010
A2			1.50			0.059
B	0.20		0.30	0.008		0.012
c	0.18		0.25	0.007		0.010
e	0.635 BASIC			0.025 BASIC		
D	9.80	9.91	10.01	0.386	0.390	0.394
E	5.79	5.99	6.20	0.228	0.236	0.244
E1	3.81	3.91	3.99	0.150	0.154	0.157
L	0.41	0.635	1.27	0.016	0.025	0.050
h	0.25		0.50	0.010		0.020
ZD	CLASSREF			0.033 REF.		
R1	0.20		0.33	0.008		0.013
R	0.20			0.008		
θ	0°		8°	0°		8°
θ1	0°			0°		
θ2	5°	10°	15°	5°	10°	15°
JEDEC	MO-137 (AF)					

Chant World Technology Inc.			ANGULAR ±
TITLE QSO/SSO PACKAGE OUTLINE 28L BODY 150 MIL	X.XXX ±0.005 X.XX ±0.05 XX. ±0.2		ROUGH-NESS
DESIGNED SANDY CHEN 98.04.05	UNIT		QTY
CHECKED SANDY CHEN 98.04.05	FILE NAME : P3F028P1		A3
APPROVED C.C. CHO 00.01.20	DWG. NO.: CW-P3-003C		

【MEMO】

About Alcor Micro, Corp

Alcor Micro, Corp. designs, develops and markets highly integrated and advanced peripheral semiconductor, and software driver solutions for the personal computer and consumer electronics markets worldwide. We specialize in USB solutions and focus on emerging technology such as USB and IEEE 1394. The company offers a range of semiconductors including controllers for USB hub, integrated keyboard/USB hub and USB Flash memory card reader…etc. Alcor Micro, Corp. is based in Taipei, Taiwan, with sales offices in Taipei, Japan, Korea and California.

Alcor Micro is distinguished by its ability to provide innovative solutions for spec-driven products. Innovations like single chip solutions for traditional multiple chip products and on-board voltage regulators enable the company to provide cost-efficiency solutions for the computer peripheral device OEM customers worldwide.