

# TLE7184F

System IC for B6 motor drives

Automotive Power



Never stop thinking

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## 1 Overview

### Features

- Drives 6 N-Channel Power MOSFETs
- Integrated 5V Vreg-Controller to power  $\mu\text{C}$
- Integrated switch for VDH voltage
- Separate control input for each MOSFET
- Adjustable dead time
- Shoot through protection
- Analog adjustable Short Circuit Protection levels
- Low quiescent current mode
- 1 bit diagnosis  $\overline{\text{ERR}}$
- Over Temperature shut down and analog temperature output
- Over Temperature pre-warning
- Under Voltage shut down
- Adjustable Over Voltage shut down
- Current sense OpAmp
- Over current shut down based on Current sense OpAmp, fixed shut down level
- 0 ...94% at 25 kHz Duty cycle of phase voltage
- Green Product (RoHS compliant)
- AEC Qualified



PG-VQFN-48

### Description

The TLE7184F is a system IC for Brushless Motor Control. It incorporates a voltage supply for a  $\mu\text{C}$ , a bridge driver for a B6 configuration, an application typical PWM interface and some other smaller features. Target is to reduce the number of discrete components in typical BLDC automotive applications and give enough flexibility for custom specific adaptations.

It works with 3-phase motors and brush DC motors. Its exposed pad package allows the usage even at high ambient temperatures.

Type	Package	Marking
TLE7184F	PG-VQFN-48	TLE7184F

## 2 Block Diagram

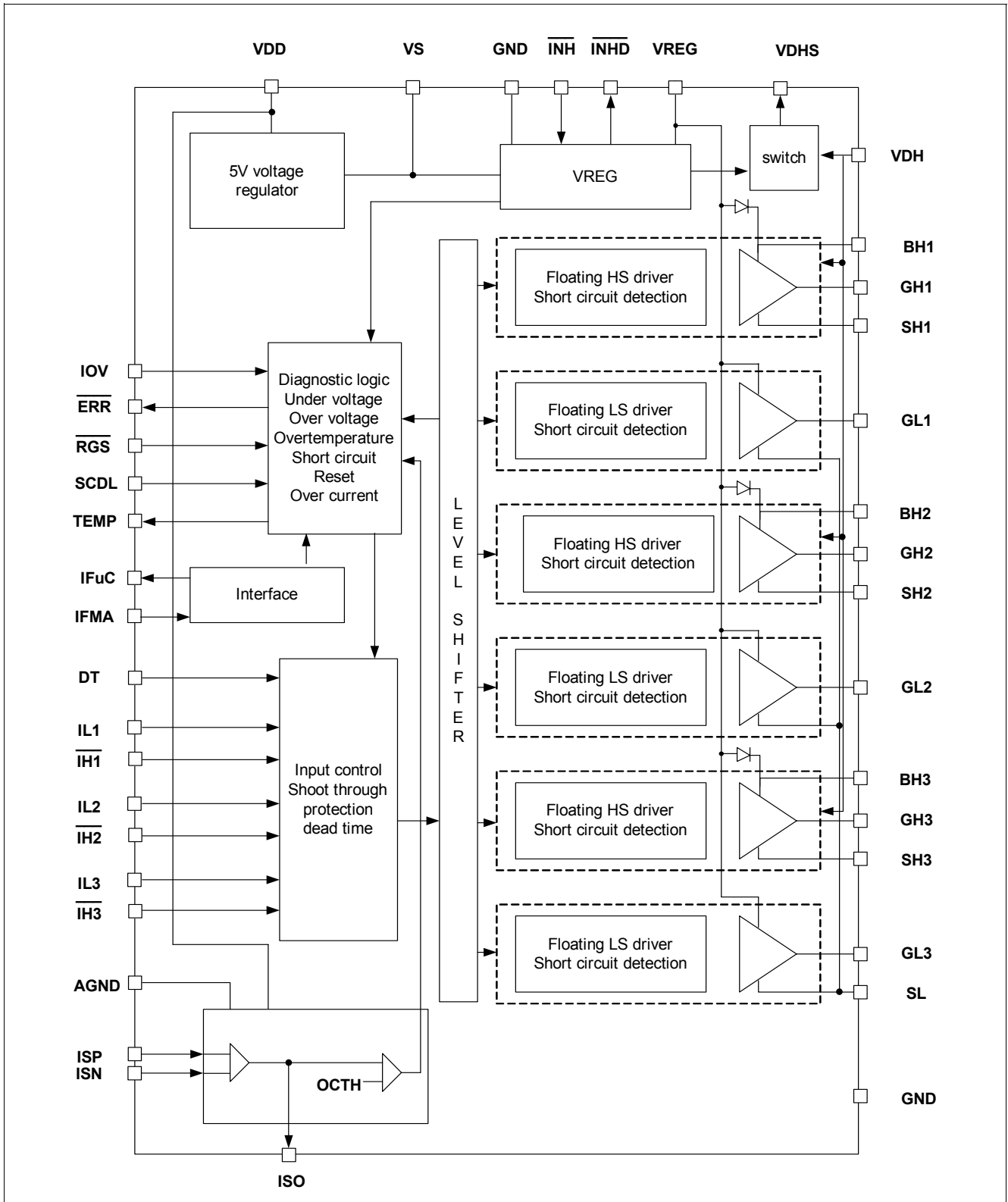


Figure 1 Block Diagram

### 3 Pin Configuration

#### 3.1 Pin Assignment TLE7184F

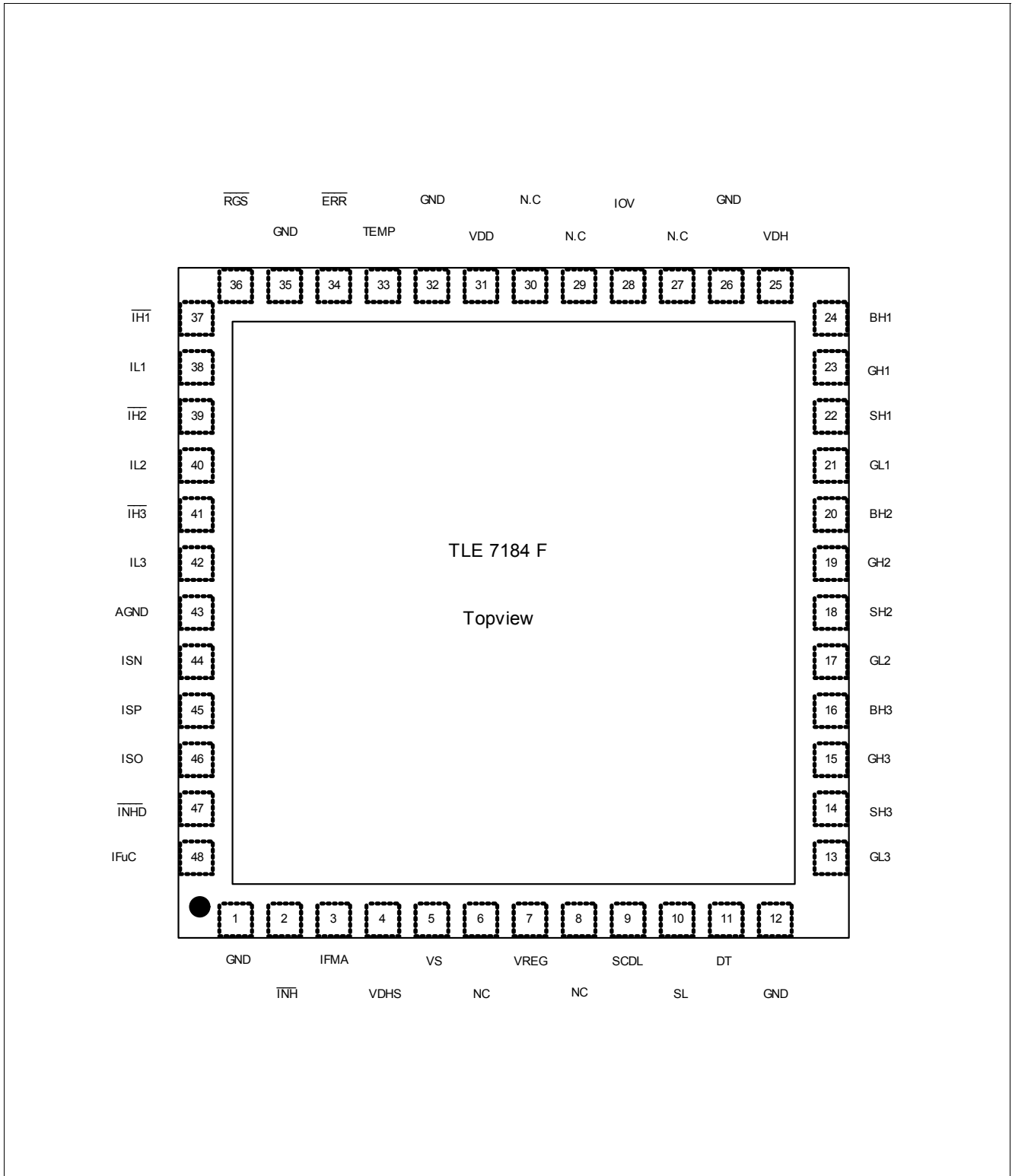


Figure 2 Pin Configuration

### 3.2 Pin Definitions and Functions

Pin	Symbol	Function
5	VS	Supply Pin
7	VREG	Output of supply for driver output stages - connect to capacitor
31	VDD	Output of 5V supply for $\mu$ C - connect to capacitor
2	$\overline{\text{INH}}$	Input pin wake up the complete system IC
47	$\overline{\text{INHD}}$	Digital output 5V for $\overline{\text{INH}}$ state (high when $\overline{\text{INH}}$ is high)
4	VDHS	Switched output of VDH voltage; switch open in sleep mode
33	TEMP	Output pin for analog temperature signal
36	$\overline{\text{RGS}}$	Reset and Go-to-Sleep input pin for reset of error registers, set HIGH to avoid to go-to-sleep
38	IL1	Input for low side switch 1 (active high)
37	$\overline{\text{IH1}}$	Input for high side switch 1 (active low)
40	IL2	Input for low side switch 2 (active high)
39	$\overline{\text{IH2}}$	Input for high side switch 2 (active low)
42	IL3	Input for low side switch 3(active high)
41	$\overline{\text{IH3}}$	Input for high side switch 3(active low)
11	DT	Input pin for adjustable dead time function, connect to GND via resistor
9	SCDL	Analog input pin for adjustable Short Circuit Detection function, connect to voltage divider
28	IOV	Input pin for Over Voltage detection.
34	$\overline{\text{ERR}}$	Open drain error output
25	VDH	Voltage input common drain high side for short circuit detection
24	BH1	Pin for + terminal of the bootstrap capacitor of phase 1
23	GH1	Output pin for gate of high side MOSFET 1
22	SH1	Pin for source connection of high side MOSFET 1
21	GL1	Output pin for gate of low side MOSFET 1
20	BH2	Pin for + terminal of the bootstrap capacitor of phase 2
19	GH2	Output pin for gate of high side MOSFET 2
18	SH2	Pin for source connection of high side MOSFET 2
17	GL2	Output pin for gate of low side MOSFET 2
16	BH3	Pin for + terminal of the bootstrap capacitor of phase 3
15	GH3	Output pin for gate of high side MOSFET 3
14	SH3	Pin for source connection of high side MOSFET 3
13	GL3	Output pin for gate of low side MOSFET 3
10	SL	Pin for common source connection of low side MOSFETs
44	ISN	Input for OpAmp - terminal
45	ISP	Input for OpAmp + terminal
46	ISO	Output of OpAmp
43	AGND	Analog GND for Opamp and analog temperature output
3	IFMA	Interface to master ECU (used for wake up)
48	IFuC	Interface to $\mu$ C

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**Pin Configuration**

<b>Pin</b>	<b>Symbol</b>	<b>Function</b>
1	GND	Ground pin
12	GND	Ground pin
26	GND	Ground pin
32	GND	Ground pin
35	GND	Ground pin
6	NC	connect to GND
8	NC	connect to GND
27	NC	connect to GND
29	NC	connect to GND
30	NC	connect to GND

Exposed pad to be connected to GND



## 4 General Product Characteristics

### 4.1 Absolute Maximum Ratings

#### Absolute Maximum Ratings <sup>1)</sup>

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
<b>Voltages</b>						
4.1.1	Voltage range at VS, IFMA, $\overline{\text{INH}}$ , IOV	$V_{VS1}$	-0.3	45	V	–
4.1.2	Voltage range at IFMA, $\overline{\text{INH}}$	$V_{IFMA}$	-6.0	45	V	$R \geq 10\text{k}\Omega$
4.1.3	Voltage range at VS	$V_{VS2}$	-3.0	45	V	$R_{VS} \geq 4.7\Omega$ ; 60s, 5x;
4.1.4	Voltage range at VS	$V_{VS3}$	-3.0	45	V	$R_{VS} \geq 2.0\Omega$ ;; 200ms, 5x;
4.1.5	Voltage range at VREG output	$V_{VREG}$	-0.3	15	V	–
4.1.6	Voltage range at VDH, VDHS	$V_{VDHx}$	-0.3	55	V	–
4.1.7	Voltage range at VDH	$V_{VDH1}$	-3.0	55	V	With $R_{VDH}$ $\geq 10\Omega$ ; 60s, 5x; $T_j \leq 150\text{ °C}$
4.1.8	Voltage range at $\overline{\text{IHx}}$ , $\overline{\text{ILx}}$ , $\overline{\text{RGS}}$ , $\overline{\text{ERR}}$ , IFuC, TEMP, DT, VDD, ISO, $\overline{\text{INHd}}$ , SCDL,	$V_{DP}$	-0.3	6	V	–
4.1.9	Voltage range at ISP, ISN	$V_{OPI}$	-5.0	5.0	V	–
4.1.10	Voltage range at BHx	$V_{BH}$	-0.3	55	V	–
4.1.11	Voltage range at GHx	$V_{GH}$	-0.3	55	V	–
4.1.12	Voltage range at GHx	$V_{GHP}$	-7.0	55	V	$t_p < 1\mu\text{s}$ ; $f=50\text{kHz}$
4.1.13	Voltage range at SHx	$V_{SH}$	-2.0	45	V	–
4.1.14	Voltage range at SHx	$V_{SHP}$	-7.0	45	V	$t_p < 1\mu\text{s}$ ; $f=50\text{kHz}$
4.1.15	Voltage range at GLx	$V_{GL}$	-0.3	18	V	–
4.1.16	Voltage range at GLx	$V_{GLP}$	-7.0	18	V	$t_p < 0.5\mu\text{s}$ ; $f=50\text{kHz}$
4.1.17	Voltage range at SL	$V_{SL}$	-0.3	5.0	V	–
4.1.18	Voltage range at SL	$V_{SLP}$	-7.0	5.0	V	$t_p < 0.5\mu\text{s}$ ; $f=50\text{kHz}$
4.1.19	Voltage difference Gxx-Sxx	$V_{GS}$	-0.3	15	V	–
4.1.20	Voltage difference BHx-SHx	$V_{BS}$	-0.3	15	V	–
4.1.21	Minimum bootstrap capacitor $C_{BS}$	$C_{BS}$	330	–	nF	–
<b>Temperatures</b>						
4.1.22	Junction temperature	$T_j$	-40	150	°C	–
4.1.23	Storage temperature	$T_{stg}$	-55	150	°C	–
4.1.24	Case temperature <sup>2)</sup>	$T_{Case}$	–	145	°C	–

**Absolute Maximum Ratings (cont'd)<sup>1)</sup>**

$T_j = -40\text{ °C}$  to  $+150\text{ °C}$ ; all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
<b>ESD Susceptibility</b>						
4.1.25	ESD Resistivity <sup>3)</sup>	$V_{ESD}$	-2	+2	kV	–
4.1.26	CDM	$V_{CDM}$	–	500	V	–

1) Not subject to production test, specified by design.

2) Calculation based on  $T_{jmax}$ ,  $R_{thJC}$  and the assumption of 1W power dissipation

3) ESD susceptibility HBM according to EIA/JESD 22-A 114B

*Note: Stresses above the ones listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.*

*Note: Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuous repetitive operation.*

**4.2 Functional Range**

Pos.	Parameter	Symbol	Limit Values		Unit	Conditions
			Min.	Max.		
4.2.1	Supply voltage at VS	$V_{VS}$	6.0	45	V	below 7V reduced functionality <sup>1) 2)</sup>
4.2.2	Quiescent current ( $I_{VS} + I_{VDH} + I_{IFMA}$ )	$I_Q$	–	50	μA	$V_S < 16V$ ; sleep mode $V_{VS} = V_{VDH} = V_{IFMA}$
4.2.3	Supply current at VS (device enabled)	$I_{VS(0)}$	–	19	mA	$V_S = 8...18V$ ; no load <sup>3)</sup> ; $f_{PWM} = 25kHz$ ;
4.2.4	Duty cycle HS	$D_{HS}$	0	94	%	$f_{PWM} = 25kHz$ ;
4.2.5	Duty cycle LS	$D_{LS}$	0	100	%	continuous operation
4.2.6	Junction temperature	$T_j$	-40	150	°C	–

1) MOS driver output deactivated and ERROR pin set to low if VREG is lower UVVR

2) MOS driver output stage will operate at  $V_S = 6.7V$  with 5mA load current at VREG

3) no load at VDD, ERR, ISO, IFμC, VDHS, GXX, TEMP, DT

The limitations in the PWM frequency are given by thermal constraints and limitations in the duty cycle (charging time of bootstrap capacitor).

All maximum ratings have to be considered

All basic functions will work between  $T_j = 150\text{ °C}$  and Over Temperature shut down. In this temperature range, the parameters might leave the specified range.

*Note: Within the functional range the IC operates as described in the circuit description. The electrical characteristics are specified within the conditions given in the related electrical characteristics table.*

### 4.3 Thermal Resistance

Note: This thermal data was generated in accordance with JEDEC JESD51 standards. For more information, go to [www.jedec.org](http://www.jedec.org).

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
4.3.1	Junction to Case <sup>1)</sup>	$R_{thJC}$	–	–	5	K/W	–
4.3.2	Junction to Ambient <sup>1)</sup>	$R_{thJA}$	–	29	–	K/W	<sup>2)</sup>

1) Not subject to production test, specified by design.

2) Specified  $R_{thJA}$  value is according to Jedec JESD51-2,-5,-7 at natural convection on FR4 2s2p board; The Product (Chip+Package) was simulated on a 76.2 x 114.3 x 1.5 mm board with 2 inner copper layers (2 x 70µm Cu, 2 x 35µm Cu). Where applicable a thermal via array under the exposed pad contacted the first inner copper layer.

### 4.4 Default State of Inputs

Table 1 Default State of Inputs

Characteristic	State	Remark
Default state of ILx (if ILx left open -pull down)	Low	Low side MOSFETs off
Default state of IHx (if IHx left open - pull up)	High	High side MOSFETs off
Default state of RGS (if RGS left open - pull down)	Low	Errors is reset and system IC goes to sleep
Default state of INH (if INH left open - pull down)	Low	no wake up by INH
Default state of SCDL (if SCDL left open - pull up)	High	Error is set; all MOSFETs switched off
Default state of IFMA (if IFMA left open - pull up) <sup>1)</sup>	High	no wake up by IFMA
Default state of IOV (if IOV left open - pull down)	Low	no Over Voltage detection by IOV
Default state of DT (if DT left open)	max. dead time	max. dead time

1) external capacitance < 25pF

## 5 MOSFET Driver

### 5.1 Inputs and Dead Time

There are 6 independent control inputs to control the 6 MOSFETs individually. However, the control inputs for the High Side MOSFETs  $\overline{IHx}$  are inverted. Hence, the control inputs for High Side  $\overline{IHx}$  and Low Side MOSFETs  $ILx$  of the same half bridge can be tight together to control one half bridge by one control signal. To avoid shoot through currents within the half bridges, a dead time is provided by the TLE7184F.

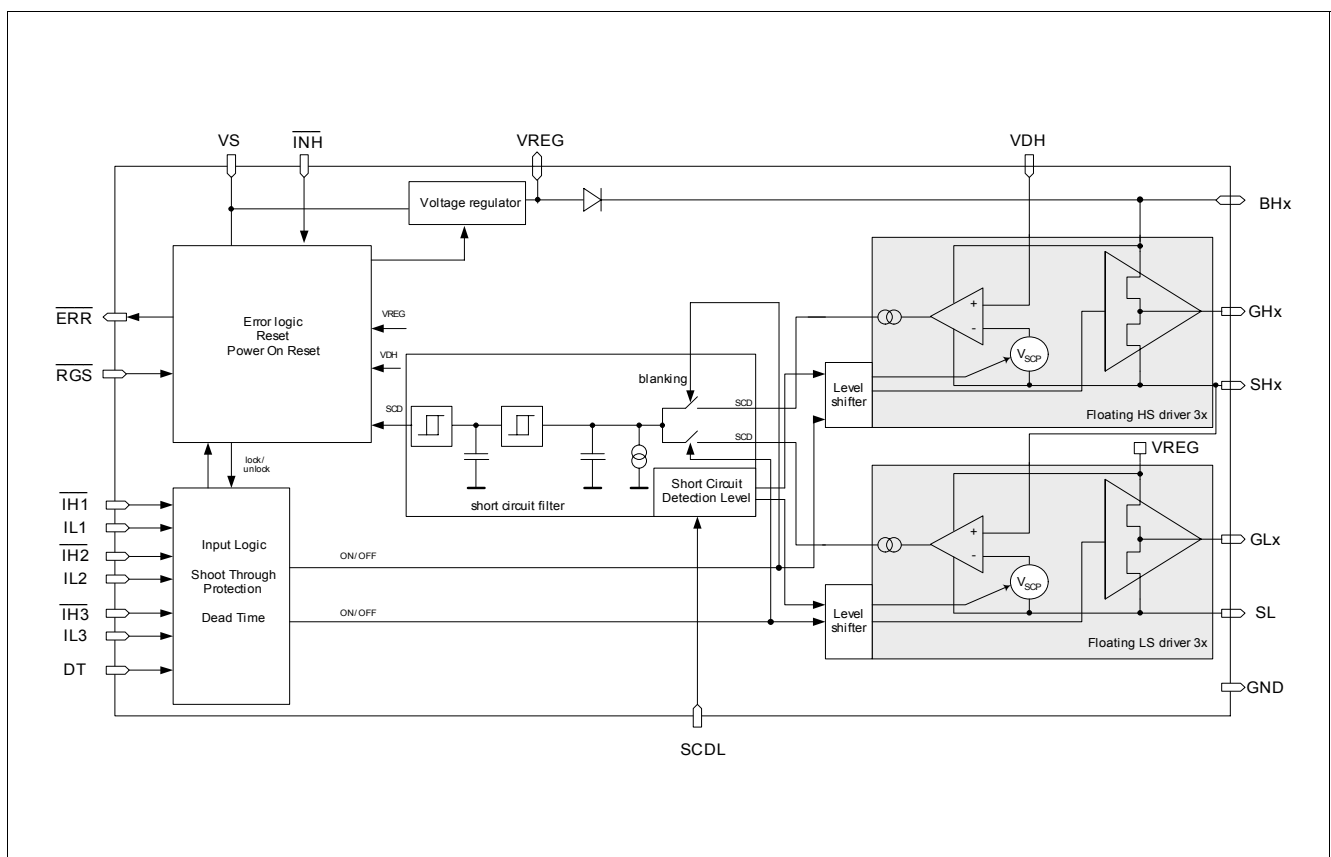
For more details about the dead time please see [Chapter 9.2.10](#)

### 5.2 Output Stages

The 3 low side and 3 high side powerful push-pull output stages of the TLE7184F are all floating blocks.

All 6 output stages have the same output power and thanks to the used bootstrap principle they can be switched all up to high frequencies.

Each output stage has its own short circuit detection block. For more details about short circuit detection see [Chapter 9.2.11](#).<sup>1)</sup>



**Figure 3 Block Diagram of Driver Stages including Short Circuit Detection**

1) The high side outputs are not designed to be used for low side MOSFETs; the low side outputs are not designed to be used for high side MOSFETs

### 5.3 Bootstrap Principle

The TLE7184F provides a bootstrap based supply for its high side output stages. The benefit of this principle is a fast switching of the high side switches - supporting active freewheeling in high side.

The bootstrap capacitors are charged by switching on the external low side MOSFETs connecting the bootstrap capacitor to GND. Under this condition the bootstrap capacitor will be charged from the VREG capacitor. If the low side MOSFET is switched off and the high side MOSFET is switched on, the bootstrap capacitor will float together with the SHx voltage to the supply voltage of the bridge. Under this condition the supply current of the high side output stage will discharge the bootstrap capacitor. This current is specified. The size of the capacitor together with this current will determine how long the high side MOSFET can be kept on without recharging the bootstrap capacitor.

When all external MOSFETs are switched off, the SHx voltage can be undefined. Under this condition, the bootstrap capacitors can be discharged, dependent on the SHx voltage.

### 5.4 Electrical Characteristics

#### Electrical Characteristics MOSFET Drivers

$V_S = 7.0$  to  $33$  V,  $T_j = -40$  °C to  $+150$  °C all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
<b>Inputs</b>							
5.4.1	Low level input voltage of ILx; $\overline{\text{IHx}}$	$V_{\text{ILL}}$	–	–	1.6	V	–
5.4.2	High level input voltage of ILx; $\overline{\text{IHx}}$	$V_{\text{IHL}}$	2.8	–	–	V	–
5.4.3	Input hysteresis of $\overline{\text{IHx}}$ ; ILx <sup>1)</sup>	$d_{\text{VI}}$	100	–	–	mV	–
5.4.4	$\overline{\text{IHx}}$ pull-up resistors to VDD	$R_{\text{IH}}$	33.5	–	66.5	k $\Omega$	–
5.4.5	ILx pull-down resistors to GND	$R_{\text{IL}}$	210	–	490	k $\Omega$	–
<b>MOSFET driver output</b>							
5.4.6	Output source resistance	$R_{\text{Sou}}$	2	–	13.5	$\Omega$	Iload=20mA
5.4.7	Output sink resistance	$R_{\text{Sink}}$	2	–	9	$\Omega$	Iload=20mA
5.4.8	High level output voltage Gxx vs. Sxx	$V_{\text{Gxx1}}$	–	11	14	V	13,5V $\leq V_{\text{VS}} \leq 45\text{V}^2)$ , $V_{\text{IOV}} \leq V_{\text{OVIOV}}$ , $V_{\text{VDH}} \leq V_{\text{OVVDH}}$ $I_{\text{load}} = 37,5\text{mA}$
5.4.9	High level output voltage GHx vs. SHx <sup>1)</sup>	$V_{\text{Gxx2}}$	6	–	–	V	$V_{\text{VS}} = 8\text{V}$ , $C_{\text{load}} = 20\text{nF}$ , dc=94%; $f_{\text{PWM}} = 20\text{kHz}$
5.4.10	High level output voltage GHx vs. SHx <sup>1)3)</sup>	$V_{\text{Gxx3}}$	6 + $V_{\text{diode}}$	–	–	V	$V_{\text{VS}} = 8\text{V}$ , $C_{\text{load}} = 20\text{nF}$ , dc=94%; $f_{\text{PWM}} = 20\text{kHz}$ ; passive freewheeling

**Electrical Characteristics MOSFET Drivers**

$V_S = 7.0$  to  $33$  V,  $T_j = -40$  °C to  $+150$  °C all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
5.4.11	High level output voltage GLx vs. GND	$V_{Gxx4}$	6.7	–	–	V	$V_{VS}=8V$ , $C_{load}=20nF$ , dc=94%; $f_{PWM}=20kHz$ ;
5.4.12	Rise time	$t_{rise}$	–	200	–	ns	$C_{Load}=11nF$ ;
5.4.13	Fall time	$t_{fall}$	–	200	–	ns	$R_{Load}=1\Omega$ $V_{VS}=7V$ 20-80%
5.4.14	High level output voltage (in passive clamping)	$V_{GUV}$	–	–	1.2	V	sleep mode or $VS\_UVLO^{1) 4)}$
5.4.15	Pull-down resistor at BHx to GND	$R_{BHUV}$	–	–	80	k $\Omega$	
5.4.16	Pull-down resistor at VREG to GND	$R_{VRUV}$	–	–	30	k $\Omega$	
5.4.17	Bias current into BHx	$I_{BH}$	–	–	150	$\mu A$	$V_{BHx}-V_{SHx}=5...13V$ ; no switching
5.4.18	Current between BHx and SHx	$I_{BSH}$	15	35	60	$\mu A$	$V_{BHx}-V_{SHx}=5...13V$
5.4.19	Resistor between SHx and GND	$R_{SHGN}$	48	80	112	k $\Omega$	
5.4.20	Bias current out of SL	$I_{SL}$	–	–	2	mA	$0V \leq V_{SH} \leq V_S + 1$ V; no switching; $V_{CBS} > 5V$
5.4.21	Input propagation time (low on)	$t_{P(ILN)}$	0	–	200	ns	$C=11nF$ ; $R_{Load}=1\Omega$
5.4.22	Input propagation time (low off)	$t_{P(ILF)}$	0	–	200	ns	
5.4.23	Input propagation time (high on)	$t_{P(IHN)}$	0	–	200	ns	
5.4.24	Input propagation time (high off)	$t_{P(IHF)}$	0	–	200	ns	
5.4.25	Absolute input propagation time difference between above propagation times	$t_{P(diff)}$	–	–	100	ns	

**VREG**

5.4.26	VREG output voltage	$V_{VREG}$	11	12.5	14	V	$V_{VS} \geq 13,5V$ ; $I_{load}=37,5mA$
5.4.27	VREG over current limitation	$I_{VREGOCL}$	100	–	500	mA	no activation of error; $V_{VREG} > V_{VRSD}$
5.4.28	Voltage drop between Vs and VREG	$V_{VsVREG}$	–	–	0.5	V	$V_{VS} \geq 7V$ ; $I_{load}=37,5mA$ ; Ron operation

- 1) Not subject to production test; specified by design
- 2) Values above 33V not subjected to production test; specified by design
- 3)  $V_{diode}$  is the bulk diode of the external low side MOSFET
- 4) see [Chapter 9.2.15](#)

## 6 Shunt Signal Conditioning

The TLE7184F incorporates a fast and precise operational amplifier for conditioning and amplification of the current sense shunt signal. The gain of the OpAmp is adjustable by external resistors within a range higher than 5. The usage of higher gains in the application might be limited by required settling time and band width.

It is recommended to apply a small offset to the OpAmp, to avoid operation in the lower rail at low currents.

The output of the OpAmp ISO is not short-circuit proof.

In addition to the integrated operational amplifier, the TLE7184F incorporates a comparator to detect over current situations. The output voltage  $V_{ISO}$  is compared to a reference voltage  $V_{OCTH}$  close to the upper rail of the 5V OpAmp supply (VDD). If  $V_{ISO}$  reaches this level an error is set.

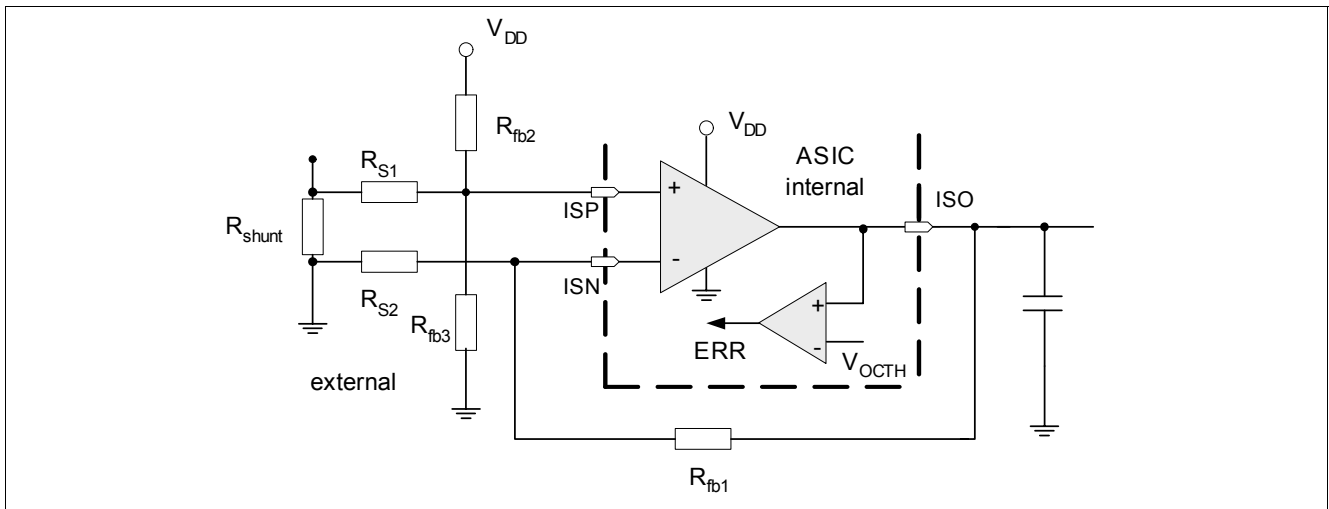


Figure 4 Shunt Signal Conditioning Block Diagram and Over Current Limitation

Over current shut down see [Chapter 9.2.13](#).

### 6.1 Electrical Characteristics

#### Electrical Characteristics - Current sense signal conditioning

$V_S = 6.0$  to  $33$  V,  $T_j = -40$  °C to  $+150$  °C, gain = 5 to 75, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)<sup>1)</sup>

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.1.1	Series resistors	$R_S$	100	500	1000	$\Omega$	–
6.1.2	Feedback resistor Limited by the output voltage dynamic range	$R_{fb}$	2000	7500	–	$\Omega$	–
6.1.3	Resistor ratio (gain ratio)	$R_{fb}/R_S$	5	–	–	–	–
6.1.4	Steady state differential input voltage range across VIN	$V_{IN(ss)}$	-400	–	400	mV	–
6.1.5	Input differential voltage (ISP - ISN)	$V_{IDR}$	-800	–	800	mV	–
6.1.6	Input voltage (Both Inputs - GND) (ISP - GND) or (ISN - GND)	$V_{LL}$	-800	–	2000	mV	–
6.1.7	Input offset voltage of the I-DC link OpAmp, including temperature drift	$V_{IO}$	–	–	+/-2	mV	$R_S=500\Omega$ ; $V_{CM}=0V$ ; $V_{ISO}=1.65V$ ;

**Electrical Characteristics - Current sense signal conditioning (cont'd)**

$V_S = 6.0$  to  $33$  V,  $T_j = -40$  °C to  $+150$  °C, gain = 5 to 75, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)<sup>1)</sup>

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
6.1.8	Input bias current (ISN,ISP to GND)	$I_{IB}$	-300	–	–	µA	$V_{CM}=0V$ ; $V_{ISO}=\text{open}$
6.1.9	High level output voltage of ISO	$V_{OH}$	$V_{VDD}-0.2$	–	$V_{VDD}$	V	$I_{OH}=-3mA$
6.1.10	Low level output voltage of ISO	$V_{OL}$	-0.1	–	0.2	V	$I_{OH}=3mA$
6.1.11	Output short circuit current	$I_{SC}$	5	–	–	mA	–
6.1.12	Differential input resistance <sup>2)</sup>	$R_I$	100	–	–	kΩ	–
6.1.13	Common mode input capacitance <sup>2)</sup>	$C_{CM}$	–	–	10	pF	10kHz
6.1.14	Common mode rejection ratio at DC CMRR = $20 \cdot \text{Log}((V_{out\_diff}/V_{in\_diff}) \cdot (V_{in\_CM}/V_{out\_CM}))$	$C_{MRR}$	80	100	–	dB	–
6.1.15	Common mode suppression <sup>3)</sup> with CMS = $20 \cdot \text{Log}(V_{out\_CM}/V_{in\_CM})$ Freq = 100kHz Freq = 1MHz Freq = 10MHz	$C_{MS}$	–	62 43 33	–	dB	$V_{IN}=360mV \cdot \sin(2 \cdot \pi \cdot \text{freq} \cdot t)$ ; $R_S=500\Omega$ ; $R_{fb}=7500\Omega$
6.1.16	Slew rate	$d_{V/dt}$	–	10	–	V/µs	Gain >= 5; $R_L=1.0k\Omega$ ; $C_L=500pF$
6.1.17	Large signal open loop voltage gain (DC)	$A_{OL}$	80	100	–	dB	–
6.1.18	Unity gain bandwidth	$G_{BW}$	10	20	–	MHz	$R_L=1k\Omega$ ; $C_L=100pF$
6.1.19	Phase margin <sup>2)</sup>	$F_M$	–	50	–	°	Gain >= 5; $R_L=1k\Omega$ ; $C_L=100pF$
6.1.20	Gain margin <sup>2)</sup>	$A_M$	–	12	–	dB	$R_L=1k\Omega$ ; $C_L=100pF$
6.1.21	Bandwidth	$B_{WG}$	1.6	–	–	MHz	Gain=15; $R_L=1k\Omega$ ; $C_L=500pF$ ; $R_S=500\Omega$
6.1.22	Output settle time to 98% $R_{fb}/R_S=15$ $R_{fb}/R_S=75$	$t_{set1}$	– –	1 4.6	1.8 8	µs	$R_L=1k\Omega$ ; $C_L=500pF$ ; $0.3 < V_{ISO} < 4.8V$ ; $R_S=500\Omega$

1) A minimum capacitance of 100pF is needed at the output of the OpAmp (parasitic or real capacitor)

2) Not subject to production test; specified by design

3) Without considering any offsets such as input offset voltage, internal miss match and assuming no tolerance error in external resistors.



## 7 5 V Low Drop Voltage Regulator

The TLE7184F incorporates a 5V LDO for  $\mu\text{C}$  supply. The voltage regulator is protected against Over Temperature by the central temperature sensor (see [Chapter 9.2.1](#) and [Chapter 9.2.2](#)). It has an integrated current limitation and Under Voltage detection.

Parameters for Under Voltage detection see [Chapter 9.2.5](#).

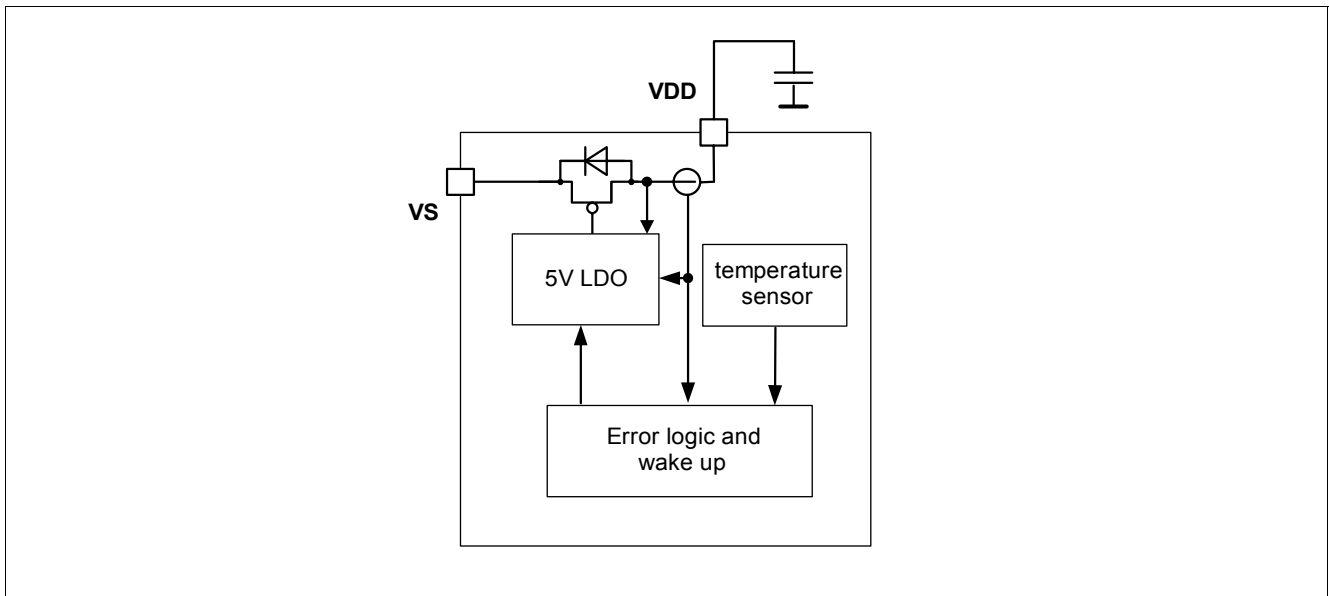


Figure 5 Block diagram of 5V LDO

### 7.1 Electrical Characteristics

#### Electrical Characteristics - Current sense signal conditioning

$V_S = 6.0$  to  $45\text{ V}$ ,  $T_j = -40\text{ }^\circ\text{C}$  to  $+150\text{ }^\circ\text{C}$ , all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
7.1.1	Output voltage	$V_{DD1}$	4.85	–	5.25	V	$I_{load} \leq 70\text{mA}$ ; $C_{load} = 1...22\mu\text{F}^{1)}$
7.1.2	Output voltage	$V_{DD2}$	4.90	–	5.20	V	$5\text{mA} \leq I_{load} \leq 25\text{mA}$ ; $C_{load} = 1...22\mu\text{F}^{1)}$
7.1.3	LDO over current limitation	$I_{OCL}$	130	–	270	mA	no activation of error
7.1.4	Load regulation	$D_{VDD}$	–	50	100	mV	$I_{load}$ step $0...20\text{mA}$ ; $C_{VDD} = 1\mu\text{F}$
7.1.5	Power supply ripple rejection <sup>2)</sup>	$P_{SRR}$	50	–	–	dB	100Hz sine wave; $0.5\text{V}_{pp}$ $V_S \geq 7\text{V}$
7.1.6	Power supply ripple rejection <sup>2)</sup>	$P_{SRR}$	–	31	–	dB	100Hz sine wave; $0.5\text{V}_{pp}$ $6\text{V} \leq V_S < 7\text{V}$

1) ceramic C with 100nF with ESR<0.1 $\Omega$  in parallel

2) Not subject to production test; specified by design

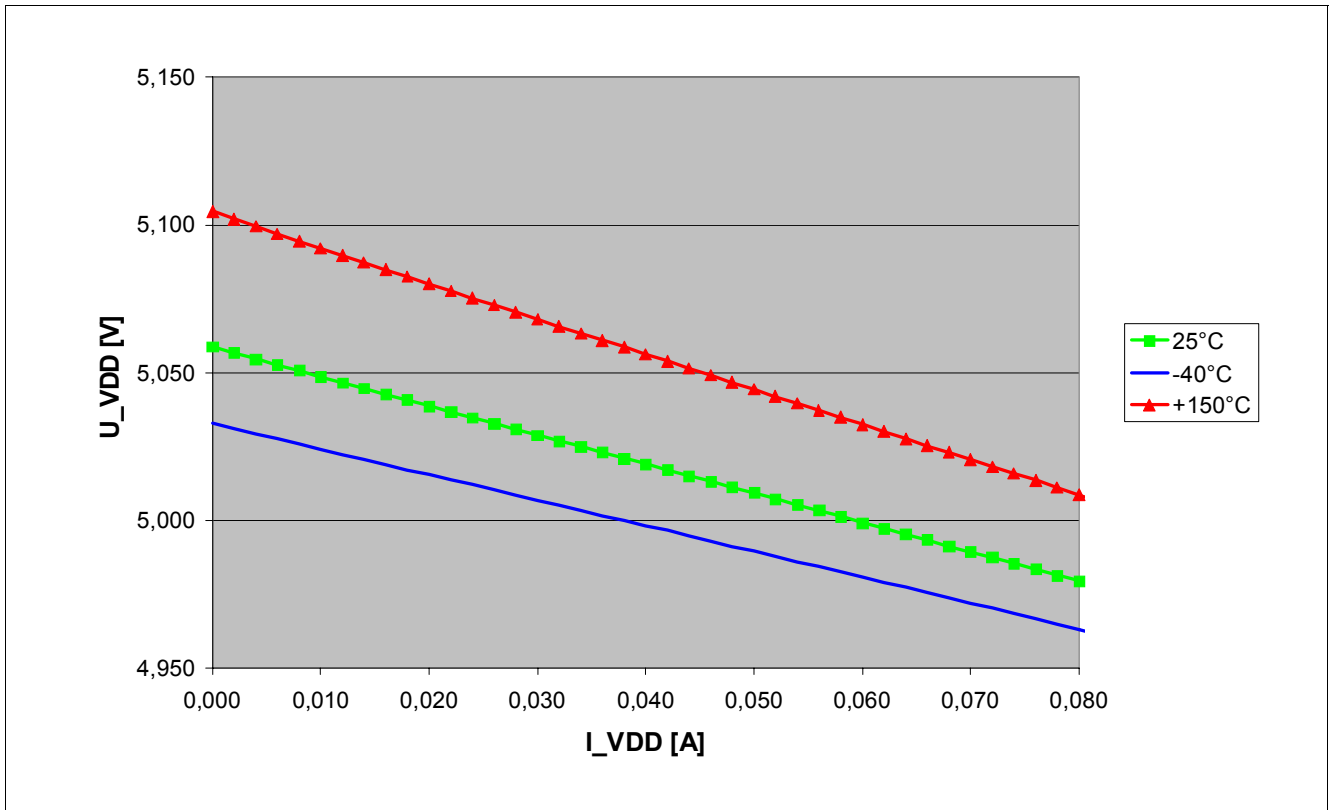


Figure 6 Typ. VDD output voltage vs. load current

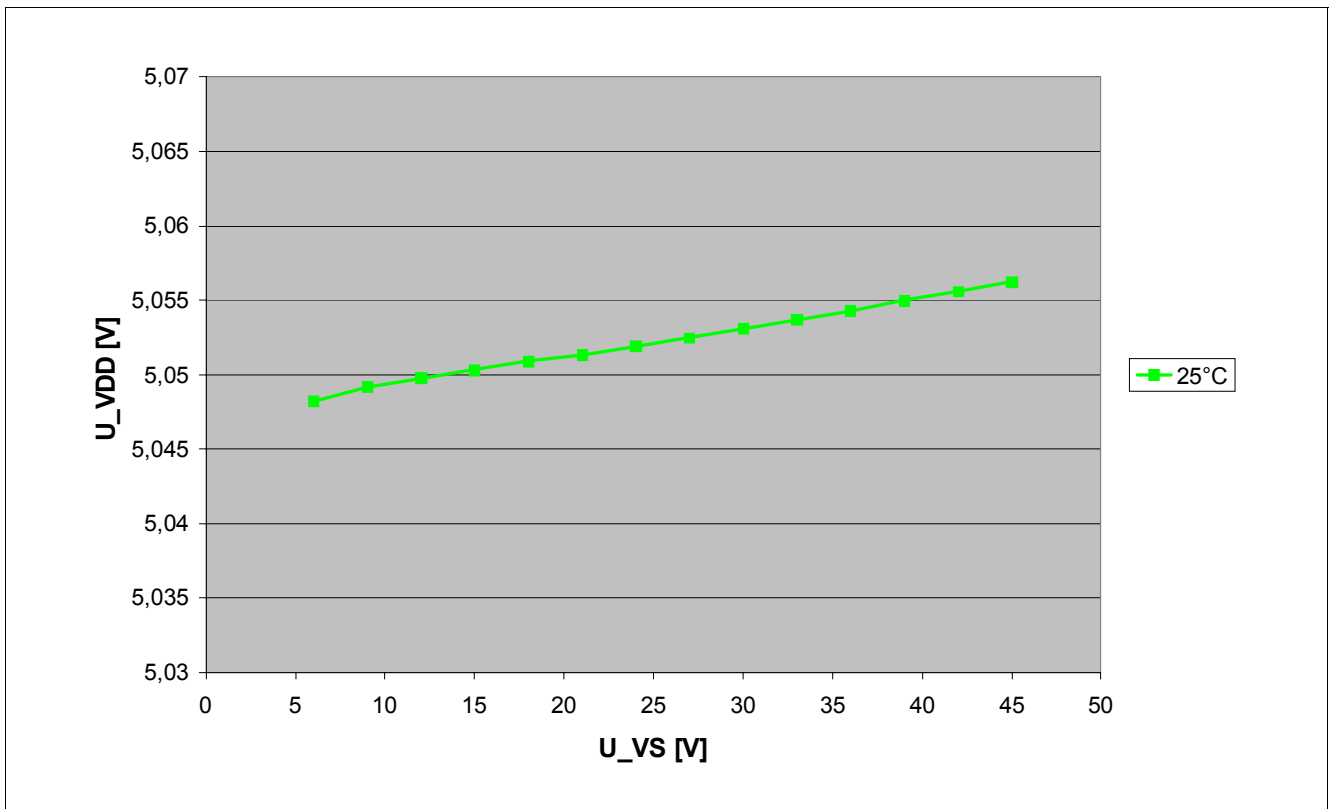


Figure 7 Typ. VDD output voltage vs. load current

## 8 Interface, VDH Switch and $\overline{\text{INH}}$ Digital Output

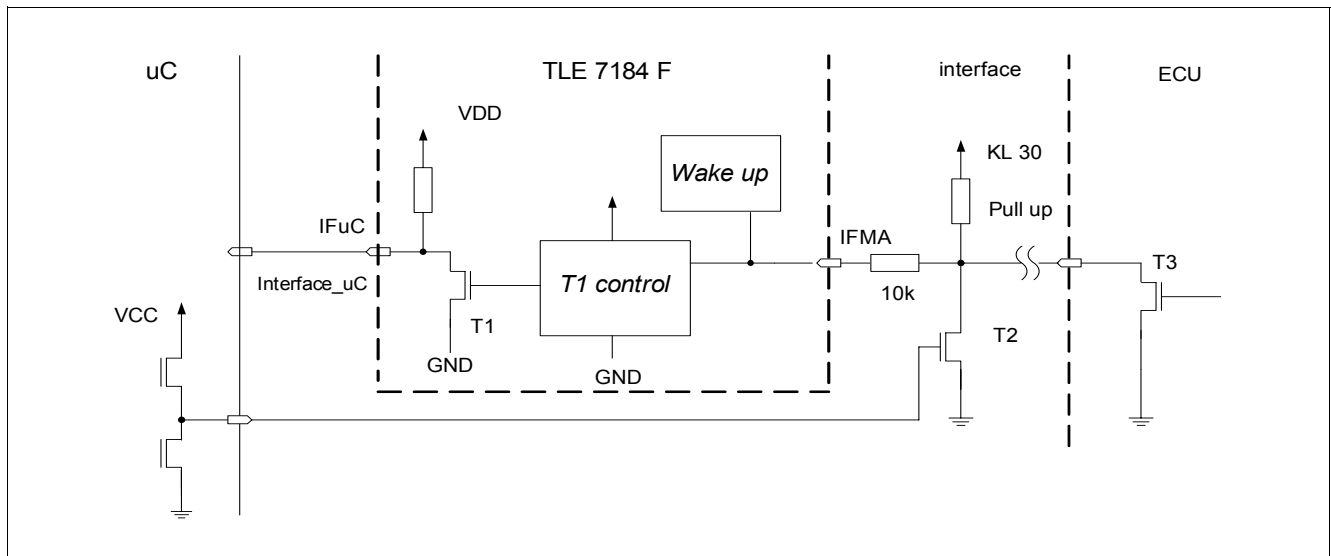
### 8.1 PWM Interface (IFMA)

The TLE7184F has an integrated interface supporting the typical PWM interface between a remote master ECU and the  $\mu\text{C}$ . The link to the external master ECU is a single wire communication based on the battery voltage and running typ. with about 10 to 400 Hz. The information is encoded in the duty cycle of the signal.

This communication line requires a signal conditioning to connect to the on board  $\mu\text{C}$ .

The integrated circuit supports the incoming data path.

The outgoing data path is formed by external components



**Figure 8 Structure PWM Interface**

The integrated circuitry is described in [Figure 8](#).

The main task of this interface is level shifting and protection of the  $\mu\text{C}$ .

The IFuC signal is following the IFMA signal, passing the duty cycle information from IFMA to the IFuC.

The  $\mu\text{C}$  port is used as input and is listening to the IFuC signal. The voltage at IFMA is monitored. If IFMA is low the IFuC open drain output is switched on - forcing the IFuC signal to low.

If IFMA is high, the IFuC open drain output is deactivated and the IFuC signal is pulled to high by the internal pull-up resistor.

The IFMA input is used as well for wake-up. See [Chapter 9.1](#)

### 8.2 VDHS Switch

The System IC has an integrated switch connecting the VDH pin to the VDHS pin. This allows to place an external voltage divider for VDH voltage monitoring at the VDHS pin and to disconnect this voltage divider from VDH during sleep mode to assure low current consumption. The VDHS switch is only deactivated when the VDD regulator is switched off.

### 8.3 Digital Output $\overline{\text{INH}}$

The System IC provides a digital output  $\overline{\text{INH}}$  showing the logic state of  $\overline{\text{INH}}$  (e.g. KL15) after complete wake-up of the driver (approx. 1ms). The input levels of INH for the INHD output are defined separately from the levels for wake up. Voltage levels for  $\overline{\text{INH}}$  wake up function please see [Chapter 9.4](#) section Wake-up and go-to-sleep. The output stage consists of an integrated low side switch with a pull-up resistor to VDD.

## 8.4 Electrical Characteristics

### Electrical Characteristics - Protection and diagnostic functions

$V_S = 6.0$  to  $20V$ ,  $T_j = -40$  °C to  $+150$  °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
<b>Interface - static parameters</b>							
8.4.1	IFMA input voltage high level (for IF $\mu$ C high)	$V_{IMHL}$	59	–	–	%	of $V_{VS}$ ; IC not in Sleep Mode
8.4.2	IFMA input voltage low level (for IF $\mu$ C low)	$V_{IMLL}$	–	–	46	%	of $V_{VS}$ ; IC not in Sleep Mode;
8.4.3	IFMA input hysteresis (for IF $\mu$ C)	$V_{IMhy}$	0.5	–	9	%	of $V_{VS}$ ; IC not in Sleep Mode
8.4.4	IFMA wake up voltage high level = $V_S - V_{IFMA}$	$V_{IMWH}$	2	–	4	V	valid in Sleep Mode
8.4.5	IFMA internal pull-up resistor to $V_S$	$R_{IMu}$	210	340	495	k $\Omega$	–
8.4.6	IFMA internal pull-down resistor to GND	$R_{IMd}$	420	700	980	k $\Omega$	not active in Sleep Mode
8.4.7	Matching of internal pull-up / pull-down resistor <sup>1)</sup>	$R_{IMu}/R_{IMd}$	-5	–	+5	%	–
8.4.8	IF $\mu$ C output low voltage	$V_{luLL}$	–	–	0.5	V	no external load
8.4.9	IF $\mu$ C internal pull-up resistor to $V_{DD}$	$R_{lu}$	10	–	20	k $\Omega$	–
<b>Interface - dynamic parameters</b>							
8.4.10	IF $\mu$ C duty cycle	$d_{lu}$	0	–	100	%	–
8.4.11	Propagation time rising edge IF $\mu$ C	$t_{PRE}$	–	–	6	$\mu$ s	Including rising time to 80% of $V_{VDD}$ ; $C_{load}=100pF$
8.4.12	Propagation time falling edge IF $\mu$ C	$t_{PFE}$	–	–	5	$\mu$ s	Including falling time to 20% of $V_{VDD}$ ; $C_{load}=100pF$
8.4.13	Deviation between rising and falling IF $\mu$ C	$t_{PD}$	–	–	4	$\mu$ s	$C_{load}=100pF$
<b>VDH switch</b>							
8.4.14	Ron VDH switch	$R_{VDH}$	–	–	150	$\Omega$	Load current = 1mA
<b>INHD digital output</b>							
8.4.15	Low level input voltage $\overline{INH}$ (for INHD=low)	$V_{INHDL}$	–	–	1.5	V	–
8.4.16	High level input voltage $\overline{INH}$ (for INHD=high)	$V_{INHDH}$	2.1	–	–	V	–
8.4.17	Input hysteresis of $\overline{INH}$ for $\overline{INHD}$ <sup>1)</sup>	$d_{VINHD}$	100	–	–	mV	–
8.4.18	$\overline{INHD}$ low level output voltage	$V_{INHD}$	–	–	0.5	V	no external load
8.4.19	$\overline{INHD}$ Internal pull-up resistor to $V_{DD}$	$R_{INHD}$	50	–	100	k $\Omega$	–

1) Not subject to production test; specified by design

## 9 Description of Modes, Protection and Diagnostic Functions

### 9.1 Description of modes

The operation of TLE7184F can be described by different operation modes

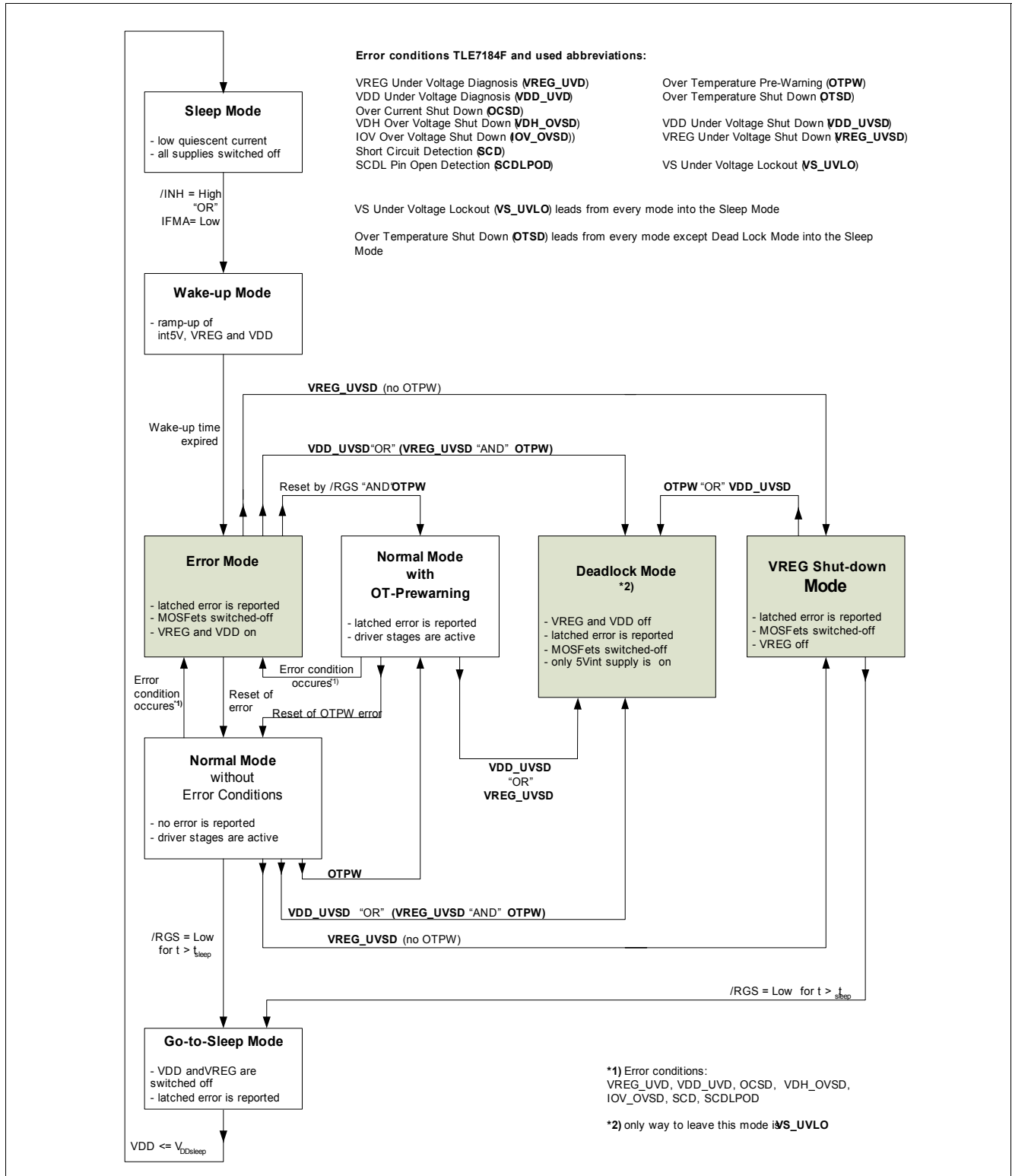


Figure 9 State diagram TLE7184F

**Sleep Mode:**

The sleep mode is entered if the device is in the Go-to-sleep Mode and the VDD voltage is lower than  $V_{DD\text{sleep}}$ . The complete chip is deactivated beside the wake-up function (see Wake-up Mode). This mode is designed for lowest current consumption from the power net of the car. The passive clamping is active. For details see the description of passive clamping, see [Chapter 9.2.15](#).

The only way to leave the Sleep Mode is to go to the Wake-up Mode.

**Wake-up Mode:**

The TLE7184F wakes up if  $\overline{\text{INH}}$  (=KL15) is high or if IFMA is low and  $V_{\text{VS}}$  is higher than  $V_{\text{VSLO}}$ .

In this mode all supplies are ramping up. As soon as the internal 5V is available, a so called wake-up timer starts to run. If the IC reaches this state, the wake up will continue even if the wake up signals at  $\overline{\text{INH}}$  or IFMA disappear. The PWM interface (IFMA) is active as soon as the VDD voltage is sufficient high. During this time it is expected that the supplies are powered up and the  $\mu\text{C}$  sets the  $\overline{\text{RGS}}$  to high. All external MOSFETs are switched off actively or passively. When the wake up timer is expired the IC goes into the Error mode.

In this mode all errors will be ignored beside Over Temperature Shut Down or  $V_{\text{S}}$  Under Voltage Lockout.

**Error Mode**

The Error Mode can be reached in 3 different ways:

1. The device is in Wake-up Mode and the wake up timer expires
2. The device is in Normal Mode and one or more of the following errors occur: VREG Under Voltage Shut Down, VDD Under Voltage Shut Down, Over Current Shut Down, VDH Over Voltage Shut Down, IOV Over Voltage Shut Down, Short Circuit Detection or SCDL Open Detection.
3. The device is in Normal Mode with OT-Prewarning and one or more of the following errors occur: VREG Under Voltage Shut Down, VDD Under Voltage Shut Down, Over Current Shut Down, VDH Over Voltage Shut Down, IOV Over Voltage Shut Down, Short Circuit Detection or SCDL Open Detection.

In this mode an Error is set at the ERROR Pin and all external MOSFETs are actively switched off as long as the bootstrap voltages allows it. The interface is active. VDHS switch is on and the current sense functions are working. VDD and VREG are active. Passive clamping is not active.

The Error mode can be left in the following ways:

1. If no error is present, the IC can be sent to Normal Mode by a reset with the  $\overline{\text{RGS}}$  pin.
2. If a VREG Under Voltage Shut Down occurs and no Over Temperature Prewarning is present, the device will go to VREG Shut-down Mode.
3. If VDD Under Voltage Shut Down occurs or a VREG Under Voltage Shut Down together with a Over Temperature Prewarning occurs, the device will go into Deadlock Mode.
4. If Over Temperature Prewarning is present, the IC can be sent to Normal Mode with OT-Prewarning by a reset with the  $\overline{\text{RGS}}$  pin.

**Normal Mode**

The Normal Mode can be reached in two different ways:

1. The device is in Error Mode, no error is present and a reset is performed by the  $\overline{\text{RGS}}$  pin.
2. The device is in Normal Mode with OT-Prewarning, the chip temperature is below the OT-Prewarning level and a reset is performed by the  $\overline{\text{RGS}}$  pin.

In the Normal Mode all functions are active and available with the regular limitations of the bootstrap principle. The gate drive output stages can be controlled with the input pins.

The Normal Mode can be left in 5 ways:

1. The devices goes to the Go-To-Sleep Mode by setting  $\overline{\text{RGS}}$  to low for a time longer than  $t_{\text{sleep}}$ .
2. If a Over Temperature Prewarning occurs the device goes into the Normal Mode with OT-Prewarning.

## Description of Modes, Protection and Diagnostic Functions

3. If a VREG Under Voltage Shut Down occurs and no Over Temperature Prewarning is present, the device will go to VREG Shut-down Mode.
4. If VDD Under Voltage Shut Down occurs or a VREG Under Voltage Shut Down together with a Over Temperature Prewarning occurs, the device will go into Deadlock Mode.
5. If one or more of the following errors occur, the device goes to the Error Mode: VREG Under Voltage Shut Down, VDD Under Voltage Shut Down, Over Current Shut Down, VDH Over Voltage Shut Down, IOV Over Voltage Shut Down, Short Circuit Detection or SCDL Open Detection.

### Go-To-Sleep Mode

The Go-To-Sleep Mode can be reached in 2 different ways:

1. The device is in Normal Mode and  $\overline{\text{RGS}}$  is set to low for a time longer than  $t_{\text{sleep}}$ .
2. The device is in VREG Shut-down Mode and  $\overline{\text{RGS}}$  is set to low for a time longer than  $t_{\text{sleep}}$ .

In this mode all external MOSFETs are actively or passively switched off. An Error is set and is shown as long as VDD is sufficient high. In this mode VDD and VREG is switched off. As soon as VDD voltage reaches the  $V_{\text{VDDsleep}}$  level the IC goes into the Sleep Mode.

### Normal Mode with Over Temperature Prewarning

This mode can be reached in 2 different ways:

1. The device is in Error Mode, the chip temperature is above the prewarning level while a reset is performed by the  $\overline{\text{RGS}}$  pin.
2. The device is in Normal Mode and the chip temperature increases above the prewarning level.

In this mode all functions are active and available. The gate drive output stages can be controlled with the input pins with the regular limitations of the bootstrap principle.

The  $\overline{\text{ERR}}$  pin is set to low and is latched.

There are 3 possibilities to leave this mode:

1. This mode can be left into the Normal Mode by applying a reset at  $\overline{\text{RGS}}$  if the temperature has dropped below the Over Temperature pre-warning level.
2. The device goes into Error Mode if one of the following errors occurs: VREG Under Voltage Shut Down, VDD Under Voltage Shut Down, Over Current Shut Down, VDH Over Voltage Shut Down, IOV Over Voltage Shut Down, Short Circuit Detection or SCDL Open Detection.
3. The device goes into Deadlock Mode if either a VREG Under Voltage Shut Down or a VDD Under Voltage Shut Down occurs.

If the temperature is still in the pre-warning range and  $\overline{\text{RGS}}$  is low, the  $\overline{\text{ERR}}$  pin gets high only during the time were  $\overline{\text{RGS}}$  is low and the IC stays in the "Normal Mode with Over Temperature Prewarning".

### Deadlock Mode

This mode is intended to prevent the IC for long time toggling in Over Temperature if a short is present at the VDD pin.

There are 4 ways to enter this mode:

1. The IC is in Error Mode and a VDD Under Voltage Shut Down occurs or a VREG Under Voltage Shut Down together with a Over Temperature Prewarning occurs
2. The IC is in Normal Mode with Over Temperature Prewarning and a VDD Under Voltage Shut Down or a VREG Under Voltage Shut Down occurs.
3. The IC is in Normal Mode and a VDD Under Voltage Shut Down occurs or a VREG Under Voltage Shut Down together with a Over Temperature Prewarning occurs.
4. The IC is in VREG Shut Down Mode and a VDD Under Voltage Shut Down or a Over Temperature Prewarning occurs.

In this mode VDD and VREG are switched off. The gates of the external MOSFETs are passively clamped.

---

**Description of Modes, Protection and Diagnostic Functions**

The VDHS switch is deactivated.

The IC will not react to IFMA or  $\overline{\text{INH}}$  signals. Even a Over Temperature Shut Down detection will have no influence. The internal logic is supplied and prevents the IC from going into “Go to sleep mode”.

The only way to leave this state is that VS is lower than  $V_{\text{VSL0}}$ , means a VS Under Voltage Lockout occurs. In this case the IC goes to Sleep Mode.

### **VREG Shut Down Mode**

This mode is intended to prevent the IC for long time toggling in Over Temperature if a short is present at the VREG pin.

There are 2 ways to enter this mode:

1. The IC is in the Error Mode and a VREG Under Voltage Shut-down occurs without a Over Temperature Prewarning.
2. The IC is in the Normal Mode and a VREG Under Voltage Shut-down occurs without a Over Temperature Prewarning.

In this mode VREG is switched off, but VDD is still present. VDHS switch is still active. The PWM interface (IFMA) is working.

The IC will not react to IFMA or  $\overline{\text{INH}}$  signals.

In this situation the  $\mu\text{C}$  is still able to provide diagnostic information by the interface. It can prevent the IC from Go-to-Sleep Mode and to avoid unintended toggling as long there is no Over Temperature Shut Down.

This state can be left by 2 ways:

1. The  $\mu\text{C}$  has to set  $\overline{\text{RGS}}$  to low for a time longer than  $t_{\text{sleep}}$ . In this case the IC goes to Sleep Mode.
2. If a VDD Under Voltage Shut Down or a Over Temperature Prewarning occurs the IC will go into the Deadlock Mode.

## **9.2 Protection and Diagnosis Functions**

### **9.2.1 Over Temperature Shut Down (OTSD)**

If the junction temperature is exceeding the Over Temperature shut down level an error signal is set. The driver IC will pull- down the gate-source voltage of all external MOSFETs, deactivate the VDD and VREG supply and go directly into the Sleep Mode.

In the Sleep Mode the regular wake-up conditions will be used. Over Temperature cycling is possible and will lead to accelerated aging of the IC.

In Deadlock Mode an Over Temperature Shut Down is ignored.

### **9.2.2 Over Temperature Prewarning (OTPW)**

The IC provides a digital Over Temperature Pre-Warning. If no other errors are present, the IC goes into “Normal Mode with Over Temperature Prewarning”. This function is not available in Deadlock Mode.

### **9.2.3 Analog Temperature Monitoring**

The TEMP output of the TLE7184F provides an analog voltage signal proportional to the chip temperature. This function is not available in Deadlock Mode.

### **9.2.4 VS Under Voltage Lockout (VS\_UVLO)**

The TLE7184F has an integrated VS Under Voltage Lockout, to assure that the behavior of the complete IC is predictable in all supply voltage ranges.



If the supply voltage at VS reaches the Under Voltage shut down level  $V_{VSLO}$  for a minimum specified filter time the IC goes into Go-to-Sleep Mode and finally into Sleep Mode.

### 9.2.5 VDD Under Voltage Diagnosis (VDD\_UVD)

The TLE7184F has an integrated VDD Under Voltage Diagnosis, to assure that the behavior of the bridge driver output stages is predictable in all supply voltage ranges.

If the voltage at VDD reaches the Under Voltage diagnosis level  $V_{UVVDD}$  for a minimum specified filter time an error is set the IC goes into Error Mode.

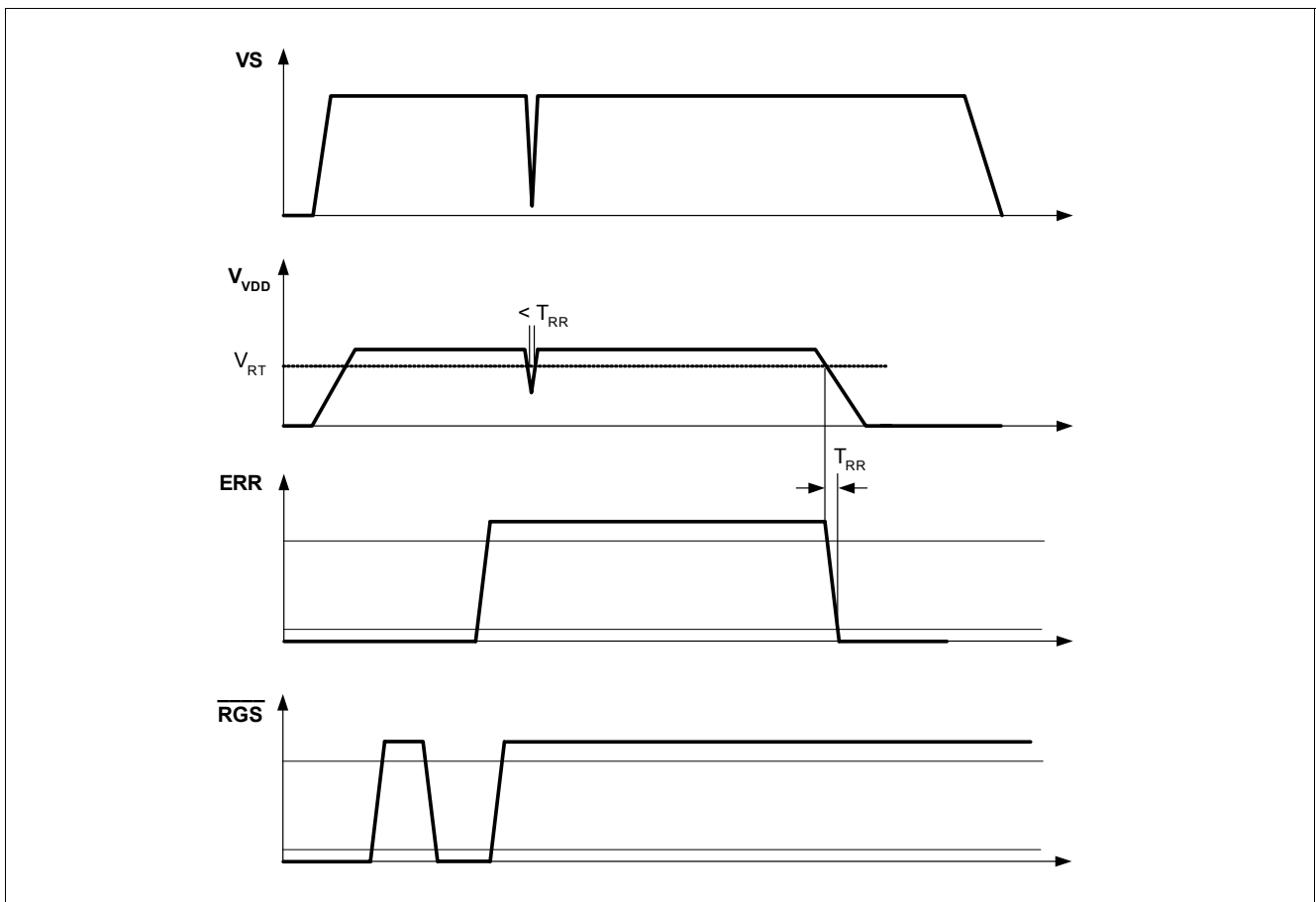


Figure 10 Timing of VDD Under Voltage Diagnosis

### 9.2.6 VDD Under Voltage Shut Down (VDD\_UVSD)

The TLE7184F has an integrated VDD Under Voltage Shut Down, to avoid operation with VDD shorted to GND.

If the supply voltage at VDD reaches the Under Voltage shut down level  $V_{VDDsleep}$ , and the wake-up time is expired, VREG and VDD will be switched off and the IC will go to the Deadlock Mode.

### 9.2.7 VREG Under Voltage Diagnosis (VREG\_UVD)

The TLE7184F has an integrated VREG Under Voltage Diagnosis, to assure that the behavior of the bridge driver output stages is predictable in all supply voltage ranges.

If the voltage at VREG reaches the Under Voltage diagnosis level  $V_{UVVR}$  for a minimum specified filter time an error is set the IC goes into Error Mode.

---

**Description of Modes, Protection and Diagnostic Functions**

As long as the VS Under Voltage Lock Out is not reached, the low side MOSFETs will stay actively switched off. The status of the high side MOSFET drivers is dependent on the bootstrap voltage - which depends on the SHx voltage. It is expected that the SHx will be pulled to VDH level by the high side MOSFETs and this will switch off the high side MOSFETs passively.

In this situation the short circuit detection of this output stage is deactivated to avoid wrong error reporting.

### 9.2.8 VREG Under Voltage Shut Down (VREG\_UVSD)

The TLE7184F has an integrated VREG Under Voltage Shut Down, to avoid operation with VREG shorted to GND. If the supply voltage at VREG reaches the Under Voltage shut down level  $V_{VRSD}$ , "AND" no Over Temperature Prewarning is set "AND" the wake up time is expired, VREG will be switched off and the IC will go to the VREG Shut Down Mode. In this condition the  $\mu\text{C}$  is still supplied and can communicate via the PWM interface (IFMA), the MOSFETs are switched off and an error is set. The only way to leave this mode is to go to Sleep Mode.

If the supply voltage at VREG reaches the Under Voltage shut down level  $V_{VRSD}$ , "AND" Over Temperature Prewarning is set and the wake-up time is expired, VREG and VDD will be switched off and the IC will go to the "Dead Lock Mode".

The only way to leave this Deadlock Mode is to provoke a VS Under Voltage Shut Down, for example by removing battery voltage.

### 9.2.9 IOV and VDH Over Voltage Shut Down (IOV\_OVSD, VDH\_OVSD)

The TLE7184F has an integrated Over Voltage shut down to minimize risk of destruction of the IC at high supply voltages caused by violation of the maximum ratings.

The voltage is observed at the Over Voltage input pin IOV and at the VDH pin. If the voltage at the IOV pin or at the VDH exceeds the Over Voltage shut down level for more than the specified filter time the IC goes into Error Mode.

The effective Over Voltage level can be adjusted by a voltage divider at IOV connected to VDHS. The Over Voltage level at VDH is fix.

### 9.2.10 Dead Time and Shoot Through Protection

In bridge applications it has to be assured that the external high side and low side MOSFETs are not "on" at the same time, connecting directly the battery voltage to GND. The dead time generated in the TLE7184F is fixed to a minimum value if the DT pin is connected to GND. This function assures a minimum dead time if a common input signal for ILx and IHx is used.

The dead time can be increased beyond the internal fixed dead time by connecting the DT pin via a dead time resistor  $R_{DT}$  to GND - the larger the dead time resistor the larger the dead time.

If an exact dead time of the bridge is needed the use of the  $\mu\text{C}$  PWM generation unit is recommended.

In case of an open DT pin, the dead time is set to the internal maximum value.

In addition to this dead time, the TLE7184F provides a locking mechanism, avoiding that both external MOSFETs of one half bridge can be switched on at the same time. This functionality is called shoot through protection.

If the command to switch on both high and low side switches in the same half bridge is given at the input pins, the command will be ignored. The outputs will stay in the situation like before the conflicting input.

### 9.2.11 Short Circuit Protection (SCP)

The TLE7184F provides a short circuit protection for the external MOSFETs. It is a monitoring of the drain-source voltage of the external MOSFETs. (see [Figure 3](#))

The drain-source voltage monitoring of the short circuit detection for a certain external MOSFET is active as soon as the corresponding driver output stage is set to "on", the dead time and the blanking time is expired.

---

**Description of Modes, Protection and Diagnostic Functions**

The blanking time starts when the dead time is expired and assures that the switch on process of the MOSFET is not taken into account. It is recommended to keep the switching times of the MOSFETs below the blanking time. The short circuit detection level is adjustable in an analogue way by the voltage setting at the SCDL pin. There is a 1:1 translation between the voltage applied to the SCDL pin and the drain-source voltage limit. E.g. to trigger the SCD circuit at 1 V drain-source voltage, the SCDL pin must be set to 1 V as well. The drain-source voltage limit can be chosen between 0.3 ... 2 V.

If after the expiration of the blanking time the drain source voltage of the observed MOSFET is still higher than the SCDL level, the SCD filter time  $t_{SCP}$  starts to run. A capacitor is charged with a current. If the capacitor voltage reaches a specific level (filter time  $t_{SCP}$ ), the error signal is set and the IC goes into Error Mode. If the SCD condition is removed before the SC is detected, the capacitor is discharged with the same current. The discharging of the capacitor happens as well when the MOSFET is switched off. It has to be considered that the high side and the low side output of one phase are working with the same capacitor.

### 9.2.12 SCDL Pin Open Detection (SCDL\_open)

For safety reasons an pull-up resistor at the SCDL pin assures that in case of an open pin the SCDL voltage is pulled to high levels. In this case an error is set and the IC goes into Error Mode.

### 9.2.13 Over Current Shut Down (OCSD)

The TLE7184F is monitoring the output signal of the operational amplifier. If the output signal reaches a specified level close to the upper rail (VDD) for a specified time, the System IC detects over current and sets an error signal. The driver output pulls down the gate-source voltage of all external MOSFETs actively and stays in the Error Mode.

### 9.2.14 VDD Current Limitation

The TLE7184F has an integrated voltage supply for an external  $\mu\text{C}$ . The output current of the supply is limited to a specified value. This limitation does not cause any error reporting. If the current is limited for a longer time, the Over Temperature protection will react.

### 9.2.15 Passive Gxx Clamping

If VS Under Voltage Lock Out is detected or the device is in Sleep Mode, a passive clamping is active as long as the voltage at VS or VDH is higher than 3V. Even below 3V it is assured that the MOSFET driver stage will not switch on the MOSFET actively.

The passive clamping means that the BHx and the VREG pin are pulled to GND with specified pull down resistors. Together with the intrinsic diode of the push stage of the output stages which connect the gate output to BHx respectively VREG, this assures that the gate of the external MOSFETs are not floating undefined.

## 9.3 $\overline{\text{ERR}}$ Pin

The TLE7184F has a status pin to provide diagnostic feedback to the  $\mu\text{C}$ . The logical output of this pin is an open drain output with integrated pull-down resistor to GND (see [Figure 11](#)).

### Reset of error registers and Disable

The TLE7184F can be reset by the enable pin  $\overline{\text{RGS}}$ . If the  $\overline{\text{RGS}}$  pin is pulled to low for a specified minimum time, the error registers are cleared. If the error is still existing when the RGS pin is pulled to low, no reset will be performed and the ERR pin stays low. The only exemption of this behavior is the Over Temperature Prewarning. Even if the junction temperature is exceeding the over temperature prewarning level, the ERR signal goes to high when  $\overline{\text{RGS}}$  is pulled low.

[Figure 12](#) describes the timing behavior during error reset:

Description of Modes, Protection and Diagnostic Functions

For more details see description of Error Mode and Normal Mode with Over Temperature Pre-Warning in [Chapter 9.1](#).

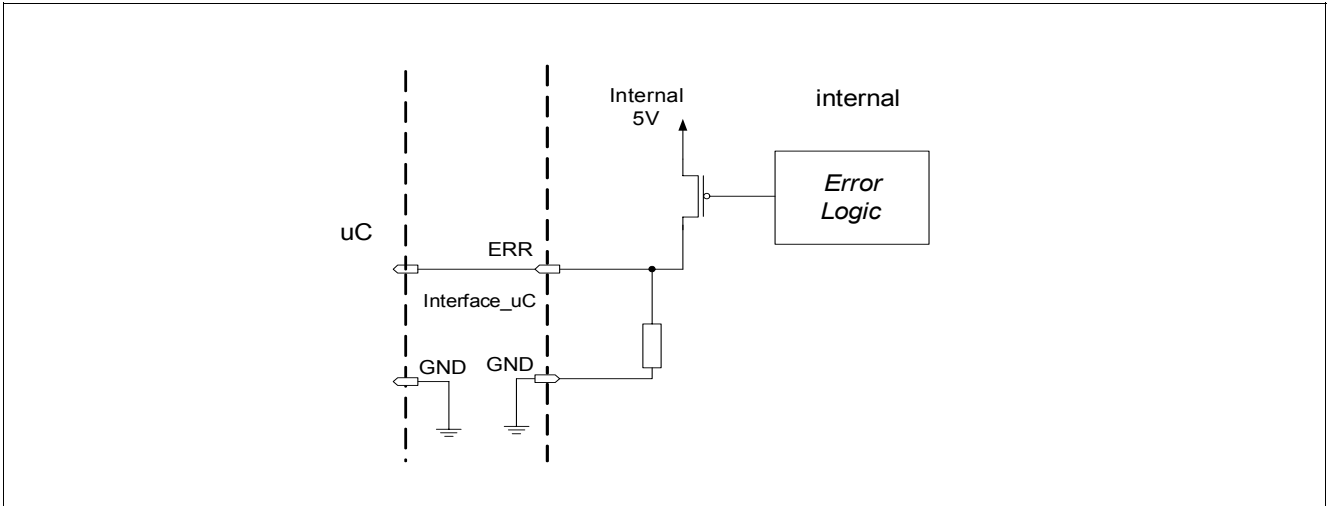


Figure 11 Structure of ERR output

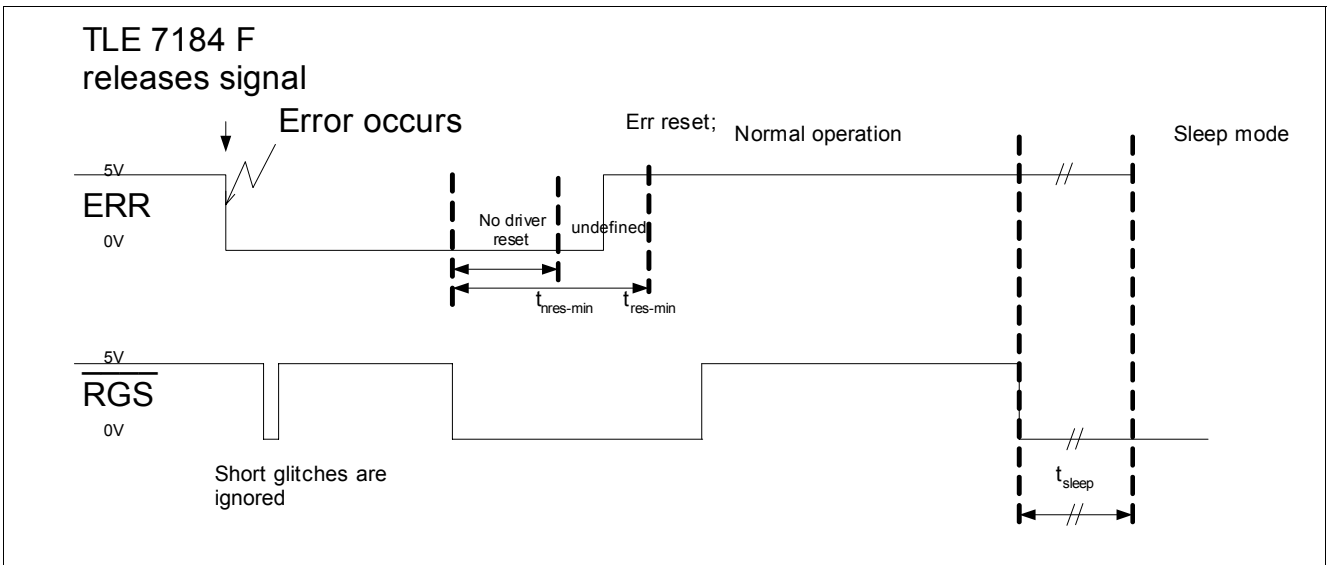


Figure 12 Enable / Disable timing

## 9.4 Electrical Characteristics

### Electrical Characteristics - Protection and diagnostic functions

$V_S = 7.0$  to  $33V$ ,  $T_j = -40$  °C to  $+150$  °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
<b>Dead time</b>							
9.4.1	Programmable internal dead time	$t_{DT}$	0.08 0.25 0.62 1.0 2.0	0.14 0.41 1.05 1.85 3.82	0.20 0.57 1.45 2.7 5.6	$\mu s$	$R_{DT}=0 \Omega$ $R_{DT}=10 k\Omega$ $R_{DT}=47 k\Omega$ $R_{DT}=100 k\Omega$ $R_{DT}=1000 k\Omega$
9.4.2	Max. internal dead time	$t_{DT\_MAX}$	2.3	–	6.4	$\mu s$	DT pin open
9.4.3	Dead time deviation between channels	$d_{IDT}$	-20	–	20	%	–
			-15	–	15	%	$R_{DT} \leq 47 k\Omega$
9.4.4	Dead time deviation between channels LSoft -> HS on	$d_{IDTH}$	-14	–	14	%	–
			-12	–	12	%	$R_{DT} \leq 47 k\Omega$
9.4.5	Dead time deviation between channels HSoft -> LS on	$d_{IDTL}$	-14	–	14	%	–
			-12	–	12	%	$R_{DT} \leq 47 k\Omega$
<b>Short circuit protection</b>							
9.4.6	Short circuit protection detection level	$V_{SCPDL}$	0.3	–	2	V	programmed by SCDL pin
9.4.7	Short circuit protection detection Accuracy	$A_{SCP}$	-30	–	+30	%	$0.3V \leq V_{SCDL} < 1.2V$
9.4.8	Short circuit protection detection Accuracy	$A_{SCP}$	-10	–	+10	%	$1.2V \leq V_{SCDL} \leq 2.0V$
9.4.9	Filter time of short circuit protection	$t_{SCP(off)}$	2.3	–	4.3	$\mu s$	Ixx static on
9.4.10	Blanking time plus filter time of short circuit detection	$t_{SCEPTT}$	4	–	8	$\mu s$	Ixx switching "off" to "on"
9.4.11	Internal pull-up resistor SCDL to $V_{DD}$	$R_{SCDL}$	180	300	420	k $\Omega$	–
9.4.12	SCDL open pin detection level	$V_{SCPOP}$	2.0	–	2.5	V	–
9.4.13	Filter time of SCDL open pin	$t_{SCPOP}$	1	–	3.4	$\mu s$	–
9.4.14	SCDL open pin detection level hysteresis	$V_{SCOPH}$	–	0.3	–	V	–
<b>Over- and Under Voltage monitoring</b>							
9.4.15	Over Voltage shut down at IOV	$V_{OVIOV}$	4.15	–	4.4	V	IOV voltage increasing
9.4.16	Pull down resistor at IOV to GND	$R_{IOV}$	300	–	700	k $\Omega$	–
9.4.17	Over Voltage shut down at VDH	$V_{OVVDH}$	33	–	37	V	VDH increasing
9.4.18	Over Voltage shut down filter time for IOV or VDH	$t_{OV}$	13	–	23	$\mu s$	–
9.4.19	Under Voltage diagnosis at VREG	$V_{UVVR}$	5.5	–	6.5	V	VREG decreasing

**Description of Modes, Protection and Diagnostic Functions**
**Electrical Characteristics - Protection and diagnostic functions (cont'd)**

$V_S = 7.0$  to  $33V$ ,  $T_j = -40$  °C to  $+150$  °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
9.4.20	Under Voltage diagnosis filter time for VREG	$t_{UVVR}$	10	–	30	µs	–
9.4.21	Under Voltage shut down at VREG	$V_{VRSD}$	1.5	–	2.3	V	VREG decreasing
9.4.22	Under Voltage lockout at VS	$V_{VSLO}$	4.4	5.0	5.5	V	$V_{VS}$ decreasing
9.4.23	Under Voltage lockout filter time for VS	$t_{UVLO}$	1	–	3	µs	–

**ERR pin<sup>1)</sup>**

9.4.24	ERR output voltage	$V_{ERR}$	4.4	–	–	V	No external load
9.4.25	Rise time ERR (20 - 80% of internal 5V)	$t_{f(ERR)}$	–	–	3	µs	$C_{LOAD}=1nF$ ;
9.4.26	Internal pull-down resistor ERR to GND	$R_{f(ERR)}$	25	–	52	kΩ	–

**Reset and Enable**

9.4.27	Low time of uC RGS signal without reset	$t_{nres}$	–	–	0.5	µs	–
9.4.28	Low time of uC RGS pin necessary to trigger reset and to clear error registers	$t_{res}$	3	–	–	µs	–

**Wake-up and go-to-sleep**

9.4.29	Low level input voltage of RGS	$V_{RGSLL}$	–	–	1.6	V	–
9.4.30	High level input voltage of RGS	$V_{RGSHL}$	2.8	–	–	V	–
9.4.31	Input hysteresis of RGS <sup>2)</sup>	$d_{RGS}$	100	–	–	mV	–
9.4.32	RGS pull-down resistors to GND	$R_{RGS}$	100	–	210	kΩ	–
9.4.33	Low level input voltage of $\overline{INH}$ <sup>3)</sup> for wake up	$V_{INHL}$	–	–	0.75	V	–
9.4.34	High level input voltage of $\overline{INH}$ <sup>3)</sup> for wake up	$V_{INHH}$	2.1	–	–	V	–
9.4.35	$\overline{INH}$ pull-down resistors to GND	$R_{INH}$	100	–	210	kΩ	–
9.4.36	Wake up delay time	$t_{wake}$	9	–	17	ms	–
9.4.37	RGS low time for go-to-sleep	$t_{sleep}$	20	–	50	µs	–
9.4.38	$V_{DD}$ voltage for changing from Go-to-Sleep Mode to Sleep Mode	$V_{DDsleep}$	1.5	–	2.3	V	–
9.4.39	$V_{DD}$ Under Voltage Shut Down	$V_{UVSDVDD}$	1.5	–	2.3	V	–

1) ERR pin and Reset & Enable functional between  $V_{VS}=6 \dots 7V$ , but characteristics might be out of specified range

2) Not subject to production test; specified by design

3) These levels are valid for wake up of the IC. The input levels for  $\overline{INH}$  deciding the output state of  $\overline{INH}$  are shown in [Chapter 8.4](#)

**Description of Modes, Protection and Diagnostic Functions**
**Electrical Characteristics - Protection and diagnostic functions**

$V_S = 6.0$  to  $33V$ ,  $T_j = -40$  °C to  $+150$  °C, all voltages with respect to ground, positive current flowing into pin (unless otherwise specified)

Pos.	Parameter	Symbol	Limit Values			Unit	Conditions
			Min.	Typ.	Max.		
<b>Temperature monitoring</b>							
9.4.40	Over Temperature shut down	$T_{j(SD)}$	160	170	180	°C	<sup>1)</sup> –
9.4.41	Over Temperature pre-warning	$T_{j(PW)}$	130	140	150	°C	<sup>1)</sup> –
9.4.42	Difference between Over Temperature shut down level and Over Temperature pre-Warning level	$d_{Tj(SDPW)}$	20	30	40	°C	<sup>1)</sup> –
9.4.43	Analog temperature output at 25°C	$V_{ATRT}$	1.15	–	1.8	V	$C_{load} \leq 1.5nF$ ; $T_j = 25^\circ C$
9.4.44	Analog temperature output coefficient	$K_{ATRT}$	4.57	–	5.20	mV/K	$C_{load} \leq 1.5nF$ 1)
9.4.45	Analog temperature output drift over lifetime <sup>1)</sup>	$V_{ATRTd}$	0	–	+6	mV	$C_{load} \leq 1.5nF$
9.4.46	Analog temperature range <sup>1)</sup>	$T_{AT}$	-40	–	175	°C	–
<b>Over current detection</b>							
9.4.47	Over current detection level in% of $V_{VDD}$	$V_{OCTH}$	92	–	96.5	%	–
9.4.48	Filter time for over current detection	$t_{OC}$	1.8	–	4.2	µs	–
<b>Under Voltage monitoring VDD</b>							
9.4.49	Under Voltage shut down at $V_{DD}$ <sup>2)</sup>	$V_{UVVDD}$	3.7	–	4.2	V	$V_{VDD}$ decreasing
9.4.50	Under Voltage shut down filter time	$t_{UVVDD}$	15	–	45	µs	–

1) Not subject to production test; specified by design

2) For Under Voltage detection level during go-to-sleep see  $V_{DDsleep}$

## 10 Application Description

In the automotive sector there are more and more applications requiring high performance motor drives, such as HVAC fans, engine cooling fans, pumps etc.. In these applications 3 phase motors, synchronous and asynchronous, are used, combining high output performance, low space requirements and high reliability.

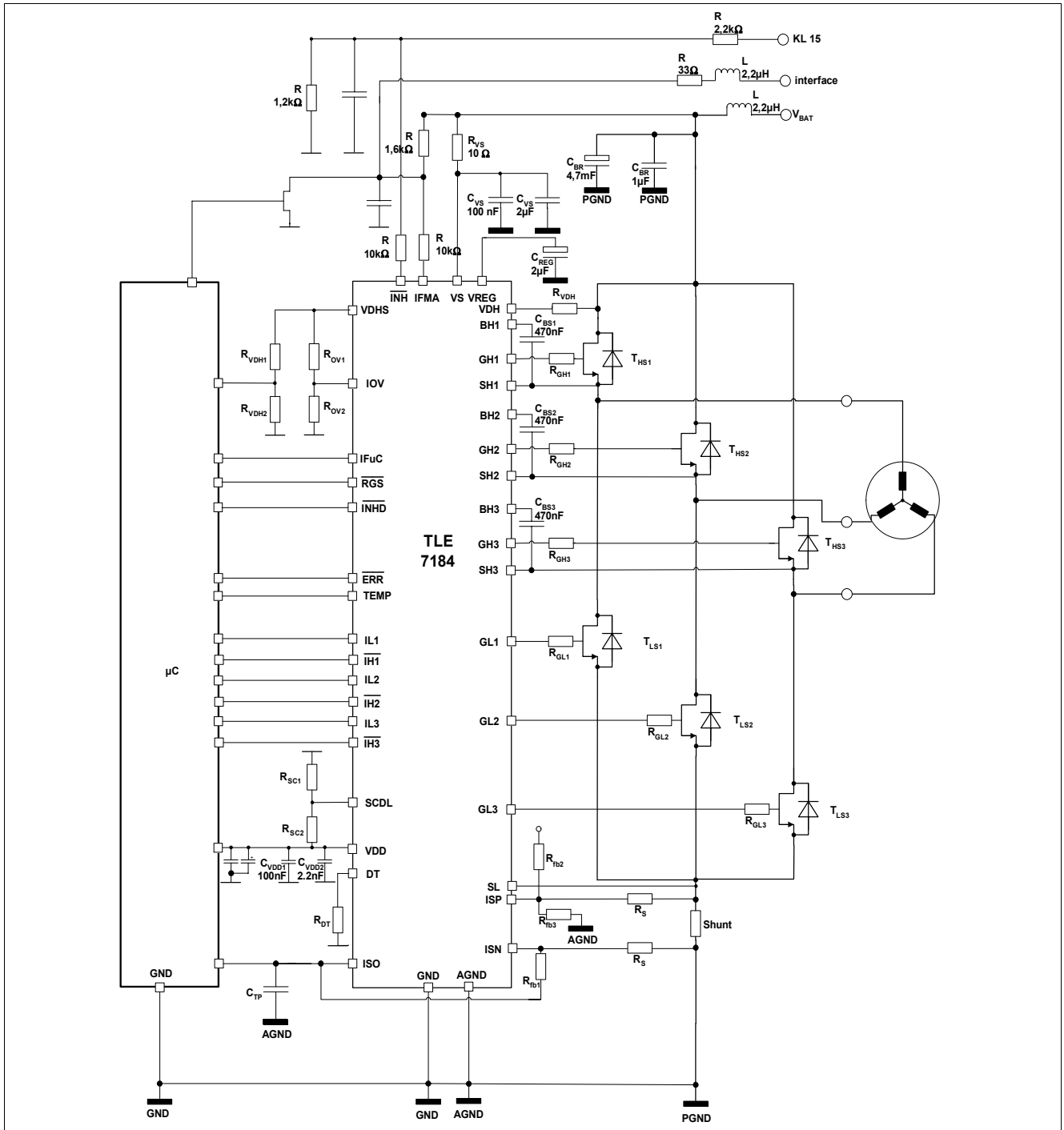


Figure 13 Application Circuit TLE7184F

Note: This is a simplified example of an application circuit. The function must be verified in the real application



## 11 Package Outlines

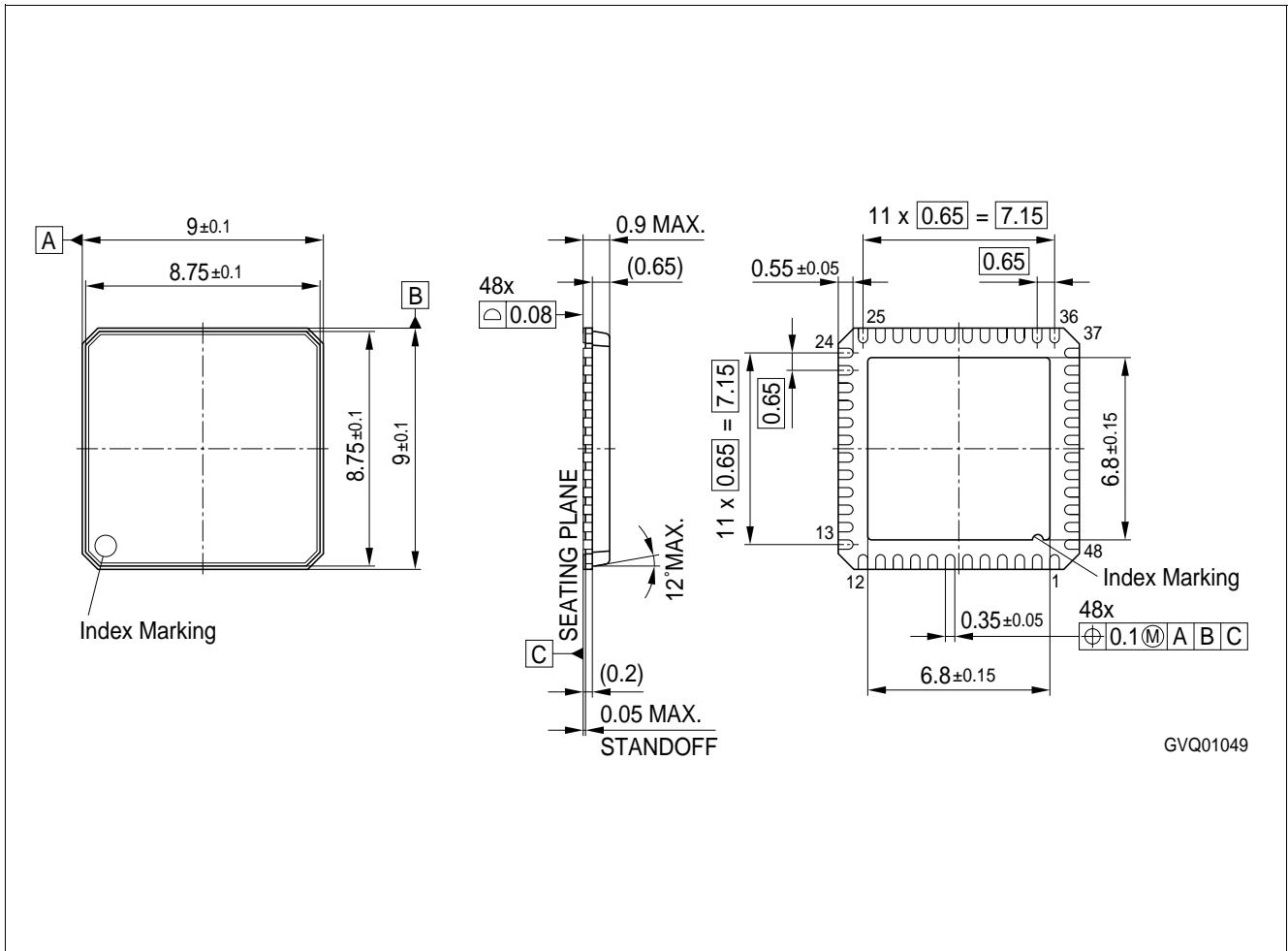


Figure 14 PG-VQFN-48

### Green Product (RoHS compliant)

To meet the world-wide customer requirements for environmentally friendly products and to be compliant with government regulations the device is available as a green product. Green products are RoHS-Compliant (i.e. Pb-free finish on leads and suitable for Pb-free soldering according to IPC/JEDEC J-STD-020).

## 12 Revision History

Revision	Date	Changes
Rev.1.0	2008-12-04	<ul style="list-style-type: none"><li>- Test conditions of bias current into BHx modified</li><li>- Current between BHx and SHx adapted</li><li>- IFMA internal pull-up resistor to VS modified</li><li>- Matching of internal pull-up / pulldown resistor expanded</li><li>- Filter time of short circuit protection test conditions improved</li><li>- Blanking time plus filter time of short circuit detection test conditions added</li><li>- Filter time for over current detection expanded</li></ul>

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