

**RADIATION HARDENED
 LOGIC LEVEL POWER MOSFET
 THRU-HOLE (MO-036AB)**

**2N7612M1
 IRHLG77110
 100V, Quad N-CHANNEL
 TECHNOLOGY**



Product Summary

Part Number	Radiation Level	RDS(on)	ID
IRHLG77110	100K Rads (Si)	0.22Ω	1.8A
IRHLG73110	300K Rads (Si)	0.22Ω	1.8A



International Rectifier's R7™ Logic Level Power MOSFETs provide simple solution to interfacing CMOS and TTL control circuits to power devices in space and other radiation environments. The threshold voltage remains within acceptable operating limits over the full operating temperature and post radiation. This is achieved while maintaining single event gate rupture and single event burnout immunity.

These devices are used in applications such as current boost low signal source in PWM, voltage comparator and operational amplifiers.

Features:

- 5V CMOS and TTL Compatible
- Fast Switching
- Single Event Effect (SEE) Hardened
- Low Total Gate Charge
- Simple Drive Requirements
- Ease of Paralleling
- Hermetically Sealed
- Light Weight

Absolute Maximum Ratings

Pre-Irradiation

	Parameter		Units
ID @ VGS = 4.5V, TC=25°C	Continuous Drain Current	1.8	A
ID @ VGS = 4.5V, TC=100°C	Continuous Drain Current	1.1	
IDM	Pulsed Drain Current ①	7.2	
PD @ TC = 25°C	Max. Power Dissipation	1.4	W
	Linear Derating Factor	0.01	W/°C
VGS	Gate-to-Source Voltage	±10	V
EAS	Single Pulse Avalanche Energy ②	97	mJ
IAR	Avalanche Current ①	1.8	A
EAR	Repetitive Avalanche Energy ①	0.14	mJ
dv/dt	Peak Diode Recovery dv/dt ③	11	V/ns
TJ	Operating Junction	-55 to 150	°C
TSTG	Storage Temperature Range		
	Lead Temperature	300 (0.063in/1.6mm from case for 10s)	
	Weight	1.3 (Typical)	g

For footnotes refer to the last page

Electrical Characteristics For Each N-Channel Device @ T_J = 25°C (Unless Otherwise specified)

	Parameter	Min	Typ	Max	Units	Test Conditions
B _V DSS	Drain-to-Source Breakdown Voltage	100	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔB _V DSS/ΔT _J	Temperature Coefficient of Breakdown Voltage	—	0.11	—	V/°C	Reference to 25°C, I _D = 1.0mA
R _{DS(on)}	Static Drain-to-Source On-State Resistance	—	—	0.22	Ω	V _{GS} = 4.5V, I _D = 1.1A ④
V _{GS(th)}	Gate Threshold Voltage	1.0	—	2.0	V	V _{DS} = V _{GS} , I _D = 250μA
ΔV _{GS(th)} /ΔT _J	Gate Threshold Voltage Coefficient	—	-4.4	—	mV/°C	
g _{fs}	Forward Transconductance	3.0	—	—	S	V _{DS} = 10V, I _{DS} = 1.1A ④
I _{DSS}	Zero Gate Voltage Drain Current	—	—	1.0	μA	V _{DS} = 80V, V _{GS} = 0V
		—	—	10		V _{DS} = 80V, V _{GS} = 0V, T _J = 125°C
I _{GSS}	Gate-to-Source Leakage Forward	—	—	100	nA	V _{GS} = 10V
I _{GSS}	Gate-to-Source Leakage Reverse	—	—	-100		V _{GS} = -10V
Q _g	Total Gate Charge	—	—	15	nC	V _{GS} = 4.5V, I _D = 1.8A
Q _{gs}	Gate-to-Source Charge	—	—	2.5		V _{DS} = 50V
Q _{gd}	Gate-to-Drain ('Miller') Charge	—	—	6.0		
t _{d(on)}	Turn-On Delay Time	—	—	15	ns	V _{DD} = 50V, I _D = 1.8A, V _{GS} = 4.5V, R _G = 7.5Ω
t _r	Rise Time	—	—	20		
t _{d(off)}	Turn-Off Delay Time	—	—	65		
t _f	Fall Time	—	—	25		
L _S + L _D	Total Inductance	—	10	—	nH	Measured from Drain lead (6mm /0.25in from pack.) to Source lead (6mm/0.25in from pack.) with Source wire internally bonded from Source pin to Drain pad
C _{iss}	Input Capacitance	—	653	—	pF	V _{GS} = 0V, V _{DS} = 25V f = 1.0MHz
C _{oss}	Output Capacitance	—	119	—		
C _{rss}	Reverse Transfer Capacitance	—	2.7	—		
R _g	Gate Resistance	—	16	—	Ω	f = 1.0MHz, open drain

Source-Drain Diode Ratings and Characteristics (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
I _S	Continuous Source Current (Body Diode)	—	—	1.8	A	T _J = 25°C, I _S = 1.8A, V _{GS} = 0V ④
I _{SM}	Pulse Source Current (Body Diode) ①	—	—	7.2		
V _{SD}	Diode Forward Voltage	—	—	1.2	V	T _J = 25°C, I _F = 1.8A, di/dt ≤ 100A/μs
t _{rr}	Reverse Recovery Time	—	—	100	ns	V _{DD} ≤ 25V ④
Q _{RR}	Reverse Recovery Charge	—	—	223	nC	
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible. Turn-on speed is substantially controlled by L _S + L _D .				

Thermal Resistance (Per Die)

	Parameter	Min	Typ	Max	Units	Test Conditions
R _{thJA}	Junction-to-Ambient	—	—	90	°C/W	Typical socket mount

Note: Corresponding Spice and Saber models are available on International Rectifier Web site.

For footnotes refer to the last page

Radiation Characteristics

IRHLG77110, 2N7612M1

International Rectifier Radiation Hardened MOSFETs are tested to verify their radiation hardness capability. The hardness assurance program at International Rectifier is comprised of two radiation environments. Every manufacturing lot is tested for total ionizing dose (per notes 5 and 6) using the TO-39 package. Both pre- and post-irradiation performance are tested and specified using the same drive circuitry and test conditions in order to provide a direct comparison.

Table 1. Electrical Characteristics @ Tj = 25°C, Post Total Dose Irradiation ⑤⑥ (Per Die)

	Parameter	Up to 300K Rads (Si) ¹		Units	Test Conditions
		Min	Max		
BV _{DSS}	Drain-to-Source Breakdown Voltage	100	—	V	V _{GS} = 0V, I _D = 250μA
V _{GS(th)}	Gate Threshold Voltage	1.0	2.0		V _{GS} = V _{DS} , I _D = 250μA
I _{GSS}	Gate-to-Source Leakage Forward	—	100	nA	V _{GS} = 10V
I _{GSS}	Gate-to-Source Leakage Reverse	—	-100		V _{GS} = -10V
I _{DSS}	Zero Gate Voltage Drain Current	—	10	μA	V _{DS} = 80V, V _{GS} = 0V
R _{DS(on)}	Static Drain-to-Source On-State Resistance (TO-39) ④	—	0.25	Ω	V _{GS} = 4.5V, I _D = 1.1A
R _{DS(on)}	Static Drain-to-Source On-state Resistance (MO-036AB) ④	—	0.22	Ω	V _{GS} = 4.5V, I _D = 1.1A
V _{SD}	Diode Forward Voltage ④	—	1.2	V	V _{GS} = 0V, I _D = 1.8A

1. Part numbers IRHLG77110, IRHLG73110

International Rectifier radiation hardened MOSFETs have been characterized in heavy ion environment for Single Event Effects (SEE). Single Event Effects characterization is illustrated in Fig. a and Table 2.

Table 2. Typical Single Event Effect Safe Operating Area (Per Die)

Ion	LET (MeV/(mg/cm ²))	Energy (MeV)	Range (μm)	VDS (V)							
				@VGS= 0V	@VGS= -1V	@VGS= -2V	@VGS= -4V	@VGS= -5V	@VGS= -6V	@VGS= -7V	@VGS= -8V
Br	37	305	39	100	100	100	100	100	100	100	100
I	60	370	34	100	100	100	100	100	100	-	-
Au	84	390	30	100	100	100	100	100	-	-	-

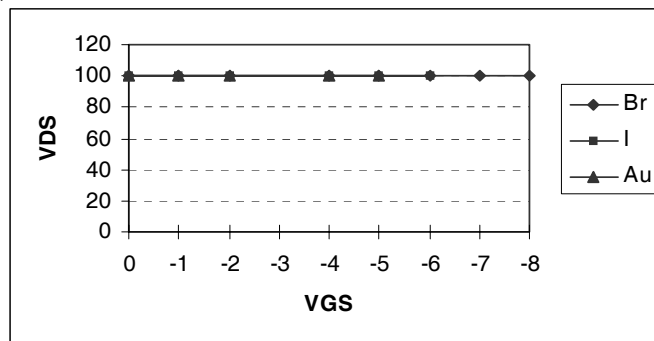


Fig a. Typical Single Event Effect, Safe Operating Area

For footnotes refer to the last page

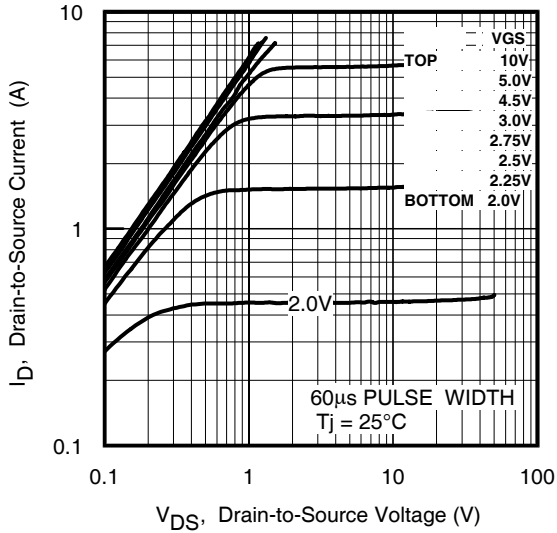


Fig 1. Typical Output Characteristics

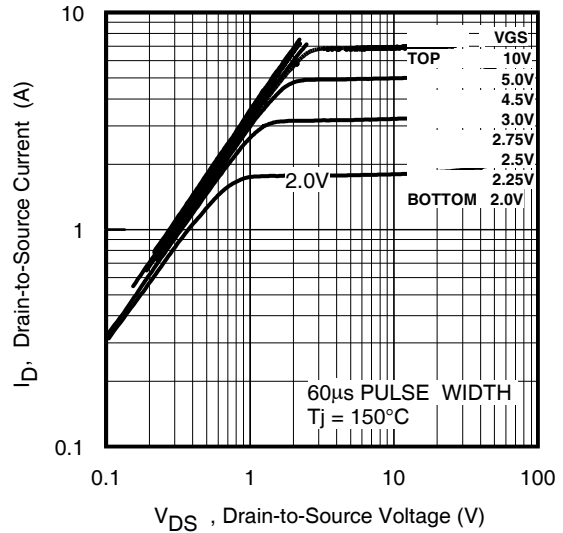


Fig 2. Typical Output Characteristics

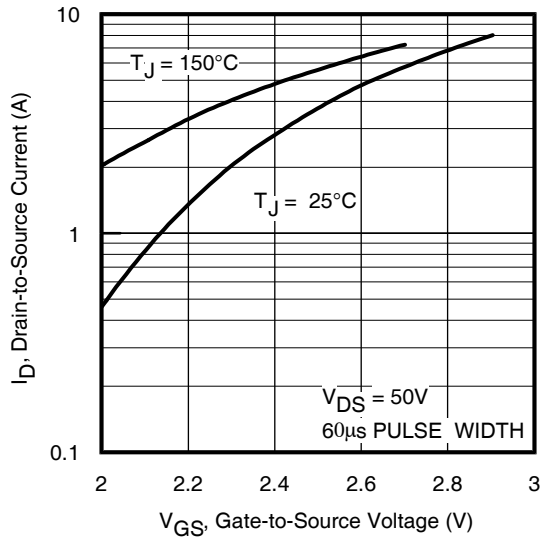


Fig 3. Typical Transfer Characteristics

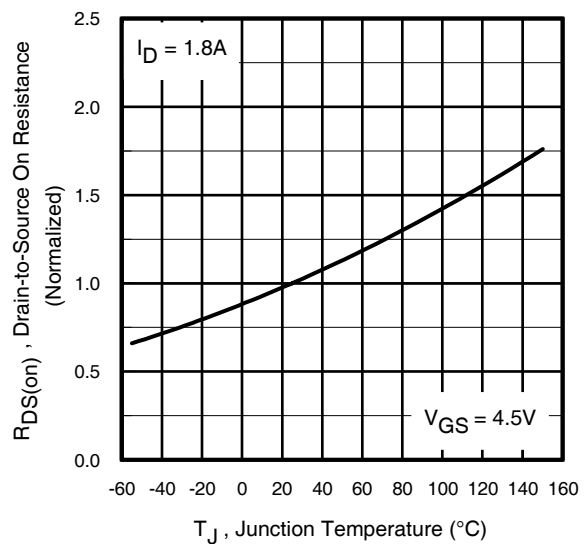


Fig 4. Normalized On-Resistance Vs. Temperature

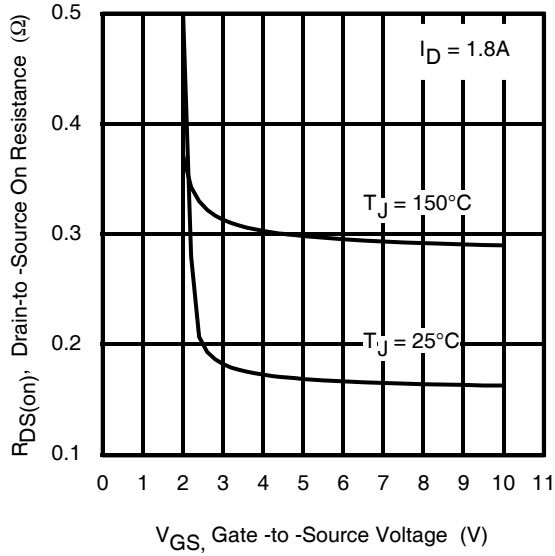


Fig 5. Typical On-Resistance Vs Gate Voltage

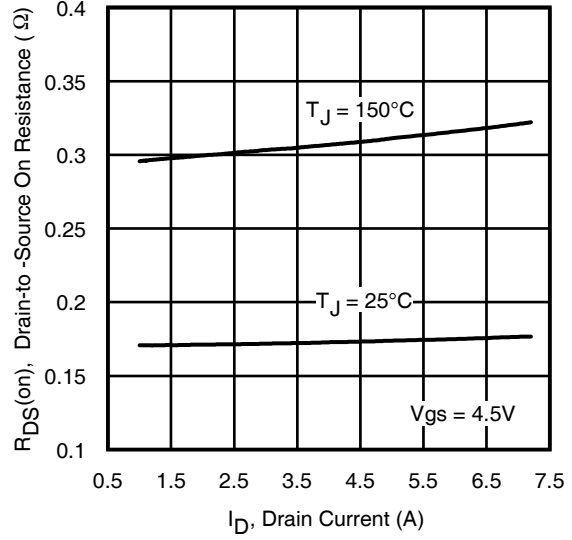


Fig 6. Typical On-Resistance Vs Drain Current

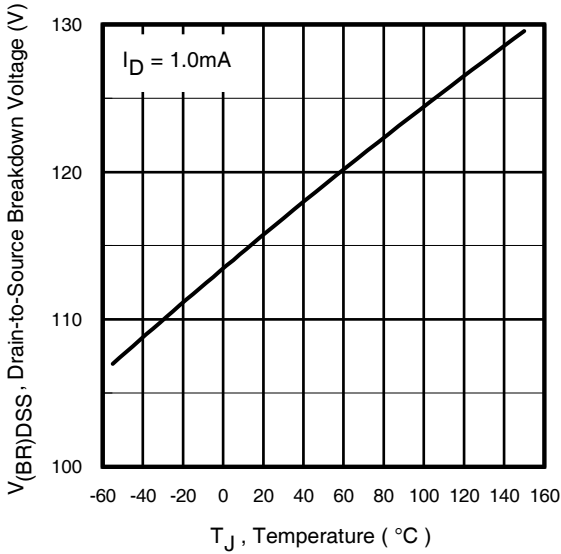


Fig 7. Typical Drain-to-Source Breakdown Voltage Vs Temperature

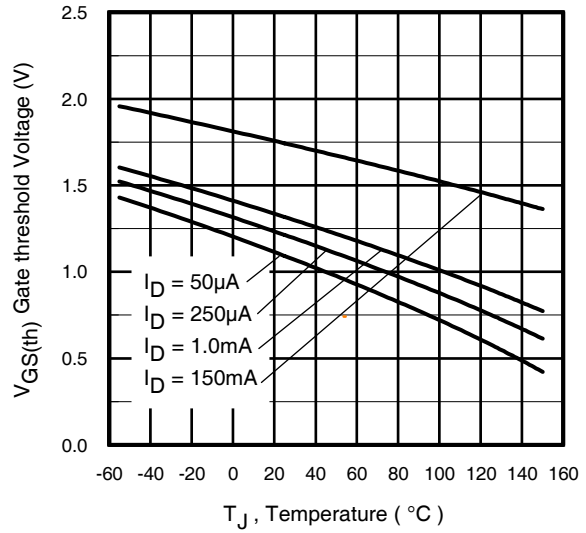


Fig 8. Typical Threshold Voltage Vs Temperature

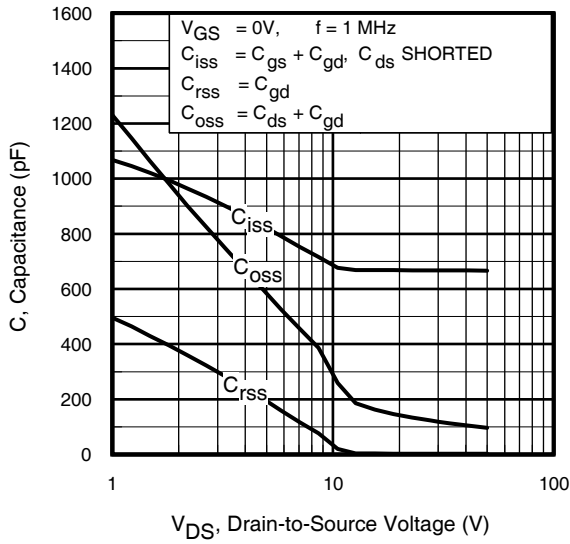


Fig 9. Typical Capacitance Vs. Drain-to-Source Voltage

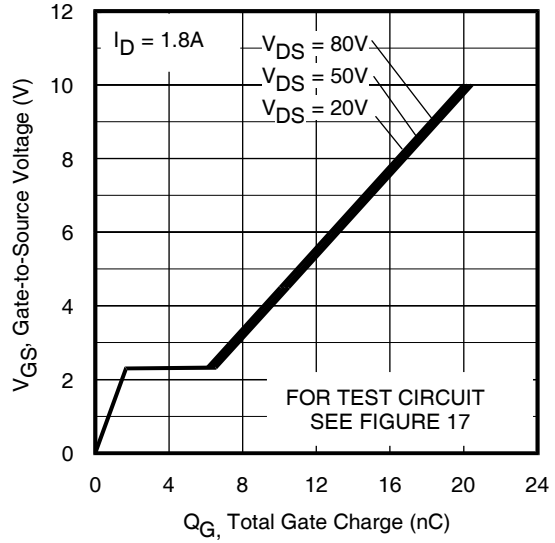


Fig 10. Typical Gate Charge Vs. Gate-to-Source Voltage

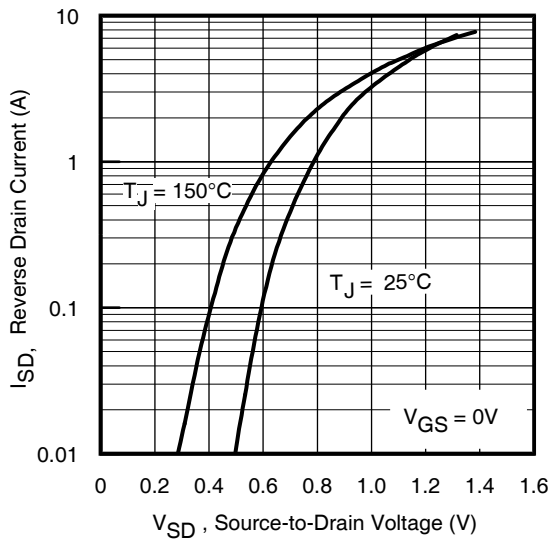


Fig 11. Typical Source-to-Drain Diode Forward Voltage

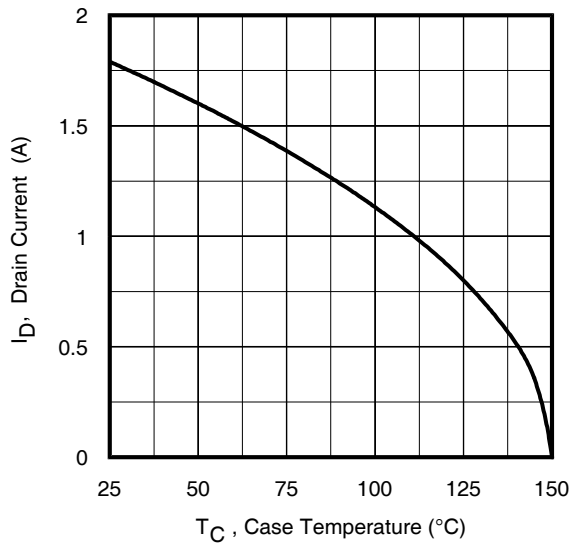


Fig 12. Maximum Drain Current Vs. Case Temperature

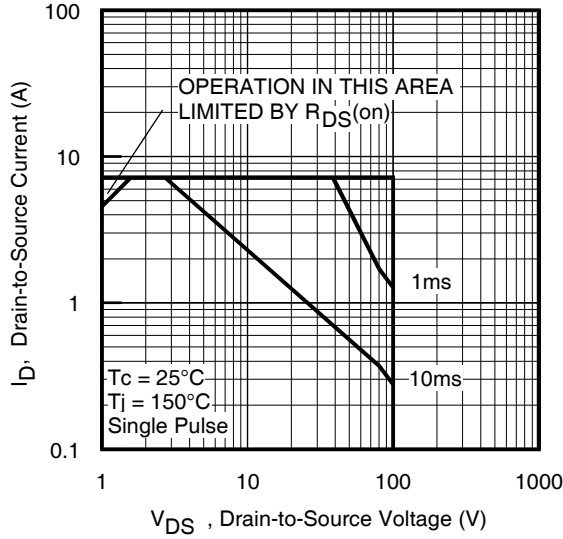


Fig 13. Maximum Safe Operating Area

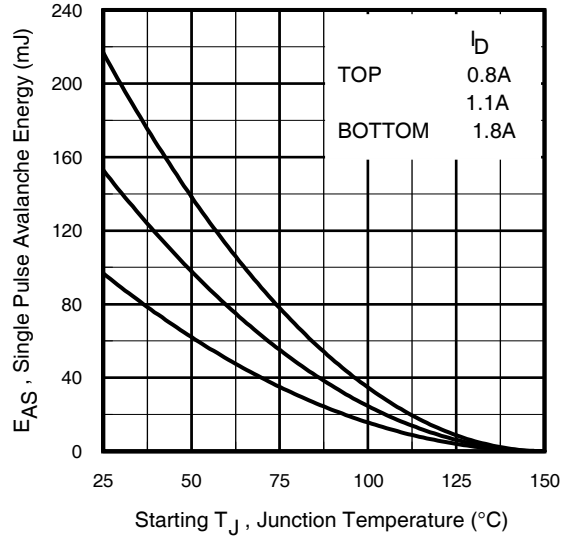


Fig 14. Maximum Avalanche Energy Vs. Drain Current

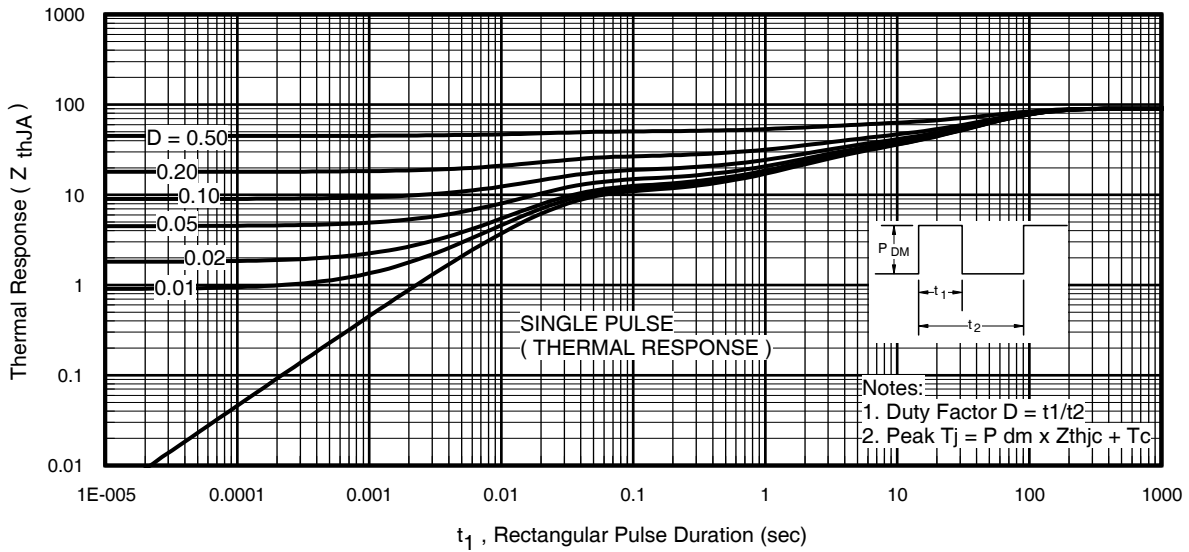


Fig 15. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

IRHLG77110, 2N7612M1

Pre-Irradiation

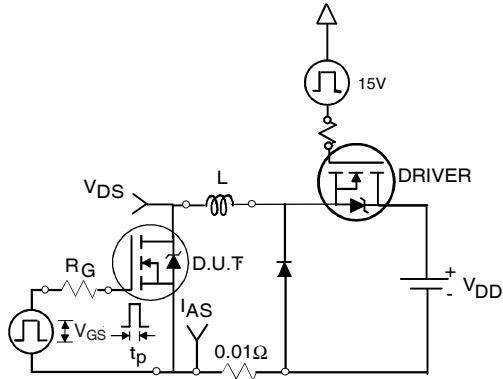


Fig 16a. Unclamped Inductive Test Circuit

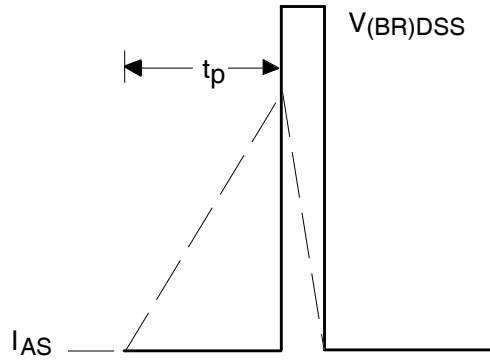


Fig 16b. Unclamped Inductive Waveforms

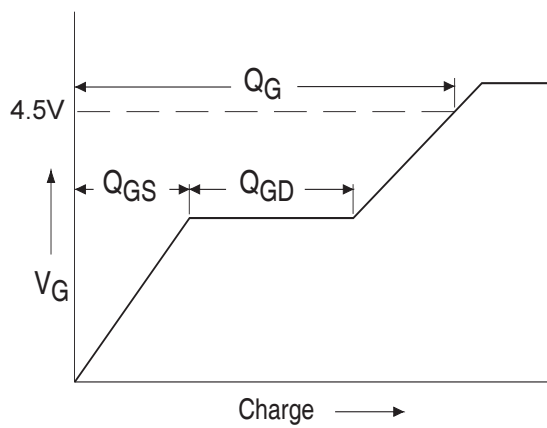


Fig 17a. Basic Gate Charge Waveform

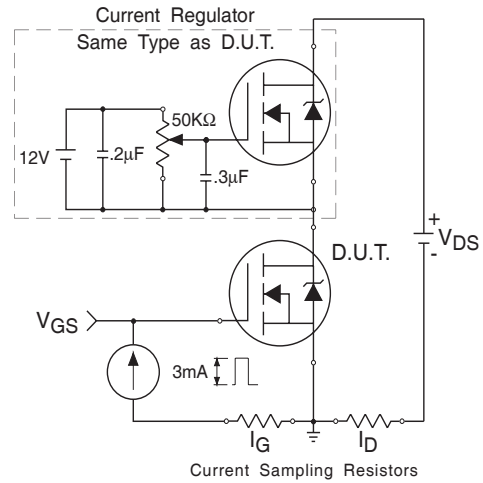


Fig 17b. Gate Charge Test Circuit

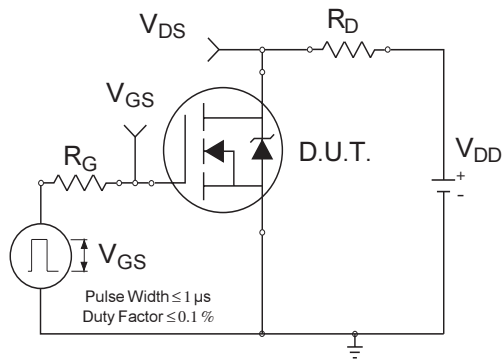


Fig 18a. Switching Time Test Circuit

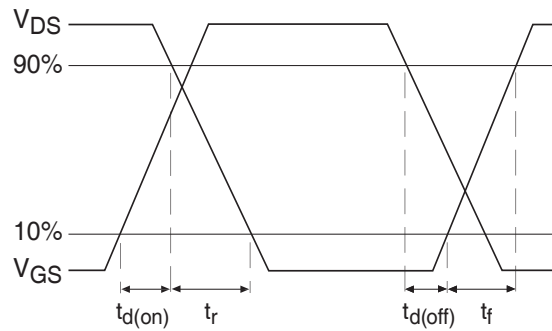
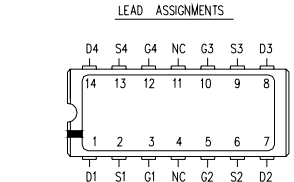
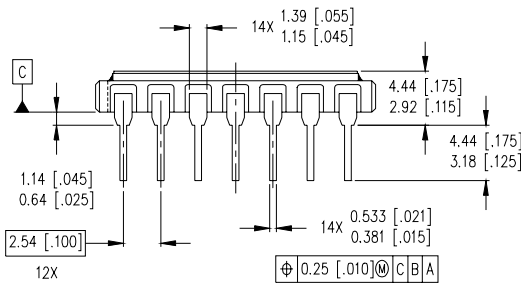
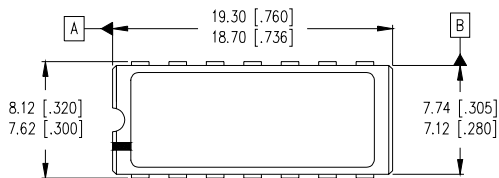


Fig 18b. Switching Time Waveforms

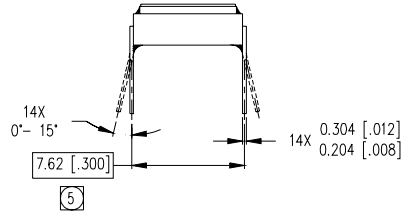
Footnotes:

- ① Repetitive Rating; Pulse width limited by maximum junction temperature.
- ② $V_{DD} = 25V$, starting $T_J = 25^\circ C$, $L = 6.6mH$
Peak $I_L = 1.8A$, $V_{GS} = 10V$
- ③ $I_{SD} \leq 1.8A$, $di/dt \leq 497A/\mu s$,
 $V_{DD} \leq 100V$, $T_J \leq 150^\circ C$
- ④ Pulse width $\leq 300 \mu s$; Duty Cycle $\leq 2\%$
- ⑤ **Total Dose Irradiation with V_{GS} Bias.**
10 volt V_{GS} applied and $V_{DS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.
- ⑥ **Total Dose Irradiation with V_{DS} Bias.**
80 volt V_{DS} applied and $V_{GS} = 0$ during irradiation per MIL-STD-750, method 1019, condition A.

Case Outline and Dimensions — MO-036AB



LEGEND
 G = GATE S = SOURCE
 D = DRAIN NC = NO CONNECTION



- NOTES:
- 1. DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
 - 2. CONTROLLING DIMENSION: INCH.
 - 3. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
 - 4. OUTLINE CONFORMS TO JEDEC OUTLINE MO-036AB.
 - ⑤ MEASURED WITH THE LEADS CONSTRAINED TO BE PERPENDICULAR TO DATUM PLANE C.

International
IR Rectifier

IR WORLD HEADQUARTERS: 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105
IR LEOMINSTER : 205 Crawford St., Leominster, Massachusetts 01453, USA Tel: (978) 534-5776
 TAC Fax: (310) 252-7903

Visit us at www.irf.com for sales contact information.
 Data and specifications subject to change without notice. 03/2008