August 1994

INTEGRATED INFORMATION TECHNOLOGY INC

IIT VCP

Single Chip Video Codec and Multimedia Communications Processor

OVERVIEW

The IIT VCP is a single-chip programmable video codec and multimedia communications processor. The VCP requires only memory and interface circuits for implementation of a complete multimedia and conferencing subsystem.

The VCP performs a super-set of the functions of IIT's Vision Controller and Vision Processor chips. For video conferencing applications it can act as a full CIF resolution H.261 codec and provide forward error correction and bitstream multiplexing to the H.221 and H.242 standards. For video playback applications the VCP can decode the MPEG system protocol and decode both MPEG 1 and MPEG 2 standard video. In addition to multiplexing and codec functions, the VCP provides programmable video pre- and post-processing functions including video scaling, temporal filtering, output interpolation, color conversion and picture-in-picture.

Figure 1 shows a block diagram of a typical VCP system. It has separate digital video buses, one for input and one for output. The buses interface directly to available TV capture and display chipsets. The VCP uses a DRAM frame buffer to store the uncompressed and reference images. Internally the VCP uses a programmable video signal processor core based on the IIT Vision Processor (VP) chip to compress and decompress the video. The microcode for the VP core is stored in on-chip ROM and RAM. Audio is processed externally and passed directly to the VCP through a serial Audio bus. Internally the VCP contains a RISC microprocessor which supervises the video codec. The RISC also supervises a hardware engine which performs error correction on the compressed data, multiplexes the compressed audio and video data, and parses the bitstream protocol. The program, data and stack memory for the RISC is provided by external SRAM which also provides delay equalization FIFOs for H.221. The RISC boots from an on-chip ROM. The compressed audio/video bitstream is transferred over the parallel Host bus or the serial bitstream TDM (Time Division Multiplexed) bus.

FEATURES

- H.261, MPEG1 codec, MPEG2 decode
- Proprietary compression standards
- H.221, H.242 and BCH up to 6 B channels
- MPEG1/2 audio/video system decode
- MPEG1/2 audio/video system encode
- Real-time video scaling to arbitrary size
- Supports IIT VCI Applications Interface
- Glue-less audio DSP interface
- MVIP, IOM2 and CHI bus interface
- Separate video in and out buses

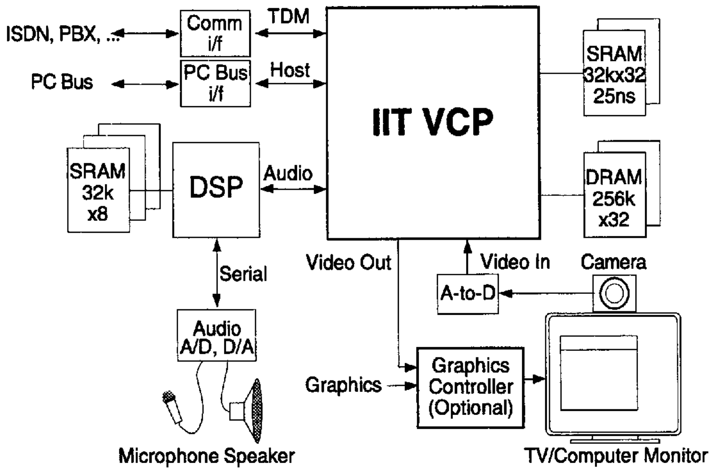

Figure 1 VCP System

2445 Mission College Boulevard, Santa Clara, California 95054. Telephone (408) 727-1885. Fax (408) 980-0432

COPYRIGHT NOTICE

TRADEMARK ACKNOWLEDGMENT

Integrated Information Technology, IIT, Vision Processor, Vision Controller, VCP, MPP, MEP, LVP and VPIC are registered trademarks of Integrated Information Technology, Inc.

JPEG is the Joint Photographic Experts Group of the ISO/IEC. References to "JPEG" in this document refer to ISO/IEC Draft International Standard 10918-1 dated 12th Feb 1992.

MPEG is the Moving Picture Experts Group of the ISO/IEC. References to "MPEG" in this document refer to the ISO/IEC JTC1 SC29 committee draft ISO 11172 dated 9th Jan 1992.

H.261 refers to the International Standard described in recommendation H.261 of the CCITT Working Party 15-1.

All other trademarks are trademarks of their respective companies and are used to identification purposes only.

DISCLAIMER

Integrated Information Technology, Inc. makes no representations or warranties regarding the content of this technical specification. This information is preliminary and is subject to change at any time without notice. Integrated Information Technology, Inc. assumes no responsibility for any errors contained herein.

Products in this document may be covered by IIT patent number 5,379,351. Additional patents are pending.

The customer should notice that in the field of personal computer systems and graphics there are a number of patents held by various parties. It is the responsibility of the user to assure that a particular implementation does not infringe on those patents.

CONTENTS

Figures

Tables

INTRODUCTION

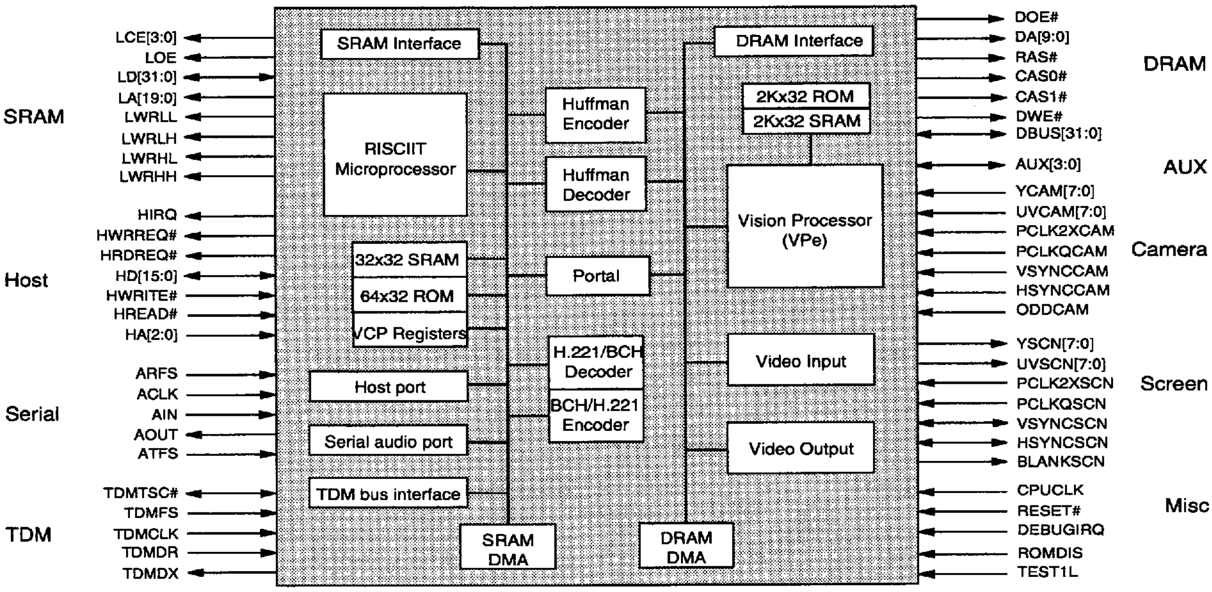

Figure 2. VCP Block Diagram

INTRODUCTION

Figure 2 shows the internal architecture of the VCP. Both the internal buses of the chip and the external interfaces can be divided into two groups, one handling uncompressed and intermediate data and the other handling compressed data. The Video In and Video Out buses allow uncompressed data in and out of the chip. The Host Bus, TDM Bus and Audio Interface all transfer compressed information, either audio or video or both. Internally there are two major data paths in the chip; the DRAM bus handles uncompressed data or intermediate data which is in the process of being compressed or decompressed. The SRAM Bus handles compressed data and RISC instructions and data.

Passage of data through the system is controlled by the two DMA controllers (SRAM and DRAM) associated with the internal buses. These run under the supervision of the RISC processor.

The architecture of the VCP is a super-set of that of the VC and VP chips; it provides more flexible video processing capabilities, more general data transfer options between DRAM and SRAM, additional BCH and H.221 functions and superior compressed data interfaces. The following sections describe the functional blocks in more detail.

RISC MICROCONTROLLER

The VCP RISC is a faster, enhanced version of that used in the VC chip. As in the VC it is a 32-bit instruction, 32-bit data pipelined RISC microprocessor. In addition to being clocked at least four times faster than the VC RISC, it adds a number of instructions which speed up byte and word accesses and has improved interrupt processing capabilities. The VCP RISC does not have an instruction cache; rather it has a full 32-bit interface to external SRAM which improves code access time by a factor of two. Unlike the VC, the VCP does not require an external boot ROM for power-up initialization; the VCP RISC boot ROM is on-chip. The VCP RISC also has a small amount of on-chip SRAM in which it can keep commonly used data; access to this memory is overlapped with the next instruction fetch and has no cost. The VCP RISC maintains the pipelined architecture of the VC RISC and is programmed using an enhanced optimizing 'C' language compiler.

SRAM INTERFACE

The SRAM interface controls all accesses to the VCP SRAM; the primary use of this SRAM is for program, stack and data storage for the VCP RISC. It is also used to implement buffer storage for video and bitstream framing and video rate buffering. It provides a glue-less interface to SRAM chips and also provides four address decodes and byte enables to allow memory mapped I/O devices to be controlled by the RISC. These allow the RISC to supervise external programmable devices and allow the VCP to act as the System Controller in embedded systems. The interface is 32-bits wide; 16-bit and 8-bit devices are also supported.

SRAM DMA

The SRAM DMA controller is a ten channel DMA controller which moves data between the SRAM and the following sections:

- TDM
- Audio
- Portal
- Huffman encoder & decoder
- Host

Each of these sections has two channels, one for reading and the other for writing. Each channel has a fixed priority and operates under the supervision of the RISC. This architecture allows the external SRAM to act as FIFO storage for the numerous buffering operations required and eliminates on-chip FIFOs. The internal SRAM data bus is 32-bits wide, although some of the devices (TDM, Audio, Huffman, Host) are 16 bits or 8 bits (Host debug).

COMMUNICATION RESOURCES

The VCP has three communication resources which are linked to the SRAM via the DMA channels. Each resource can be used for general purpose communication between the VCP and other devices in the system and is under software control. In most IIT Px64 Systems, the TDM port is connected to an ISDN chipset and the Audio Serial port is connected to audio DACs or to a DSP for audio processing. The Host port is connected to the source of command and control information and of any High or Low Speed data.

TDM INTERFACE

The TDM (Time Division Multiplexed) Interface implements a high-speed, bidirectional serial bus which is intended to transfer the encoded bitstream to the network interface. It can implement a number of high-speed serial protocols including Concentration Highway Interface (CHI), GCI, K2, SLD, MVIP and IOM2 formats. The TDM port can also act as a general purpose 16Mbit/sec serial link when not constrained by the TDM protocols.

HOST INTERFACE

The Host Interface provides a general purpose parallel interface to the VCP. It contains three ports, a debug port, a command port and a DMA port. It is used for communication between a Host processor and the VCP, and can also be used to transfer the following:

- Bitstream in/out
- Audio data in/out
- User data in/out

The Host Interface has three registers which control the operation of the interrupts and flags. Flags are used to indicate the VCP's readiness to accept or supply data over the host port DMA channel. The interrupts may be used for exception indication from RISC to Host or from Host to RISC. The interrupts are maskable.

AUDIO INTERFACE

The Audio interface is a bidirectional serial port designed to connect to a DSP serial port for transfer of compressed audio data. Audio compression is handled outside the VCP. For decode, the audio data will be demultiplexed from the bitstream and passed to the external DSP for decoding. For encoding, the external DSP will transfer the compressed audio data to the VCP which will multiplex it with the compressed video and user data from the Host interface.

PORTAL

The Portal connects the DRAM and SRAM buses. It provides a 32-bit bidirectional gateway between the buses. Most transfers will be between functional blocks on the same bus (e.g. SRAM and Host Interface, DRAM and Video interface). However in some instances it is desirable to transfer between buses and the Portal provides the mechanism for doing this.

PROCESSING RESOURCES

The nature of compressed bitstreams usually forces encoders and decoder to use non-byte aligned data structures and processing. The VCP RISC, in common with most microprocessors, is not well suited to bit manipulation operations and so hardware resources are made available to help the processor with these kinds of tasks. The processing resources available to the RISC processor are connected to the SRAM bus and mapped into the RISC register space. These resources include Huffman encoder and decoder, H.261 compliant BCH encoder and decoder, and H.221 and bitstream multiplexer/demultiplexer.

HUFFMAN ENCODER AND DECODER

The Huffman encoder and decoder are high-speed engines which encode and decode using MPEG, JPEG and H.261 Huffman tables. The decode tables are programmable and can be changed by the application; the encode tables are fixed. Zero-run length/amplitude (RLA) tokens are transferred on the DRAM bus to and from the Vision Processor core. The Huffman coded data is transferred by an SRAM DMA channel.

H.261 BCH ASSIST

The H.261 BCH section finds frame alignment and performs error detection/correction compliant with the H.261 specification. Data is supplied to this section under program control from the RISC.

H.221 ASSIST

The H.221 Assist section provides bit-handling hardware to assist RISC software in aligning, multiplexing and formatting audio, video and user data in compliance with the H.221 specification. Data is supplied to this section under program control from the RISC. The H.242, H.230 and H.243 specifications are also supported using RISC software. This combination of hardware and software can compensate for the delays encountered in up to six ISDN 'B' channels simultaneously.

DRAM DMA CONTROLLER

The DRAM DMA controller has multiple channels which transfer 32-bit data between the DRAM and the following:

- Video interface
- Huffman encoder & decoder
- Portal
- Vision Processor
- DRAM Refresh

The Video interface, VPe and Huffman sections all contain memory which allows the DMA controller to transfer data in DRAM page mode. One DMA channel provides DRAM refresh.

EMBEDDED VISION PROCESSOR (VPe)

The Embedded Vision Processor (VPe) implements a super-set of the functions of the IIT Vision Processor (VP) chip. In addition to running at higher clock speeds, it includes a number of architectural improvements which provide additional performance and code compaction over the VP chip.

The VPe core implements a programmable video signal processor which executes the compression and decompression operations required by the MPEG, JPEG and H.261 standards as well as some proprietary algorithms. Some of the improvements allow the VPe core to perform video pre- and post-processing functions in software. This provides much more flexible video processing than is offered by the circuits in the Vision Controller chip and enables the VCP to perform arbitrary filtering and scaling of incoming and outgoing video.

The microcode program for the VPe is stored in 2K words of on-chip ROM; in addition 2K word on-chip SRAM is provided to allow new microcode subroutines to be downloaded. Most VPe instructions are 32-bits wide, in contrast to the 64 bit microcode word of the VP chips (vers. 2-4).

DRAM INTERFACE

The DRAM interface provides glue-less connection to DRAM memory chips. It supports from 512K bytes to 8 Megabytes of DRAM, implemented using x1, x4 or x16 chips. The DRAM interface is also configurable in depth to allow addressing of 16Mbit DRAMS when they become available. A wide variety of DRAM speed grades may be used.

The DRAM interface is 32-bits wide and, at high VCP clock speeds, provides sufficient bandwidth to decode and display CCIR601 resolution images at 60 frames per second . For less demanding applications such as MPEG1 SIF resolution decode or H.261 QCIF codec, the bus can operate in a 16-bit mode. In this mode a single 256k x 16 DRAM chip can be used.

VIDEO INPUT

The Video Input section captures video frames and stores them in the DRAM. It also provides hardware preprocessing functions which can be used in conjunction with software running on the VPe. In particular it contains storage to buffer incoming video, multi-tap decimation filters and a temporal filter. The decimation filters allow conversion between CCIR601 resolution images and SIF, CIF and QCIF resolutions. The temporal filter improves the picture quality, especially in low-bitrate applications. The Video Input contains a programmable CRT controller which can genlock to an external video source.

VIDEO OUTPUT

The Video Output section displays video frames stored in the DRAM. It also provides hardware post-processing functions which can be used in conjunction with software running on the VPe. In particular it contains storage to buffer outgoing video, color conversion circuitry, multi-tap decimation and interpolation filters and a Temporal Artifact filter. The decimation and interpolation filters allow conversion between SIF, CIF, QCIF or any commonly used format and display formats for computer and TV video encoder chips such as CCIR601 and 640x480 VGA. The Temporal Artifact filter improves the picture quality, especially in low-bitrate applications by helping to remove time varying edge effects and blocking artifacts. The Video Output contains a programmable CRT controller which handles interlaced and progressive scanning. The CRT controller can be programmed to generate video syncs and blanks or can be genlocked to an external video source.

CLOCK GENERATORS

The VCP relies on 5 external clocks for timing and synchronization between the I/O resources and the main processing and control elements. The external clocks are: ACLK to provide timing for the DSP and audio serial line, TDMCLK to provide timing for the TDM port, PCLKCAM and PCLKSCN for video timing and CPUCLK for main processor timing.

FUNCTIONAL DESCRIPTION

VIDEO BUSES

The VCP has two video buses, one for input and one for output. These buses transfer digital video pixels into and out of the chip. In most systems pixels from a camera will be transferred over the input bus. In stand-alone applications the output bus will be connected to a monitor or LCD panel. In workstation applications the output bus will feed an overlay circuit so that the output video appears in a window of the Graphical User Interface.

Each video bus has 16 data pins which transfer luminance and chrominance (YUV) pixels in CCIR601 pixel format (4:2:2). In this format, there are half as many chrominance (U or V) pixels per line as luminance (Y) pixels; there are as many chrominance lines as luminance. The output video bus also has a mode for outputting 24-bit or 16-bit RGB pixels.

CRT CONTROLLERS

Each video bus is controlled by a pixel clock and horizontal and vertical synchronization (sync) signals. Pixels are clocked into and out of the VCP by the pixel clocks; the sync signals determine when the active video data is transferred. The timing of the active video and sync signals is determined by CRT Controllers (CRTCs) inside the VCP. There are two independent CRTCs, one for input and one for output. The input CRTC is always slaved to the timing of the camera; the output CRTC timing can be independent and internally generated, or slaved to the camera or slaved to some other video sync source.

VIDEO PROCESSING

The VCP contains circuitry to both pre- and post-process video. This circuitry provides color conversion, scaling and filtering functions through a combination of special hardware and software. In order to match internal clock rates with external pixel clock rates the VCP has internal line buffers. The line buffers are 360 pixels long which allows the processing circuitry to handle up to CCIR 601 resolutions (720 x 486 or 720 x 576 pixels in the Y component) and 360 samples in the U and V components to allow easy 4:2:2 to 4:1:1conversion. Pictures with resolutions above CCIR 601 can be captured and displayed by the VCP, but some video processing functions cannot be performed.

VIDEO PRE-PROCESSING

Figure 3 shows the video pre-processing functional blocks. Video can be input in CCIR 601 YUV pixel format. The first block scales the input video down horizontally by any factor, for example, the 640 pixels of 12.3MHz sampled NTSC could be scaled to the 176 pixels of QCIF. A seven-tap programmable filter is used to perform this scaling. The next block changes the vertical chrominance sub-sampling to 4:1:1 so that there are half as many chrominance lines as luminance lines. This is the format used by MPEG, H.261 and most video compression algorithms. Following this is a Temporal Filter which affects the luminance (Y) pixels only. This allows small changes in pixel values from one frame to the next to be ignored greatly improving the correlation between frames and thus the compressed image quality. The filter is programmable and implements the following algorithm on a pixel-by-pixel basis:

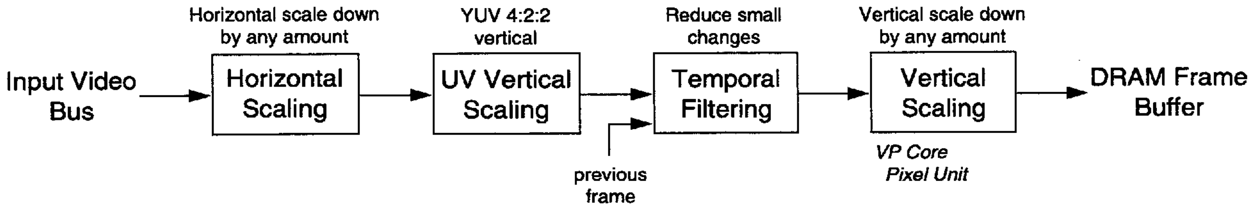

Figure 3. Video Pre-processing

Result = LUT(Input - Old) + Input

where LUT() is the look-up-table function. The filter is recursive in that the Result image for one frame becomes the Old frame for the next.

The Horizontal Scaling, UV Scaling and Temporal Filter functions are performed by special hardware and are all optional; they can be disabled by the VCP RISC processor. In addition the VPe core pixel unit can be used to apply programmable video processing functions. Typically this would be used to perform further scaling vertically for NTSC to CIF (240 line to 288 line) conversion or conversion from CIF to QCIF. Other filters can be applied to the input image, the complexity of which is limited only by available computation cycles.

Table 1 shows how the video pre-processing functions would be used in a number of different applications. The pre-processing is very flexible and the table shows only a small sample of the possible processing. It is assumed that in most applications the digital video will be provided by a digital TV chipset. These typically provide either CCIR 601 resolution (704x240 luminance pixels) or "square pixel" formats (640x480) which are more suitable for computer displays. The scaling capabilities of the VCP mean that either format can be handled.

The horizontal filter can automatically choose between 5 sets of filter coefficients based on the fractional component of the new position of the pixel in the video data stream. The filter coefficients are 8 bits wide.

The filter length is selectable 1, 3 or 7 taps. The relationship between the PCLKCAM and the master CPUCLK is shown in table 2.

For H.261 applications the VP Pixel Processing Unit can be used to scale not only between the 240 lines of NTSC to the 288 lines of CIF, but also reduce CIF to QCIF for low-bitrate operation or compatibility with small-screen video phones.

Taps	Restrictions
1	Pixel rate < (2xCPUCLK)/2
3	Pixel rate < (2xCPUCLK)/2
7	Pixel_rate < (2xCPUCLK)/4

Table 2. PCLK2XCAM to CPUCLK relationship

Application	**Standalone Video Phone**	**PC Video Conferencing**	**MPEG 1 Encode**	**M-JPEG Encode**
Input Video Format	CCIR 601 720x243	640x480	CCIR 601 720x243	640x480
Horizontal Scaling	CIF 720 -> 352 QCIF 720 -> 176	CIF 640 -> 352 QCIF 640 -> 176	SIF 720 -> 352	-
UV Vertical Scaling	✔	✔	✔	✔
Temporal Filtering	✔	✔	-	-
Vertical Scaling	CIF 240 -> 288 lines QCIF 240 -> 176 lines	CIF 240 -> 288 lines QCIF 240 -> 176 lines	-	-
DRAM Video Format	CIF or QCIF	CIF or QCIF	SIF	640x480 YUV

Table 1. Video Pre-processing Applications

VIDEO POST-PROCESSING

Figure 4 shows the video post-processing functional blocks. The first three processing steps are performed by the VPe core. A de-blocking filter can be applied to decoded images to improve the picture quality. This filter reduces blocking artifacts which can be visible at low bitrates. The VPe core can then interpolate any number lines to scale up the image; this can be used to convert from QCIF to CIF, or from CIF to NTSC or to allow the decoded image to fit in an arbitrary-sized window in a Graphical User Interface (GUI). Next, images from the camera can be decimated, mirrored and inlaid into the decoded image in order to implement a picture-in-picture (PIP) function. The size of the PIP, its position on the screen and the mirroring of the PIP image are all controllable by software.

Software control is also available for graphics and text overlay. The VCP DMA Engine can be programmed to bit-BLT image segments and character fonts around the DRAM. This replaces the dedicated hardware graphics used in the VCP and allows Graphics and Noise Filter to be enabled at the same time.

The scaled images are passed to the Noise Reduction stage. The Noise Reduction works in a similar manner to the input Temporal Filter using the same algorithm (see above). However the filter is not recursive because the Result is displayed only and not stored back into the DRAM frame buffer.

The next stage in the processing is an interlacing filter which generates even and odd fields from decoded frames for applications which use TV screens. This improves both the spatial and temporal appearance of the decoded images on interlaced displays. Following the interlacing filter is an interpolation section which uses bilinear interpolation to increase the resolution of the chrominance components by a factor of 2 in the vertical dimension. This interpolation section converts from the H.261 and MPEG chrominance sub-sampling to that used by CCIR 601. The resulting YUV pixels can then be passed

Taps	Restrictions
1	Pixel rate < (2xCPUCLK)/2
3	Pixel rate < (2xCPUCLK)/2
5	Pixel rate < (2xCPUCLK)/3
7	Pixel rate < (2xCPUCLK)/4

Table 3. PCLK2XSCN to CPUCLK relationship

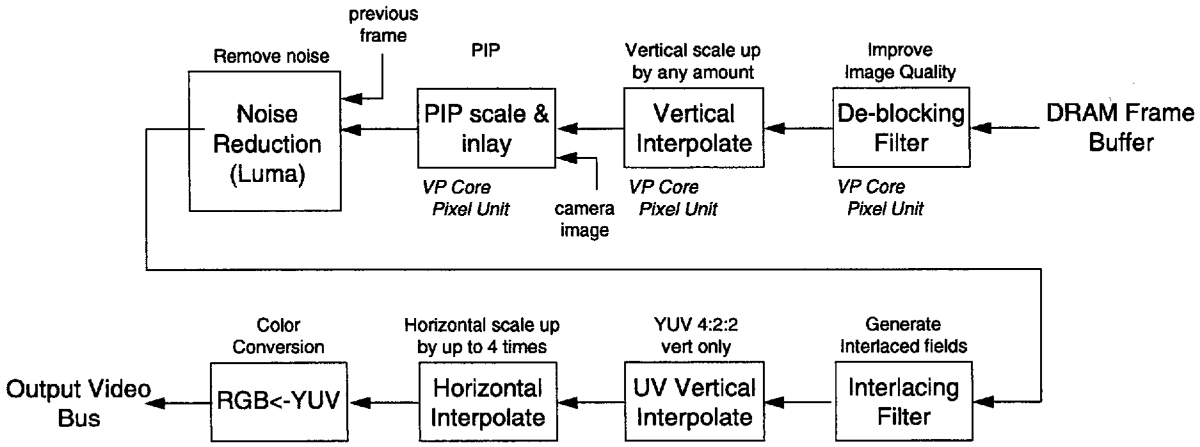

Figure 4. Video Post-processing

through a seven-tap horizontal interpolation filter which increases the horizontal resolution of the image by up to four times.

The horizontal filter can automatically choose between 5 sets of filter coefficients based on the fractional component of the new position of the pixel in the video data stream. The filter coefficients are 8 bits wide. The filter length is selectable 1, 3, 5 or 7 taps. The relationship between the PCLK2XSCN and CPUCLK is shown in table 3.

When used in conjunction with the software vertical interpolation, this allows the decoded image to fit in an arbitrary-sized window in a Graphical User Interface (GUI). Finally the YUV pixel output can optionally be converted to RGB (red, green, blue) color space for non-TV output applications. The RGB format can be either 16-bit or 24-bits multiplexed onto the 16-bit Video Out bus.

Table 4 shows how the various video post-processing functions might be used in a number of different applications; the figure is not exhaustive, the post-processing section can be programmed for many other applications. As with the pre-processing section, the post-processing can take care of scaling to both the CCIR 601 (720x243 or 720x288 pixels per field) resolutions used by TV displays and the "square pixel" format used for computers. For PC applications external overlay or inlay circuits can be used to combine the VCP video with the PC GUI. In such cases the VCP post-processing provides arbitrary scaling to fit the video in the GUI window.

Application	**Standalone Video Phone**	**PC Video Conferencing**	**Standalone MPEG Decode**	**PC M-JPEG Decode**
DRAM Video Format	CIF or QCIF	CIF or QCIF	SIF	640x480 YUV
Deblocking Filter	✔	✔	-	-
Vertical Scale	QCIF 176 -> 240 lines CIF 288 -> 240 lines	QCIF 176 -> arbitrary CIF 288 -> arbitrary	-	480 lines -> arbitrary
PIP	✔	✔	-	-
NR / Graphics	Graphics overlay	Noise Reduction	Graphics overlay	-
Interlacing	✔	-	✔	-
UV Vert Interpolate	✔	✔	✔	✔
Horizontal Filtering	QCIF 176 -> 704 CIF 352 -> 720	QCIF 176 -> arbitrary CIF 352 -> arbitrary	352 -> 720	640 pixels -> arbitrary
YUV -> RGB	-	✔	✔	✔
Output Video Format	CCIR 601 704x240	Variable window size Square pixel RGB	720x240 RGB	Variable window size Square pixel RGB

Table 4. Video Post-processing Applications

VIDEO TIMING

Figure 5 shows the timing of pixel transfers on the Video In bus when using the doubled (PCLK2XCAM) clock and clock qualifier (PCLKQCAM).

The Video Out bus can also be clocked either by double pixel clock and clock qualifier or by a single pixel clock. The double clock would typically be used for TV displays, the single for computer displays. Figure 6 shows the Video Out bus timing using a double pixel clock. Figures 7 and 8 show the Video In/Out bus timing using a single pixel clock. PCLKQSCN and PCLKQCAM are ignored in 1x clock mode.

For both buses the maximum double and single pixel clock is 33 MHz or CPUCLK, whichever is lower.

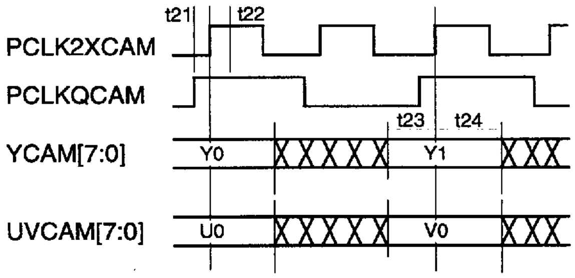

Figure 5. 2x Clock Mode Video In Bus Timing

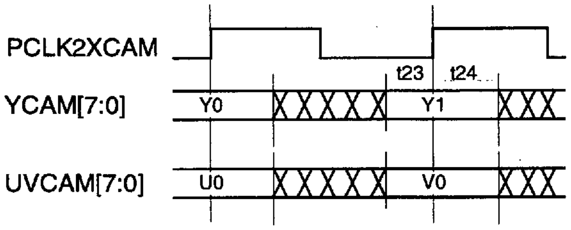

Figure 7. 1x Clock Mode Video In Bus Timing

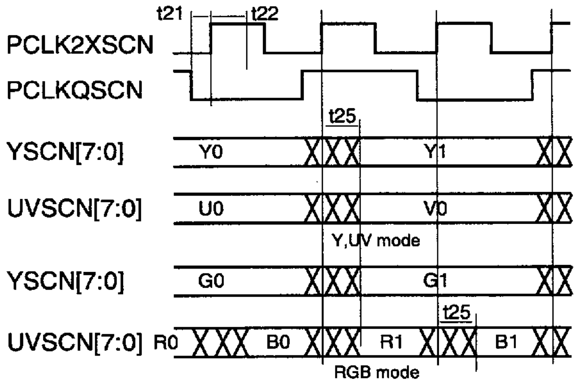

Figure 6. 2x Clock Video Out Bus Timing

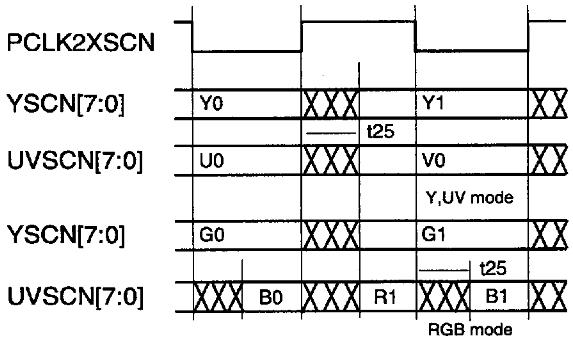

Figure 8. 1x Clock Video Out Bus Timing

Symbol	Description	CPUCLK=20MHz		30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
t6	PCLK2XCAM and PCLK2XSCN period	50ns	-	33ns	-	30ns	-	30ns	-
t21	PCLKQCAM and PCLKQSCN setup time to PCLK2X	6ns	-	6ns	-	6ns	-	4ns	-
t22	PCLKQCAM and PCLKQSCN hold time to PCLK2X	2ns	-	2ns	-	2ns	-	2ns	-
t23	Video data and syncs setup time to PCLK2X	6ns	-	6ns	-	6ns	-	4ns	-
t24	Video data and syncs hold time to PCLK2X	2ns	-	2ns	-	2ns	-	2ns	-
t25	Video data and syncs output delay time to PCLK2XSCN	0	2ns	0	2ns	0	2ns	0	2ns

Table 5. Video input and Output Bus Timing

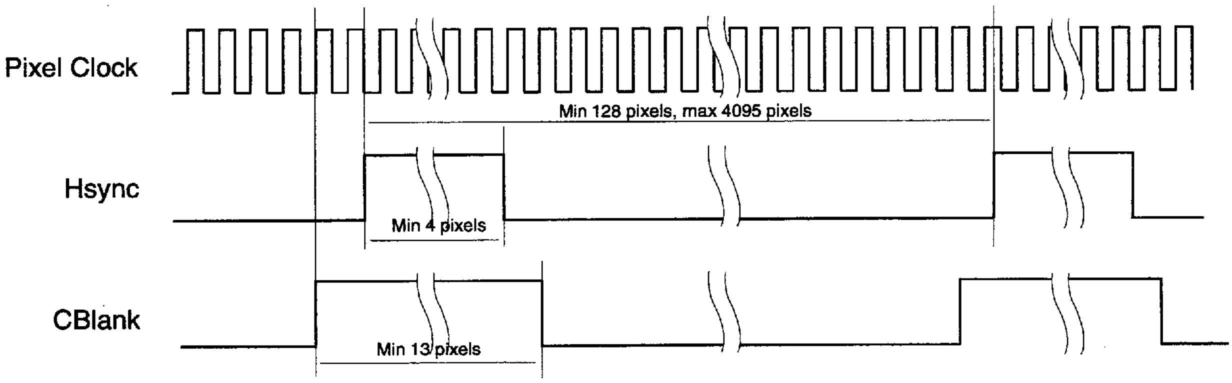

Figure 9. Horizontal Video Timing.

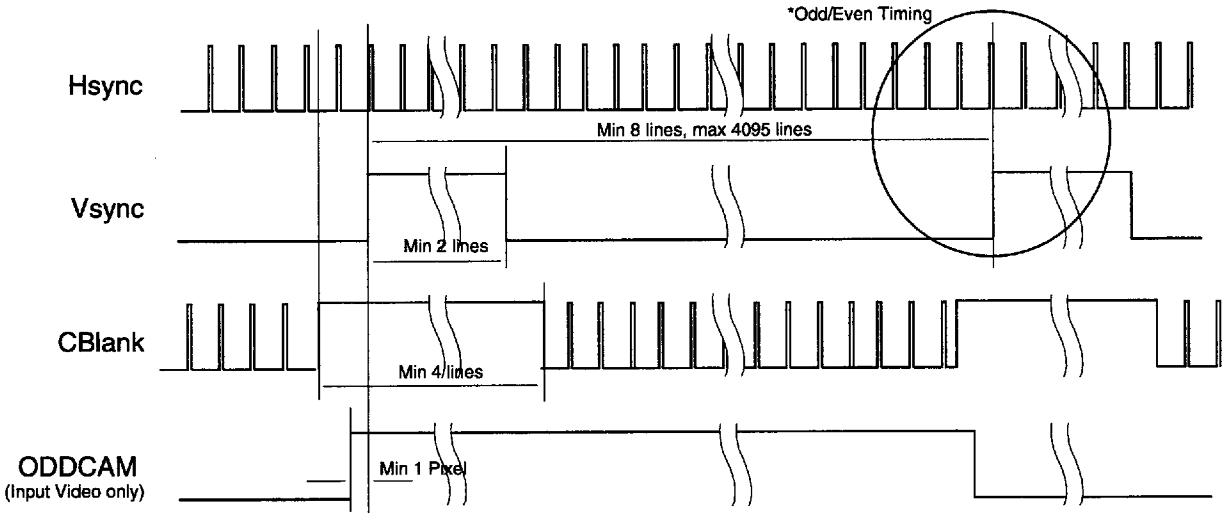

Figure 10. Vertical Video Timing

The timing of the syncs, blanking and odd/even field indication are shown in Figures 9, 10 and 11. The output video field indication is done by modifying the relative positions of VSYNCSCN and HSYNCSCN. At the start of an even field the horizontal and vertical sync pulses will start on the same clock edge, in odd fields the horizontal sync pulse will be delayed by one clock cycle. The sense of both horizontal and vertical syncs is programmable.

Table 5 shows the detailed AC timing for the video input and output buses.

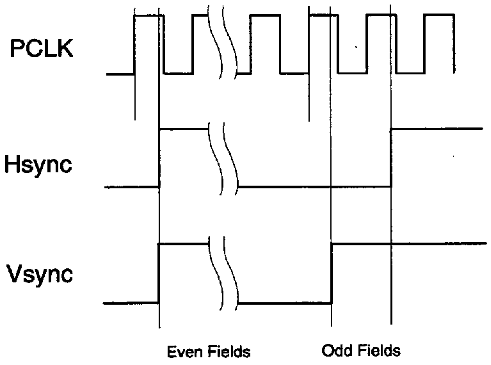

Figure 11. Odd/Even Video Output Timing

DRAM BUFFER

The DRAM buffer is used for storing uncompressed images, reference frames and intermediate data. When the VCP is encoding video captured frames are stored in raster format in the DRAM in three separate areas corresponding to the Y, U and V components. Similarly when decoding the images to be displayed are held in the DRAM. When both encoding and decoding, reference images and partially compressed data are also stored in the buffer.

All DRAM control is provided by the VCP DRAM bus. It can interface to DRAM chips organized x16, x4 and x1 bit wide. Figure 12 shows some example configurations. The DRAM interface is 32-bits wide and, at high VCP clock speeds, provides sufficient bandwidth to decode and display CCIR601 resolution images at 60 frames per second. For less demanding applications such as MPEG1 SIF resolution decode or H.261 QCIF codec, the bus can operate in a 16-bit mode. In this mode a single 256k x 16 DRAM chip can be used; the most significant and least significant 16-bits of the DBUS[31:0] should be connected (i.e. bit 31 to bit 15, bit 30 to bit 14, etc.).

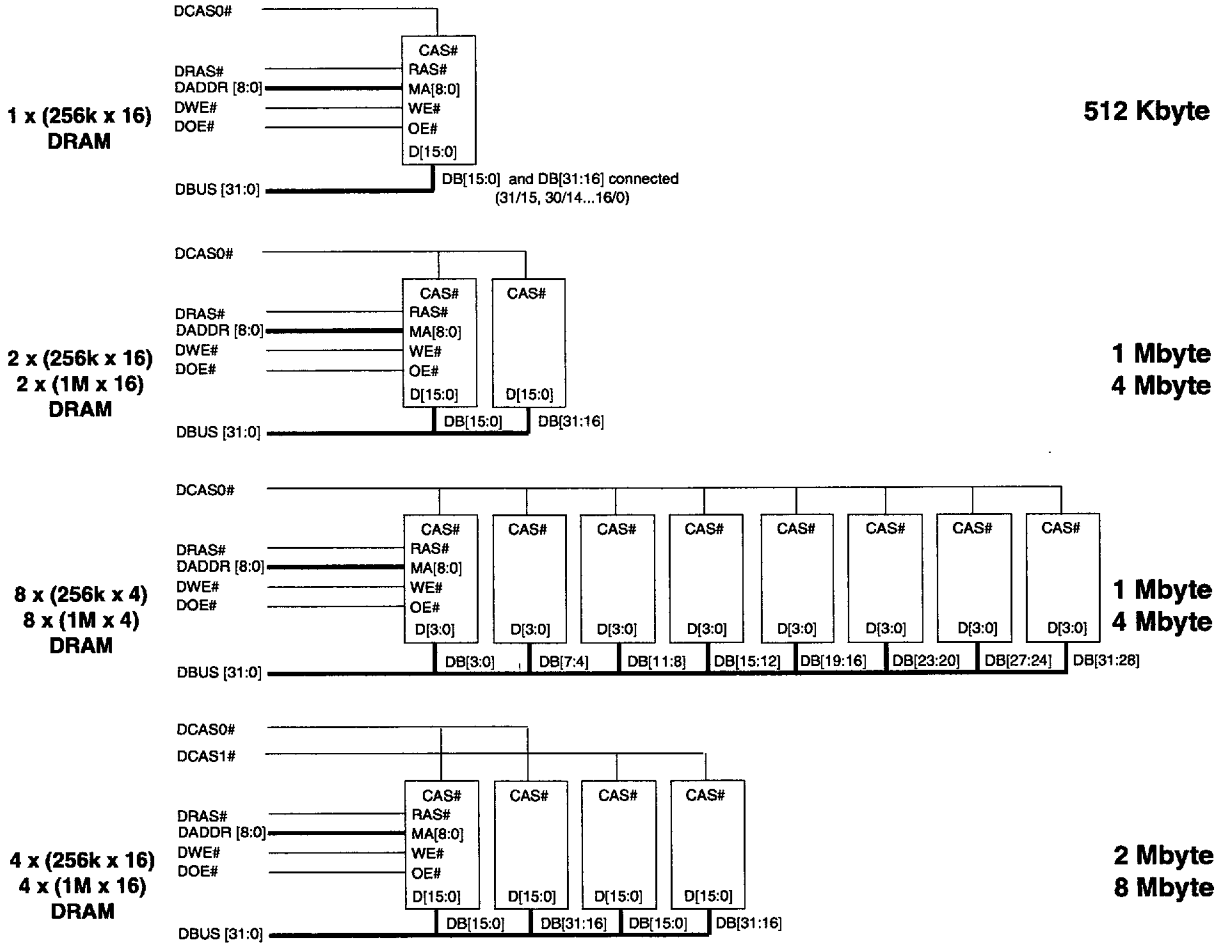

Figure 12. DRAM Configurations

The DRAM interface is programmable to enable support of DRAMs with a variety of page mode cycle times, RAS to CAS delay times and RAS precharge times. Table 7 and figures 13 and 14 show the DRAM output signal timing in terms of T states. The output signals may also be skewed in relation to each other and this should be taken into account when choosing DRAM for any application. The DRAM output signal skews are listed in table 6.

The VCP DRAM controller uses page mode accesses whenever possible and takes care of DRAM refresh. The VCP uses RAS only refresh mode, the refresh period is programmable.

The page mode cycle time of DRAMs varies from one manufacturer to another. A typical 70ns DRAM has a page mode cycle time of 40ns. For a VCP with a 33MHz CPUCLK a 3T cycle

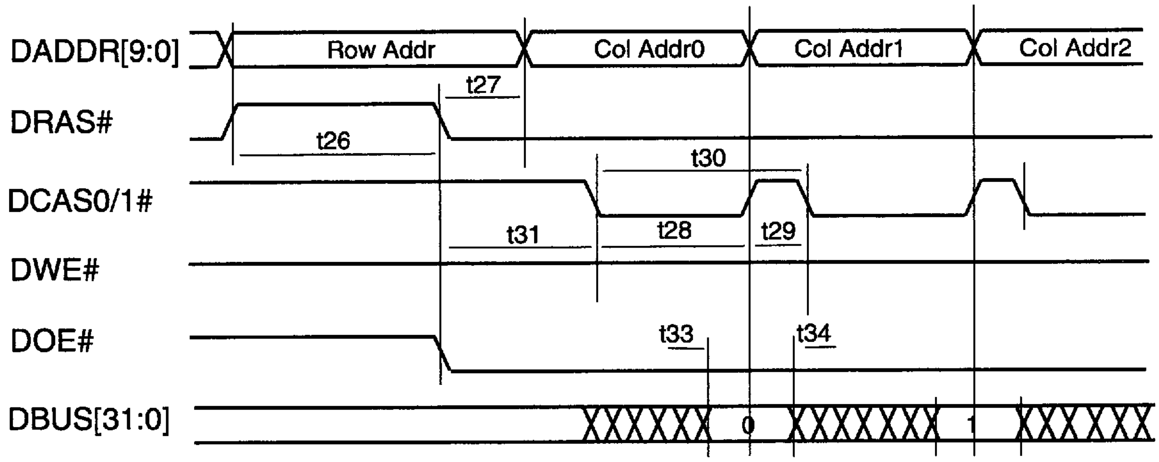

Figure 13. DRAM Read Timing

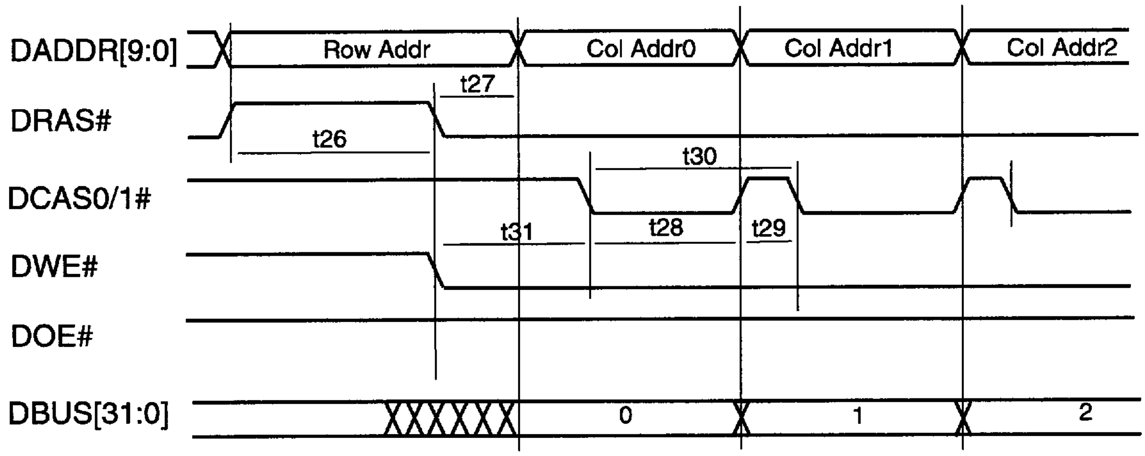

Figure 14. DRAM Write Timing

takes 45ns which will meet the specifications of the 70ns DRAM.

When operating with 2T page mode cycle times with a 33MHz VCP, the burst transfer rate of the DRAM interface is 128 Mbytes/s.

Symbol	Description	Programmable	
		Min	Max
t26	RAS precharge time	3T	5T
t27	Row address hold time	1T	3T
t28	CAS pulse width low	1T	2T
t29	CAS pulse width high	1T	2T
t30	Fast Page Mode access time	2T	4T
t31	RAS to CAS delay time	2T	4T
	* 1T = Internal PLL clock cycle		

Table 7. DRAM Interface Signal Logical Timing

Symbol	Description	CPUCLK=20MHz		30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
t32	DRAM port output signal skew	0	3ns	0	3ns	0	3ns	0	3ns
t33	Read cycle data setup time to CAS rising edge	5ns	-	5ns	-	3ns	-	3ns	-
t34	Read cycle data hold time to CAS rising edge	0	-	0	-	0	-	0	-

Table 6. DRAM Interface Signal Skew Timing

SRAM INTERFACE

The SRAM interface controls access to external SRAM which is used for RISC code, stack and data as well as buffer storage for the TDM, Audio, Host and H.221 sections. The SRAM bus supports four independent address spaces, each having programmable bus width and wait-states. The interface can thus support not only SRAM but also EPROM and memory mapped I/O ports for stand-alone applications.

The timing of SRAM accesses is shown in Figures 15 and 16. From 0 to 32 wait states can be inserted into each cycle, each wait state being one VCP CLOCK cycle long. All accesses by the SRAM DMA controller which services the TDM, Audio, Host and H.221 sections will have a minimum of one wait state inserted by the Interface. RISC accesses can be zero wait state. The SRAMs used with the VCP running at 0 wait state, 33MHz, must support a write pulse width less than or equal to 15ns.

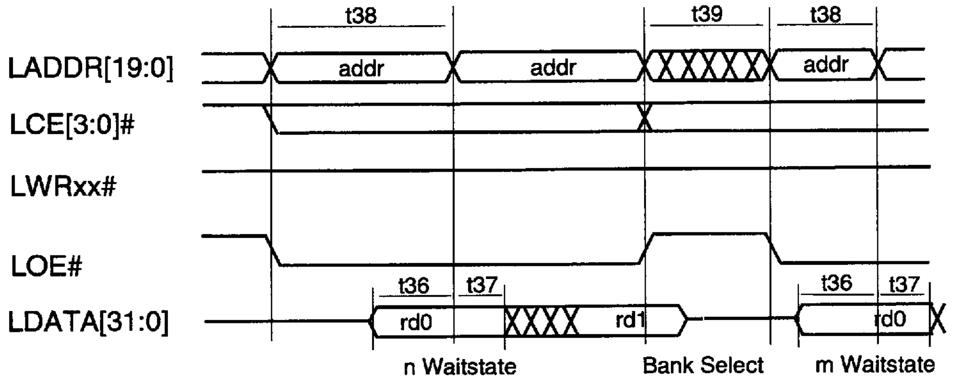

Figure 15. SRAM Read Timing

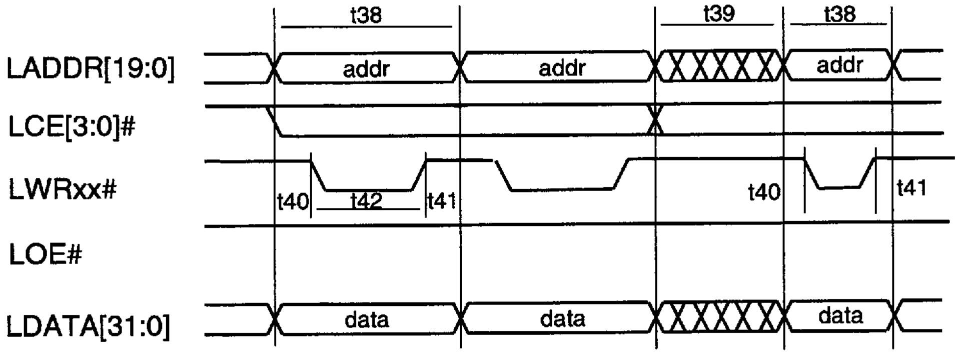

Figure 16. SRAM Write Timing

It is possible, when switching from a low speed bank to a high speed bank, for the turn off delay of the low speed bank to overlap the first access of the high speed bank. To prevent data corruption t39 (Bank Select Delay Time) is programmable for each bank from 0 to 3T states. See table 9 for details.

The signals for the SRAM bus are generated from the internal RISC clock and are timed in integer multiples of CPUCLK cycles, except for the write strobe, which is delayed by one quarter cycle from the address setup and advanced one quarter cycle from the start of the next access cycle.

The SRAM port signal skew may vary with VCP speed grade, see table 8 for details.

Symbol	Description	Programmable	
		Min	Max
t38	SRAM access time	1T	33T
t39	Bank Select delay time	0T	3T
t40	Address setup time to write strobe	0.25T	0.25T
t41	Address hold time to write strobe	0.25T	0.25T
t42	Write strobe pulse width low	0.5T	32.5T
* 1T = CPUCLK pin cycle, Each Wait-state = 1T			

Table 9. SRAM Port Output Signal Logical Timing

Symbol	Description	CPUCLK=20MHz		30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
t35	SRAM port output signal skew	0	3ns	0	3ns	0	3ns	0	2ns
t36	Read cycle data setup time to data latch	6ns	-	6ns	-	6ns	-	4ns	-
t37	Read cycle data hold time to data latch	2ns	-	2ns	-	2ns	-	2ns	-

Table 8. SRAM Port Output Signal Skew Timing

TDM BUS

The TDM port implements a five-wire serial bus which provides an easy connection between the VCP and available communications chips. The TDM bus is a Time Division Multiplexed bus which multiplexes data on up to 64 channels. Each channel is allocated a different time slot on the bus, and the VCP can be set to send and/receive data on any combination of different time slots. Data is assumed to be ordered by time slot (i.e. if timeslots 6, 8 and 17 are used, the first byte DMA'ed to memory is the byte in time slot 6, followed by 8 and 17 in order. Re-ordering must be done in software).

The interface consists of a Frame Sync (TDMFS), data transmit and receive signals (TDMDX, TDMDR), external buffer enable (TDMTSC#) and a clock (TDMCLK). The Frame sync and Clock signals are inputs to the VCP, so the timing of the data transfer is externally controlled. The TDM port can support a number of different timings on the TDM bus. These possibilities are described in Table 10. A timing diagram for a particular configuration is shown in Figure 17.

The TDM bus can transfer data at a maximum rate of 16 Mbits/s. A more typical configuration would support up to 4.096Mbits/s with a TDMFS fre-

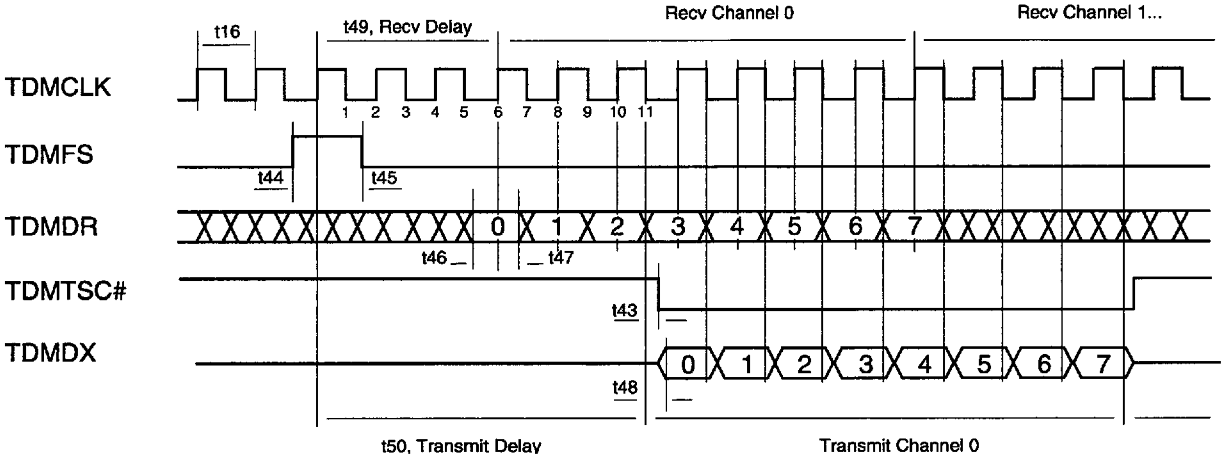

Figure 17. TDM Bus Timing

Symbol	Description
TDMCTL.sel2x	Serial clock 2x or 1x select
TDMCTL.clkphase	2x Serial clock phase to rising edge of TDMFS
TDMCTL.fe	Selects edge of serial clock to use when sampling TDMFS
TDMCTL.rce	Selects edge of serial clock to use when sampling TDMDR
TDMCTL.xce	Selects edge of serial clock to use when driving TDMDX
TDMCTL.xmitEndian	Selects little or big endian data type transmit
TDMCTL.rcvEndian	Selects little or big endian data type receive

Table 10. TDM Bus Programmability

quency of 8KHz. The TDM port hardware is flexible enough to interface to a wide range of communications chips for ISDN, PABX, LAN and WAN connectivity. In particular it will interface directly to chips which support the Concentration Highway Interface (CHI), ISDN Oriented Modular Revision 2 (IOM-2) interface and Multi-Vendor Integration Protocol (MVIP).

The TDM bus programmability includes independent receive, transmit and frame sync clock edge selection and independent receive and transmit data offsets. This is illustrated in table 12.

Symbol	Description	Programmable	
		Min	Max
t49	TDM Receive delay to TDMFS	0	8T
t50	TDM transmit delay to TDMFS	0	8T
* 1T = TDMCLK cycle			

Table 12. TDM Delay Timing

Symbol	Description	CPUCLK=20MHz		30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
t16	TDMCLK period	100ns	-	62.5ns	-	62.5ns	-	62.5ns	-
t43	TDMTSC# control output delay to TDMCLK	0	2	0	2	0	2	0	2
t44	TDMFS setup time to TDMCLK	6	-	4	-	4	-	4	-
t45	TDMFS hold time to TDMCLK	2	-	2	-	2	-	2	-
t46	TDMDR data setup time to TDMCLK	6	-	4	-	4	-	4	-
t47	TDMDR data hold time to TDMCLK	2	-	2	-	2	-	2	-
t48	TDMDX data output delay to TDMCLK	0	2	0	2	0	2	0	2

Table 11. TDM Bus AC Timing

AUDIO PORT

The Audio port is a bidirectional serial port which carries audio data to and from the VCP. It interfaces directly to the serial ports on Analog Devices 2101 DSPs and other DSPs with compatible ports. The port consists of a five-wire interface which can transfer data at rates of up to 16 Mbits/s. It is a single-channel serial bus with a fixed word length of 16 bits. It supports independent transmit and receive frame syncs with a fixed delay of one clock cycle between the frame sync and the transmission or receipt of data. It uses "normal" framing, so data is transmitted or received on the cycle after the Frame Sync is active. Data is transferred at the same rate as the ACLK. Figure 18 and table 13 show the timing of transfers on the Audio port.

Depending on the application, the Audio port can be interfaced directly to a DSP or to an audio Analog-to-Digital & Digital-to-Analog codec, in which case the VCP is responsible for any audio compression. Some video conferencing applications require multiple DSPs for audio compression and echo cancellation. The DSPs can communicate either through shared memory or by daisy-chaining serial ports (both serial ports are required for this on the DSP next to the VCP).

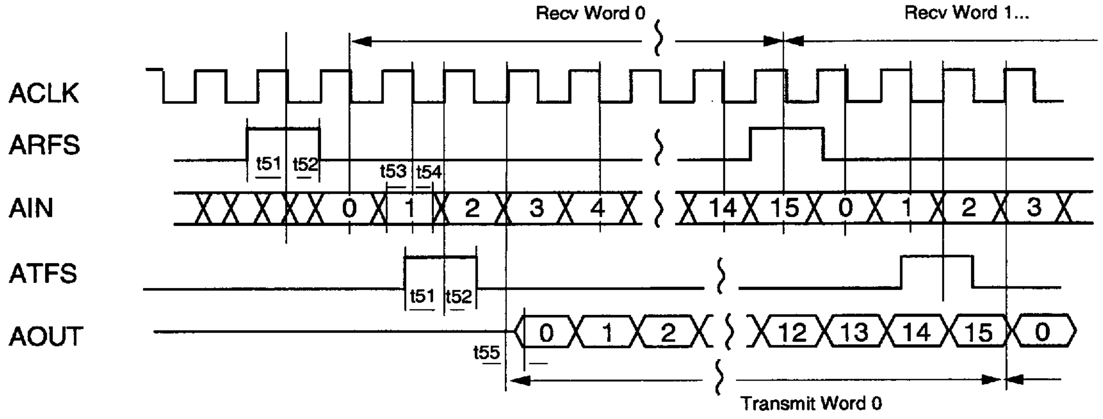

Figure 18. Audio Bus Timing

Symbol	Description	CPUCLK=20MHz		30Mhz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
t11	ACLK period	100ns	-	62.5ns	-	62.5ns	-	62.5ns	-
t51	ATFS/ARFS setup time to ACLK	6	-	4	-	4	-	4	-
t52	ATFS/ARFS hold time to ACLK	2	-	2	-	2	-	2	-
t53	AIN setup time to ACLK	6	-	4	-	4	-	4	-
t54	AIN hold time to ACLK	2	-	2	-	2	-	2	-
t55	AOUT output delay time	0	2	0	2	0	2	0	2

Table 13. Audio Bus Timing

HOST PORT

The Host Port is used by an external Host to control the VCP and may also be used to transfer high- or low-speed user data, audio and bitstream information. The Host port is a generic 16-bit parallel bus which accesses six registers in the VCP. The registers and their functions are detailed in the Register Description section. There are three ports in the Host Interface, a DMA port, a VCXI port and a Debug port. Figure 19 illustrates the timing relationships of the Host port.

The DMA port typically transfers user data to be multiplexed with the audio and video data in the H.221 compliant bitstream. This is the mechanism by which applications such as file transfer and shared screens are implemented during a video conference. In addition, the audio and multiplexed bitstream can be carried over this interface.

The Host port uses the HRDREQ# and HWRREQ# pins to indicate its readiness to send and receive data. The HIRQ line is used by the VCP to indicate that the HOSTIRQSTAT register should be interrogated.

The VCXI port transfers commands and status information between the VCP and an external Host. In some systems, the VCP will act as the System Controller and so there will be no external Host. However in most there will be another microprocessor responsible for controlling the system. It controls the VCP through the VCXI port, using the VCXI's "shared variable" mechanism. This gives the Host read/write access to global control variables in the VCP RISC's 'C' program and provides a simple and effective control mechanism.

The Debug port provides an additional path to the VCP RISC for debugging purposes. This

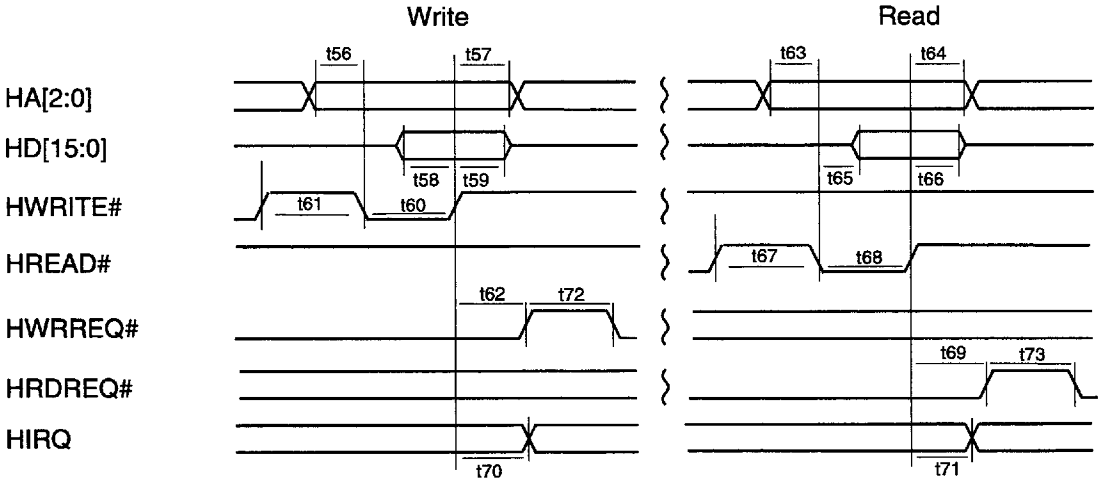

Figure 19. Host Bus Timing

allows software debuggers access to the state of the VCP hardware and software without the disturbing the VCXI or DMA ports.

The Host port is implemented with a 16-bit data bus, a 3-bit address bus, read and write strobes and read and write request lines. The request lines indicate when there is data waiting for the Host to read or when the Host should write the data word. The lines can be programmed to indicate this for any combination of the DMA, VCXI or Debug ports.

Table 14 shows the timing of the Host port signals.

Design Note:
The pulse width high time of HRDREQ# (t73) and HWRREQ# (t72) is well defined only as a minimum value (no less than three CPUCLK cycles), the maximum value is software dependent.

The VCP Host DMA channel bandwidth depends upon presense of other DMA in the system, its priority and status. The bus may also be occupied by the RISC instruction currently being executed. For example, load and store instructions use the memory cycle for RISC I/O and block DMA. This means that, even for burst transfers where the filesize has been negotiated in advance, it is not possible to specify a maximum period between Host DMA requests.

In reality, for systems using the IIT H.320 codec or MPEG1 decoder software, it is safe to calculate bus bandwidth to be about CPUCLK/3 words/sec and reasonable to assume that maximum data holdoff due to internal VCP DMA activity will not be longer than a few 10's of CPUCLK cycles.

Symbol	Description	CPUCLK=20MHz		30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
t56	HA to HWRITE# setup time	6	-	4	-	4	-	4	-
t57	HA to HWRITE# hold time	2	-	2	-	2	-	2	-
t58	HD to HWRITE# setup time	6	-	4	-	4	-	4	-
t59	HD to HWRITE# hold time	2	-	2	-	2	-	2	-
t60	HWRITE# pulse width low	30	-	30	-	30	-	30	-
t61	HWRITE# pulse width high	30	-	30	-	30	-	30	-
t62	HWRREQ# to HWRITE# output delay	0	8	0	8	0	8	0	8
t63	HA to HREAD# setup time	6	-	4	-	4	-	4	-
t64	HA to HREAD# hold time	2	-	2	-	2	-	2	-
t65	HD to HREAD# output delay	0	6	0	4	0	4	0	4
t66	HD to HREAD# hold time	2	-	2	-	2	-	2	-
t67	HREAD# pulse width high	30	-	30	-	30	-	30	-
t68	HREAD# pulse width low	30	-	30	-	30	-	30	-
t69	HRDREQ# to HREAD# output delay	0	8	0	8	0	8	0	8
t70	HIRQ to HWRITE# output delay	0	8	0	8	0	8	0	8
t71	HIRQ to HREAD# output delay	0	8	0	8	0	8	0	8
t72	HWRREQ# pulse width high	150	see note	100	see note	91	see note	75	see note
t73	HRDREQ# pulse width high	150	see note	100	see note	91	see note	75	see note

Table 14. Host Port Timing

CLOCK GENERATORS

Figure 20 shows the clock distribution to the various sections of the VCP. CPUCLK is the main system input clock to the VCP and is used to derive the T-CLK for DRAM bus timing and the VPCLK. The two pixel clocks (PCLK2XCAM and PCLK2XSCN), the audio clock (ACLK) and TDM port clock (TDMCLK) are asynchronous and must be less than half the frequency of the clock of the section to which they are interfacing or less than the absolute maximum for that clock, whichever is lower.

The RISC processor uses the CPUCLK, and executes one instruction per cycle. This clock is also used by the H.221/242/BCH sections, the SRAM DMA controller and the I/O resources served by the SRAM DMA controller.

The 2x T-Clock is used to time the memory accesses of the DRAM in addition to the timing of the various processing resources and the video filters. The T-CLK must be at least 4 times faster than the PCLKs to enable full 7 tap filtering (ie 2xCPUCLK > 4xPCLK). In situations where reduced filtering capacity is needed, the clock relationship can be relaxed.

The clock to the VPe is generated on board the VCP and is selectable from 1x, 4/3x to 2x the CPUCLK. The VCP is speed graded for both CPUCLK and VPCLK maximum speeds, the maximum speed of each clock is marked on the package.

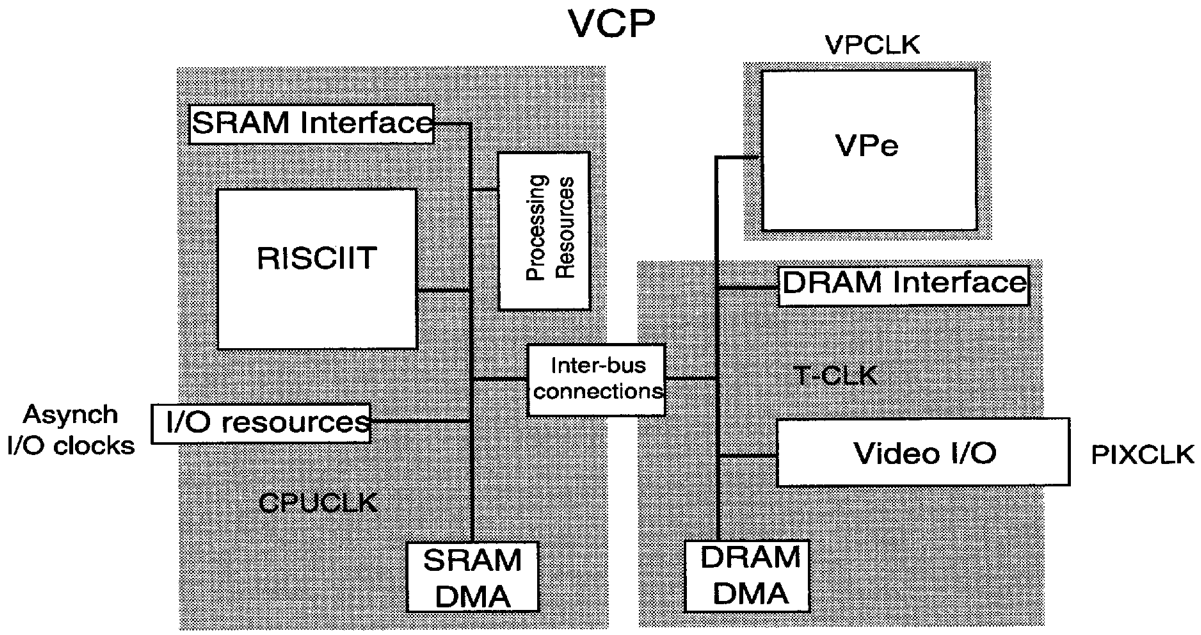

Figure 20. The VCP Clock Distribution

PIN DESCRIPTION

Name	I/O	Definition
LOE#	O	RISC Port output enable
LCE#[3:0]	O	RISC Port chip enables. RISC boots from internal ROM or LCE# = 0x03 depending on the value of ROMDIS.
LWRLL#	O	RISC port write enable byte 0
LWRLH#	O	RISC port write enable byte 1
LWRHL#	O	RISC port write enable byte 2
LWRHH#	O	RISC port write enable byte 3
LD[31:0]	I/O	RISC port data bus
LA[19:0]	O	RISC port address bus
RESET#	I	System reset (active low). Must be low for at least 16 clock cycles to ensure chip reset.
CPUCLK	I	RISC and System clock input
DEBUGIRQ	I	System debug interrupt
ROMDIS	I	Disable the internal boot ROM and boot from external ROM located at LCE# = 0x03
TEST2	O	Test output (phase45)
TEST1L	I	Test input (extpll)
AUX[3:0]	I/O	Auxiliary Control Lines
HIRQ	O	Host Interrupt Request. Indicates an interrupt from the VC to the host.
HWRREQ#	O	Host DMA channel Write Request
HRDREQ#	O	Host DMA channel Read Request
HD[15:0]	I/O	Host Data Bus. Compressed data is passed to and from the VC across this bus. It is also used to pass commands and parameters from the host to the VC.
HA[2:0]	I	Host Address Bus. This bus is used by the host to address one of eight registers in the host interface.
HREAD#	I	Host Read. Enables data from the host interface onto the HDATA[15:0] bus.
HWRITE#	I	Host Write. Latches data from the HDATA[15:0] bus into the host interface registers.

Name	I/O	Definition
VSYNCCAM	I	Vertical Sync for Camera Video port. Programmable for rising or falling edge.
HSYNCCAM	I	Horizontal Sync for Camera Video port. Programmable for rising or falling edge.
ODDCAM	I	Odd/Even field select for Camera Video port
PCLK2XCAM	I	Pixel Clock; two times the actual pixel clock for Camera Video port
PCLKQCAM	I	Pixel Clock qualifier in for Camera Video port
YCAM[7:0]	I	Y Luminance data bus for Camera Video port
UVCAM[7:0]	I	UV Chrominance data bus for Camera Video port
VSYNCSCN	I/O	Vertical Sync for Screen Video port Programmable for rising or falling edge
HSYNCSCN	I/O	Horizontal Sync for Screen Video port Programmable for rising or falling edge
BLANKSCN	O	Blanking for Screen Video port
PCLK2XSCN	I	Pixel Clock; two times the actual pixel clock for Screen Video port
PCLKQSCN	I	Pixel Clock qualifier in for Screen Video port
YSCN[7:0]	O	Y Luminance data bus for Screen Video port
UVSCN[7:0]	O	UV Chrominance data bus for Screen Video port
RAS#	O	Reference DRAM Row Address Strobe
CAS0#	O	Reference DRAM Column Address Strobe bank 0
CAS1#	O	Reference DRAM Column Address Strobe bank 1
DA[9:0]	O	Reference DRAM Multiplexed Address
DWE#	O	Reference DRAM Write Enable
DOE#	O	Reference DRAM Output Enable
DBUS[31:0]	I/O	Reference DRAM Data Bus

Name	I/O	Definition
ACLK	I	Audio Port Serial Clock
AIN	I	Audio Port Serial Data In
AOUT	O	Audio Port Serial Data Out
ARFS	I	Audio Port Receive Frame Sync
ATFS	I	Audio Port Transmit Frame Sync
TDMCLK	I	TDM Bus Serial Clock
TDMDR	I	TDM Bus Serial Data Receive
TDMDX	O	TDM Bus Serial Data Transmit
TDMFS	I	TDM Bus Frame Sync
TDMTSC#	O	TDM Bus Tristate Control; used to enable external driver for TDMDX

REGISTER DESCRIPTION

The Host Interface allows communication between the VCP RISC and an external Host (if any). There are three access ports in the Host Interface for VCXI, DMA and Debug data transfer. All Host Interface registers are aligned on 16-bit boundaries and so the HADDR pins are 16-bit word addresses.

hostdmaport 0x0 (R/W) hostdmaport

31	...	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	...	x	D15 - D0															

15-0: Host Data
DMA data transferred between the VCP RISC processor and the Host. Typically this port is used for high-speed or low-speed data multiplexed in the H.221 bitstream.

hostvcxport 0x1 (R/W) hostvcxport

31	...	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	...	x	x	x	x	x	x	x	x	x	D7 - D0							

7-0: VCXI Data
VCXI data transferred between the VCP RISC processor and the Host. Typically this port is used for VCXI commands and data.

hostdbgport 0x2 (R/W) hostdbgport

31	...	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
x	...	x	x	x	x	x	x	x	x	x	D7 - D0							

7-0: Debug Data
Debug data transferred between the VCP RISC processor and the Host. Typically this port is used for debugging only.

hostctl

0x3 (R/W)

31	...	8	7	6	5	4	3	2	1	0
x	...	x	H2R Irq	Input select 2-0			Output select 2-0			Clr R2H

7: **Host-to-RISC Interrupt Request**
When the Host writes a '1' to this bit a Host-to-RISC interrupt is generated to the RISC.

6-4: **Input select 2-0**
Determines which of the DMA, VCXI and Debug ports contribute to the HWRREQ pin. The logic for this pin is

```
HWRREQ =  (DMATRE & Isel0) |
          (VCXTRE & Isel1) |
          (DBGTRE & Isel2)
```

3-1: **Output select 2-0**
Determines which of the DMA, VCXI and Debug ports contribute to the HRDREQ pin. The logic for this pin is

```
HRDREQ =  (DMADW & Osel0) |
          (VCXDW & Osel1) |
          (DBGDW & Osel2)
```

0: **Clear RISC-to-Host interrupt**
When the Host writes a '1' to this bit it clears the RISC-to-Host interrupt.

hostmask

0x4 (R/W)

31	...	8	7	6	5	4	3	2	1	0
x	...	x	End ian Sel	Dbug TRE En	Dbug DW En	DMA TRE En	DMA DW En	VCX TRE En	VCXI DW En	R2H Irq En

The bits in this register determine if a condition causes a Host interrupt on the HIRQ pin. If not, the interrupt status is still set in the *hostirqstat* register.

7: **Data Endian Select**
When this bit is set to '1', the Host port expects little endian data. Otherwise data is big endian.

6: **Debug Port TRE Interrupt Enable**
When this bit is set to '1', the Host is interrupted when the Debug port is waiting for data to be written by the Host.

5: **Debug Port DW Interrupt Enable**
When this bit is set to '1', the Host is interrupted when the Debug port contains data which the Host should read.

4: **DMA Port TRE Interrupt Enable**
When this bit is set to '1', the Host is interrupted when the DMA port is waiting for data to be written by the Host.

3: **DMA Port DW Interrupt Enable**
When this bit is set to '1', the Host is interrupted when the DMA port contains data which the Host should read.

2: **VCXI Port TRE Interrupt Enable**
When this bit is set to '1', the Host is interrupted when the VCXI port is waiting for data to be written by the Host.

1: **VCXI Port DW Interrupt Enable**
When this bit is set to '1', the Host is interrupted when the VCXI port contains data which the Host should read.

0: **RISC-to-Host Interrupt Enable**
When this bit is set to '1', the RISC-to-Host interrupt will cause an interrupt to the Host.

hostirqstat 0x5 (Rd) hostirqstat

31	...	8	7	6	5	4	3	2	1	0
x	...	x	x	Dbug TRE	Dbug DW	DMA TRE	DMA DW	VCX TRE	VCXI DW	R2H Irq

6: **Debug Port TRE Interrupt Status**
When this bit is set to '1', the Debug port is waiting for data to be written by the Host.

5: **Debug Port DW Interrupt Status**
When this bit is set to '1', the Debug port contains data which the Host should read.

4: **DMA Port TRE Interrupt Status**
When this bit is set to '1', the DMA port is waiting for data to be written by the Host.

3: **DMA Port DW Interrupt Status**
When this bit is set to '1', the DMA port contains data which the Host should read.

2: **VCXI Port TRE Interrupt Status**
When this bit is set to '1', the VCXI port is waiting for data to be written by the Host.

1: **VCXI Port DW Interrupt Status**
When this bit is set to '1', the VCXI port contains data which the Host should read.

0: **RISC-to-Host Interrupt Status**
When this bit is set to '1', the RISC-to-Host interrupt has occurred.

PINOUT 240 POWER QUAD FLAT PACK

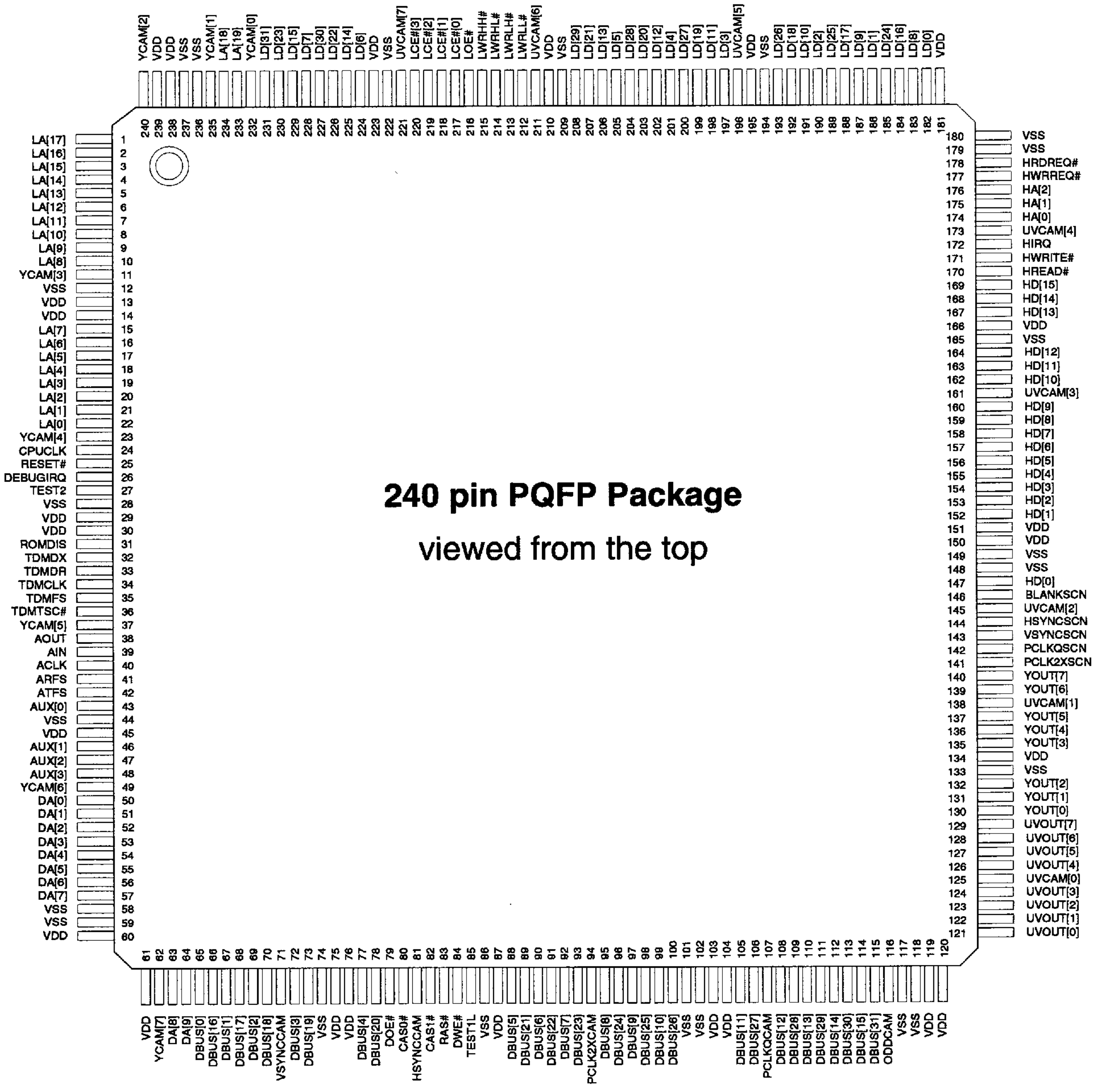

Figure 21. 240 QFP VCP Pinout

PINOUT 225 BALL GRID ARRAY (BGA)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	
R	UVSCN [0]	DBUS [15]	DBUS [29]	PCLK QCAM	DBUS [10]	DBUS [8]	DBUS [22]	DBUS [21]	RAS#	CAS0#	DBUS [19]	DBUS [2]	DBUS [0]	YCAM [7]	DA[6]	R
P	UVSCN [2]	UVSCN [1]	DBUS [31]	DBUS [28]	DBUS [26]	DBUS [24]	DBUS [7]	DBUS [6]	CAS1#	DBUS [20]	DBUS [18]	DBUS [16]	DA[8]	DA[7]	DA[3]	P
N	UVSCN [4]	UVSCN [3]	ODD CAM	DBUS [14]	DBUS [27]	DBUS [9]	DBUS [23]	DBUS [5]	NC	DBUS [4]	DBUS [17]	DA[9]	DA[5]	DA[4]	DA[0]	N
M	YSCN [0]	UVSCN [5]	UV CAM[0]	DBUS [30]	DBUS [13]	DBUS [11]	PCLK2 XCAM	TEST 1L	HSYNC CAM	DBUS [3]	DBUS [1]	DA[2]	DA[1]	AUX[3]	AUX[1]	M
L	YSCN [4]	YSCN [1]	UVSCN [7]	UVSCN [6]	VSS	DBUS [12]	DBUS [25]	DWE#	DOE#	VSYNC CAM	VSS	YCAM [6]	AUX[0]	ARFS	ACLK	L
K	YSCN [7]	UVCAM [1]	YSCN [5]	YSCN [3]	YSCN [2]	VDD	VDD	VSS	VDD	VDD	AUX[2]	ATFS	AOUT	YCAM [5]	TDM TSC#	K
J	HSYNC SCN	VSYNC SCN	PCLK QSCN	PCLK2 XSCN	YSCN [6]	VDD	VSS	VSS	VSS	VDD	AIN	TDMFS	TDM CLK	TDMDR	TDMDX	J
H	HD[1]	HD[2]	HD[0]	BLANK SCN	UVCAM [2]	VSS	VSS	VSS	VSS	VSS	CPU CLK	RES ET#	DEBUG IRQ	ROM DIS	TEST2	H
G	HD[3]	HD[4]	HD[5]	HD[6]	UVCAM [3]	VDD	VSS	VSS	VSS	VDD	LA[4]	LA[2]	LA[1]	LA[0]	YCAM [4]	G
F	HD[7]	HD[8]	HD[9]	HD[12]	HD[15]	VDD	VDD	VSS	VDD	VDD	LA[8]	YCAM [3]	LA[6]	LA[5]	LA[3]	F
E	HD[10]	HD[11]	HD[13]	HWR ITE#	VSS	LD[18]	LD[19]	LD[5]	LCE# [1]	LD[22]	VSS	LA[12]	LA[11]	LA[9]	LA[7]	E
D	HD[14]	HRE AD#	UVCAM [4]	HA[0]	LD[17]	LD[26]	LD[4]	LD[13]	LWR HL#	UVCAM [7]	LD[7]	LD[31]	LA[15]	LA[13]	LA[10]	D
C	HIRQ	HA[2]	HWR REQ#	LD[24]	LD[25]	LD[3]	LD[12]	LD[21]	LWR LH#	LCE# [0]	LD[6]	LD[23]	LA[18]	LA[16]	LA[14]	C
B	HA[1]	LD[0]	LD[16]	LD[9]	LD[10]	LD[11]	LD[20]	UVCAM [6]	NC	LOE#	LCE# [3]	LD[30]	LA[19]	YCAM [2]	LA[17]	B
A	HRD REQ#	LD[8]	LD[1]	LD[2]	UVCAM [5]	LD[27]	LD[28]	LD[29]	LWR LL#	LWR HH#	LCE# [2]	LD[14]	LD[15]	YCAM [0]	YCAM [1]	A
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	

Bottom View

Figure 22. 225 BGA VCP Pinout

ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS

Storage Temperature Range	-65°C to 150°C
Operating Temperature Range	-65°C to 110°C
Voltage Range on any Pin	-0.5V to (Vcc + 0.5V)
Power Dissipation	__ Watts @ 33MHz

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range	0°C to 70°C
Supply Voltage Vcc	4.75V to 5.25V

DC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

Symbol	Parameter	Min	Max	Unit	Notes
Vih	High Level Input Voltage	2.0	Vcc+0.25	V	All inputs TTL levels except CLK
Vil	Low Level Input Voltage	-0.3	0.8	V	All inputs TTL levels except CLK
Vch	CLK High Level Input	3.7	Vcc+0.25	V	CMOS level input
Vcl	CLK Low Level Input	-0.3	0.8	V	CMOS level input
Voh	High Level Ouptput Voltage	3.0	-	V	IOH = 1mA
Vol	Low Level Output Voltage	-	0.45	V	IOL = 4mA
Ili	Input Leakage Current	-	±15	μA	
Ilo	Output Leakage Current	-	±15	μA	
Cin	Input Capacitance	-	10	pF	fc = 1 MHz
Co	Input/Output Capacitance	-	12	pF	fc = 1 MHz
Cclk	CLK Capacitance	-	20	pF	fc = 1 MHz

Table 15. DC Electrical Characteristics

AC ELECTRICAL CHARACTERISTICS

(over recommended operating conditions)

All timings are in nanoseconds (ns).

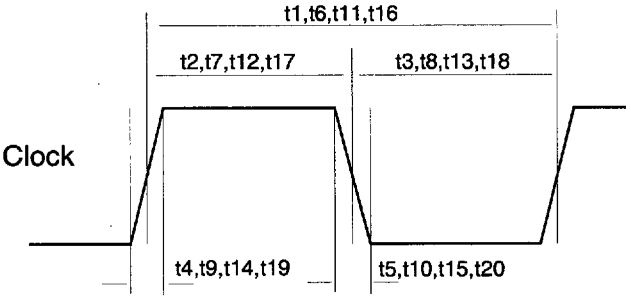

Figure 25. Clock Timing Diagram

Symbol	Description	CPUCLK=2OMHz		30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
t1	Clock Period	50ns	100ns	33.3n	100ns	30.3ns	100ns	25ns	100ns
t2	Clock low time	44ns	-	27ns	-	24ns	-	21ns	-
t3	Clock high time	44ns	-	27ns	-	24ns	-	21ns	-
t4	Clock rise time	-	8	-	6	-	3	-	3
t5	Clock fall time	-	8	-	6	-	3	-	3

Table 16. CPUCLK Timing

Symbol	Description	CPUCLK=20MHz		30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
t6	Pixel Clock Period	50ns	-	33ns	-	30ns	-	30ns	-
t7	Pixel Clock low time	20ns	-	15ns	-	15ns	-	15ns	-
t8	Pixel Clock high time	20ns	-	15ns	-	15ns	-	15ns	-
t9	Pixel Clock rise time	-	3ns	-	4ns	-	4ns	-	4ns
t10	Pixel Clock fall time	-	3ns	-	4ns	-	4ns	-	4ns

Table 17. PCLK2XCAM and PCLK2XSCN Timing

Symbol	Description	CPUCLK=20MHz		30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
t11	Audio Clock Period	62.5ns	-	62.5ns	-	62.5ns	-	62.5ns	-
t12	Audio Clock low time	25ns	-	25ns	-	25ns	-	25ns	-
t13	Audio Clock high time	25ns	-	25ns	-	25ns	-	25ns	-
t14	Audio Clock rise time	-	8	-	6	-	3	-	3
t15	Audio Clock fall time	-	8	-	6	-	3	-	3

Table 18. ACLK Timing

Symbol	Description	CPUCLK=20MHz		30MHz		33MHz		40MHz	
		Min	Max	Min	Max	Min	Max	Min	Max
t16	TDM Clock Period	62.5ns	-	62.5ns	-	62.5ns	-	62.5ns	-
t17	TDM Clock low time	25ns	-	25ns	-	25ns	-	25ns	-
t18	TDM Clock high time	25ns	-	25ns	-	25ns	-	25ns	-
t19	TDM Clock rise time	-	8	-	6	-	3	-	3
t20	TDM Clock fall time	-	8	-	6	-	3	-	3

Table 19. TDMCLK Timing

MECHANICAL

240-LEAD QUAD FLAT PACK

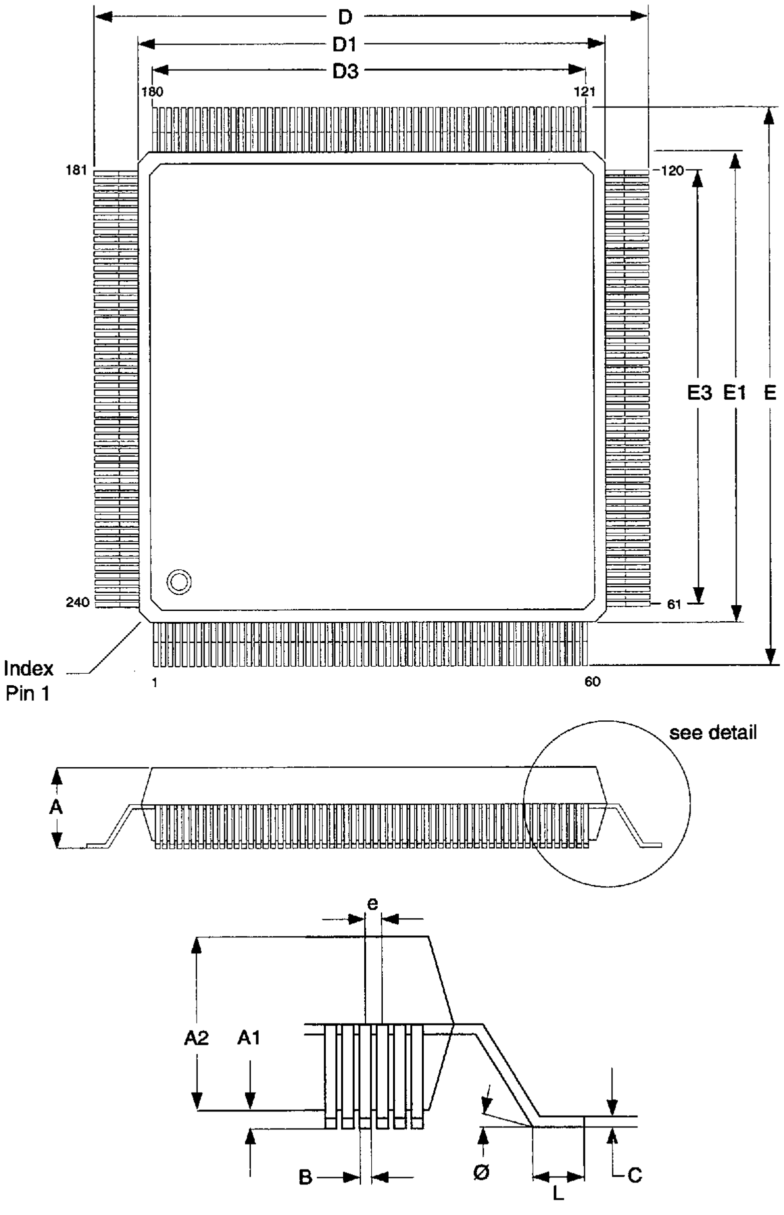

Figure 24. PQFP Mechanical

Note: All dimensions are in inches (millimeters)

Symbol	Min	Nom	Max
A	-	-	0.165 (4.20)
A1	0.010 (0.25)	-	-
A2	0.126 (3.20)	0.134 (3.40)	0.142 (3.60)
B	0.006 (0.14)	0.009 (0.22)	0.012 (0.30)
C	0.004 (0.9)	0.006 (0.15)	0.008 (0.20)
D	1.352 (34.35)	1.362 (34.60)	1.372 (34.85)
D1	1.256 (31.90)	1.260 (32.00)	1.264 (32.10)
D3	1.161 (29.50) REF		
e	0.020 (0.50) BASIC		
E	1.352 (34.35)	1.362 (34.60)	1.372 (34.85)
E1	1.256 (31.90)	1.260 (32.00)	1.264 (32.10)
E3	1.161 (29.50) REF		
L	0.018 (0.45)	0.024 (0.60)	0.030 (0.75)
θ	0	3.5	7

Table 20. PQFP Mechanical

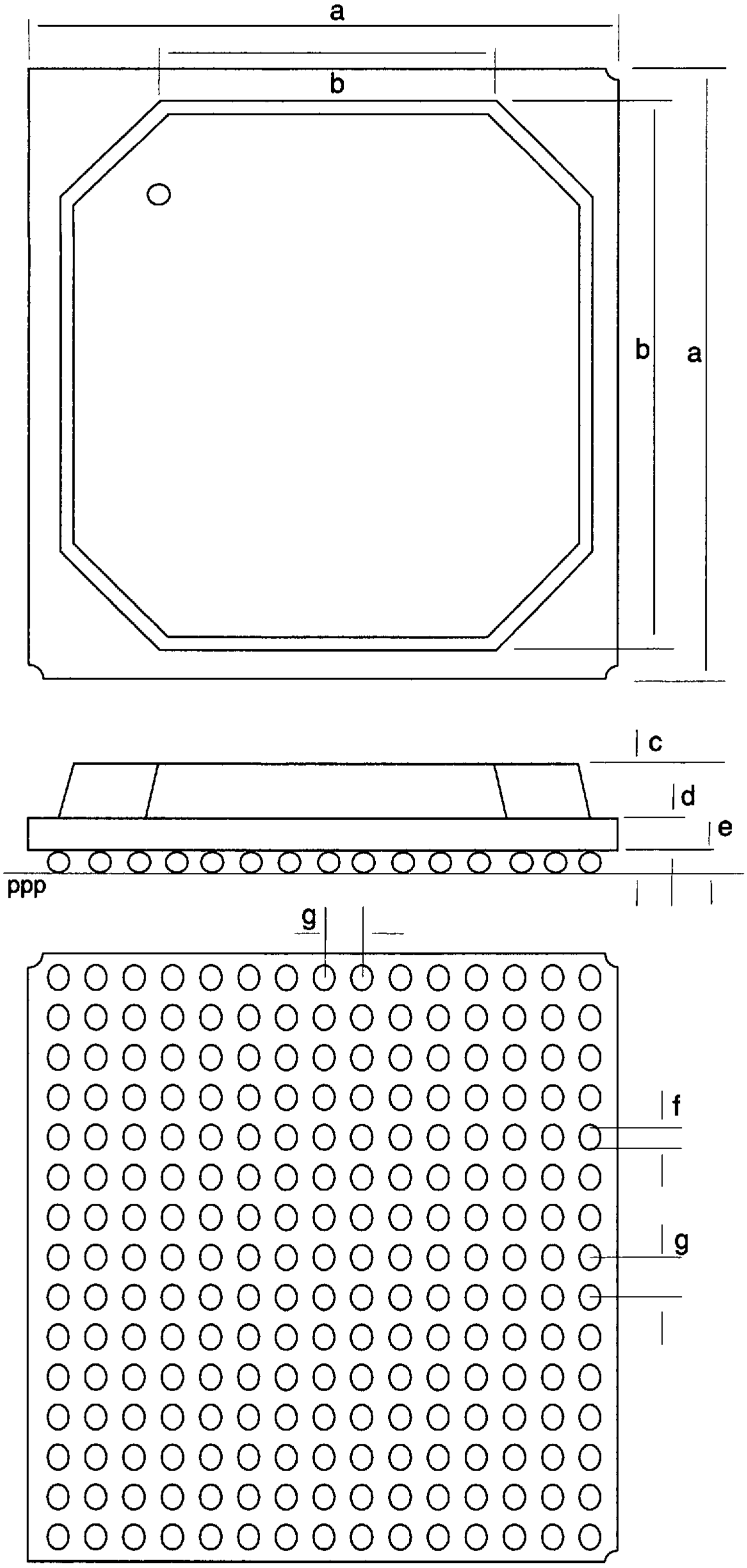

Figure 25. BGA Mechanical

Notes:

1. g represents basic solder ball grid pitch.

2. Index may be marked by ink or lazer. Is closest to pin A1.

3. Primary datum for c, d and e is defined by spherical crowns of solder balls.

4. Heat dissipation figures assume compliance with IIT board layout and assembly recomendations.

5. All dimensions are in inches (millimeters).

Symbol	Min	Nom	Max
a	1.055 (26.80)	1.063 (27.00)	1.071 (27.20)
b	-	0.945 (24.00)	0.972 (24.70)
c	0.079 (2.00)	0.084 (2.13)	0.090 (2.30)
d	0.012 (0.31)	0.014 (0.36)	0.016 (0.41)
e	0.020 (0.50)	0.024 (0.60)	0.028 (0.70)
f	0.024 (0.60)	0.030 (0.76)	0.035 (0.90)
g	-0.0591		
ppp	-	-	0.010 (0.25)
BGA	15x15 = 225		
Theta/Ja	25 Centigrade/Watt		

Table 21. BGA Mechanical