



DESCRIPTION

The PT6530 are 1/3 duty and 1/4 duty LCD display drivers that can directly drive up to 300 segments and can control up to eight general-purpose output ports. These products also incorporate a key scan circuit that accepts input from up to 30 keys to reduce printed circuit board wiring.

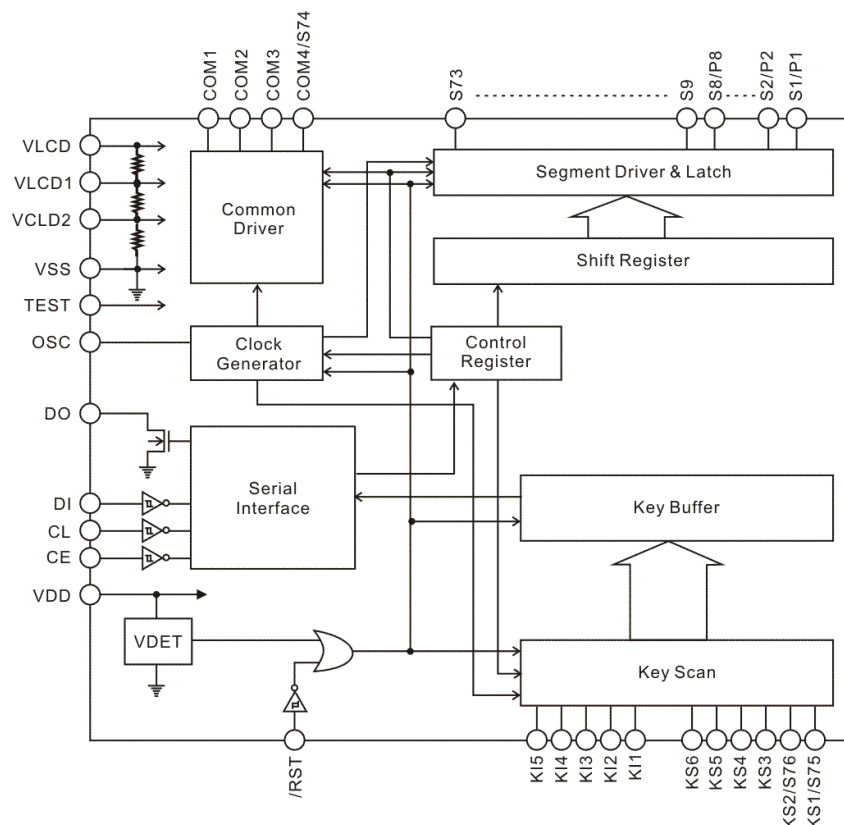
APPLICATION

- Electronic Equipment with LCD Display

FEATURES

- Key input function for up to 30 keys (A key scan is performed only when a key is pressed.)
- 1/3 duty and 1/4 duty drive schemes can be controlled from serial data.
- 1/2 bias and 1/3 bias drive schemes can be controlled from serial data.
- Capable of driving up to 228 segments using 1/3 duty and up to 300 segments using 1/4 duty.
- Sleep mode and all segments off functions that are controlled from serial data.
- Segment output port/general-purpose output port function switching that is controlled from serial data.
- Serial Interface for clock, Data Input, Data Output, Strobe pins.
- Direct display of display data without the use of a decoder provides high generality.
- Independent VLCD for the LCD driver block (VLCD can be set to in the range VDD – 0.5 to 6.0V)
- Provision of an on-chip voltage-detection type reset circuit prevents incorrect displays.
- RES pin provided for forcibly initializing the IC internal circuits.
- RC oscillator circuit.

BLOCK DIAGRAM



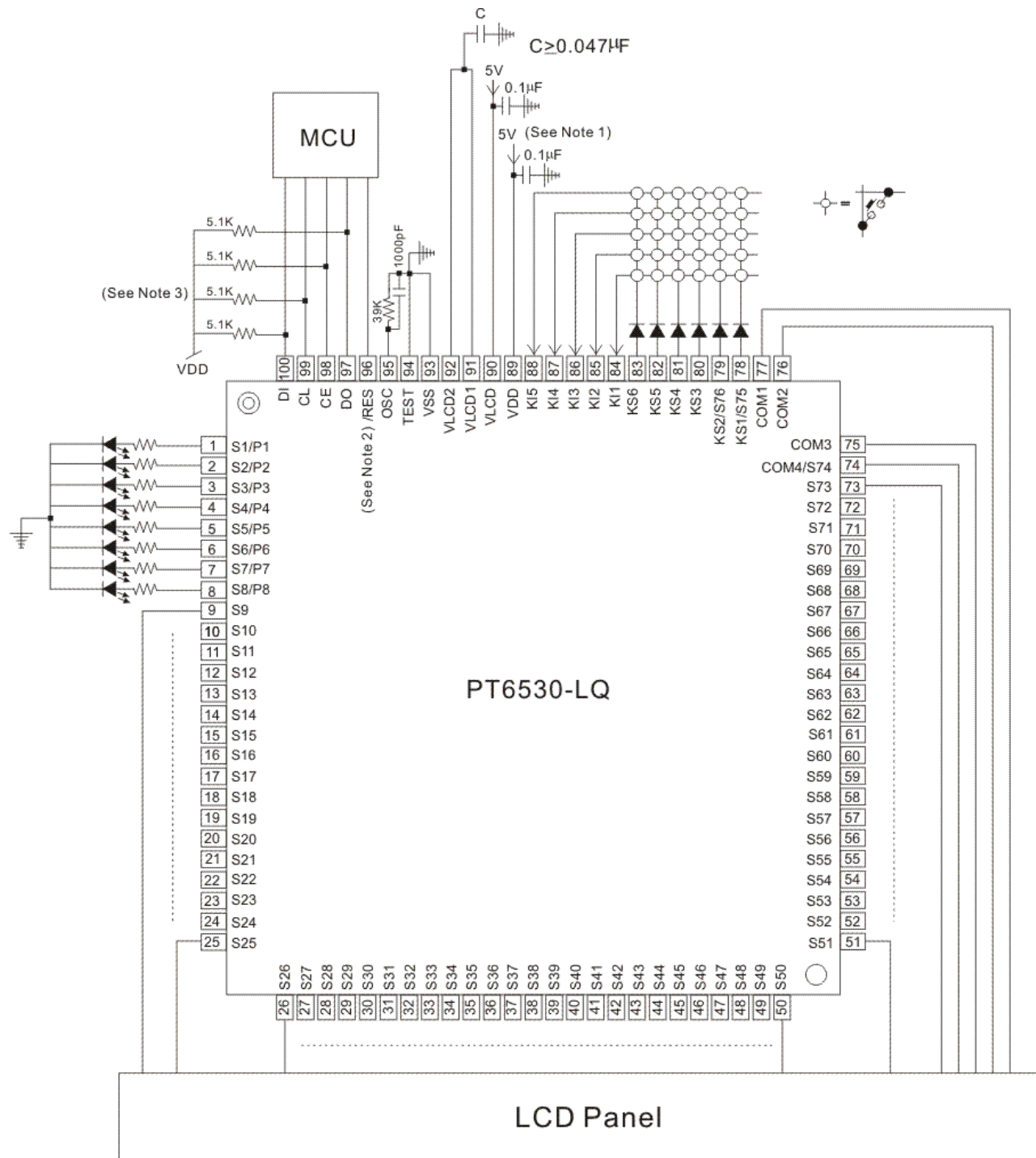


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1. APPLICATION CIRCUITS

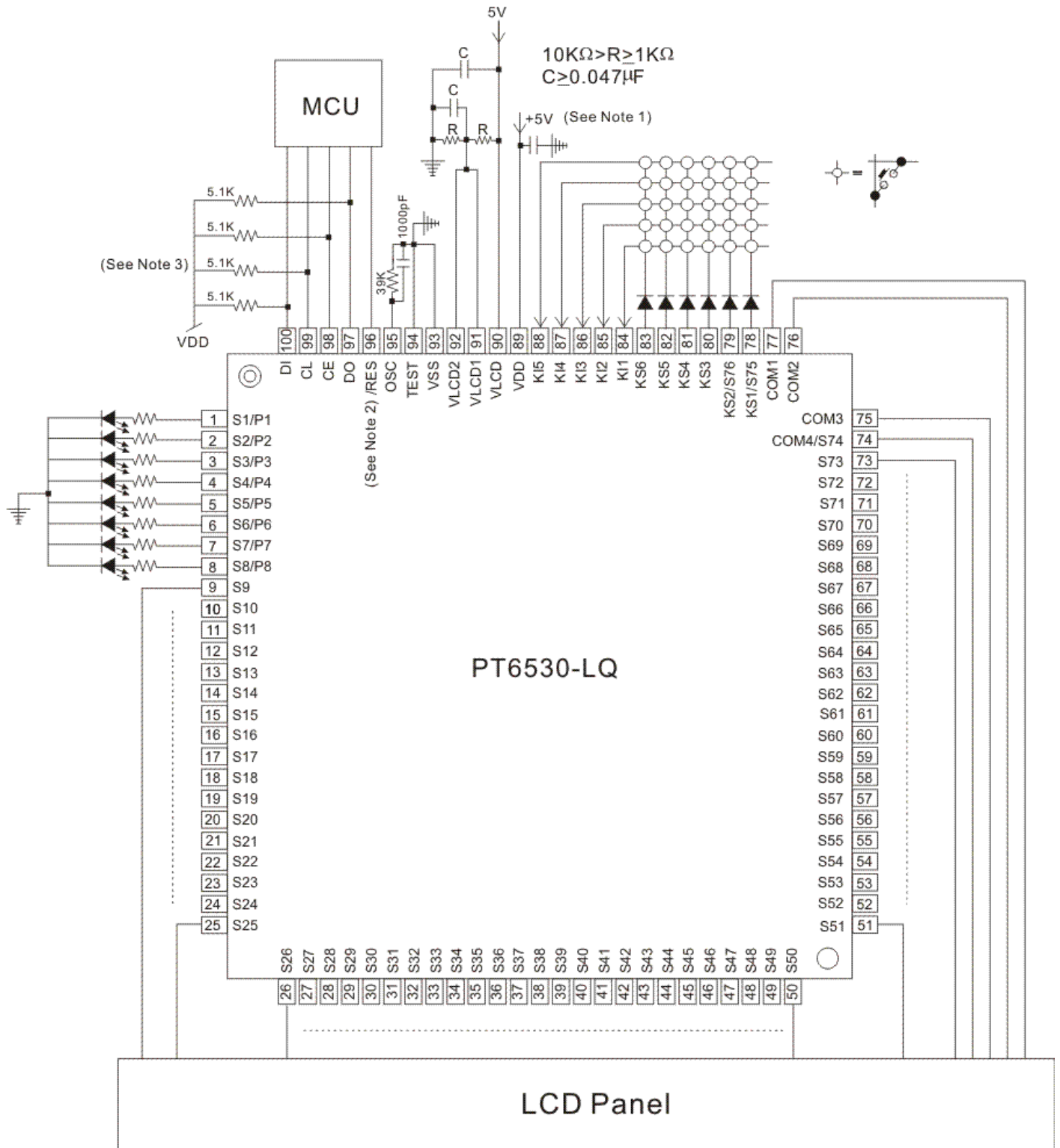
1.1 1/3 DUTY 1/2 BIAS (FOR NORMAL PANEL USE)



Notes:

1. A capacitor can be connected to the power supply line to make the power supply voltage VDD rise time (when power is applied) and the power supply voltage VDD fall time power drops) are at least 1ms when PT6530 is reset via VDET.
2. If the /RES pin is not used to initiate the System Reset Function, it must be connected VDD.
3. The DO pin is an open-drain output and therefore needs a pull-up resistor. This resistor is between 1K and 10KΩ. The value of this resistor must be in accordance with that capacitance of the external wiring so that the signal waveforms are in proper form.

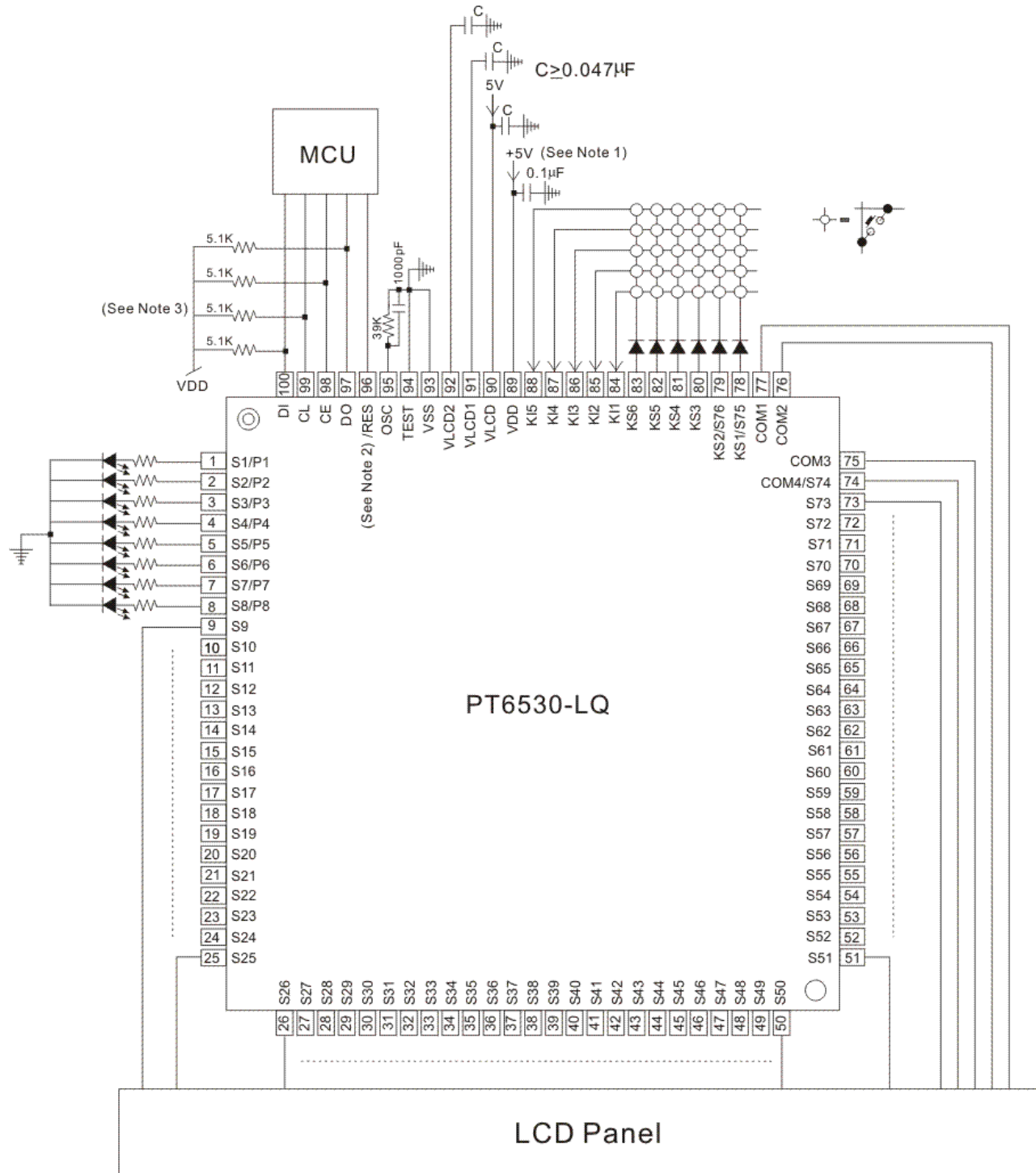
1.2 1/3 DUTY 1/2 BIAS (FOR LARGE PANEL USE)



Notes:

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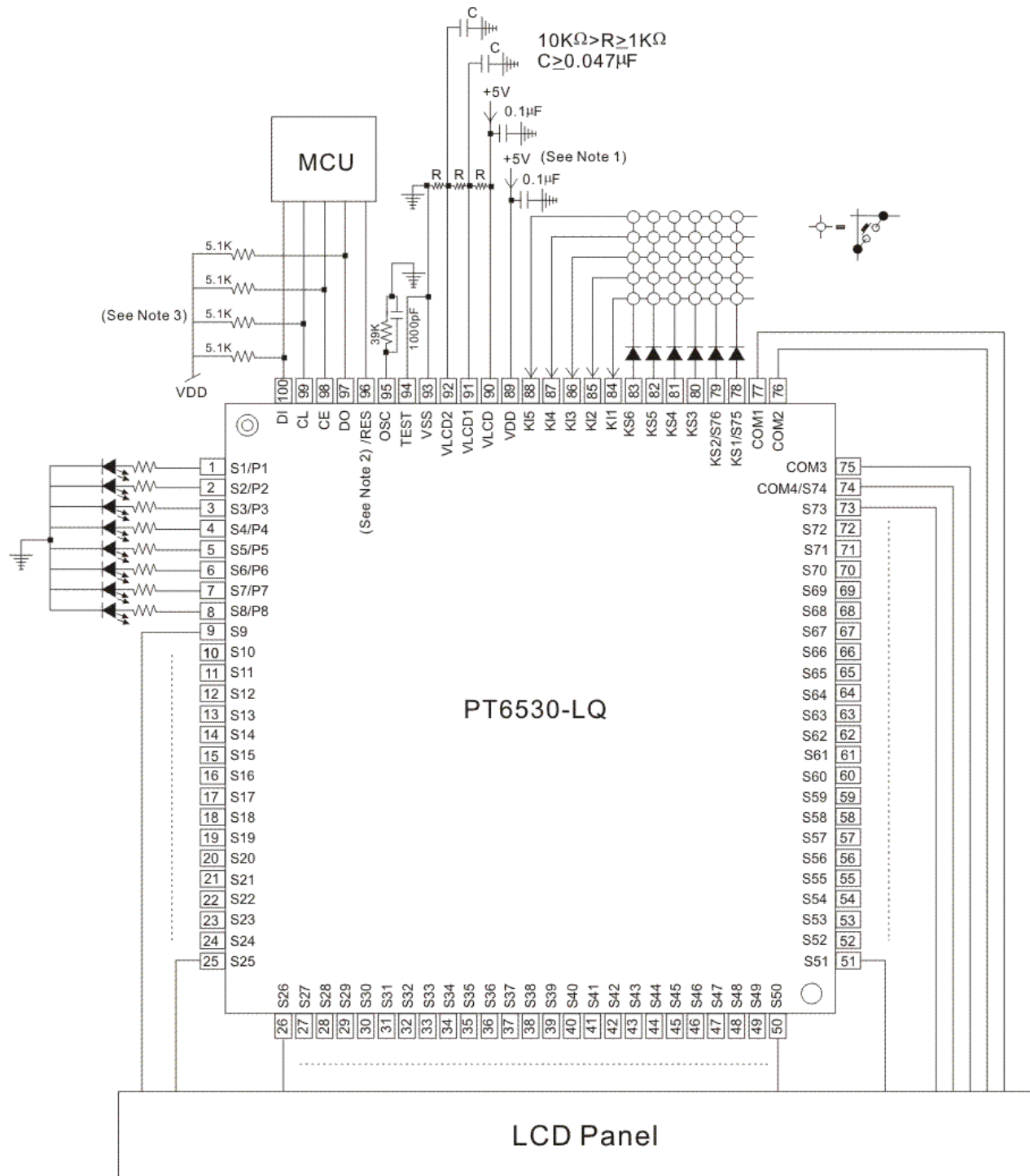
1.3 1/3 DUTY 1/3 BIAS (FOR NORMAL PANEL USE)



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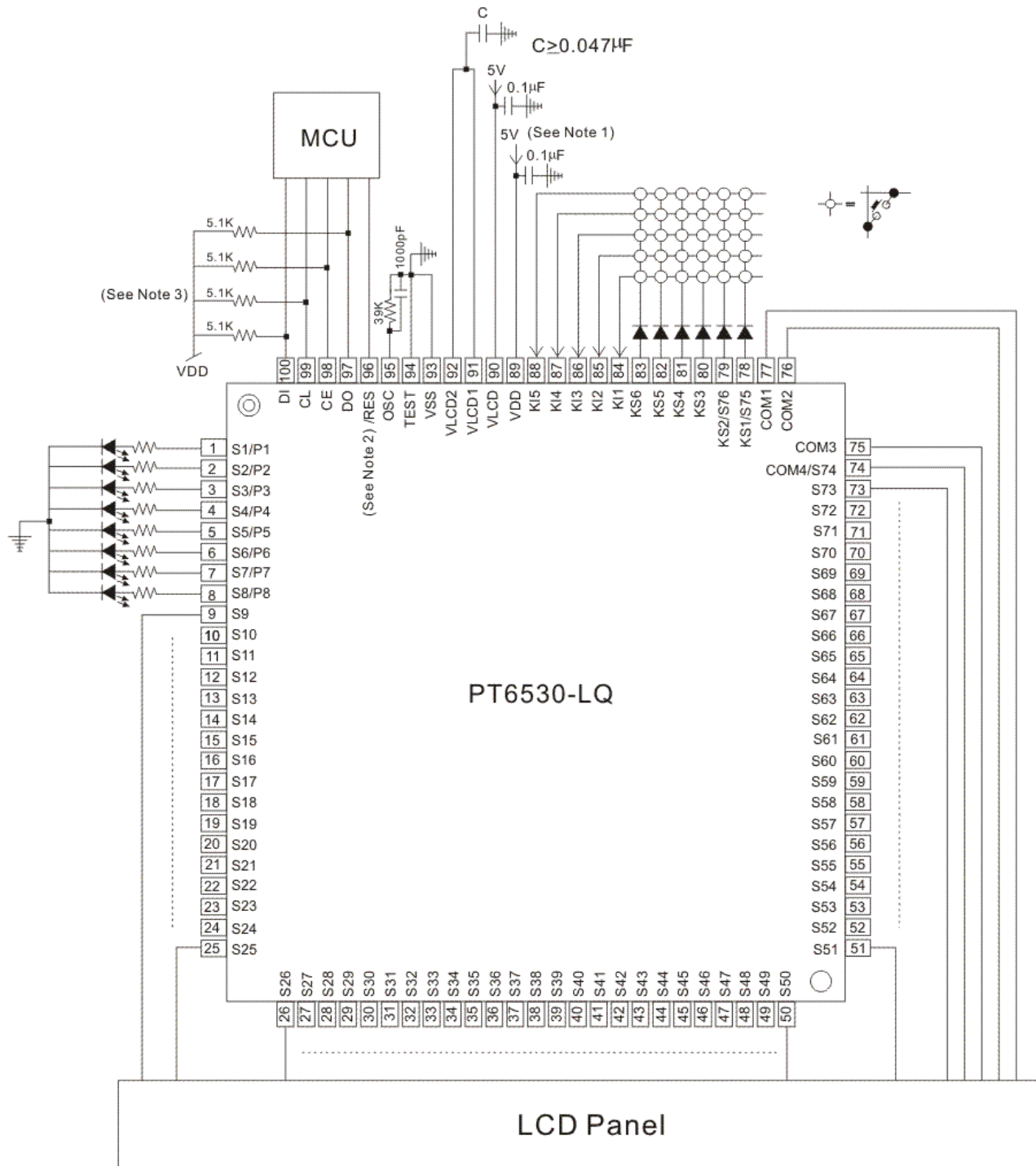
1.4 1/3 DUTY 1/3 BIAS (FOR LARGE PANEL USE)



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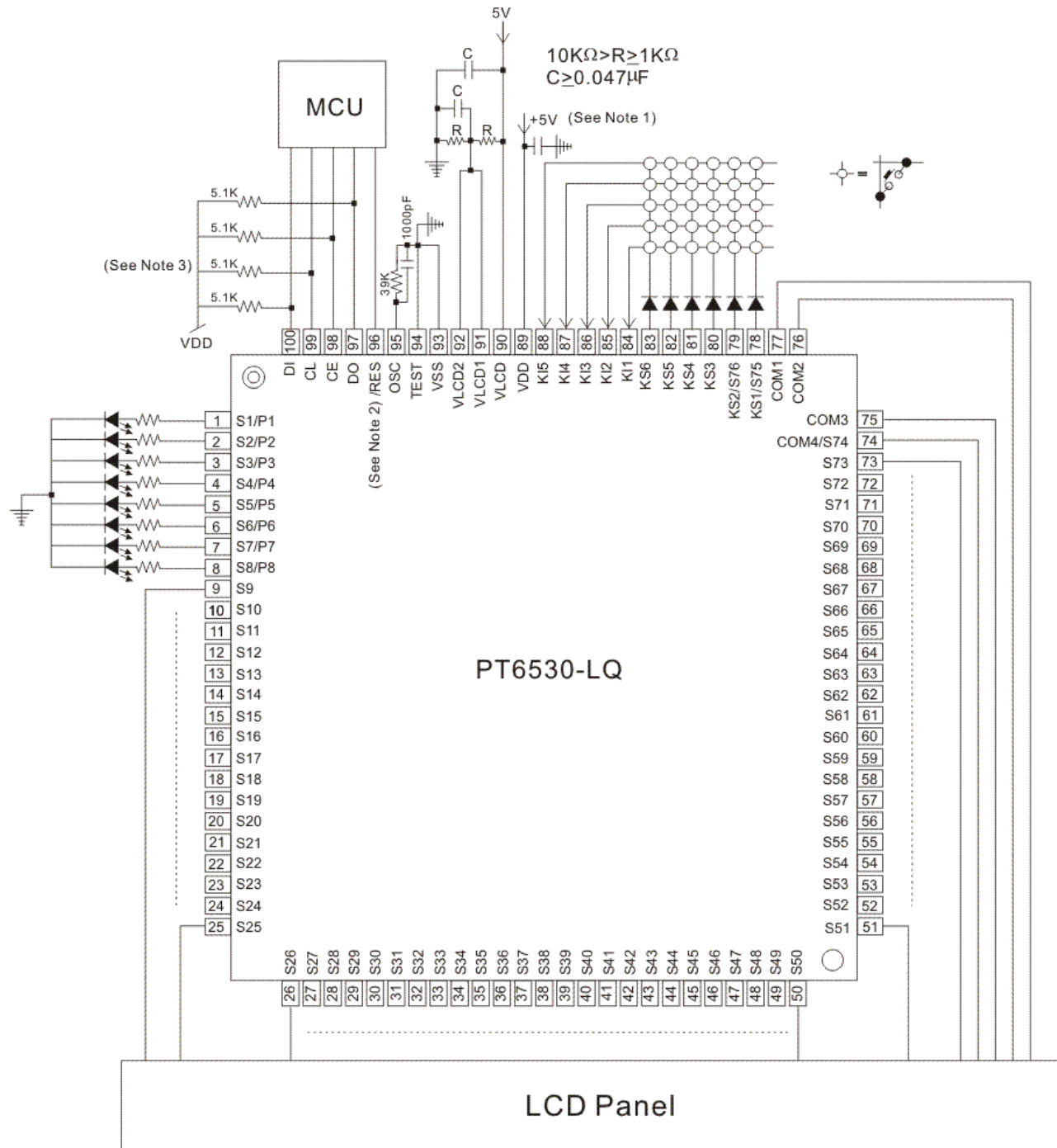
1.5 1/4 DUTY 1/2 BIAS (FOR NORMAL PANEL USE)



Notes:

1. A capacitor can be connected to the power supply line to make the power supply voltage VDD rise time (when power is applied) and the power supply voltage VDD fall time power drops) are at least 1ms when PT6530 is reset via VDET.
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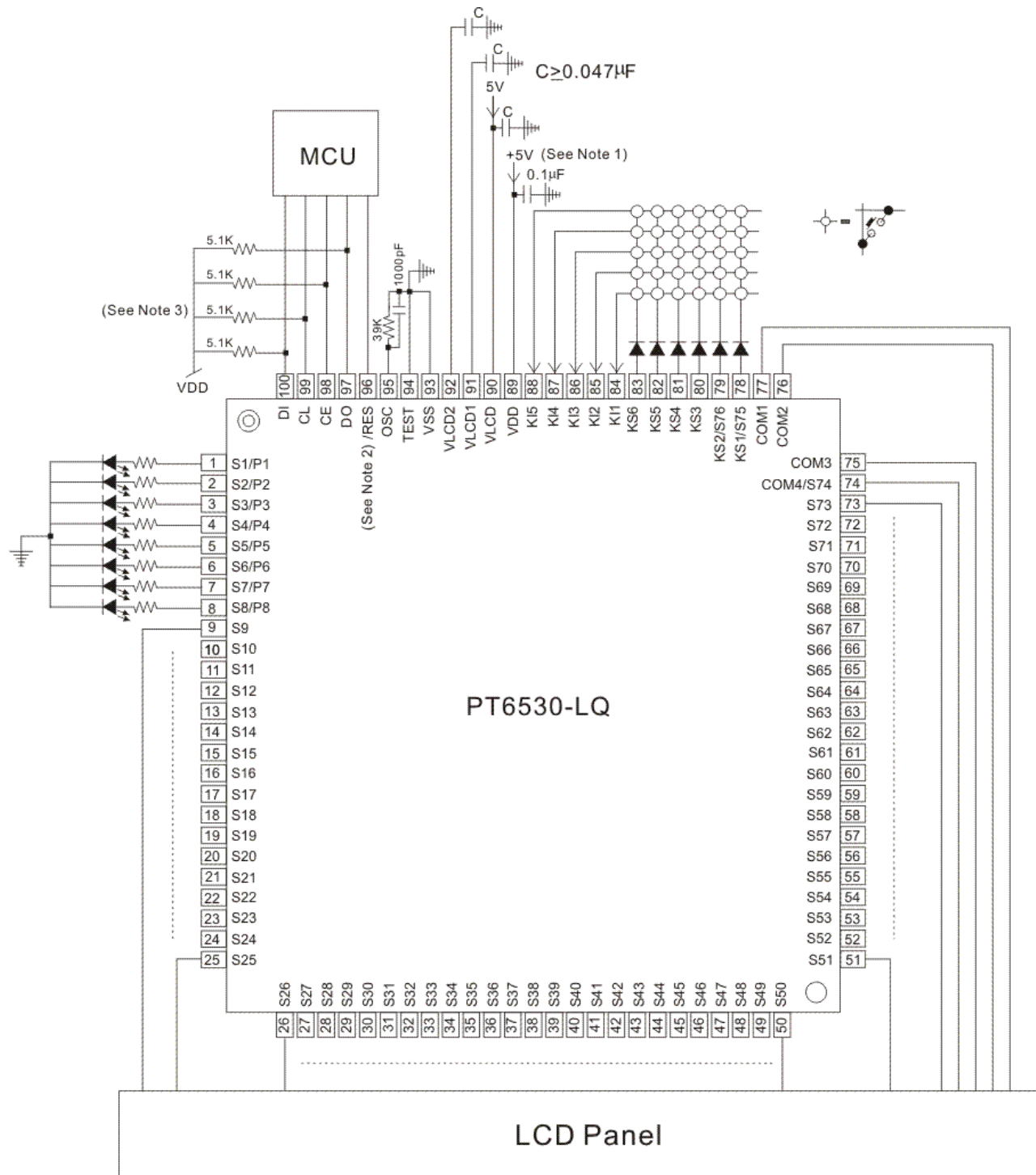
1.6 1/4 DUTY 1/2 BIAS (FOR LARGE PANEL USE)



Notes:

1. A capacitor can be connected to the power supply line to make the power supply voltage VDD rise time (when power is applied) and the power supply voltage VDD fall time power drops) are at least 1ms when PT6530 is reset via VDET.
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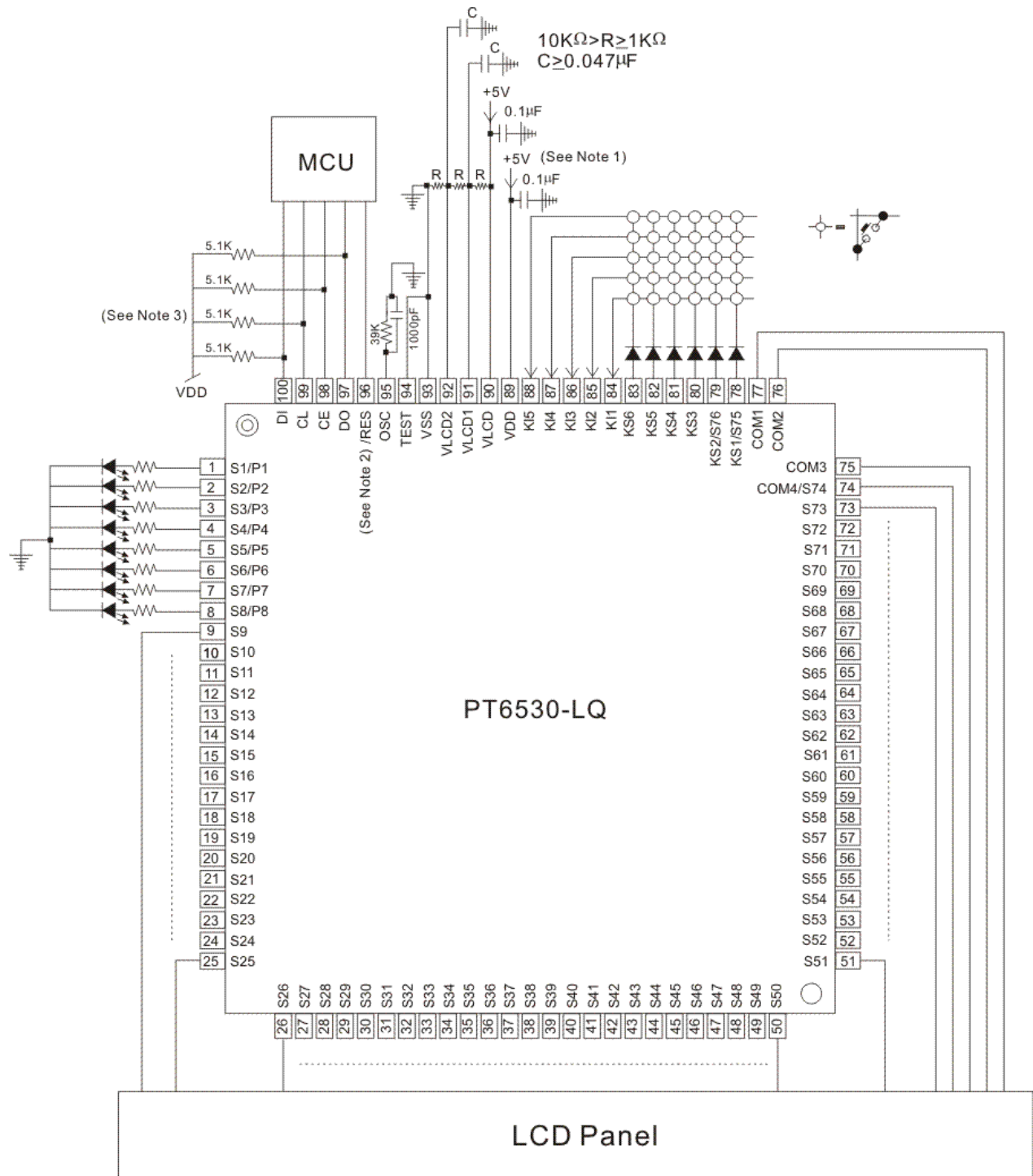
1.7 1/4 DUTY 1/3 BIAS (FOR NORMAL PANEL USE)



Notes:

- 1 A capacitor can be connected to the power supply line to make the power supply voltage VDD rise time (when power is applied) and the power supply voltage VDD fall time power drops) are at least 1ms when PT6530 is reset via VDET.
- 2 If the /RES pin is not used to initiate the System Reset Function, it must be connected VDD.
- 3 The DO pin is an open-drain output and therefore needs a pull-up resistor. This resistor is between 1K and 10KΩ. The value of this resistor must be in accordance with that capacitance of the external wiring so that the signal waveforms are in proper form.

1.8 1/4 DUTY 1/3 BIAS (FOR LARGE PANEL USE)



Notes:

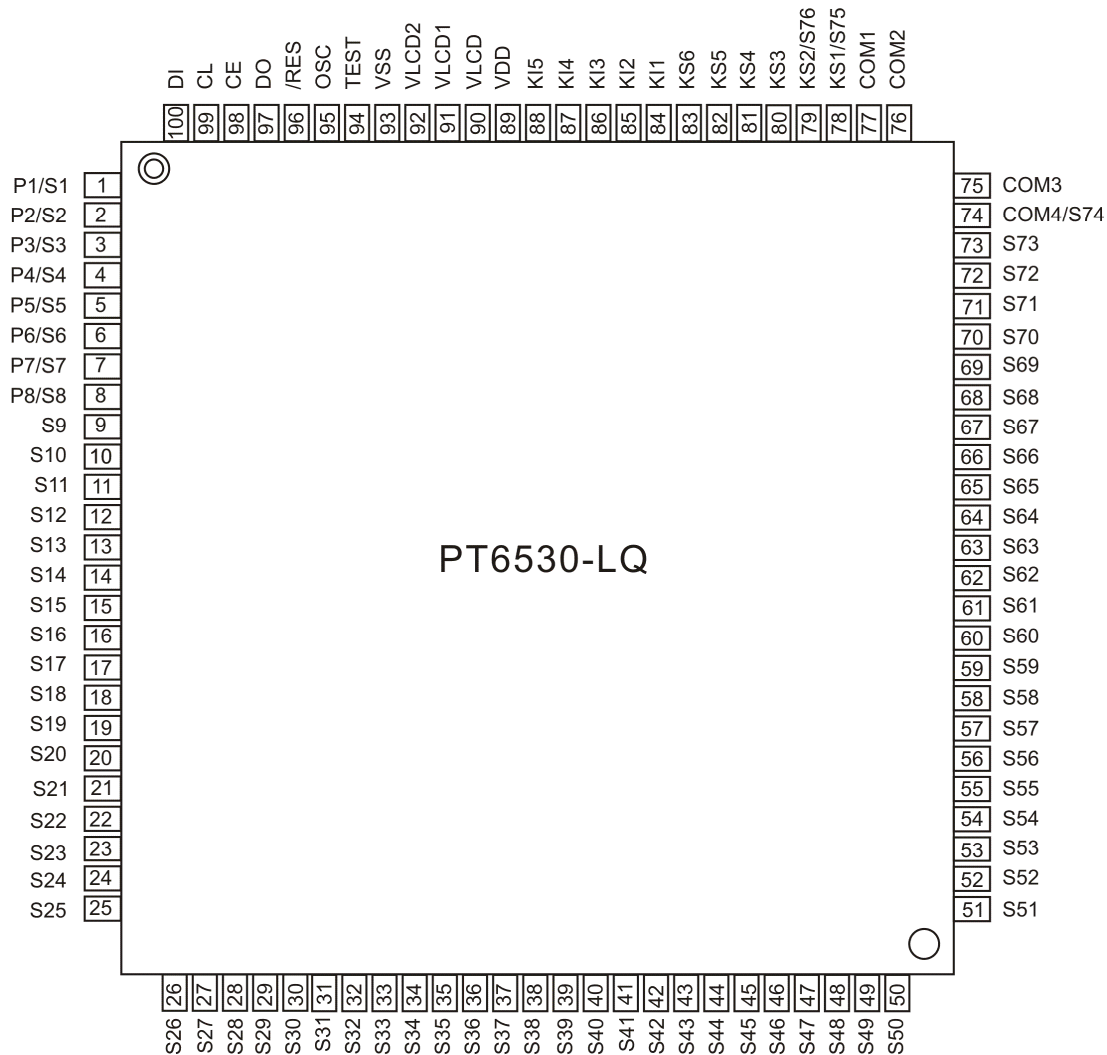
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3. The DO pin is an open-drain output and therefore needs a pull-up resistor. This resistor is between 1K and 10KΩ. The value of this resistor must be in accordance with that capacitance of the external wiring so that the signal waveforms are in proper form.



2. ORDER INFORMATION


| Valid Part Number | Package Type | Top Code |
|-------------------|----------------|-----------|
| PT6530 | 100 Pins, LQFP | PT6530-LQ |

3 PIN CONFIGURATION





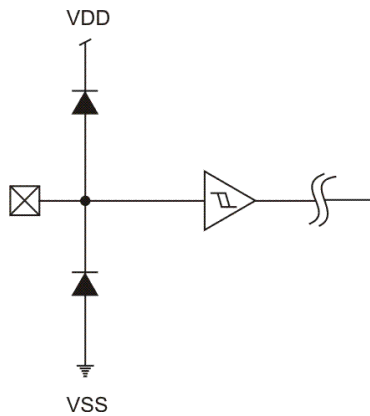
4. PIN DESCRIPTION

| Pin Name | I/O | Active | Handling when unused | Description | Pin No. |
|----------------------------------|------------------|--|----------------------|---|-----------------------|
| S1/P1 ~ S8/P8 S9 ~ S73 | O | - | OPEN | Segment outputs for displaying the display data transferred by serial data input. The S1/P1 to S8/P8 pins can be used as general-purpose output ports under serial data control. | 1 ~ 8 9 ~ 73 |
| COM1 COM2 COM3 COM4/S74 | O | - | OPEN | Common driver outputs The frame frequency fo is given by: fo = (fosc/384)Hz. The COM4/S74 pin can be used as a segment output in 1/3 duty. | 77 76 75 74 |
| KS1/S75 KS2/S76 KS3 ~ KS6 | O | - | OPEN | Key scan outputs Although normal key scan timing lines require diodes to be inserted in the timing lines to prevent shorts, since these outputs are unbalanced CMOS transistor outputs, these outputs will not be damaged by shorting when these outputs are used to form a key matrix. The KS1/S75 and KS2/S76 pins can be used as segment outputs when so specified by the control data. | 78 79 80 ~ 83 |
| KI1 ~ KI5 | I | H | GND | Key scan inputs These pins have built-in pull-down resistors. | 84 ~ 88 |
| OSC | I/O | - | VDD | Oscillator connection An oscillator circuit is formed by connecting an external resistor and capacitor at this pin. | 95 |
| CE CL DI DO | I I I O | H  - - | GND OPEN | Serial data interface connections to the controller. Note that DO, being an open-drain output, requires a pull-up resistor. CE :Chip enable CL :Synchronization clock DI :Transfer data DO :Output data | 98 99 100 97 |
| /RES | I | L | VDD | Reset signal input /RES = low.....Display off Key scan disabled All key data is reset to low /RES = high.....Display on Key scan enabled However, serial data can be transferred when /RES is low. | 96 |
| TEST | I | - | - | This pin must be connected to ground. | 94 |
| VLCD1 | I | - | OPEN | Used for applying the LCD drive 2/3 bias voltage externally. Must be connected to VLCD2 when a 1/2 bias drive scheme is used. | 91 |
| VLCD2 | I | - | OPEN | Used for applying the LCD drive 1/3 bias voltage externally. Must be connected to VLCD1 when a 1/2 bias drive scheme is used. | 92 |
| VDD | - | - | - | Logic block power supply connection. Provide a voltage of between 4.5 and 6.0V. | 89 |
| VLCD | - | - | - | LCD driver block power supply connection. Provide a voltage of between VDD -0.5 and 6.0V. | 90 |
| VSS | - | - | - | Power supply connection. Connect to ground. | 93 |

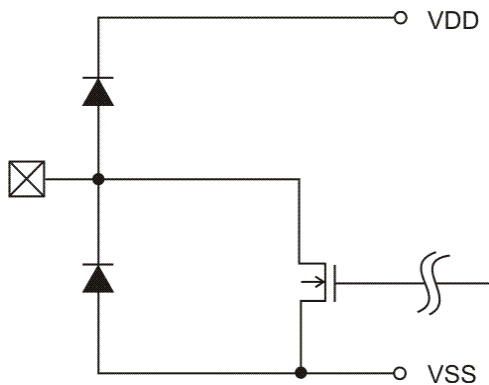
5. INPUT/OUTPUT CONFIGURATIONS

The schematic diagrams of the input and output circuits of the logic section are shown below:

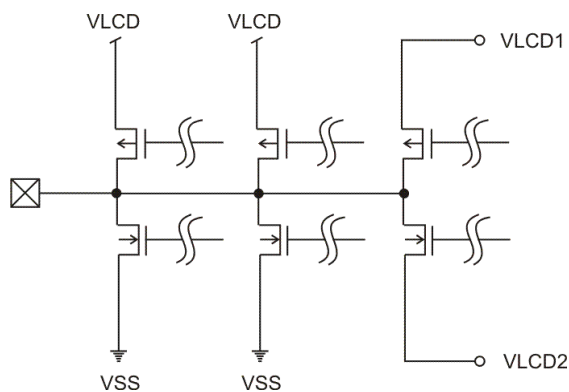
INPUT PIN: CL, CE, DI



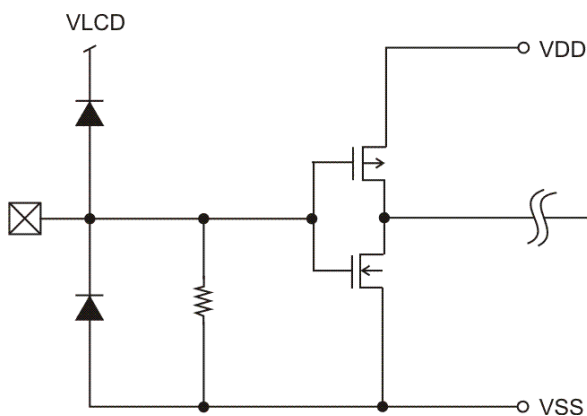
OUTPUT PIN: DO



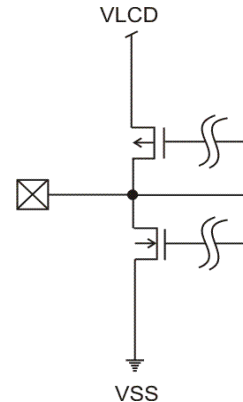
OUTPUT PIN: S1/P1 TO S8/P8, S9 TO S73, S75/KS1, S76/KS2



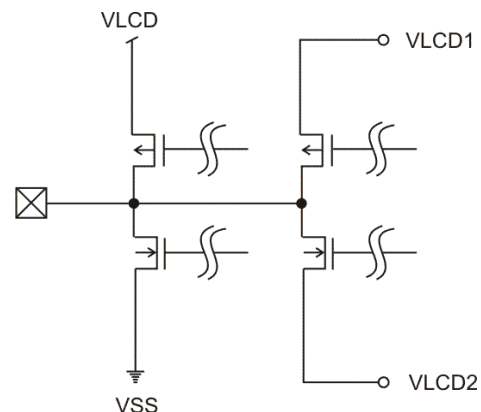
INPUT PIN: KI1 TO KI5



OUTPUT PIN: KS3 TO KS6



OUTPUT PIN: COM1 TO COM3, COM4/S74

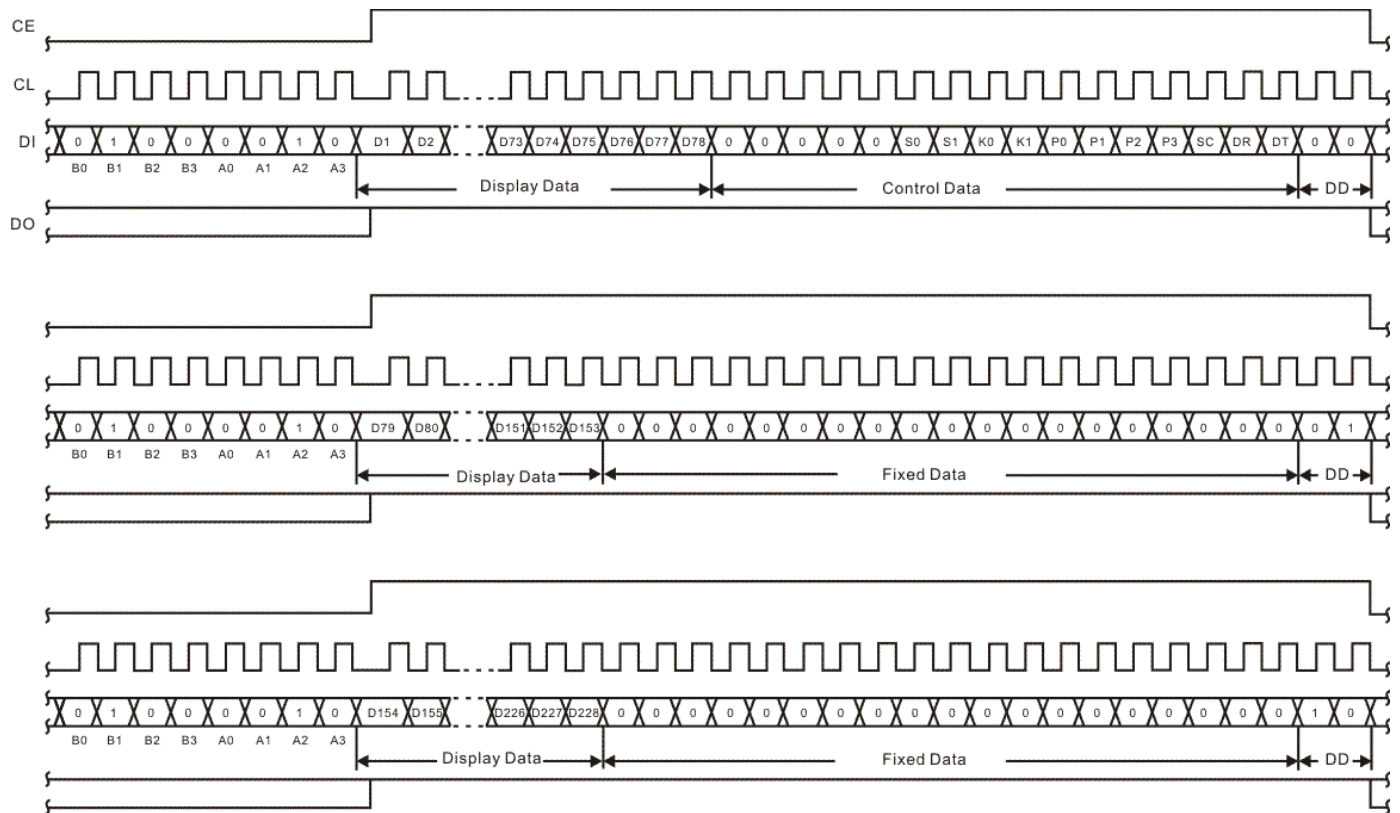


6. FUNCTION DESCRIPTION

6.1 SERIAL DATA INPUT

6.1.1 1/3 DUTY

WHEN CL IS STOPPED AT THE LOW LEVEL

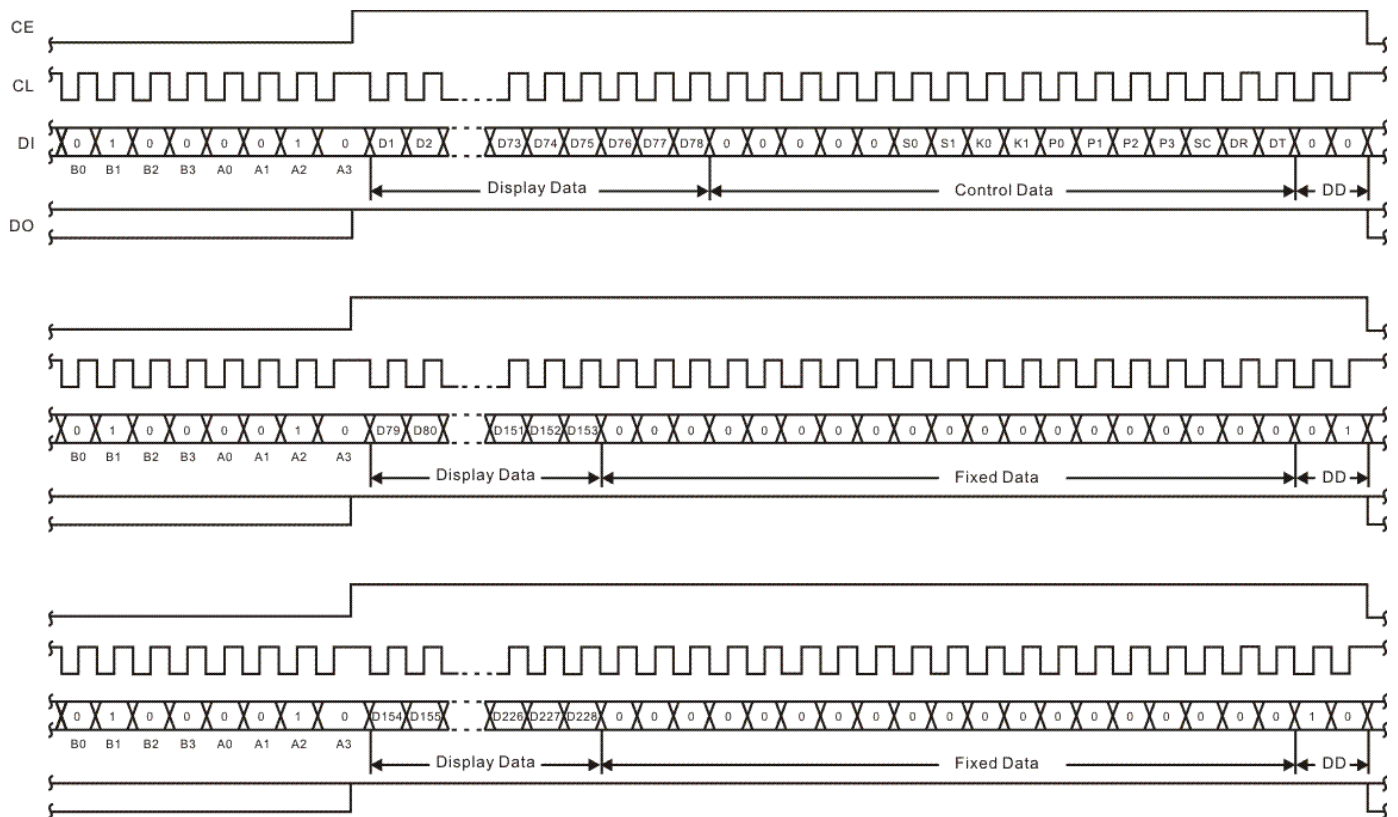


Notes:

1. B0 to B3, A0 to A3 = Serial Interface address
2. DD=Direction Date



WHEN CL IS STOPPED AT THE HIGH LEVEL



Notes:

1. B0 to B3, A0 to A3=Serial Interface address
2. DD=Direction Data

Serial Interface address: 42H

D1 to D228: Display data

S0, S1: Sleep control data

K0, K1: Key scan output/segment output selection data

P0 to P3: Segment output port/general-purpose output port selection data

SC: Segment on/off control data

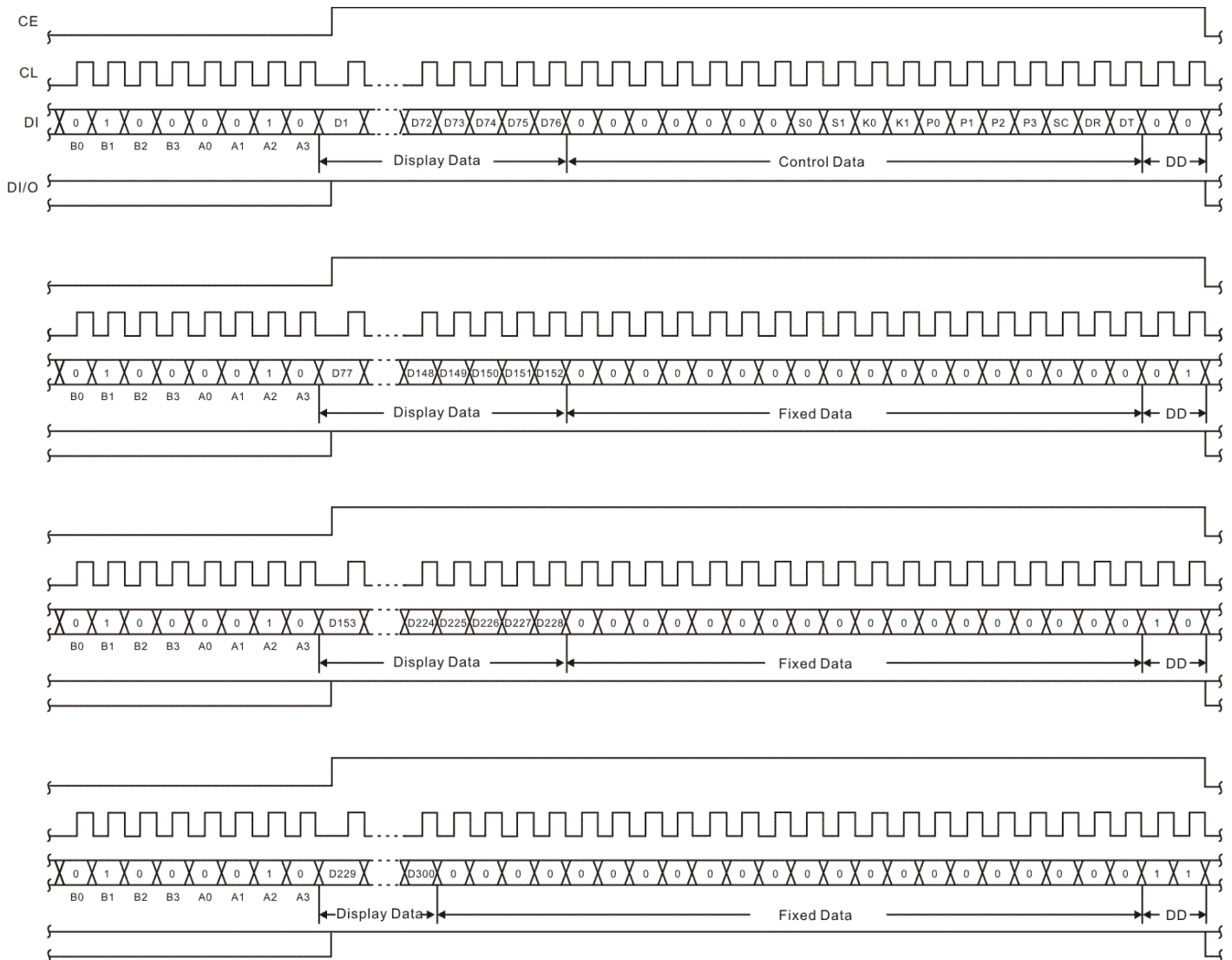
DR: 1/2 bias or 1/3 bias drive selection data

DT: 1/3 duty or 1/4 duty drive selection data



6.1.2 1/4 DUTY

WHEN CL IS STOPPED AT THE LOW LEVEL

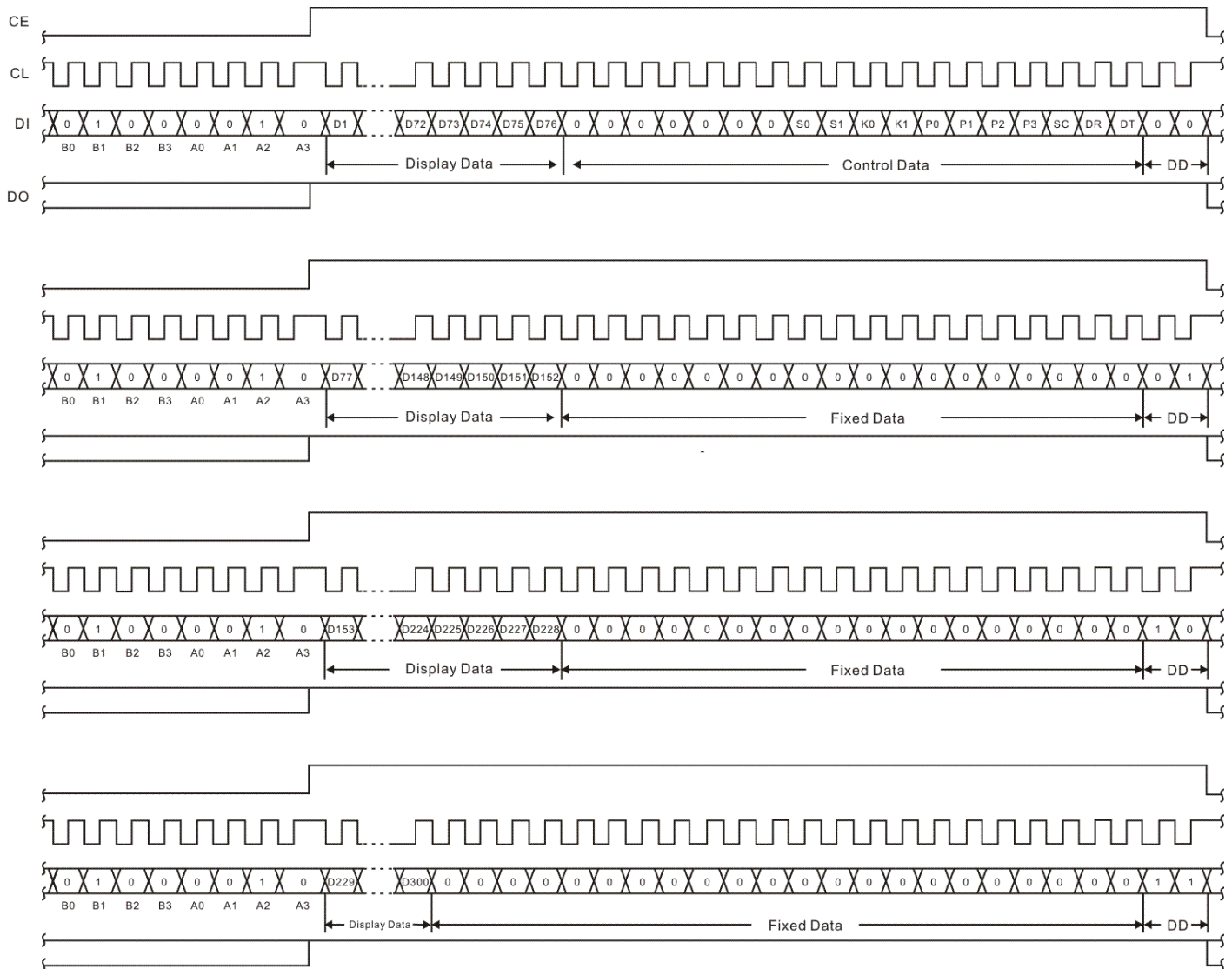


Notes:

1. B0 to B3, A0 to A3=Serial Interface address
2. DD=Direction Data



WHEN CL IS STOPPED AT THE HIGH LEVEL



Notes:

1. B0 to B3, A0 to A3=Serial Interface address
2. DD=Direction Data

Serial interface address: 42H

D1 to D228: Display data

S0, S1: Sleep control data

K0, k1: Key scan output/segment output selection data

P0 to P3: Segment output port/general-purpose output port selection data

SC: Segment on/off control data

DR: 1/2 bias or 1/3 bias drive selection data

DT: 1/3 duty or 1/4 duty drive selection data



6.2 CONTROL DATA

6.2.1 S0, S1: SLEEP CONTROL DATA

These control data bits switch between normal mode and sleep mode and set the states of the KS1 to KS6 key scan outputs during key scan standby.

| Control Data | | Mode | OSC Oscillator | Segment Outputs Common Outputs | Output Pin States During Key Scan Standby | | | | | |
|--------------|----|--------|----------------------|-----------------------------------|---|-----|-----|-----|-----|-----|
| S0 | S1 | | | | KS1 | KS2 | KS3 | KS4 | KS5 | KS6 |
| 0 | 0 | Normal | Oscillator operating | Operating | H | H | H | H | H | H |
| 0 | 1 | Sleep | Stopped | L | L | L | L | L | L | H |
| 1 | 0 | Sleep | Stopped | L | L | L | L | L | H | H |
| 1 | 1 | Sleep | Stopped | L | H | H | H | H | H | H |

Note: This assumes that the KS1/S75 and KS2/S76 output pins are selected for key scan output.

6.2.2 K0, K1: KEY SCAN OUTPUT/SEGMENT OUTPUT SELECTION DATA

These control data bits switch the functions of the KS1/S75 and KS2/S76 output pins between key scan output and segment output.

| Control Data | | Output Pin State | | Maximum Number of Input Keys |
|--------------|----|------------------|---------|------------------------------|
| K0 | K1 | KS1/S75 | KS2/S76 | |
| 0 | 0 | KS1 | KS2 | 30 |
| 0 | 1 | S75 | KS2 | 25 |
| 1 | X | S75 | S76 | 20 |

Notes:

1. X=Don't care
2. KS_n (n=1 or 2): Key scan output
3. S_n (n=75 or 76): Segment output

6.2.3 DT: 1/3 DUTY OR 1/4 DUTY DRIVE SELECTION DATA

This control data bit switches between LCD 1/3 duty or 1/4 duty drive.

| DT | Duty Drive Scheme | Output Pin State (COM4/S74) |
|----|-------------------|-----------------------------|
| 0 | 1/4 duty drive | COM4 |
| 1 | 1/3 duty drive | S74 |

Notes:

1. COM4: Common output
2. S74: Segment output

6.2.4 P0 TO P3: SEGMENT OUTPUT/GENERAL-PURPOSE OUTPUT PORT SELECTION DATA

These control data bits switch the functions of the S1/P1 to S8/P8 output pins between the segment output port and the general-purpose output port.

| Control Data | | | | Output Pin State | | | | | | | |
|--------------|----|----|----|------------------|-------|-------|-------|-------|-------|-------|-------|
| P0 | P1 | P2 | P3 | S1/P1 | S2/P2 | S3/P3 | S4/P4 | S5/P5 | S6/P6 | S7/P7 | S8/P8 |
| 0 | 0 | 0 | 0 | S1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 |
| 0 | 0 | 0 | 1 | P1 | S2 | S3 | S4 | S5 | S6 | S7 | S8 |
| 0 | 0 | 1 | 0 | P1 | P2 | S3 | S4 | S5 | S6 | S7 | S8 |
| 0 | 0 | 1 | 1 | P1 | P2 | P3 | S4 | S5 | S6 | S7 | S8 |
| 0 | 1 | 0 | 0 | P1 | P2 | P3 | P4 | S5 | S6 | S7 | S8 |
| 0 | 1 | 0 | 1 | P1 | P2 | P3 | P4 | P5 | S6 | S7 | S8 |
| 0 | 1 | 1 | 0 | P1 | P2 | P3 | P4 | P5 | P6 | S7 | S8 |
| 0 | 1 | 1 | 1 | P1 | P2 | P3 | P4 | P5 | P6 | P7 | S8 |
| 1 | 0 | 0 | 0 | P1 | P2 | P3 | P4 | P5 | P6 | P7 | P8 |

Notes:

1. Sn (n=1 to 8): Segment output port
2. Pn (n=1 to 8): General-purpose output port

The table below lists the correspondence between the display data and the output pins when these pins are selected to be general-purpose output ports.

| Output Pin | Corresponding Display Data | |
|------------|----------------------------|----------|
| | 1/3 Duty | 1/4 Duty |
| S1/P1 | D1 | D1 |
| S2/P2 | D4 | D5 |
| S3/P3 | D7 | D9 |
| S4/P3 | D10 | D13 |
| S5/P5 | D13 | D17 |
| S6/P6 | D16 | D21 |
| S7/P7 | D19 | D25 |
| S8/P8 | D22 | D29 |

For example, if the circuit is operated in 1/4 duty and the S4/P4 output pin is selected to be a general-purpose output port, the S4/P4 output pin will output a high level (VLCD) when the display data D13 is 1, and will output a low level (Vss) when D13 is 0.

6.2.5 SC: SEGMENT ON/OFF CONTROL DATA

This control data bit controls the on/off state of the segments.

| SC | Display State |
|----|---------------|
| 0 | On |
| 1 | Off |

However, note that when the segments are turned off by setting SC to 1, the segments are turned off by outputting segment off waveforms from the segment output pins.

6.2.6 DR: 1/2 BIAS OR 1/3 BIAS DRIVE SELECTION DATA

This control data bit switches between LCD 1/2 bias or 1/3 bias drive.

| DR | Bias Drive Scheme |
|----|-------------------|
| 0 | 1/3 bias drive |
| 1 | 1/2 bias drive |



6.3 DISPLAY DATA AND OUTPUT PI CORRESPONDENCE

6.3.1 1/3 DUTY

| Output Pin | COM1 | COM2 | COM3 | Output Pin | COM1 | COM2 | COM3 | Output Pin | COM1 | COM2 | COM3 |
|------------|------|------|------|------------|------|------|------|------------|------|------|------|
| S1/P1 | D1 | D2 | D3 | S27 | D79 | D80 | D81 | S53 | D157 | D158 | D159 |
| S2/P2 | D4 | D5 | D6 | S28 | D82 | D83 | D84 | S54 | D160 | D161 | D162 |
| S3/P3 | D7 | D8 | D9 | S29 | D85 | D86 | D87 | S55 | D163 | D164 | D165 |
| S4/P4 | D10 | D11 | D12 | S30 | D88 | D89 | D90 | S56 | D166 | D167 | D168 |
| S5/P5 | D13 | D14 | D15 | S31 | D91 | D92 | D93 | S57 | D169 | D170 | D171 |
| S6/P6 | D16 | D17 | D18 | S32 | D94 | D95 | D96 | S58 | D172 | D173 | D174 |
| S7/P7 | D19 | D20 | D21 | S33 | D97 | D98 | D99 | S59 | D175 | D176 | D177 |
| S8/P8 | D22 | D23 | D24 | S34 | D100 | D101 | D102 | S60 | D178 | D179 | D180 |
| S9 | D25 | D26 | D27 | S35 | D103 | D104 | D105 | S61 | D181 | D182 | D183 |
| S10 | D28 | D29 | D30 | S36 | D106 | D107 | D108 | S62 | D184 | D185 | D186 |
| S11 | D31 | D32 | D33 | S37 | D109 | D110 | D111 | S63 | D187 | D188 | D189 |
| S12 | D34 | D35 | D36 | S38 | D112 | D113 | D114 | S64 | D190 | D191 | D192 |
| S13 | D37 | D38 | D39 | S39 | D115 | D116 | D117 | S65 | D193 | D194 | D195 |
| S14 | D40 | D41 | D42 | S40 | D118 | D119 | D120 | S66 | D196 | D197 | D198 |
| S15 | D43 | D44 | D45 | S41 | D121 | D122 | D123 | S67 | D199 | D200 | D201 |
| S16 | D46 | D47 | D48 | S42 | D124 | D125 | D126 | S68 | D202 | D203 | D204 |
| S17 | D49 | D50 | D51 | S43 | D127 | D128 | D129 | S69 | D205 | D206 | D207 |
| S18 | D52 | D53 | D54 | S44 | D130 | D131 | D132 | S70 | D208 | D209 | D210 |
| S19 | D55 | D56 | D57 | S45 | D133 | D134 | D135 | S71 | D211 | D212 | D213 |
| S20 | D58 | D59 | D60 | S46 | D136 | D137 | D138 | S72 | D214 | D215 | D216 |
| S21 | D61 | D62 | D63 | S47 | D139 | D140 | D141 | S73 | D217 | D218 | D219 |
| S22 | D64 | D65 | D66 | S48 | D142 | D143 | D144 | COM4/S74 | D220 | D221 | D222 |
| S23 | D67 | D68 | D69 | S49 | D145 | D146 | D147 | KS1/S75 | D223 | D224 | D225 |
| S24 | D70 | D71 | D72 | S50 | D148 | D149 | D150 | KS2/S76 | D226 | D227 | D228 |
| S25 | D73 | D74 | D75 | S51 | D151 | D152 | D153 | | | | |
| S26 | D76 | D77 | D78 | S52 | D154 | D155 | D156 | | | | |

Note: This is for the case where the output pins S1/P1 to S8/P8, COM4/S74, KS1/S75 and KS2/S76 are selected for use as segment outputs.

For example, the table below lists the operation of the S11 segment output pin.

| Display Data | | | Output Pin State (S11) |
|--------------|-----|-----|---|
| D31 | D32 | D33 | |
| 0 | 0 | 0 | The LCD segments for COM1, COM2 and COM3 are off. |
| 0 | 0 | 1 | The LCD segment for COM3 is on. |
| 0 | 1 | 0 | The LCD segment for COM2 is on. |
| 0 | 1 | 1 | The LCD segments for COM2 and COM3 are on. |
| 1 | 0 | 0 | The LCD segment for COM1 is on. |
| 1 | 0 | 1 | The LCD segments for COM 1 and COM3 are on. |
| 1 | 1 | 0 | The LCD segments for COM1 and COM2 are on. |
| 1 | 1 | 1 | The LCD segments for COM1, COM2 and COM3 are on. |



6.3.2 1/4 DUTY

| Output Pin | COM1 | COM2 | COM3 | COM4 |
|------------|------|------|------|------|
| S1/P1 | D1 | D2 | D3 | D4 |
| S2/P2 | D5 | D6 | D7 | D8 |
| S3/P3 | D9 | D10 | D11 | D12 |
| S4/P4 | D13 | D14 | D15 | D16 |
| S5/P5 | D17 | D18 | D19 | D20 |
| S6/P6 | D21 | D22 | D23 | D24 |
| S7/P7 | D25 | D26 | D27 | D28 |
| S8/P8 | D29 | D30 | D31 | D32 |
| S9 | D33 | D34 | D35 | D36 |
| S10 | D37 | D38 | D39 | D40 |
| S11 | D41 | D42 | D43 | D44 |
| S12 | D45 | D46 | D47 | D48 |
| S13 | D49 | D50 | D51 | D52 |
| S14 | D53 | D54 | D55 | D56 |
| S15 | D57 | D58 | D59 | D60 |
| S16 | D61 | D62 | D63 | D64 |
| S17 | D65 | D66 | D67 | D68 |
| S18 | D69 | D70 | D71 | D72 |
| S19 | D73 | D74 | D75 | D76 |
| S20 | D77 | D78 | D79 | D80 |
| S21 | D81 | D82 | D83 | D84 |
| S22 | D85 | D86 | D87 | D88 |
| S23 | D89 | D90 | D91 | D92 |
| S24 | D93 | D94 | D95 | D96 |
| S25 | D97 | D98 | D99 | D100 |
| S26 | D101 | D102 | D103 | D104 |
| S27 | D105 | D106 | D107 | D108 |
| S28 | D109 | D110 | D111 | D112 |
| S29 | D113 | D114 | D115 | D116 |
| S30 | D117 | D118 | D119 | D120 |
| S31 | D121 | D122 | D123 | D124 |
| S32 | D125 | D126 | D127 | D128 |
| S33 | D129 | D130 | D131 | D132 |
| S34 | D133 | D134 | D135 | D136 |
| S35 | D137 | D138 | D139 | D140 |
| S36 | D141 | D142 | D143 | D144 |
| S37 | D145 | D146 | D147 | D148 |
| S38 | D149 | D150 | D151 | D152 |

| Output Pin | COM1 | COM2 | COM3 | COM4 |
|------------|------|------|------|------|
| S39 | D153 | D154 | D155 | D156 |
| S40 | D157 | D158 | D159 | D160 |
| S41 | D161 | D162 | D163 | D164 |
| S42 | D165 | D166 | D167 | D168 |
| S43 | D169 | D170 | D171 | D172 |
| S44 | D173 | D174 | D175 | D176 |
| S45 | D177 | D178 | D179 | D180 |
| S46 | D181 | D182 | D183 | D184 |
| S47 | D185 | D186 | D187 | D188 |
| S48 | D189 | D190 | D191 | D192 |
| S49 | D193 | D194 | D195 | D196 |
| S50 | D197 | D198 | D199 | D200 |
| S51 | D201 | D202 | D203 | D204 |
| S52 | D205 | D206 | D207 | D208 |
| S53 | D209 | D210 | D211 | D212 |
| S54 | D213 | D214 | D215 | D216 |
| S55 | D217 | D218 | D219 | D220 |
| S56 | D221 | D222 | D223 | D224 |
| S57 | D225 | D226 | D227 | D228 |
| S58 | D229 | D230 | D231 | D232 |
| S59 | D233 | D234 | D235 | D236 |
| S60 | D237 | D238 | D239 | D240 |
| S61 | D241 | D242 | D243 | D244 |
| S62 | D245 | D246 | D247 | D248 |
| S63 | D249 | D250 | D251 | D252 |
| S64 | D453 | D254 | D255 | D256 |
| S65 | D257 | D258 | D259 | D260 |
| S66 | D261 | D262 | D263 | D264 |
| S67 | D265 | D266 | D267 | D268 |
| S68 | D269 | D270 | D271 | D272 |
| S69 | D273 | D274 | D275 | D276 |
| S70 | D277 | D278 | D279 | D280 |
| S71 | D281 | D282 | D283 | D284 |
| S72 | D285 | D286 | D287 | D288 |
| S73 | D289 | D290 | D291 | D292 |
| KS1/S75 | D293 | D294 | D295 | D296 |
| KS2/S76 | D297 | D298 | D299 | D300 |

Note: This is for the case where the output pins S1/P1 to S8/P8, KS1/S75 and KS2/S76 are selected for use as segment outputs.

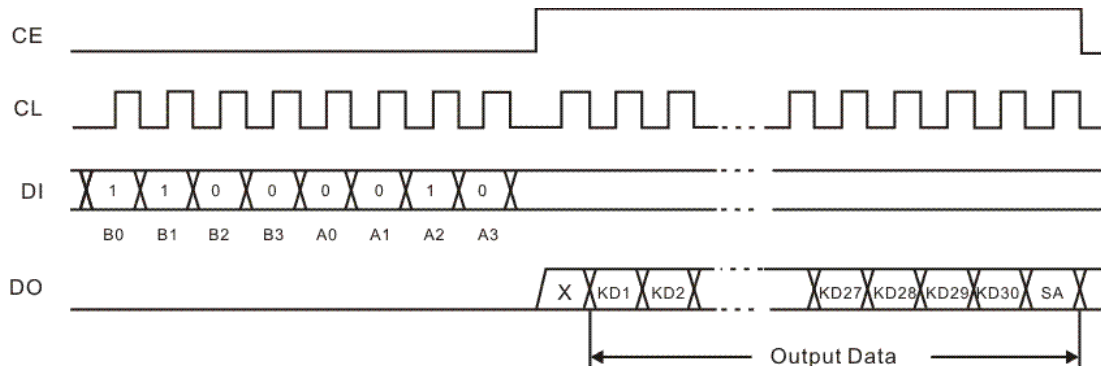


For example, the table below lists the segment output states for the S11 output pin.

| Display Data | | | | Output Pin State (S11) |
|--------------|-----|-----|-----|--|
| D41 | D42 | D43 | D44 | |
| 0 | 0 | 0 | 0 | The LCD segment for COM1, COM2, COM3 and COM4 are off. |
| 0 | 0 | 0 | 1 | The LCD segment for COM4 is on. |
| 0 | 0 | 1 | 0 | The LCD segment for COM3 is on. |
| 0 | 0 | 1 | 1 | The LCD segments for COM3 and COM4 are on. |
| 0 | 1 | 0 | 0 | The LCD segment for COM2 is on. |
| 0 | 1 | 0 | 1 | The LCD segments for COM2 and COM4 are on. |
| 0 | 1 | 1 | 0 | The LCD segments for COM2 and COM3 are on. |
| 0 | 1 | 1 | 1 | The LCD segments for COM2, COM3 and COM4 are on. |
| 1 | 0 | 0 | 0 | The LCD segment for COM1 is on. |
| 1 | 0 | 0 | 1 | The LCD segments for COM1 and COM4 are on. |
| 1 | 0 | 1 | 0 | The LCD segments for COM1 and COM3 are on. |
| 1 | 0 | 1 | 1 | The LCD segments for COM1, COM3 and COM4 are on. |
| 1 | 1 | 0 | 0 | The LCD segments for COM1 and COM2 are on. |
| 1 | 1 | 0 | 1 | The LCD segments for COM1, COM2 and COM4 are on. |
| 1 | 1 | 1 | 0 | The LCD segments for COM1, COM2 and COM3 are on. |
| 1 | 1 | 1 | 1 | The LCD segments for COM1, COM2, COM3 and COM4 are on. |

6.4 SERIAL DATA OUTPUT

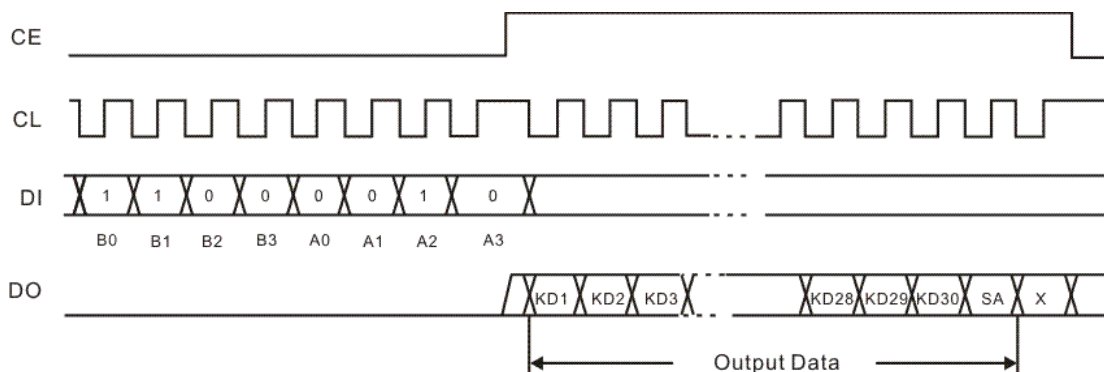
WHEN CL IS STOPPED AT THE LOW LEVEL



Notes:

1. X=Don't care
2. B0 to B3, A0 to A3: Serial Interface address

WHEN CL IS STOPPED AT THE HIGH LEVEL



Notes:

1. X=Don't care
2. B0 to B3, A0 to A3: Serial Interface address
3. Serial Interface address: 43H
4. KD1 to KD30: Key data
5. SA: Sleep acknowledge data
6. If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

6.5 OUTPUT DATA

6.5.1 KD1 TO KD30: KEY DATA

When a key matrix of up to 30 keys is formed from the KS1 to KS6 output pins and the KI1 to KI5 input pins and one of those keys is pressed, the key output data corresponding to that key will be set to 1. The table shows the relationship between those pins and the key data bits.

| Item | KI1 | KI2 | KI3 | KI4 | KI5 |
|---------|------|------|------|------|------|
| KS1/S75 | KD1 | KD2 | KD3 | KD4 | KD5 |
| KS2/S76 | KD6 | KD7 | KD8 | KD9 | KD10 |
| KS3 | KD11 | KD12 | KD13 | KD14 | KD15 |
| KS4 | KD16 | KD17 | KD18 | KD19 | KD20 |
| KS5 | KD21 | KD22 | KD23 | KD24 | KD25 |
| KS6 | KD26 | KD27 | KD28 | KD29 | KD30 |

When the KS1/S75 and KS2/S76 output pins are selected to be segment outputs by control data bits K0 and K1 and a key matrix of up to 20 keys is formed using the KS3 to KS6 output pins and the KI1 to KI5 input pins, the KD1 to KD10 key data bits will be set to 0.

6.5.2 SA: SLEEP ACKNOWLEDGE DATA

This output data is set to the state when the key was pressed. In that case DO will go to the low level. If serial data is input during this period and the mode is set (normal mode or sleep mode), the IC will be set to that mode. SA is set to 1 in the sleep mode and to 0 in the normal mode.

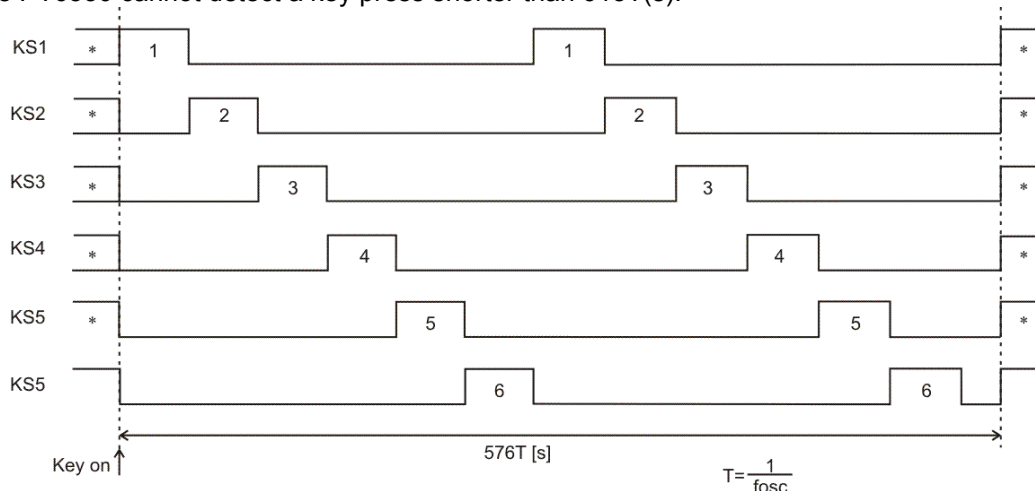
6.6 SLEEP MODE

Sleep mode is set up by setting S0 or S1 in the control data to 1. The segment outputs will all go low and the common outputs will also go low, and the oscillator on the OSC pin will stop (it will be started by a key press). This reduces power dissipation. This mode is cleared by sending control data with both S0 and S1 set to 0. However, note that the S1/P1 to S8/P8 outputs can be used as general-purpose output ports according to the state of the P0 to P3 control data bits, even in sleep mode. (See the control data description for details.)

6.7 KEY SCAN OPERATION FUNCTIONS

6.7.1 KEY SCAN TIMING

The key scan period is $288T(s)$. To reliably determine the on/off state of the keys, the PT6530 scans the keys twice and determines that a key has been pressed when the key data agrees. It outputs a key data read request (a low level on DO) $615T(s)$ after starting a key scan. If the key data does not agree and a key was pressed at that point, it scans the keys again. Thus the PT6530 cannot detect a key press shorter than $615T(s)$.



Note:

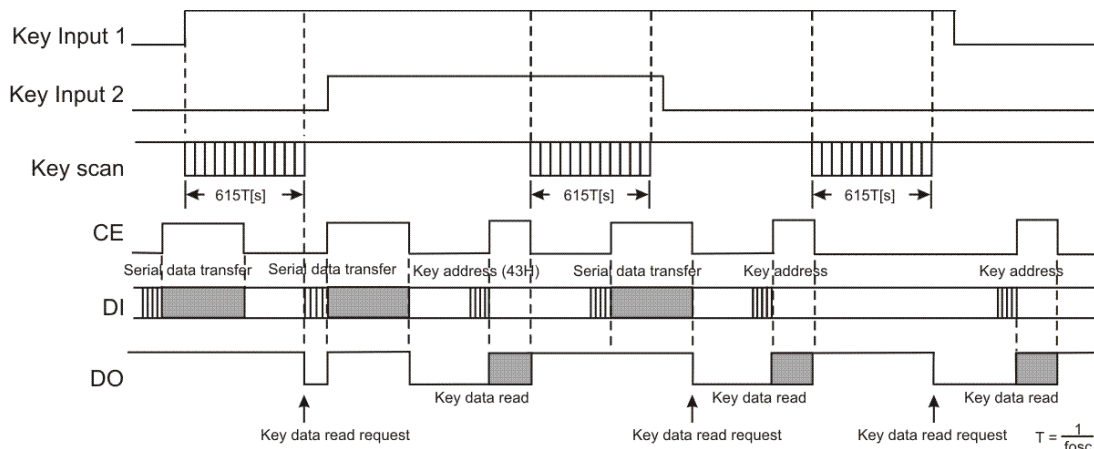
*: In sleep mode the high/low state of these pins is determined by the S0 and S1 bits in the control data. Key scan output signals are not output from pins that are set low.

6.7.2 IN NORMAL MODE

- The pins KS1 to KS6 are set high.
- When a key is pressed a key scan is started and the keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
- If a key is pressed for longer than $615T(s)$ (Where $T = \frac{1}{f_{osc}}$) the PT6530 outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.

level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.

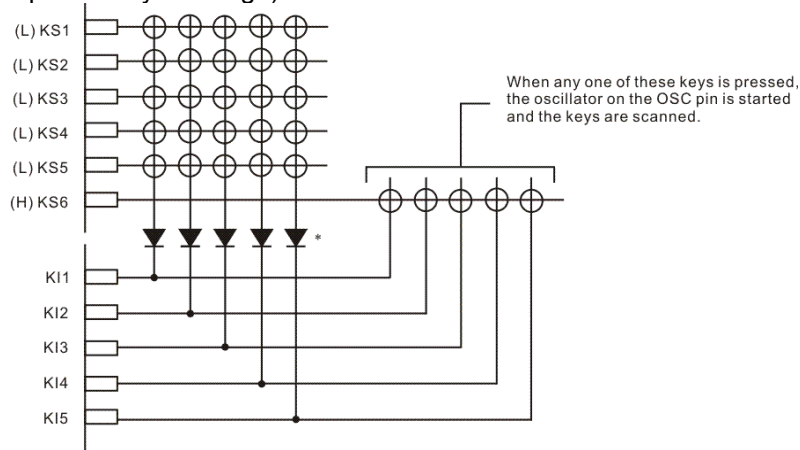
After the controller reads the key data, the key data read request is cleared (DO is set high) and the PT6530 performs another key scan. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1 and 10KΩ).



6.7.3 IN SLEEP MODE

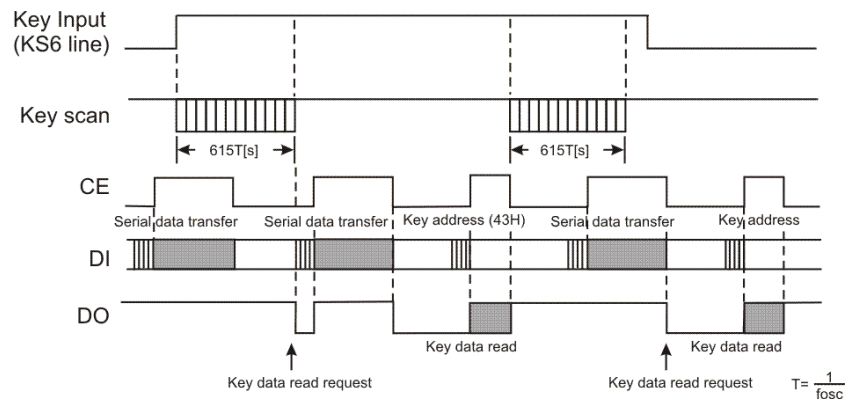
- The pins KS1 to KS6 are set to high or low by the S0 and S1 bits in the control data. (See the control data description for details.)
- If a key on one of the lines corresponding to a KS1 to KS6 pin which is set high is pressed, the oscillator on the OSC pin is started and a key scan is performed. Keys are scanned until all keys are released. Multiple key presses are recognized by determining whether multiple key data bits are set.
- If a key is pressed for longer than $615T(s)$ (Where $T = \frac{1}{f_{osc}}$) the PT6530 outputs a key data read request (a low level on DO) to the controller. The controller acknowledges this request and reads the key data. However, if CE is high during a serial data transfer, DO will be set high.
- After the controller reads the key data, the key data read request is cleared (DO is set high) and the PT6530 performs another key scan. However, this does not clear sleep mode. Also note that DO, being an open-drain output, requires a pull-up resistor (between 1 and 10K Ω).
- Sleep mode key scan example

Example: S0=0, S1=1 (sleep with only KS6 high)



Note:

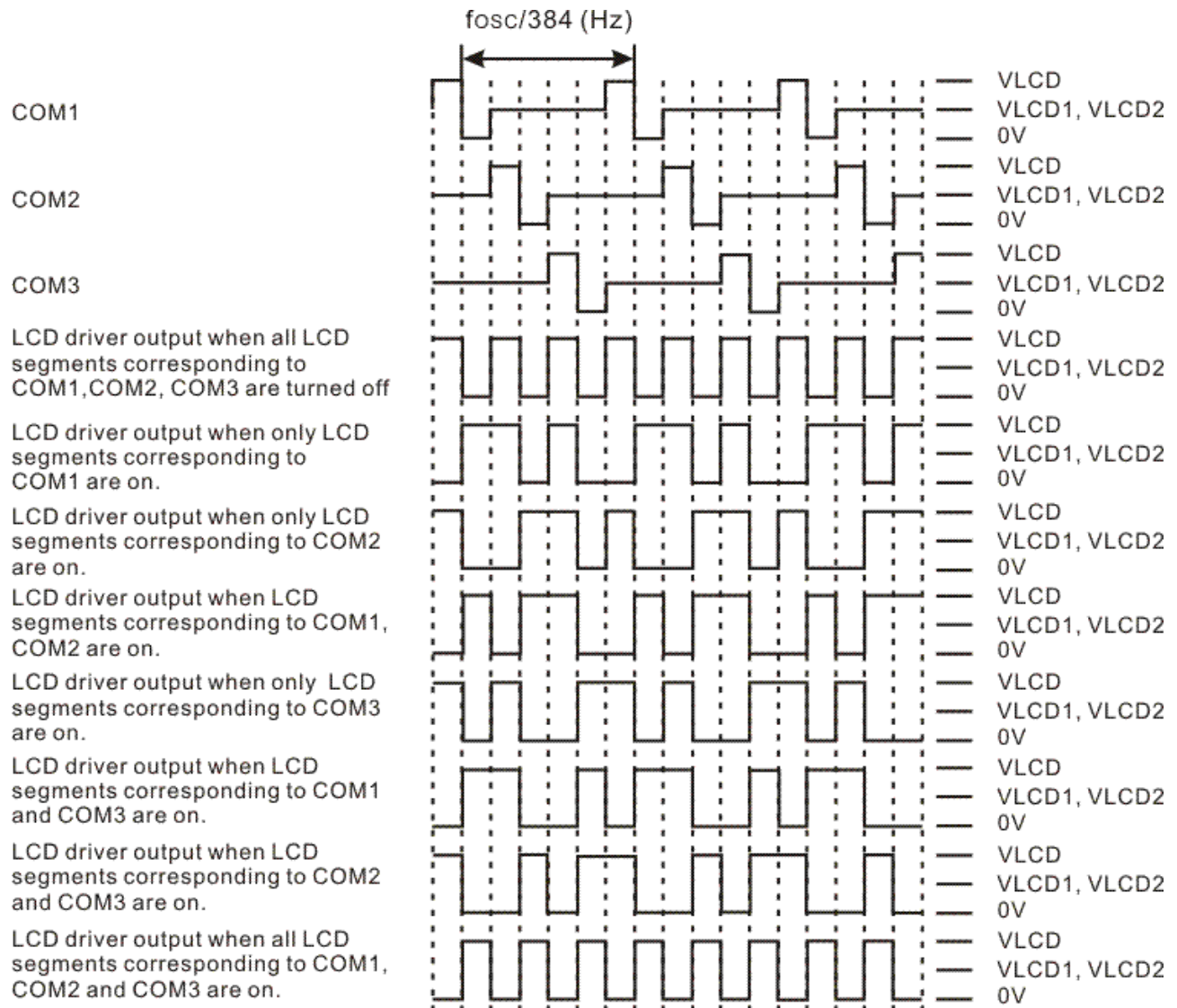
*: These diodes are required to reliably recognize multiple key presses on the KS6 line when sleep mode state with only KS6 high, as in the above example. That is, these diodes prevent incorrect operations due to sneak currents in the KS6 key scan output signal when keys on the KS1 to KS5 lines are pressed at the same time.



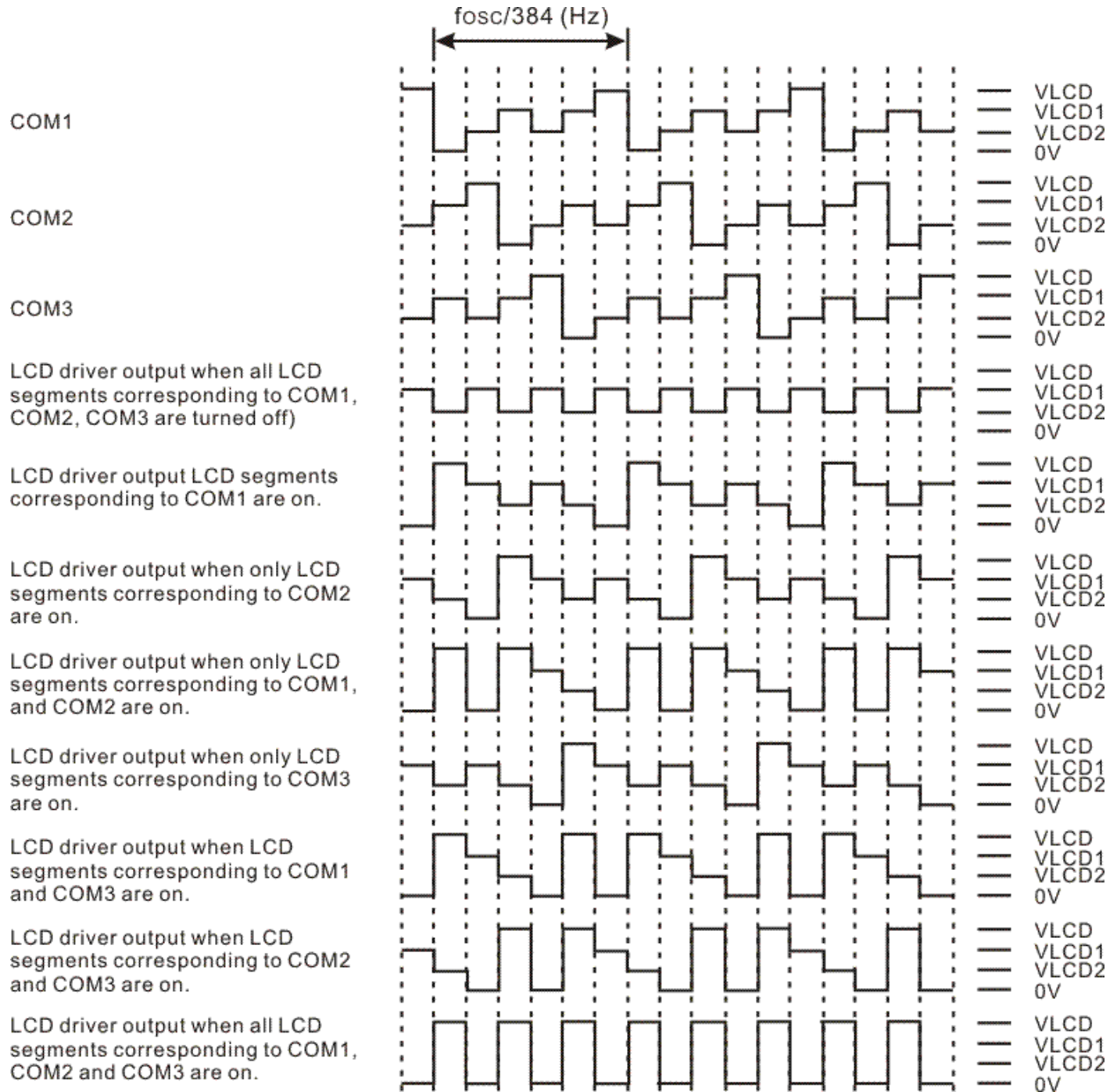
6.8 MULTIPLE KEY PRESSES

Although the PT6530 is capable of key scanning without inserting diodes for dual key presses, triple key presses on the K11 to K15 input pin lines, or multiple key presses on the KS1 to KS6 output pin lines, multiple presses other than these cases may result in keys that were not pressed recognized as having been pressed. Therefore, a diode must be inserted in series with each key. Applications that do not recognize multiple key presses of three or more keys should check the key data for three or more 1 bit and ignore such data.

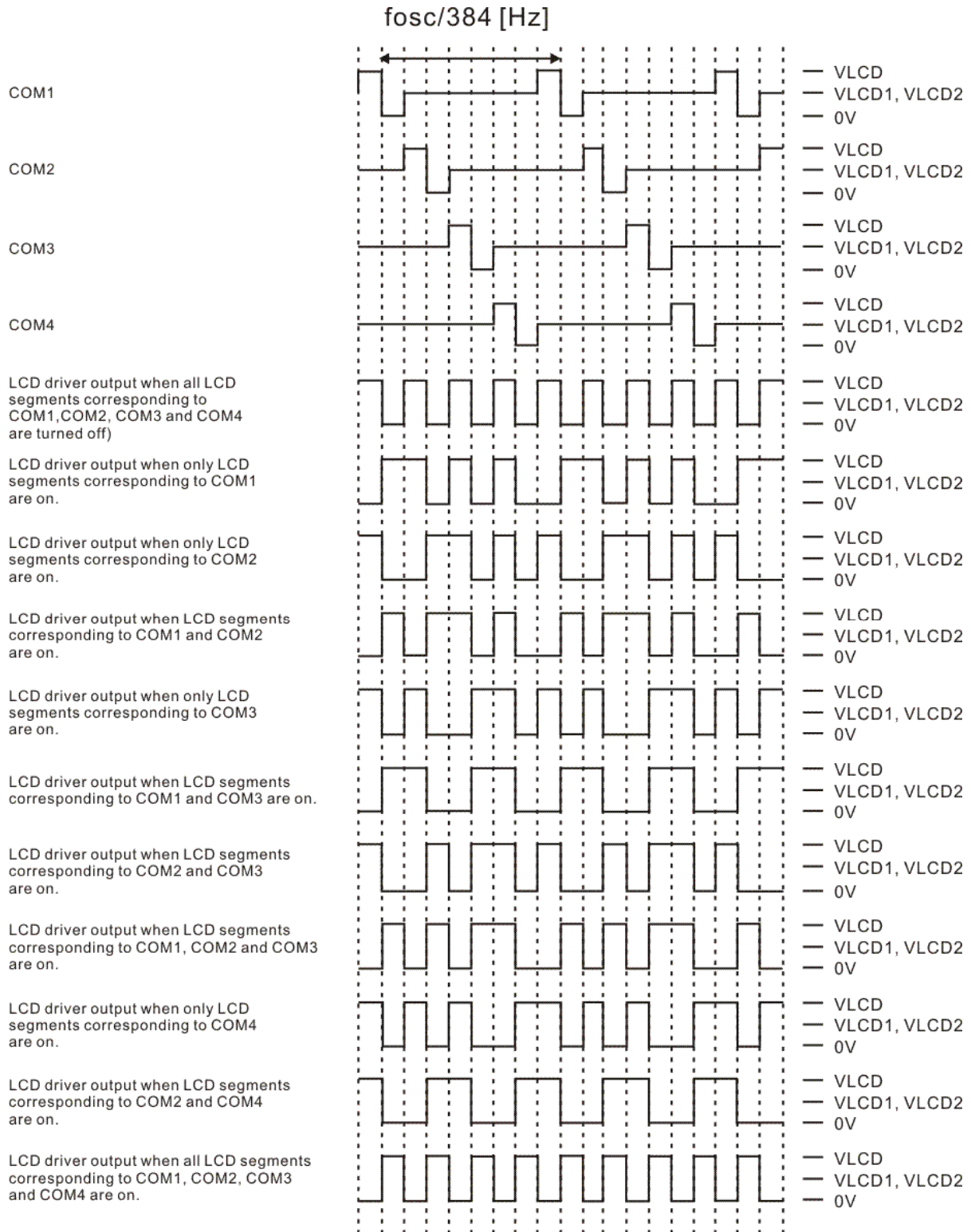
6.9 1/3 DUTY, 1/2 BIAS DRIVE TECHNIQUE



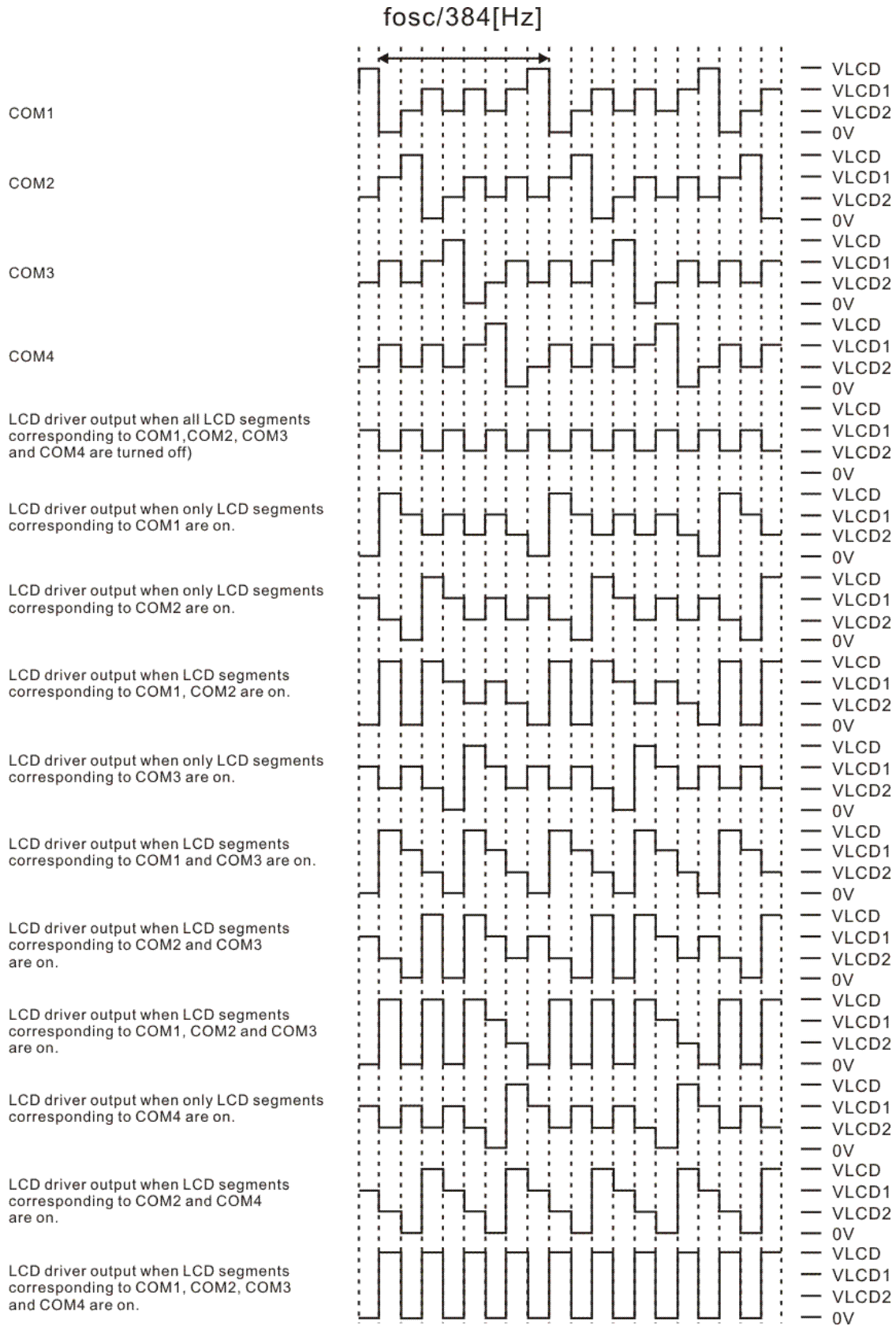
6.10 1/3 DUTY, 1/3 BIAS DRIVE TECHNIQUE



6.11 1/4 DUTY, 1/2 BIAS DRIVE TECHNIQUE



6.12 1/4 DUTY, 1/3 BIAS DRIVE TECHNIQUE



6.13 VOLTAGE DETECTION TYPE RESET CIRCUIT (VDET)

This circuit generates an output signal and resets the system when logic block power is first applied and when the voltage drops, i.e., when the logic block power supply voltage is less than or equal to the power down detection voltage VDET, which is 2.3V, typical. To assure that this function operates reliably, a capacitor must be added to the logic block power supply line so that the logic block power supply voltage VDD rise time when the logic block power is first applied and the logic block power supply voltage VDD fall time when the voltage drops are both at least 1ms. (see Figure 1 and Figure 2.)

6.14 POWER SUPPLY SEQUENCE

The following sequences must be observed when power is turned on and off. (see Figure 1 and Figure 2.)

- Power on: Logic block power supply(VDD) on → LCD driver block power supply(VLCD) on.
- Power off: LCD driver block power supply(VLCD) off → Logic block power supply(VDD) off.

However, if the logic and LCD driver block use a shared power supply, then the power supplies can be turned on and off at the same time.

6.15 SYSTEM RESET

The PT6530 supports the reset methods described below. When a system reset is applied, display is turned off, key scanning is stopped, and all the key data is reset to low. When the reset is cleared, display is turned on and key scanning become possible.

6.15.1 RESET METHODS

(1) Reset at power-on and power-down

If at least 1ms is assured as the logic block supply voltage VDD rise time when logic block power is applied, a system reset will be applied by the VDET output signal when the logic block supply voltage is brought up. If at least 1ms is assured as the logic block supply voltage VDD fall time when logic block power drops, a system reset will be applied in the same manner by the VDET output signal when the supply voltage is lowered. Note that the reset is cleared at the point when all the serial data (1/3 duty: the display data D1 to D228 and the control data, 1/4 duty: the display data D1 to D300 and the control data) has been transferred, i.e., on the fall of the CE signal on the transfer of the last direction data, after all the direction data has been transferred. However, the above operations will be performed regardless of the state (high or low) of the /RES pin. If /RES is high, the reset will be cleared at the point the above operations are completed. On the other hand, if /RES is low, the system will remain in the reset period as long as /RES is not set high, even if the above operations are completed. (see Figure 1 and Figure 2.)

(2) Reset when the logic block power supply voltage is in the allowable operating range (VDD=3.0 to 6.0V).
The system is reset when the /RES pin is set low, and the reset is cleared by setting /RES pin high.

1/3 DUTY

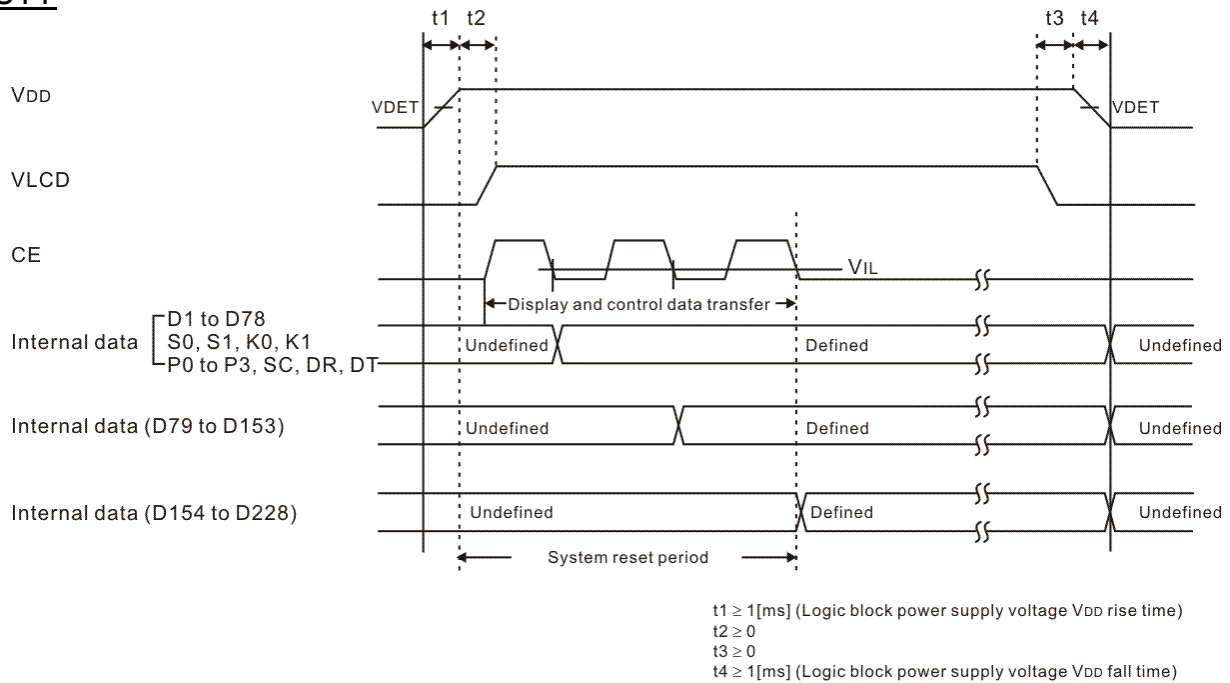


Figure 1

1/4 DUTY

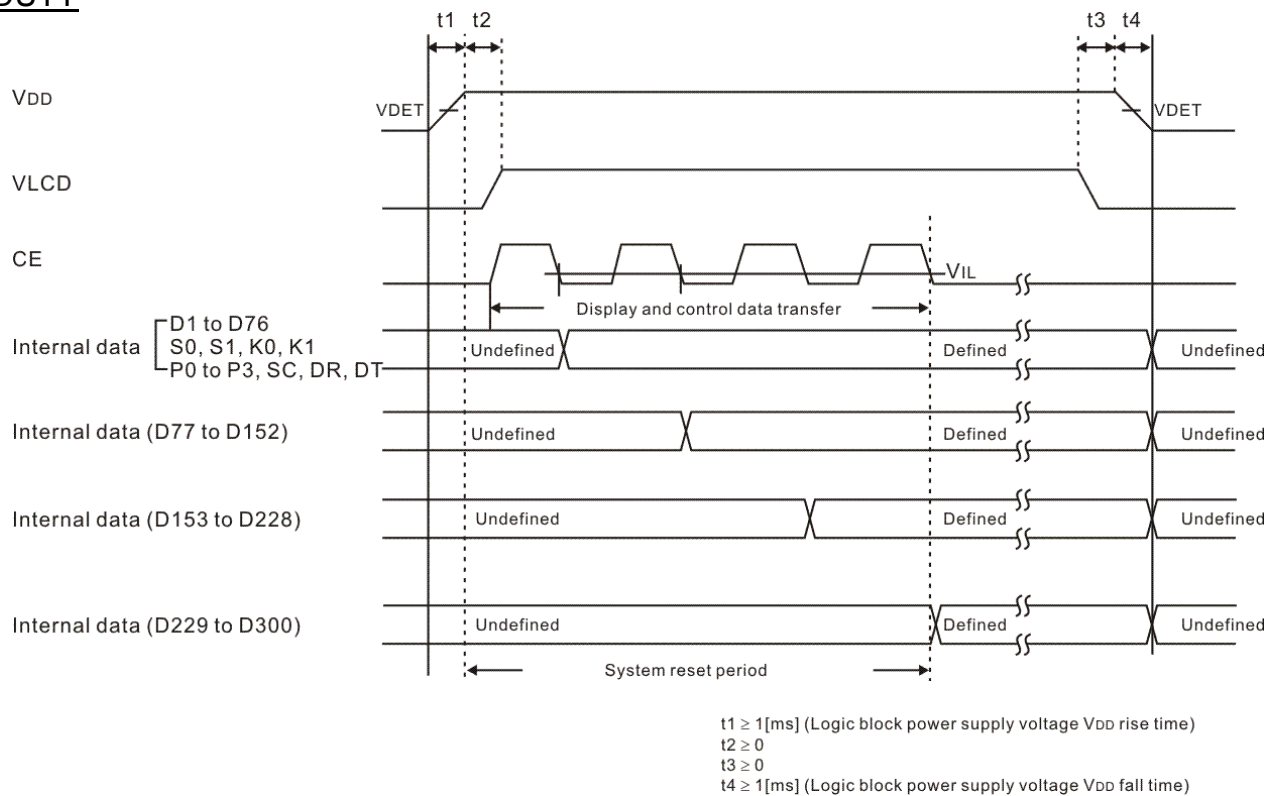


Figure 2

6.15.2 PT6530 INTERNAL BLOCK STATES DURING THE RESET PERIOD

- Clock Generator

Reset is applied and the base clock is stopped. However, the OSC pin state (normal or sleep mode) is determined after the S0 and S1 control data bits are transferred.

- Common Diver, Segment Driver & Latch

Reset is applied and the display is turned off. However, display data can be input to the latch circuit in this state.

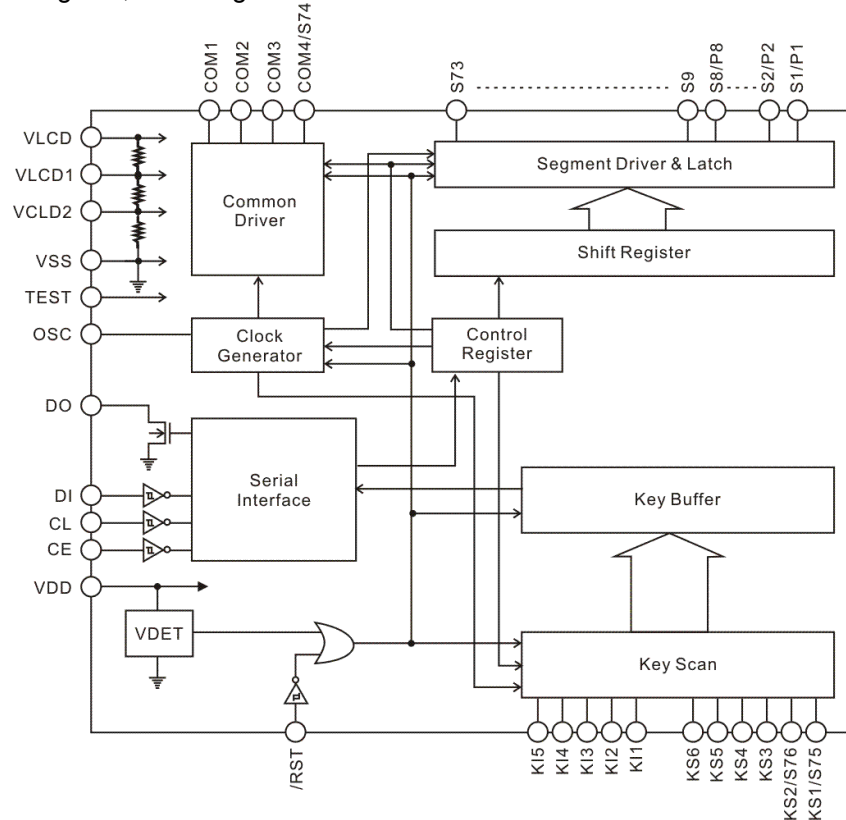
- Key Scan

Reset is applied, the circuit is set to the initial state, and at the same time the key scan operation is disabled.

- Key Buffer

Reset is applied and all the key data is set to low.

- Serial Interface, Control Register, Shift Register



☐ Block that are reset



6.15.3 OUTPUT PIN STATES DURING THE RESET PERIOD

| Output Pin | State During Reset |
|------------------|--------------------|
| S1/P1 to S8/P8 | L (Note 2) |
| S9 to S73 | L |
| COM1 to COM3 | L |
| COM4/S74 | L (Note 3) |
| KS1/S75. KS2/S76 | L (Note 2) |
| KS3 to KS5 | X (Note 4) |
| KS6 | H |
| DO | H (Note 5) |

Notes:

1. X = Don't care
2. These output pins are forcibly set to the segment output function and held low.
3. When power is first applied, this output pin is forcibly set to the common output function and held low. However, when the DT control data bit is transferred, either the common output or the segment output function is selected.
4. When power is first applied, these output pins are undefined until the S0 and S1 control data bits have been transferred.
5. Since this output pin is an open-drain output, a pull-up resistor of between 1 and 10K Ω is required. This pin remains high during the reset period even if a key data read operation is performed.

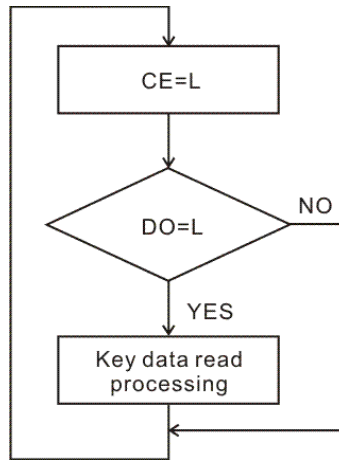
6.16 NOTE ON TRANSFERRING DISPLAY DATA FROM THE CONTROLLER

When using the PT6530 in 1/3 duty, applications transfer the display data (D1 to D228) in three operations, and in 1/4 duty, they transfer the display data (D1 to D300) in four operations. In either case, applications should transfer all of the display data within 30ms to maintain the quality of the displayed image.

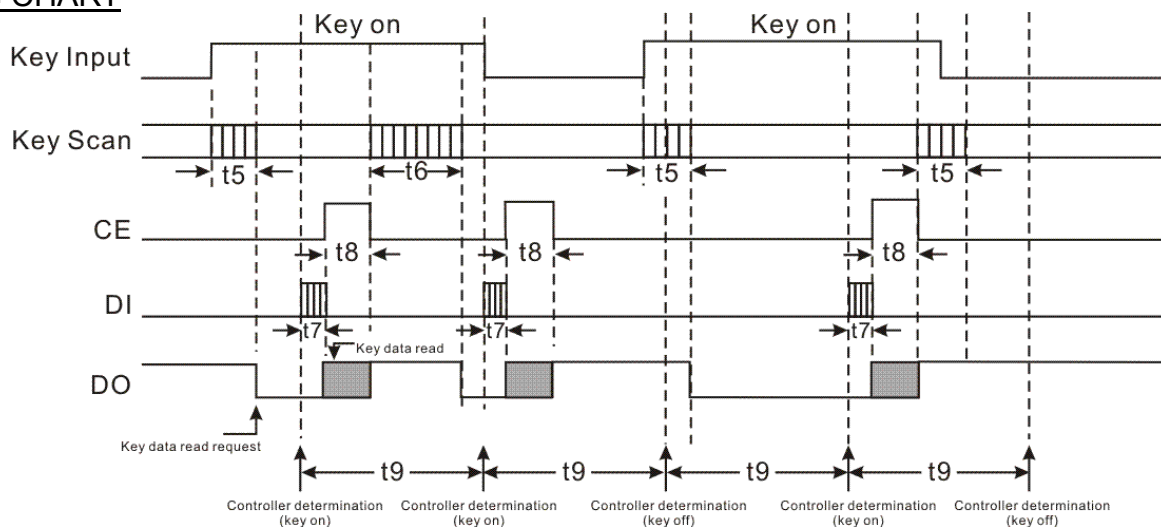
6.17 NOTE ON THE CONTROLLER KEY DATA READ TECHNIQUES

6.17.1 TIMER BASED KEY DATA ACQUISITION

FLOWCHART



TIMING CHART



t5: Key scan execution time when the key data agreed for two key scans. (615T(s))

t6: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (1230T(s))

t7: Key address (43H) transfer time $T = \frac{1}{f_{osc}}$

t8: Key data read time

EXPLANATION

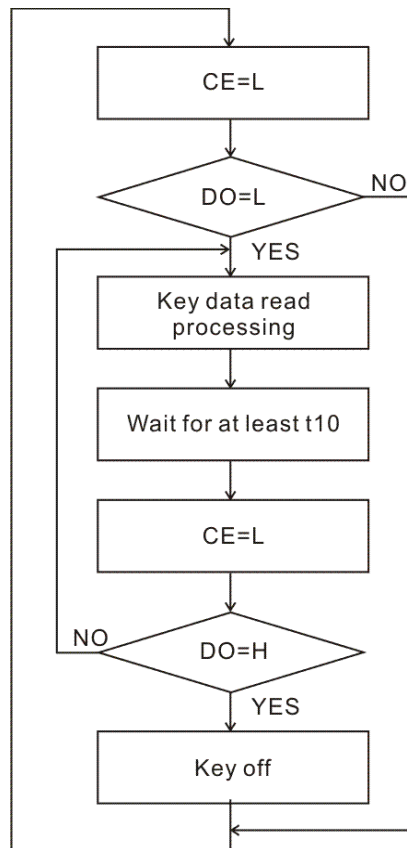
In this technique, the controller uses a timer to determine key on/off states and read the key data. The controller must check the DO state when CE is low every t9 period without fail. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation.

The period t9 in this technique must satisfy the following condition.

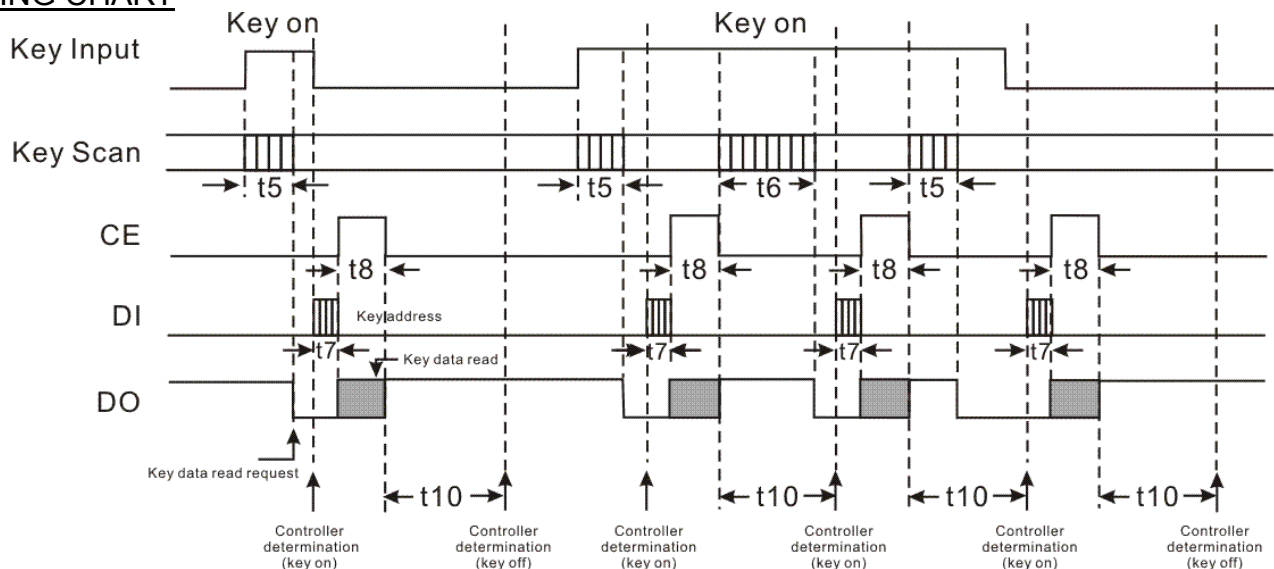
$$t9 > t6 + t7 + t8$$

If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.

6.17.2 INTERRUPT BASED KEY DATA ACQUISITION FLOWCHART



TIMING CHART



t5: Key scan execution time when the key data agreed for two key scans. (615T(s))

t6: Key scan execution time when the key data did not agree for two key scans and the key scan was executed again. (1230T(s))

t7: Key address (43H) transfer time $T = \frac{1}{f_{osc}}$

t8: Key data read time



EXPLANATION

In this technique, the controller uses interrupts to determine key on/off states and read the key data. The controller must check the DO state when CE is low. If DO is low, the controller recognizes that a key has been pressed and executes the key data read operation. After that the next key on/off determination is performed after the time t_{10} has elapsed by checking the DO state when CE is low and reading the key data. The period t_{10} in this technique must satisfy the following condition.

$$t_{10} > t_6$$

If a key data read operation is executed when DO is high, the read key data (KD1 to KD30) and sleep acknowledge data (SA) will be invalid.



7. ABSOLUTE MAXIMUM RATINGS

(V_{SS}=0V, Ta=25°C)

| Parameter | Symbol | Condition | Rating | Unit |
|-----------------------------|----------------------|---|------------------------------|------|
| Maximum Supply Voltage | V _{DD} max | V _{DD} | -0.3 ~ +7.0 | V |
| | V _{LCD} max | V _{LCD} | -0.3 ~ +7.0 | |
| Input Voltage | V _{IN1} | CE, CL, DI, /RES | -0.3 ~ V _{DD} +0.3 | V |
| | V _{IN2} | OSC, TEST | -0.3 ~ V _{DD} +0.3 | |
| | V _{IN3} | V _{LCD1} , V _{LCD2} , KI1 to KI5 | -0.3 ~ V _{LCD} +0.3 | |
| Output Voltage | V _{OUT1} | DO | -0.3 ~ V _{DD} +0.3 | V |
| | V _{OUT2} | OSC | -0.3 ~ V _{DD} +0.3 | |
| | V _{OUT3} | S1 to S76, COM1 to COM4, KS1 to KS6, P1 to P8 | -0.3 ~ V _{LCD} +0.3 | |
| Output Current | I _{OUT1} | S1 to S76 | 300 | μA |
| | I _{OUT2} | COM1 to COM4 | 3 | mA |
| | I _{OUT3} | KS1 to KS6 | 1 | |
| | I _{OUT4} | P1 to P8 | 5 | |
| Allowable Power Dissipation | Pd max | Ta = 85°C | 200 | mW |
| Operating Temperature | Topr | - | -40 ~ +85 | °C |
| Storage Temperature | Tstg | - | -65 ~ +150 | °C |

8. ALLOWABLE OPERATING RANGES

(Ta=-40 to +85°C, V_{SS}=0V)

| Parameter | Symbol | Condition | Min | Typ | Max | Unit |
|----------------------------------|-------------------|--|----------------------|---------------------|---|------|
| Supply Voltage | V _{DD} | V _{DD} | 3 | - | 6.0 | V |
| | V _{LCD} | V _{LCD} | V _{DD} -0.5 | - | 6.0 | V |
| Input Voltage | V _{LCD1} | V _{LCD1} | - | 2/3V _{LCD} | V _{LCD} | V |
| | V _{LCD2} | V _{LCD2} | - | 1/3V _{LCD} | V _{LCD} | V |
| Input High-Level Voltage | V _{IH1} | CE, CL, DI, /RES | 0.8 V _{DD} | - | V _{DD} | V |
| | V _{IH2} | KI1 to KI5 | 0.6 V _{LCD} | - | V _{LCD} | V |
| Input Low Level Voltage | V _{IL} | CE, CL, DI, /RES, (KI1 to KI5) | 0 | - | 0.2 V _{DD} (0.2V _{LCD}) | V |
| Recommended External Resistance | R _{OSC} | OSC | - | 39 | - | KΩ |
| Recommended External Capacitance | C _{OSC} | OSC | - | 1000 | - | pF |
| Guaranteed Oscillator Range | fosc | OSC | 19 | 38 | 76 | KHz |
| Data Setup Time | t _{ds} | CL, DI: Figure 4 | 160 | - | - | ns |
| Data Hold Time | t _{dh} | CL, DI: Figure 4 | 160 | - | - | ns |
| CE Wait Time | t _{cp} | CE, CL: Figure 4 | 160 | - | - | ns |
| CE Setup Time | t _{cs} | CE, CL: Figure 4 | 160 | - | - | ns |
| CE Hold Time | t _{ch} | CE, CL: Figure 4 | 160 | - | - | ns |
| High Level Clock Pulse Width | t _{OH} | CL: Figure 4 | 160 | - | - | ns |
| Low Level Clock Pulse Width | t _{OL} | CL: Figure 4 | 160 | - | - | ns |
| Rise Time | t _r | CE, CL, DI: Figure 4 | - | 160 | - | ns |
| Fall Time | t _f | CE, CL, DI: Figure 4 | - | 160 | - | ns |
| DO Output Delay Time | t _{dc} | DO, R _{PU} =4.7KΩ, C _L =10pf (see note): Figure 4 | - | - | 1.5 | μs |
| DO Rise Time | t _{dr} | DO, R _{PU} =4.7KΩ, C _L =10pf (see note): Figure 4 | - | - | 1.5 | μs |

Note: Since DO is an open-drain output, these values depend on the resistance of the pull-up resistor R_{PU} and the load capacitance C_L.

9. ELECTRICAL CHARACTERISTICS

| Parameter | Symbol | Conditions | Min. | Typ. | Max. | Unit |
|--|------------|--|--------------------------|--|--------------------------|------------|
| Hysteresis | V_H | CE, CL, DI, /RES (KI1 to KI5) | | 0.1V _{DD} (0.1V _{LCD}) | | V |
| Power-down Detection Voltage | V_{DET} | | 1.8 | 2.2 | 2.6 | V |
| Input High level Current | I_{IH} | CE, CL, DI, /RES: $V_I=V_{DD}$ | | | 5.0 | μA |
| Input Low Level Current | I_{IL} | CE, CL, DI, /RES: $V_I=0V$ | -5.0 | | | μA |
| Input Floating Voltage | V_{IF} | KI1 to KI5 | | | 0.05V _{LCD} | V |
| Pull-down Resistance | R_{PD} | KI1 to KI5: V _{LCD} =5.0V | 50 | 100 | 250 | K Ω |
| Output Off Leakage Current | I_{OFFH} | DO: VO=6.0V | | | 6.0 | μA |
| Output High Level Voltage | V_{OH1} | KS1 to KS6: $I_O=-500\mu A$ | V _{LCD} -1.0 | V _{LCD} -0.5 | V _{LCD} -0.2 | V |
| | V_{OH2} | P1 to P8: $I_O=-1mA$ | V _{LCD} -1.0 | | | |
| | V_{OH3} | S1 to S76: $I_O=-20\mu A$ | V _{LCD} -1.0 | | | |
| | V_{OH4} | COM1 to COM4: $I_O=-100\mu A$ | V _{LCD} -1.0 | | | |
| Output Low Level Voltage | V_{OL1} | KS1 to KS6: $I_O=25\mu A$ | 0.2 | 0.5 | 1.5 | V |
| | V_{OL2} | P1 to P8: $I_O=1mA$ | | | 1.0 | |
| | V_{OL3} | S1 to S76: $I_O=20\mu A$ | | | 1.0 | |
| | V_{OL4} | COM1 to COM4: $I_O=100\mu A$ | | | 1.0 | |
| | V_{OL5} | DO: $I_O=1mA$ | | 0.1 | 0.5 | |
| Output Middle Level Voltage (see note) | V_{MID1} | COM1 to COM4: 1/2 bias, $I_O=\pm 100\mu A$ | 1/2V _{LCD} -1.0 | | 1/2V _{LCD} +1.0 | V |
| | V_{MID2} | S1 to S76: 1/3 bias, $I_O=\pm 20\mu A$ | 2/3V _{LCD} -1.0 | | 2/3V _{LCD} +1.0 | |
| | V_{MID3} | S1 to S76: 1/3 bias, $I_O=\pm 20\mu A$ | 1/3V _{LCD} -1.0 | | 1/3V _{LCD} +1.0 | |
| | V_{MID4} | COM1 to COM4: 1/3 bias, $I_O=\pm 100\mu A$ | 2/3V _{LCD} -1.0 | | 2/3V _{LCD} +1.0 | |
| | V_{MID5} | COM1 to COM4: 1/3 bias, $I_O=\pm 100\mu A$ | 1/3V _{LCD} -1.0 | | 1/3V _{LCD} +1.0 | |
| Oscillator Frequency | fosc | OSC: R _{osc} =39K Ω , C _{osc} =1000pF | 30.4 | 38 | 45.6 | KHz |
| Current Drain | I_{DD1} | V _{DD} : Sleep mode | | | 100 | μA |
| | I_{DD2} | V _{DD} : V _{DD} =6.0V, output open, fosc=38KHz | | 270 | 540 | |
| | I_{LCD1} | V _{LCD} : Sleep mode | | | 5 | |
| | I_{LCD2} | V _{LCD} : V _{LCD} =6.0V, output open, 1/2 bias, fosc=38KHz | | 200 | 400 | |
| | I_{LCD3} | V _{LCD} : V _{LCD} =6.0V, output open, 1/3 bias, fosc=38KHz | | 120 | 240 | |

Note: Excluding the bias voltage generation divider resistor built into VLCD1 and VLCD2. (See Figure 3)

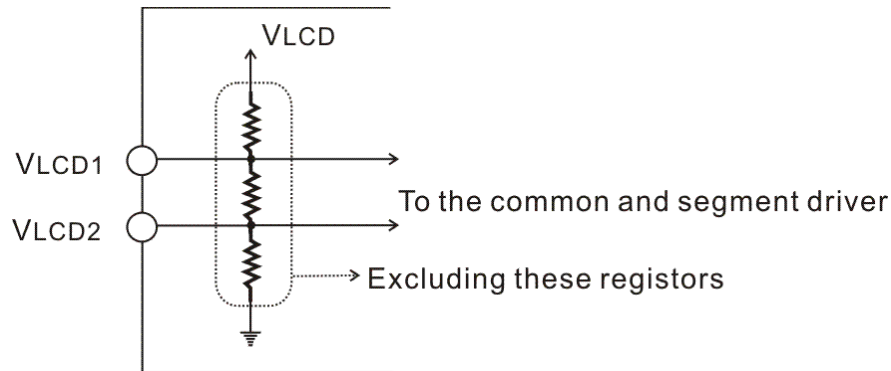
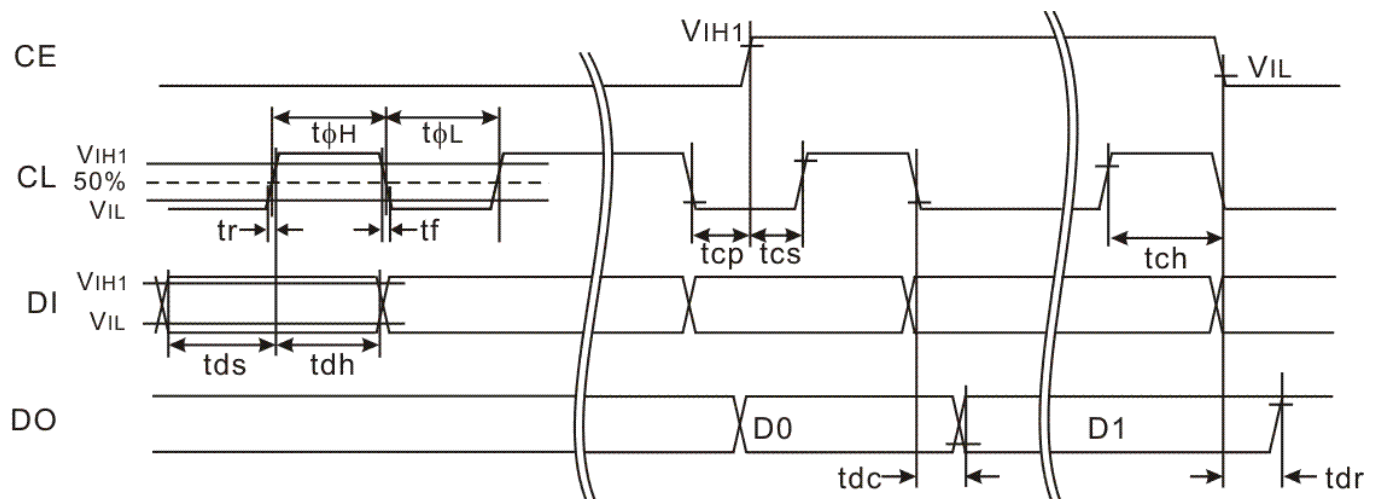


Figure 3

WHEN CL IS STOPPED AT THE LOW LEVEL



WHEN CL IS STOPPED AT THE HIGH LEVEL

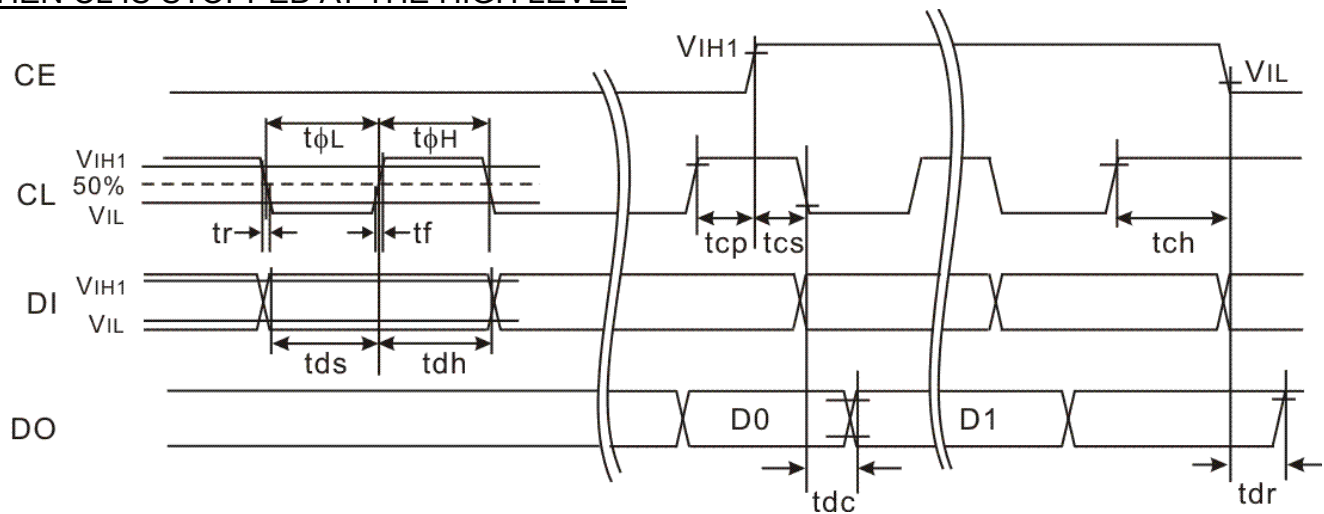
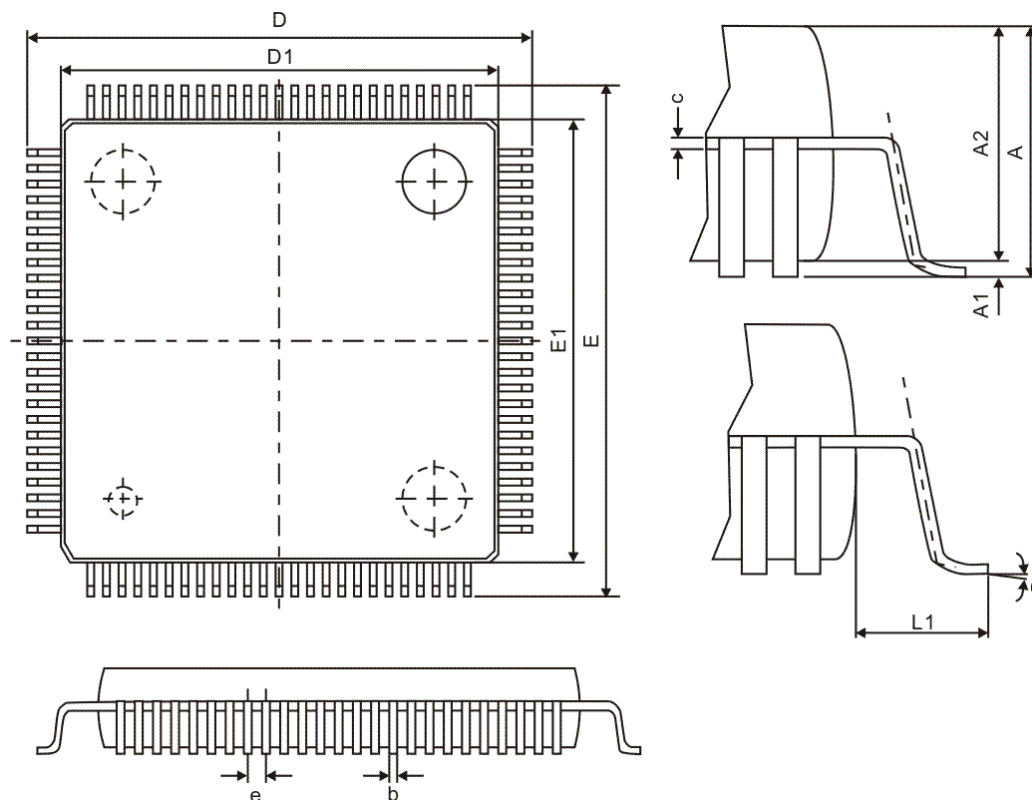


Figure 4

10. PACKAGE INFORMATION

100 PINS, LQFP



| Symbol | Min. | Nom. | Max. |
|--------|-----------|------|------|
| A | - | - | 1.60 |
| A1 | 0.05 | - | 0.15 |
| A2 | 1.35 | 1.40 | 1.45 |
| b | 0.17 | 0.22 | 0.27 |
| c | 0.09 | - | 0.20 |
| D | 16.00 BSC | | |
| D1 | 14.00 BSC | | |
| E | 16.00 BSC | | |
| E1 | 14.00 BSC | | |
| e | 0.50 BSC | | |
| L1 | 1.00 REF | | |
| θ | 0° | 3.5° | 7° |

Notes:

1. All controlling dimensions are in millimeters.
2. Refer to JEDEC MS-026BED



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