iC-MG

preliminary

8-Bit Sin/Cos INTERPOLATION IC WITH RS422 DRIVER

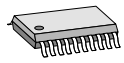
FEATURES

- Real-time tracking, no-missing-code interpolation to 200 kHz input frequency (up to x5, to 20 kHz for x50)
- Selectable interpol. factors: x1, x2, x4, x5, x10, x20, x25, x50
- Excellent accuracy (typ. 0.6 LSB) and repeatability (typ. 0.1 LSB)
- Differential PGA inputs with selectable input resistance for voltage and current signals
- Adjustable signal conditioning for offset, amplitude, phase
- Unique signal and calibration stabilization feature: supply of encoder LED or MR bridge via controlled 40 mA current source
- Fail-safe RS422 encoder quadrature outputs with index signal
- Adjustable index position and length (from 1/4 to 1 T)
- Preselectable minimum phase distance supports fail-safe counting
- Clipping, loss-of-signal and loss-of-tracking indication
- Setup via serial EEPROM interface
- Sub-system power switch offers reverse polarity protection for the overall system
- Single 5 V supply, operation from -25(40) °C to +100(125) °C

APPLICATIONS

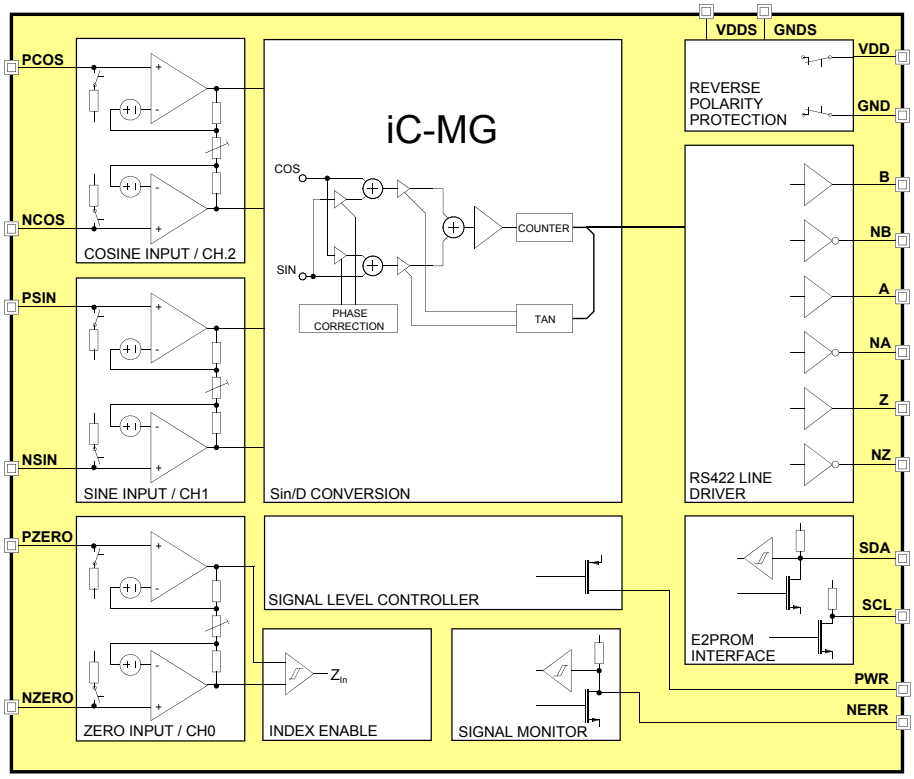
- Optical and magnetic position sensors
- Rotary encoders
- Linear encoders

PACKAGES



TSSOP20

BLOCK DIAGRAM



DESCRIPTION

Interpolator iC-MG is a non-linear A/D converter which, by applying a count-safe vector principle, digitizes sine/cosine sensor signals with selectable resolution and hysteresis. The angle value is output incrementally via differential RS422 drivers as an encoder quadrature signal with an index pulse. The minimum phase distance can be preselected, thus generating fail-safe counter signals and enhancing the noise immunity of the sensor system.

Programmable instrumentation amplifiers with selectable gain levels permit differential (in VDIFF or IDIFF mode) or single-ended input signals (in VREF or IREF mode). The modes of operation differentiate between high impedance (V modes) and low impedance (I modes). This adaptation of the iC to voltage or current signals enables MR sensor bridges or photosensors to be directly connected up to the device.

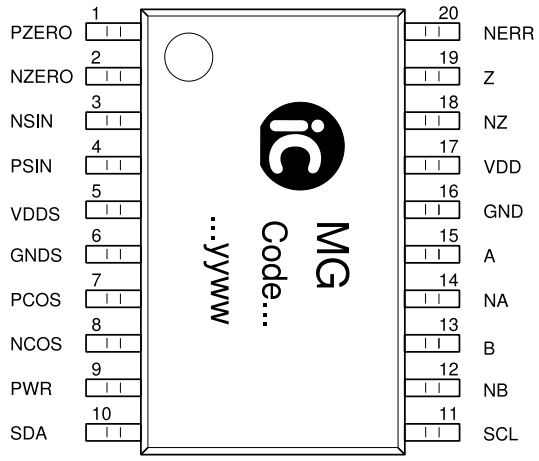
The integrated signal conditioning unit allows signal amplitudes and offset voltages to be calibrated and also any phase error between the sine and cosine signals to be corrected.

For the purpose of signal stabilization (to minimize the effects of temperature and aging), the conditioned signals are fed into the power supply controller which drives the transmitting LED of optical systems via the integrated 40 mA driver stage (output PWR). If MR sensors are connected this driver stage also powers the measuring bridges. If the control thresholds are reached this is signaled at alarm message output NERR (signal loss due to wire breakage, short circuiting, dirt or aging, for example).

iC-MG is protected against a reversed power supply voltage; the integrated supply switch for loads of up to 20 mA extends this protection to cover the overall system. The device is configured via an external EEPROM.

PACKAGES

PIN CONFIGURATION TSSOP20



PIN FUNCTIONS

No.	Name	Function
1	PZERO	Input Zero Signal +
2	NZERO	Input Zero Signal -
3	NSIN	Input Sine Signal -
4	PSIN	Input Sine Signal +
5	VDDS	Subsystem Positive Supply Output
6	GNDS	Subsystem Ground Output
7	PCOS	Input Cosine Signal +
8	NCOS	Input Cosine Signal -
9	PWR	Controlled Power Supply Output (High-Side)
10	SDA	Serial E2PROM Interface, data line
11	SCL	Serial E2PROM Interface, clock line
12	NB	Incremental Output B-
13	B	Incremental Output B+
14	NA	Incremental Output A-
15	A	Incremental Output A+
16	GND	Ground
17	VDD	+4.3 ... 5.5 V Supply Voltage
18	NZ	Incremental Index Output Z-
19	Z	Incremental Index Output Z+
20	NERR	Alarm Message and Test Signal Output (e.g. index enable signal Zin)

ABSOLUTE MAXIMUM RATINGS

Beyond these values damage may occur; device operation is not guaranteed.

Item No.	Symbol	Parameter	Conditions	Min.	Max.	Unit
G001	V()	Voltage at VDD, A, NA, B, NB, Z, NZ, SCL, SDA, PWR		-6	6	V
G002	V()	Voltage at NERR		-6	8	V
G003	V()	Voltage Pin vs. Pin			6	V
G004	V()	Voltage at PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, SCL, SDA		-0.3	VDDS +0.3	V V
G005	I(VDD)	Current in VDD		-20	400	mA
G006	I()	Current in VDDS, GNDS		-50	50	mA
G007	I()	Current in PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, SCL, SDA, NERR		-20	20	mA
G008	I()	Current in A, NA, B, NB, Z, NZ		-100	100	mA
G009	I(PWR)	Current in PWR		-100	20	mA
G010	Vd()	ESD Susceptibility at all pins	HBM, 100 pF discharged through 1.5 kΩ		2	kV
G011	Tj	Operating Junction Temperature		-40	150	°C
G012	Ts	Storage Temperature Range		-40	150	°C

THERMAL DATA

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
T01	Ta	Operating Ambient Temperature Range (extended temperature range of -40 to 125 °C on request)		-25		100	°C

All voltages are referenced to ground unless otherwise stated.
All currents into the device pins are positive; all currents out of the device pins are negative.

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.5...5.5 V, T_j = -40 °C...125 °C, IBN calibrated to 200 µA, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
General							
001	V(VDD)	Permissible Supply Voltage		4.5		5.5	V
002	I(VDD)	Supply Current in VDD	T_j = -40...125 °C, no load T_j = 27 °C, no load		 12	25	mA mA
003	I(VDDS)	Permissible VDDS Load Current		-20		0	mA
004	VDDon	Turn-on Threshold VDD		3.6	4.0	4.3	V
005	VDDoff	Turn-off Threshold VDD		3.0	3.5	3.8	V
006	VDDhys	Turn-on Threshold Hysteresis		0.4			V
007	Vc()hi	Clamp Voltage hi at inputs PSIN, NSIN, PCOS, NCOS, PZERO, NZERO, SCL, SDA		0.3		1.2	V
008	Vc()hi	Clamp Voltage hi at all pins				11	V
009	VC()lo	Clamp Voltage lo at all pins		-1.2		-0.3	V
Inputs and Signal Conditioning: PSIN, NSIN, PCOS, NCOS, PZERO, NZERO							
101	Vin()sig	Permissible Input Voltage Range	RSC, RZ = 0x1 RSC, RZ = 0x9	0.75 0		VDDS - 1.5 VDDS	V V
102	Iin()sig	Permissible Input Current Range	RSC(0), RZ(0) = 0, BIASSC = 0 RSC(0), RZ(0) = 0, BIASSC = 1	-300 10		-10 300	µA µA
103	Iin()	Input Current	RSC, RZ = 0x1	-10		10	µA
104	Rin()	Input Resistance vs. VREFin()	Nominal values following Table 9	70	100	130	%
105	TCRin()	Input Resistance Temperature Coefficient			0.15		%/K
106	VREFin()	Input Reference Voltage	No load, nominal values following Table 10	90	100	110	%
107	G	Gain Factor (Coarse x Fine)	RSC(3), RZ(3) = 0, GRx = 0x0, GFx = 0x00 RSC(3), RZ(3) = 0, GRx = 0x7, GFx = max.		2 100		
108	G-LSB	Least Significant Gain Factor Cal. Step	Sine channel Cosine channel Zero channel		1.015 1.06 1.06		
109	G-INL	Integral Non-Linearity of Gain Factor Cal.		-1		1	LSB
110	GR-CR	S/C-Chan. Gain Ratio Calibration Range	GFC = 0x10, GFS = 0x00...0xFF	39		255	%
111	Vin()diff	Recommended Diff. Input Signal Level	Vin()diff = V(PCHx) - V(NCHx); RSC, RZ ≠ 0x9 RSC, RZ = 0x9	 10 40		 500 2000	 mVpp mVpp
112	Vin()os	Input Offset Voltage	Referenced to side of input pins		25		µV
113	OFS/C-CR	S/C Offset Calibration Range	Referenced to source VOSSC; ORS, ORC = 00 ORS, ORC = 01 ORS, ORC = 10 ORS, ORC = 11		 ±100 ±200 ±600 ±1200		 %V() %V() %V() %V()
114	OFS/C-LSB	Least Significant S/C-Offset Cal. Step	Referenced to source VOSSC; ORS, ORC= 00		0.79		%
115	OFZ-LSB	Least Significant Z-Offset Cal. Step	Referenced to VOSZ; ORZ = 00		3.2		%
116	OFx-INL	Integral Non-Linearity of Offset Cal.		-5		5	LSB
117	PH-CR	S/C Phase Calibration Range			±20		°
118	PH-LSB	Least Significant S/C Phase Cal. Step			0.63		°
119	PH-INL	Integral Non-Linearity of S/C Phase Cal.		-0.8		0.8	°
120	fin()max	Permissible Max. Inp. Frequency		200			kHz

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.5...5.5 V, T_j = -40 °C...125 °C, IBN calibrated to 200 µA, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Sine-to-Digital Conversion							
201	AAabs	Absolute Angle Accuracy (following calibration)	Referred to 360 deg input signal, ideal and quasi-stable input signals, SELHYS = 0		1	2	°
202	AArel	Relative Angle Accuracy	Referred to A/B output period, ideal and quasi-stable input signals	-10		+10	%
203	AAR	Absolute Angle Repeatability	See 201; VDD = const., Tj = const.		0.2		°
Output Line Drivers: A, NA, B, NB, Z, NZ							
501	Vs()hi	Saturation Voltage hi	Vs() = VDD - V(); I() = -20 mA			400	mV
502	Vs()lo	Saturation Voltage lo	I() = 20 mA			400	mV
503	Isc()hi	Short-Circuit Current hi		-60	-40	-20	mA
504	Isc()lo	Short-Circuit Current lo		20	40	60	mA
505	Ilk()tri	Tristate Leakage Current	TRIHL(1:0) = 11		20	100	µA
506	tr()	Rise Time hi	RL = 100 Ω to GNDS; SSR(1:0) = 01 SSR(1:0) = 10	 5 20		 40 140	 ns ns
507	tf()	Rise Time lo	RL = 100 Ω to VDD; SSR(1:0) = 01 SSR(1:0) = 10	 5 30		 40 140	 ns ns
508	Ri()cal	Source Impedance	With calibration modes		2.5	4	kΩ
509	I()cal	Permissible Load Current	With calibration modes	-3		3	µA
510	Ilk()	Leakage Current with Reversed Supply Voltage				100	µA
511	MTD()	Min. Phase Distance Tolerance	referred to nominal value	-25		+25	%
Controlled Power Supply: PWR							
601	Vs()hi	Saturation Voltage hi	Vs() = VDD - V(); ADJ(8:0) = 0x19F, I() = -5 mA ADJ(8:0) = 0x1BF, I() = -10 mA ADJ(8:0) = 0x1DF, I() = -25 mA ADJ(8:0) = 0x1FF, I() = -40 mA			 1 1 1 1.2	 V V V V
602	Isc()hi	Short-Circuit Current hi	V(PWR) = 0...VDD - 1 V; ADJ(8:0) = 0x19F ADJ(8:0) = 0x1BF ADJ(8:0) = 0x1DF V(PWR) = 0...VDD - 1.2 V; ADJ(8:0) = 0x1FF	 -10 -20 -50 -100		 -4 -8 -20 -40	 mA mA mA mA
Bias Current Source and Reference Voltages							
801	VBG	Bandgap Reference Voltage		1.2	1.25	1.3	V
802	VPAH	Reference Voltage Source		45	50	55	%VDDS
803	VOSref	S/C a. Z Offset Cal. Reference Voltage Source		450	500	550	mV
804	IBN	Bias Current Source	CFGIBN = 0x0 CFGIBN = 0xF calibrated at Ta = 25 °C	110 180	 200	 370 220	µA µA µA

ELECTRICAL CHARACTERISTICS

Operating Conditions: VDD = 4.5...5.5 V, T_j = -40 °C...125 °C, IBN calibrated to 200 µA, unless otherwise noted.

Item No.	Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Alarm Message Output: NERR							
B01	Vs()lo	Saturation Voltage lo	Versus GND; I() = 4 mA			0.4	V
B02	Isc()lo	Short-Circuit Current lo	Versus GND; V(NERR) ≤ VDD V(NERR) > VTMon	4	5 2	7	mA mA
B03	Ipu()	Pull-Up Current Source	V() = 0...VDD - 1 V; EPU = 1	-400	-300	-200	µA
B04	VTMon	Setup Preparation Threshold	Increasing voltage at NERR			VDD +2	V V
B05	VTMoff	Setup Trigger Threshold	Decreasing voltage at NERR	VDD + 0.5			V
B06	VTMhys	Setup Trigger Threshold Hysteresis	VTMhys = VTMon - VTMoff	0.15	0.3		V
B07	dt(NERR)lo	Alarm Indication Time Tolerance	Nominal time see table 40	-25		+25	%
Supply Switch and Reverse Polarity Protection: VDDS, GNDS							
C01	Vs()	Saturation Voltage VDDS vs. VDD	Vs() = VDD - V(VDSS); I(VDDS) = -20 mA			250	mV
C02	Vs()	Saturation Voltage GNDS vs. GNS	Vs() = V(GNDS) - GND; I(GNDS) = 20 mA			250	mV
C03	I(VDD)rev	Supply Current in VDD with Reverse Polarity		-1		0	mA
Serial EEPROM Interface: SDA, SCL							
D01	Vs()lo	Saturation Voltage lo	I() = 4 mA			400	mV
D02	Isc()	Short-Circuit Current lo		4		75	mA
D03	Vt()hi	Input Threshold Voltage hi				2	V
D04	Vt()lo	Input Threshold Voltage lo		0.8			V
D05	Vt()hys	Input Threshold Hysteresis	Vt()hys = Vt()hi - Vt()lo	300	500		mV
D06	Ipu()	Input Pull-Up Current	V() = 0...VDDS - 1 V	-600	-300	-60	µA
D07	Vpu()	Input Pull-Up Voltage	V() = VDDS - V(); I() = -5 µA			0.4	V
D08	f(SCL)	Clock Frequency SCL		60	80	100	kHz
D09	tbusy()cfg	Configuration Sequence	Single reading sequence		18	24	ms
Temperature Monitoring							
E01	Toff	Shutdown Temperature			155		°C
E02	Thys	Shutdown Temperature Hysteresis			30		°C

DEVICE SETUP

Register Map								
Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Serial EEPROM Interface								
0x00	0	DEVID(6:0)						
Bias Current Source								
0x01	CFGIBN(3:0)				0	0	0	0
Operating Modes								
0x02	0	1	1	0	MODE(3:0)			
Input Configurations								
0x03	0	0	0	0	0	INMODE	1	1
S/C Signal Path, Input Configuration								
0x04	GFC(4:0)					GRSC(2:0)		
0x05	GFS(3:0)				0	0	0	0
0x06	VDCS(0)	0	0	0	0	GFS(6:4)		
0x07	0	0	0	VDCS(5:1)				
0x08	ORS(0)	VDCC(5:0)						0
0x09	OFS(3:0)				0	0	0	ORS(1)
0x0A	0	0	ORC(1:0)		OFS(7:4)			
0x0B	OFC(6:0)							0
0x0C	PHSC(2:0)			0	0	0	0	OFC(7)
0x0D	0	0	0	1	1	PHSC(5:3)		
0x0E	1	BIASSC	VOSSC(1:0)		RSC(3:0)			
Controlled Power Supply								
0x0F	ADJ(0)	0	0	0	1	0	0	0
0x10	ADJ(8:1)							
Z Signal Path, Input Configuration								
0x11	GFZ(4:0)					GRZ(2:0)		
0x12	OFZ(5:0)						ORZ(1:0)	
0x13	0	BIASZ	VOSZ(1:0)		RZ(3:0)			
Error Monitoring								
0x14	EMASKA(7:0)							
0x15	1	0	EMTD(2:0)			EPH	EMASKA(9:8)	
0x16	EMASKO(7:0)							
0x17	0	0	0	0	0	EPU	EMASKO(9:8)	
0x18	0	0	0	0	0	0	0	0
Zero Signal Setup								
0x19	0	0	0	0	CFGZ(3:0)			
0x1A	CFGZPOS(7:0)							
Sine-to-Digital Conversion, Minimum Phase Distance								
0x1B	SELRES(7:0)							
0x1C	0	SELRES(14:8)						
0x1D	MTD(3:0)				SELHYS(3:0)			
Output Settings								
0x1E	0	0	1	0	SSR(1:0)		TRIHL(1:0)	

Register Map								
Adr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Reserved Memory Section 1								
0x1F	Internal use only; keep all bits at zero for initialization							
0x20	Internal use only; keep all bits at zero for initialization							
Reserved Memory Section 2								
0x21	0	0	0	0	1	0	0	0
0x22	Internal use only; keep all bits at zero for initialization							
0x23	Internal use only; keep all bits at zero for initialization							
0x24	Application-specific OEM data							
0x25	Application-specific OEM data							
0x26	Application-specific OEM data							
0x27	Application-specific OEM data							
0x28	Application-specific OEM data							
0x29	Application-specific OEM data							
0x2A	Application-specific OEM data							
0x2B	Application-specific OEM data							
0x2C	Application-specific OEM data							
0x2D	Application-specific OEM data							
0x2E	Application-specific OEM data							
CRC Data								
0x2F	CHKSUM(7:0)							
Reserved Memory Section 3								
0x30	Internal use only; keep all bits at zero for initialization							
0x31	Internal use only; keep all bits at zero for initialization							
0x32	Internal use only; keep all bits at zero for initialization							
0x33	Internal use only; keep all bits at zero for initialization							
Notes	All 0 and 1 entries are mandatory for device initialization							

Table 4: Register Map

SERIAL EEPROM INTERFACE

The serial configuration interface consists of the two pins SCL and SDA and enables read access to a serial EEPROM (requirements: 1 Kbit, 128x8, 3.3 V to 5 V operation, device address 0x50 "1010 000"; recommended: Atmel AT24C01B; notes: devices ignoring A2...0 address bit settings are not suitable).

Once the supply has been switched on (power down reset) iC-MG reads the configuration from the EEPROM which has the device ID 0x50. Bit errors in the 0x00 to 0x2F memory area are monitored by the CRC deposited in register CHKSUM (see program example; the polynomial used is "1 0001 1101"). Should an error occur while the data is being read in the readin process is repeated; the system aborts following a fourth faulty attempt and tristates the output drivers.

As an alternative to the power down reset iC-MG can be triggered to again read in the configuration via pin NERR. To this end pin voltage V(NERR) must initially exceed threshold voltage VTMon (see Electrical Characteristics). Once the pin voltage has dropped to below VTMon iC-MG starts communicating with the EEPROM. The device ID stored in register DEVID is used to address the EEPROM.

Example of CRC Calculation Routine

```
unsigned char ucDataStream = 0;
int iCRCPoly = 0x11D;
unsigned char ucCRC=0;
int i = 0;

ucCRC = 1; // start value !!!
for (iReg = 0; iReg<47; iReg ++)
{
  ucDataStream = ucGetValue(iReg);
  for (i=0; i<=7; i++) {
    if ((ucCRC & 0x80) != (ucDataStream & 0x80))
      ucCRC = (ucCRC << 1) ^ iCRCPoly;
    else
      ucCRC = (ucCRC << 1);
    ucDataStream = ucDataStream << 1;
  }
}
```

OPERATING MODES

MODE	Adr 0x02, bit 3:0							
Code	Operating Mode	Pin A	Pin NA	Pin B	Pin NB	Pin Z	Pin NZ	NERR
0x00	ABZ Mode	A	NA	B	NB	Z	NZ	NERR
0x01	Calibration Mode 1		VREFIZ	VREFISC	IBN	PCH-Z	NCH-Z	
0x02	Calibration Mode 2	PCH-S	NCH-S	PCH-C	NCH-C	VDCS	VDCC	
0x0B	System Test Mode *	A_4	A_8	B_4	B_8	Z_{In}		NERR
	* Note: Setting SELRES=0x132 and SELHYS=0xF is mandatory.							

Table 5: Operating Modes

iC-MG has several modes of operation which are set via MODE. In addition to the primary operational mode *ABZ Mode* for the output of encoder quadrature signals via differential line drivers both analog and digital calibration signals can be selected which can be used to set up the integrated signal conditioning unit.

ABZ Mode

In *ABZ Mode* complementary signals are always output. Here, converter setting SELRES determines the A/B pulse count and zero signal settings CFGZ and CFGPOS the width and position of the generated zero signal (dependent on an enable from Z_{In}).

Calibration Mode 1, Mode 2

So that signal amplitudes and offset voltages can be calibrated internal analog signals are switched to the output pins directly and the digital line drivers shut down. Due to internal resistances of up to 4 kΩ a high-impedance measurement is advisable.

In *Calibration Mode 1* bias current source IBN and the internal zero signal are available after the input amplifier (signals PCH-Z and NCH-Z). The calibration of IBN is described on page 11, that of the zero signal on page 15.

In *Calibration Mode 2* the conditioned sine and cosine signals are output (signals PCH-S, NCH-S, PCH-C and NCH-C). Additionally, the intermediate potentials of both input channels are also available, with VDCS for the sine and VDCC for the cosine channel. The calibration of these intermediate voltages is described on page 14.

System Test Mode

System Test Mode permits the fine adjustment of the sine and cosine input signals using digital signals. The registers mentioned above must also be set for this mode.

The A_4 duty cycle acts as a measure for the offset of the sine channel, with the B_4 duty cycle a measure for that of the cosine channel. The duty cycle at A_8 represents the phase error between sine and cosine or any deviation from the ideal value of 90°. The calibration of differing signal amplitudes enables the duty cycle at B_8. A duty cycle of 50 % is the calibration target for all digital test signals.

Signal Z_{In} is the unmasked digitized zero signal.

BIAS CURRENT SOURCE CALIBRATION

The calibration of the bias current source is prerequisite for adherence to the given electrical characteristics and also instrumental in the determination of the chip timing (e.g. the minimum phase distance and SCL clock frequency). For setup purposes *Calibration Mode 1* is activated and the IBN current measured using a 10 kΩ resistor switched to VDDS. The setpoint is 200 µA which is equivalent to a measurement voltage of 2 V.

CFGIBN	Adr 0x01, bit 7:4		
Code k	$IBN \sim \frac{31}{39-k}$	Code k	$IBN \sim \frac{31}{39-k}$
0x0	79 %	0x8	100 %
0x1	81 %	0x9	103 %
0x2	84 %	0xA	107 %
0x3	86 %	0xB	111 %
0x4	88 %	0xC	115 %
0x5	91 %	0xD	119 %
0x6	94 %	0xE	124 %
0x7	97 %	0xF	129 %

Table 6: Bias Current Source Calibration

INPUT CONFIGURATIONS

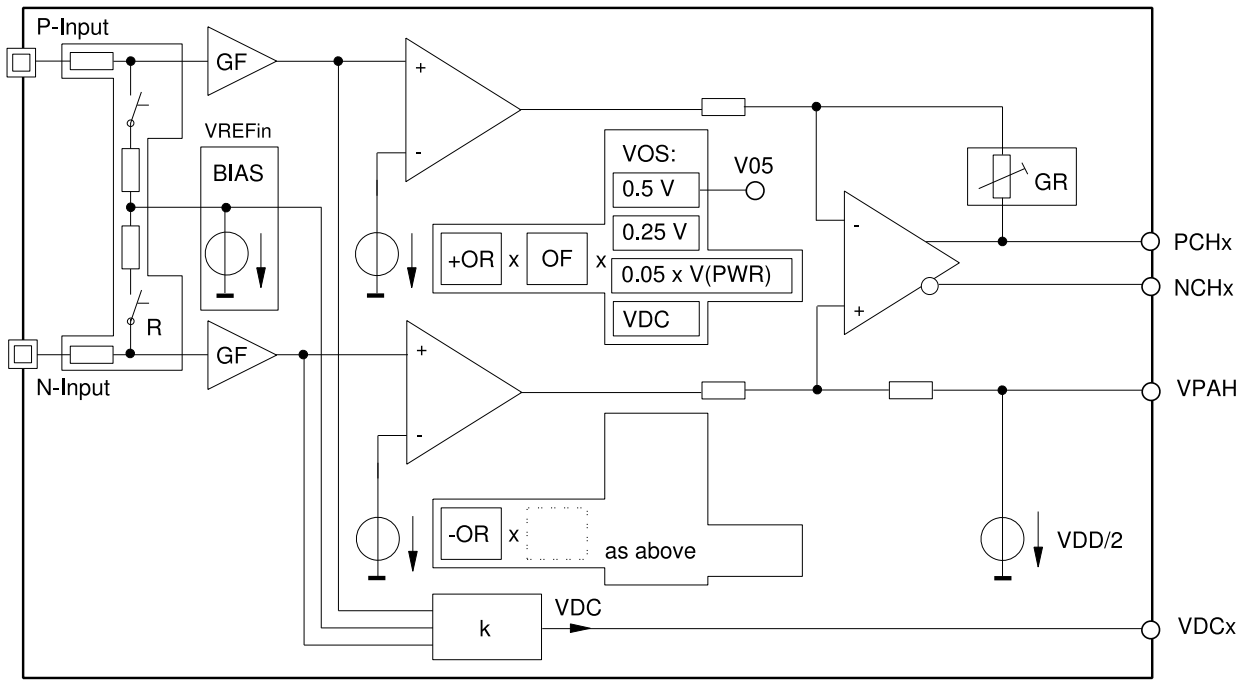


Figure 1: Input instrumentation amplifier and signal conditioning

All input stages are configured as instrumentation amplifiers and thus directly suitable for differential input signals. Referenced input signals can be processed as required; in Single-Ended Input Mode the NZERO input acts as a reference, replacing the input signals from NSIN and NCOS.

INMODE	Adr 0x03, bit 2
0	Differential input signals
1	Single-ended input signals *
Note	* Input NZERO is reference for all inputs.

Table 7: Input Signal Mode

Both current and voltage signals can be processed as input signals, selected by RSC(0) and RZ(0). In I Mode an input resistor Rin() becomes active at each input pin, converting the current signal into a voltage signal. The input resistance Rin() consists of a pad wiring resistor and resistor Rui() which is linked to the adjustable bias voltage source VREFin(). The following table shows the possible selections, with Rin() giving the typical resulting input resistance (see Electrical Characteristics for tolerances).

The input resistor should be set in such a way that intermediate potentials VDCS and VDCC lie between 125 mV and 250 mV (verifiable in Calibration Mode 2). In V Mode an optional voltage divider can be selected which reduces unacceptably large input amplitudes to ca. 25%. The circuitry is equivalent to the resistor chain in I Mode; the pad wiring resistor is considerably larger here, however.

RSC **RZ**	Adr 0x0E, bit 3:0 Adr 0x13, bit 3:0		
Code	Nominal Rin()	Internal Rui()	I/V Mode
–000	1.7 kΩ	1.6 kΩ	Current input
–010	2.5 kΩ	2.3 kΩ	Current input
–100	3.5 kΩ	3.2 kΩ	Current input
–110	4.9 kΩ	4.6 kΩ	Current input
1—1	20 kΩ	5 kΩ	Voltage input
0—1	high impedance	1 MΩ	Voltage input

Table 8: I/V Mode and Input Resistance

BIASSC **BIASZ**	Adr 0x0E, bit 6 Adr 0x13, bit 6	
Code	VREFin()	Type of sensor
0	2.5 V	Lowside current sink (I Mode)
1	1.5 V	Highside current source (I Mode)

Table 9: Input Bias Voltage

S/C SIGNAL PATH and CALIBRATION

The analog voltage signals needed to calibrate the sine signals can be measured in *Calibration Mode 2*. The characteristic digital parameters for offset, amplitude and phase errors can be measured in *System Test Mode*.

S/C Gain Settings

The gain is set in four stages:

1. The sensor supply tracking is shut down and the constant current source for the PWR output set to a suitable output current (register ADJ; current value close to the later operating point).

2. The coarse gain is selected so that differential signal amplitudes of ca. 1 Vpp are produced internally (signal PCHx vs. NCHx for the sine or cosine channel).

3. Using fine gain factor GFC the cosine signal amplitude is then adjusted to 1 Vpp.

4. The sine signal amplitude can then be calibrated to the cosine signal amplitude via fine gain factor GFS.

GRSC	Adr 0x04, bit 2:0	
Code	Range with RSC=0x9	Range with RSC≠0x9
0x0	0.5	2.0
0x1	1.0	4.1
0x2	1.3	5.3
0x3	1.7	6.7
0x4	2.2	8.7
0x5	2.6	10.5
0x6	3.3	13.2
0x7	4.0	16.0

Table 10: S/C-Channel Gain Range

GFC	Adr 0x04, bit 7:3
Code	Factor
0x00	1.00
0x01	1.06
...	$6.25\,\frac{GFC}{31}$
0x1F	6.25

Table 11: Gain Factor Cosine

GFS	Adr 0x06, bit 2:0, Adr 0x05, bit 7:4
Code	Factor
0x00	1.0
0x01	1.015
...	$6.25\,\frac{GFS}{124}$
0x7F	6.53

Table 12: Gain Factor Sine

S/C Offset Calibration

To calibrate the offset the reference source must first be selected using VOSSC. Two fixed voltages and two dependent sources are available for this purpose. The fixed voltage sources should be selected for external sensors which already provide stable, self-regulating signals.

For the operation of photosensors in optical encoders, iC-MG tracks changes in offset voltages via the signal-dependent source VDC when used in conjunction with the controlled power supply output supplying the encoder LED (pin PWR). The VDC potential automatically tracks higher DC photocurrents. To this end intermediate potentials VDCS and VDCC must be adjusted to a minimal AC ripple using the selectable k factor (this calibration must be repeated when the gain setting is altered). The ideal DC voltage level of 0.25 V to 0.5 V is selected via the input resistor Rui().

The feedback of pin voltage V(PWR) fulfills the same task as source VDC when MR bridge sensors are supplied by the controlled power supply output. In this instance the VDC sources do not need adjusting.

VOSSC	Adr 0x0E, bit 5:4
Code	Type of source
0x0	0.05 · V(PWR)
0x1	0.5 V
0x2	0.25 V
0x3	VDC (ie. VDCS, VDCC)

Table 13: S/C-Channel Offset Reference Source

VDCS	Adr 0x07, bit 4:0; Adr 0x06, bit 7
VDCC	Adr 0x08, bit 6:1
Code	$VDC = k \cdot V(P - In) + (1 - k) \cdot V(N - In)$
0x00	k = 0.33
0x01	k = 0.335
...	...
0x3F	k = 0.66

Table 14: S/C-Channel Intermediate Voltages

The calibration range for the S/C offset is dependent on the selected VOSSC source and is set using ORS and ORC. Both sine and cosine signals are then calibrated using factors OFS and OFC. The calibration target is reached when the DC fraction of the differential signals PCHx versus NCHx is zero.

ORS	Adr 0x09, bit 0; Adr 0x08, bit 7
ORC	Adr 0x0A, bit 5:4
Code	Range
00	x2
01	x4
10	x12
11	x24

Table 15: S/C-Channel Offset Range

OFS	Adr 0xA, bit 3:0; Adr 0x9, bit 7:4		
OFC	Adr 0xC, bit 0; Adr 0xB, bit 7:1		
Code	Factor	Code	Factor
0x00	0	0x00	0
0x01	0.0079	0x01	-0.0079
...	...	...	...
0x7F	1	0xFF	-1

Table 16: S/C-Channel Offset Factors

S/C Phase Correction

If the phase shift between the sine and cosine signal deviates from the ideal 90° this can be compensated for using parameter PHSC. Following this the calibration of the amplitude compensation, intermediate potentials and offset voltages may have to be corrected.

PHSC	Adr 0xD, bit 2:0; Adr 0xC, bit 7:5		
Code	Correction angle	Code	Correction angle
0x00	+ 0 °	0x20	- 0 °
0x01	+ 0.63 °	0x21	- 0.63 °
...	...	...	...
0x1F	+ 20.2 °	0x3F	- 20.2 °

Table 17: Phase Correction

Z SIGNAL PATH and CALIBRATION

The analog voltage signals needed to calibrate the zero signal are available in *Calibration Mode 1*. In addition it is possible to check the phase position of the PZERO/NZERO enable signal in *System Test Mode*.

Gain Settings

Parallel to the conditioning process for the S/C signals the zero signal gain is also set step by step:

1. The tracking of the sensor supply is shut down and the constant current source for the PWR output set to a suitable output current (register ADJ; current value close to the later operating point).

2. Coarse gain is selected so that differential signal amplitudes of ca. 1 Vpp are generated internally (signal PCHx vs. NCHx).

3. GFC then permits fine gain adjustment to 1 Vpp.

GRZ	Adr 0x11, bit 2:0	
Code	Range with RZ=0x9	Range with RZ≠0x9
0x0	0.5	2.0
0x1	1.0	4.1
0x2	1.3	5.3
0x3	1.7	6.7
0x4	2.2	8.7
0x5	2.6	10.5
0x6	3.3	13.2
0x7	4.0	16.0

Table 18: Z-Channel Gain Range

GFZ	Adr 0x11, bit 7:3
Code	Factor
0x00	1.00
0x01	1.06
...	$6.25^{\frac{GFZ}{31}}$
0x1F	6.25

Table 19: Z-Channel Gain Factor

Offset Calibration

To calibrate the offset the source of supply must first be selected using VOSZ (see S/C Offset Calibration for further information). For the zero signal path the signal dependent source is VDCS.

VOSZ	Adr 0x13, bit 5:4
Code	Type of source
0x0	0.05 · V(PWR)
0x1	0.5 V
0x2	0.25 V
0x3	VDC= VDCS

Table 20: Z-Channel Offset Reference Source

ORZ	Adr 0x12, bit 1:0
Code	Range
00	x2
01	x4
10	x12
11	x24

Table 21: Z-Channel Offset Range

OFZ	Adr 0x12, bit 7:2		
Code	Factor	Code	Factor
0x00	0	0x20	0
0x01	0.032	0x21	-0.032
...	...	...	...
0x1F	1	0x3F	-1

Table 22: Z-Channel Offset Factor

SIGNAL LEVEL CONTROLLER

Via the controlled power supply (pin PWR) the input signal levels for the sine-to-digital converter can be kept constant regardless of temperature and aging effects by tracking the sensor supply. Alternatively, the PWR output can be used as a constant current source for adjusting the signal conditioning, for example.

ADJ(6:0) selects the desired current for the PWR output; when adjusting the signal conditioning ideally amplitudes of ca. 1 Vpp should be possible for the PCHx to NCHx signal.

ADJ (8:7)	Adr 0x10, bit 7:6
Code	Function
00	Control to sine/cosine square
01	Control to sum of sine/cosine
10	Current source
11	Not permitted

Table 23: PWR Output Operating Mode

ADJ (6:5)	Adr 0x10, bit 5:4
Code	Function
00	5 mA range
01	10 mA range
10	25 mA range
11	50 mA range

Table 24: PWR Output Current Source Range

ADJ (4:0)	Adr 0x10, bit 3:0; Adr 0x0F, bit 7
Code	Function
0x00	3.125 % of Isc(PWR)
...	...
0x1F	100 % of Isc(PWR)
Note	Settings apply with current source mode.

Table 25: PWR Output Short-Circuit Current

ADJ (4:0)	Adr 0x10, bit 3:0; Adr 0x0F, bit 7
Code	Function
0x00	60%
...	...
0x1A	ca. 100%
...	...
0x1F	120%
Note	Settings apply with s/c square control mode. Recommended entry for 1.0 V is 0x1A.

Table 26: PWR Output Signal Adjustment

ADJ (4:0)	Adr 0x10, bit 3:0; Adr 0x0F, bit 7
Code	Function
0x00	VDCS + VDCC = 224 mV
...	...
0x1F	VDCS + VDCC = 472 mV
Note	Settings apply with sum control mode.

Table 27: PWR Output Signal Adjustment

SINE-TO-DIGITAL CONVERSION

SELRES	Adr 0x1C, bit 6:0; Adr 0x1B, bit 7:0		
Code	Angle Steps (per period)	Interpolation Factor	Permiss. Input Frequency
0x00E0	4	x1	200 kHz
0x01B0	8	x2	200 kHz
0x0398	16	x4	200 kHz
0x0414	20	x5	200 kHz
0x090a	40	x10	100 kHz
0x1305	80	x20	50 kHz
0x1804	100	x25	40 kHz
0x3102	200	x50	20 kHz

Table 28: Resolution of Sine-to-Digital Conversion

SELHYS	Adr 0x1D, bit 3:0
Code	Function
0x0 to 0x1	Device test only
0x2	1 increment (≈ 1.8°)
0x3 to 0xD	1.5 to 6.5 increments (≈ 2.7°-11.7°)
0xE	SELRES(6:1) increments, i.e. 0.5 LSB
0xF*	SELRES(6:0) increments, i.e. 1 LSB
Note	*Not permitted in combination with SELRES=0x00E0

Table 29: Encoding of conversion hysteresis

The angle hysteresis is set via SELHYS in multiples of the increment size. With reference to the input sine cycle the maximum length can be 45°.

OUTPUT SETTINGS

Configuration of Output Drivers

The output drivers can be used as push-pull, lowside or highside drivers. TRIHL(1:0) selects the mode of operation. In order to avoid steep edges during transmission via short cables the slew rate can be reduced using SSR (tolerances as given in Electrical Characteristics).

TRIHL	Adr 0x1E, bit 1:0
Code	Function
00	Push-pull operation
01	Highside driver mode (P channel open drain)
10	Lowside driver mode (N channel open drain)
11	Not permitted

Table 30: Output Drive Mode

SSR	Adr 0x1E, bit 3:2
Code	Function
01	Nominal value 25 ns
10	Nominal value 80 ns
Note	Entries 00 and 11 are not permitted

Table 31: Output Slew Rate

Minimum Phase Distance

The minimum phase distance for the A/B and Z output signals can be preselected using MTD(3:0). This setting limits the maximum possible output frequency for secure transmission to counters which are either unable to debounce noise spikes or only permit low input frequencies.

MTD	Adr 0x1D, bit 7:4
Code	Function
0x8	200 ns
0x9	400 ns
...	...
0xE	1.4 µs
0xF	1.6 µs
Note	Codes 0x0 to 0x7 are not permitted. All timing specifications are nominal values, see Elec. Char. No. 511 for tolerances.

Table 32: Minimum Phase Distance

When selecting the minimum phase distance the slew rate setting of the RS422 output drivers and the length of cable used must be taken into consideration.

Zero Signal Positioning

The output of the zero pulse, generated internally, is based on an enable from Z_{In} which can be observed in *System Test Mode* and in *ABZ Mode* at pin NERR (via EMASKA= 0x010 and EMTD= 0x0). As the offset calibration of the zero signal alters the signal width the correct position and width of signal Z_{In} should be checked before the digital configuration parameters are determined.

The zero pulse output position can be selected via CFGZPOS(6:0); the cycle count begins with the sine zero crossing. No zero pulse is output for all values which are either greater than or equal to the interpolation factor.

CFGZPOS	Adr 0x1A, bit 7:0
Bit	Function
7	Enables the selection below
6:0	Count of A/B period releasing the Z output

Table 33: Zero Signal Positioning

CFGZ	Adr 0x19, bit 3:0
Code	Function
1000	Enables Z= 1 with A= 1, B= 1
0100	Enables Z= 1 with A= 1, B= 0
0010	Enables Z= 1 with A= 0, B= 0
0001	Enables Z= 1 with A= 0, B= 1

Table 34: Zero Signal Logic

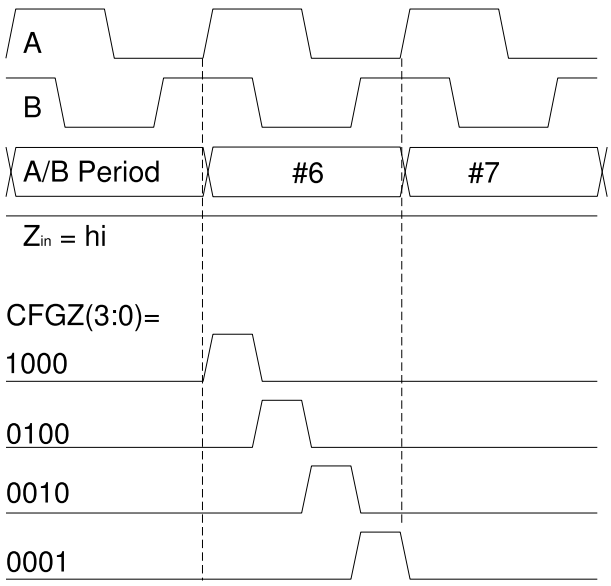


Figure 2: Zero signal logic options (example for CFGZPOS(7)=1, CFGZPOS(6:0)=0x6)

ERROR MONITORING and ALARM OUTPUT

iC-MG monitors input signals, the internal interpolator and the controlled sensor supply via which the input signal levels are stabilized. Should the sensor supply tracking reach control limits this can be interpreted as an end-of-life message, for example.

Two separate error masks determine whether error events cause the RS422 output drivers to shutdown (mask EMASKO) or are signaled as an alarm via the current-limited open drain I/O pin NERR (mask EMASKA).

EMASKO	Adr 0x17, bit 1:0; Adr 0x16, bit 7:0
Bit	Error event
9	n/a
8	Temporal tracking error (e.g. after cycling power)
7	Loss of tracking due to excessive input frequency
6	n/a
5	Excessive temperature shutdown
4	System error: I/O pin NERR pulled to low by an external error signal (only permitted with EPH = 0)
3	PWR control out of range (at max. limit)
2	PWR control out of range (at min. limit)
1	Signal clipping (excessive input level)
0	Loss of signal (poor input level or s/c phase out of range)

Table 35: Driver Shutdown Error Codes

EMASKA	Adr 0x15, bit 1:0; Adr 0x14, bit 7:0
Bit	Error event
9	n/a
8	Temporal tracking error (e.g. after cycling power)
7	Loss of tracking due to excessive input frequency
6	n/a
5	Excessive temperature warning
4	Ungated index enable signal Zin
3	PWR control out of range (at max. limit)
2	PWR control out of range (at min. limit)
1	Signal clipping (excessive input level)
0	Loss of signal (poor input level or s/c phase out of range)

Table 36: Alarm Output Error Codes

The display logic and minimum indication time are settable; an internal pull-up current source can be switched in. At the same time pin NERR has an input function to trigger a new configuration run (see Serial EEPROM Interface).

EPU	Adr 0x17, bit 2
Code	Function
0	No internal pull-up active
1	Internal 300 µA pull-up source active

Table 37: Alarm Output Pull-Up Enable

EPH	Adr 0x15, bit 2
Code	Pin logic
0	Low on error (otherwise Z)
1	Z on error (otherwise low)

Table 38: Alarm Output Logic

EMTD	Adr 0x15, bit 5:3		
Code	Indication time	Code	Indication time
0x0	0 ms	0x4	50 ms
0x1	12.5 ms	0x5	62.5 ms
0x2	25 ms	0x6	75 ms
0x3	37.5 ms	0x7	87.5 ms

Table 39: Minimal Alarm Indication Time

ORDERING INFORMATION

Type	Package	Order Designation
iC-MG	TSSOP20	iC-MG TSSOP20
Evaluation Board		iC-MG EVAL MG1D

For technical support, information about prices and terms of delivery please contact:

iC-Haus GmbH
Am Kuemmerling 18
D-55294 Bodenheim
GERMANY

Tel.: +49 (61 35) 92 92-0
Fax: +49 (61 35) 92 92-192
Web: http://www.ichaus.com
E-Mail: sales@ichaus.com

Appointed local distributors: http://www.ichaus.de/support_distributors.php