# CY62127BV MoBL®

# 1M (64K x 16) Static RAM

## Features

- **High Speed: 55 ns and 70 ns**
- **Wide voltage range: 2.7V–3.6V**
- **Low active power**
  - **— 54 mW (max.) (15 mA)**
- **Low standby power (70 ns)**
  - **— 54 μW (max.) (15 μA)**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Package available in a 44-pin TSOP Type II (forward pinout) and a 48-ball fBGA package**

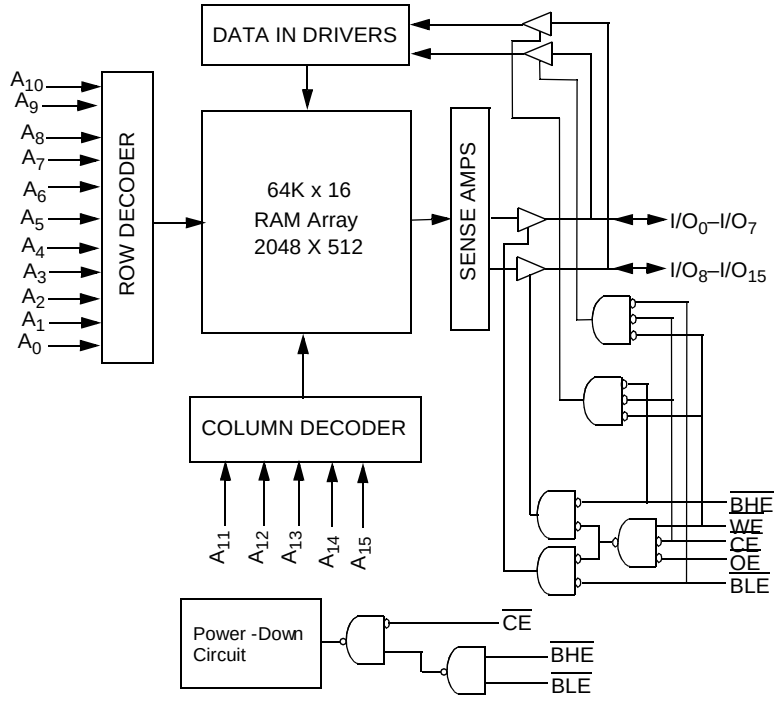
## Functional Description[1]

The CY62127BV MoBL® MoBL® is a high-performance CMOS static RAM organized as 64K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL) in portable applications such as cellular telephones. The device also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling, or when deselected ($\overline{CE}$ HIGH or both $\overline{BLE}$ and $\overline{BHE}$ are HIGH). The input/output pins ($I/O_0$ through $I/O_{15}$) are placed in a high-impedance state when: deselected ($\overline{CE}$ HIGH), outputs are disabled ($\overline{OE}$ HIGH), both Byte High Enable and Byte Low Enable are disabled ($\overline{BHE}$, $\overline{BLE}$ HIGH), or during a write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from I/O pins ($I/O_1$ through $I/O_8$), is written into the location specified on the address pins ($A_0$ through $A_{15}$). If Byte High Enable ($\overline{BHE}$) is LOW, then data from I/O pins ($I/O_9$ through $I/O_{16}$) is written into the location specified on the address pins ($A_0$ through $A_{15}$).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing the Write Enable ($\overline{WE}$) HIGH. If Byte Low Enable ($\overline{BLE}$) is LOW, then data from the memory location specified by the address pins will appear on $I/O_0$ to $I/O_7$. If Byte High Enable ($\overline{BHE}$) is LOW, then data from memory will appear on $I/O_8$ to $I/O_{15}$. See the truth table at the back of this data sheet for a complete description of read and write modes.

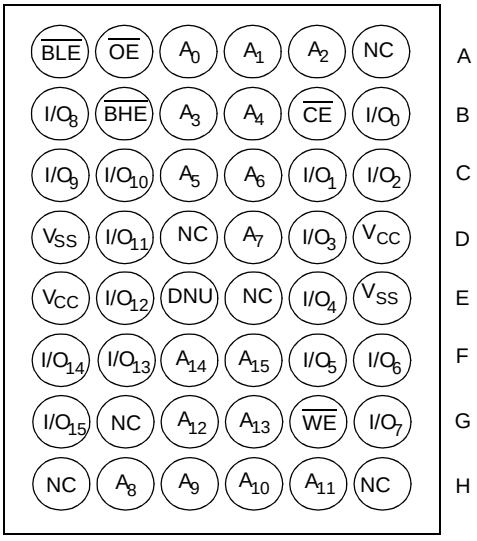
## Logic Block Diagram



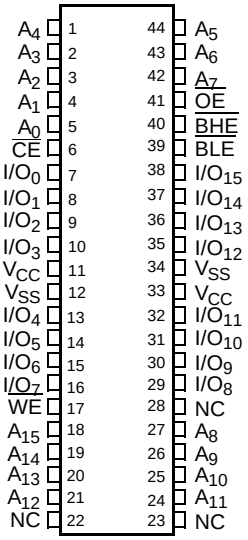

**Note:**
1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on http://www.cypress.com.

## Pin Configurations[2]

**FBGA (Top View)**




**TSOP II (Forward)**
**Top View**




## Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to 4.6V

DC Voltage Applied to Outputs in High-Z State[3] .....–0.5V to $V_{CC}$ + 0.5V

DC Input Voltage[3]..... –0.5V to $V_{CC}$ + 0.5V

Output Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... >2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... >200 mA

## Operating Range

| Range | Ambient Temperature | $V_{CC}$ |
|---|---|---|
| Industrial | –40°C to +85°C | 2.7V to 3.6V |

## Product Portfolio

| Product | $V_{CC}$ Range (V) | | | Speed (ns) | Power Dissipation (Industrial) | | |
|---|---|---|---|---|---|---|---|
| | | | | | Operating, $I_{CC}$ (mA) f = $f_{max}$ | Standby, $I_{SB2}$ (µA) | |
| | $V_{CC(min.)}$ | $V_{CC(typ.)}$[4] | $V_{CC(max.)}$ | | Max. | Typ.[4] | Max. |
| CY62127BV MoBL® | 2.7 | 3.0 | 3.6 | 55 | 20 | 0.5 | 15 |
| | | | | 70 | 15 | | |

**Notes:**
2. NC pins are not connected to the die.
3. $V_{IL(min.)}$ = –2.0V for pulse durations less than 20 ns.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at $V_{CC}$ = $V_{CC(typ.)}$, $T_A$ = 25°C.

## Electrical Characteristics Over the Operating Range

| Parameter | Description | Test Conditions | | CY62127BV MoBL®-55 Min. | CY62127BV MoBL®-55 Typ.[4] | CY62127BV MoBL®-55 Max. | CY62127BV MoBL®-70 Min. | CY62127BV MoBL®-70 Typ.[4] | CY62127BV MoBL®-70 Max. | Unit |
|---|---|---|---|---|---|---|---|---|---|---|
| $V_{OH}$ | Output HIGH Voltage | $I_{OH}$ = –1.0 mA | $V_{CC}$ = 2.7V | 2.2 | | | 2.2 | | | V |
| $V_{OL}$ | Output LOW Voltage | $I_{OL}$ = 2.1 mA | $V_{CC}$ = 2.7V | | | 0.4 | | | 0.4 | V |
| $V_{IH}$ | Input HIGH Voltage | | | 2.0 | | $V_{CC}$ + 0.3V | 2.0 | | $V_{CC}$ + 0.3V | V |
| $V_{IL}$ | Input LOW Voltage | | | –0.3 | | 0.4 | –0.3 | | 0.4 | V |
| $I_{IX}$ | Input Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$ | | –1 | | +1 | –1 | | +1 | µA |
| $I_{OZ}$ | Output Leakage Current | GND ≤ $V_I$ ≤ $V_{CC}$, Output Disabled | | –1 | | +1 | –1 | | +1 | µA |
| $I_{CC}$ | $V_{CC}$ Operating Supply Current | f = $f_{MAX}$ = $1/t_{RC}$ | $V_{CC}$ = 3.6V, $I_{OUT}$ = 0 mA, CMOS Levels | | | 20 | | | 15 | mA |
| $I_{SB1}$ | Automatic CE Power-Down Current— TTL Inputs | Max. $V_{CC}$, $\overline{CE}$ ≥ $V_{IH}$, $V_{IN}$ ≥ $V_{IH}$ or $V_{IN}$ ≤ $V_{IL}$, f = $f_{MAX}$ | | | | 2 | | | 2 | mA |
| $I_{SB2}$ | Automatic CE Power-Down Current— CMOS Inputs | Max. $V_{CC}$, $\overline{CE}$ ≥ $V_{CC}$ – 0.3V, $V_{IN}$ ≥ $V_{CC}$ – 0.3V, or $V_{IN}$ ≤ 0.3V, f = 0 | | | 0.5 | 15 | | 0.5 | 15 | µA |

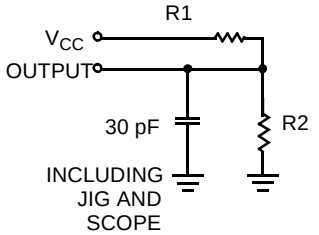
## Capacitance[5]

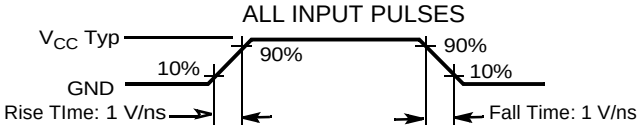
| Parameter | Description | Test Conditions | Max. | Unit |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | $T_A$ = 25°C, f = 1 MHz, $V_{CC}$ = 3.3V | 9 | pF |
| $C_{OUT}$ | Output Capacitance | | 9 | pF |

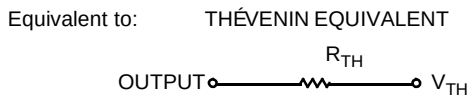
## Thermal Resistance

| Description | Test Conditions | Symbol | BGA | Unit |
|---|---|---|---|---|
| Thermal Resistance (Junction to Ambient)[5] | Still Air, soldered on a 4.25 x 1.125 inch, 4-layer printed circuit board | $\Theta_{JA}$ | 55 | °C/W |
| Thermal Resistance (Junction to Case)[5] | | $\Theta_{JC}$ | 16 | °C/W |

## AC Test Loads and Waveforms



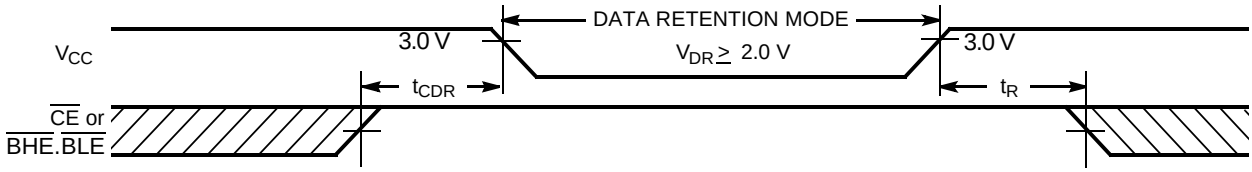

**Note:**
5. Tested initially and after any design or process changes that may affect these parameters.

| Parameters | 3.0V | Unit |
|---|---|---|
| R1 | 1.076 | K Ohms |
| R2 | 1.262 | K Ohms |
| $R_{TH}$ | 0.581 | K Ohms |
| $V_{TH}$ | 1.620 | Volts |

## Data Retention Characteristics (Over the Operating Range)

| Parameter | Description | Conditions | Min. | Typ.[4] | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{DR}$ | $V_{CC}$ for Data Retention | | 2.0 | | 3.6 | V |
| $I_{CCDR}$ | Data Retention Current | $V_{CC}$= $V_{DR}$ = 2.0V, $\overline{CE} \geq V_{CC} - 0.3V$, $V_{IN} \geq V_{CC} - 0.3V$ or $V_{IN} \leq 0.3V$ | | 0.5 | 15 | µA |
| $t_{CDR}$[5] | Chip Deselect to Data Retention Time | | 0 | | | ns |
| $t_R$[6] | Operation Recovery Time | | $t_{RC}$ | | | ns |

## Data Retention Waveform[7]




## Switching Characteristics Over the Operating Range [8]

| Parameter | Description | 55 ns | | 70 ns | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| **Read Cycle** | | | | | | |
| $t_{RC}$ | Read Cycle Time | 55 | | 70 | | ns |
| $t_{AA}$ | Address to Data Valid | | 55 | | 70 | ns |
| $t_{OHA}$ | Data Hold from Address Change | 10 | | 10 | | ns |
| $t_{ACE}$ | $\overline{CE}$ LOW to Data Valid | | 55 | | 70 | ns |
| $t_{DOE}$ | $\overline{OE}$ LOW to Data Valid | | 25 | | 35 | ns |
| $t_{LZOE}$ | $\overline{OE}$ LOW to Low Z[9] | 5 | | 5 | | ns |
| $t_{HZOE}$ | $\overline{OE}$ HIGH to High Z[9, 11] | | 20 | | 25 | ns |
| $t_{LZCE}$ | $\overline{CE}$ LOW to Low Z[9] | 10 | | 10 | | ns |
| $t_{HZCE}$ | $\overline{CE}$ HIGH to High Z[9, 11] | | 20 | | 25 | ns |
| $t_{PU}$ | $\overline{CE}$ LOW to Power-Up | 0 | | 0 | | ns |
| $t_{PD}$ | $\overline{CE}$ HIGH to Power-Down | | 55 | | 70 | ns |
| $t_{DBE}$ | $\overline{BHE}$ / $\overline{BLE}$ LOW to Data Valid | | 55 | | 70 | ns |
| $t_{LZBE}$[10] | $\overline{BHE}$ / $\overline{BLE}$ LOW to Low Z[9] | 5 | | 5 | | ns |
| $t_{HZBE}$ | $\overline{BHE}$ / $\overline{BLE}$ HIGH to High Z[9, 11] | | 20 | | 25 | ns |
| **Write Cycle**[12] | | | | | | |
| $t_{WC}$ | Write Cycle Time | 55 | | 70 | | ns |
| $t_{SCE}$ | $\overline{CE}$ LOW to Write End | 45 | | 60 | | ns |

**Notes:**

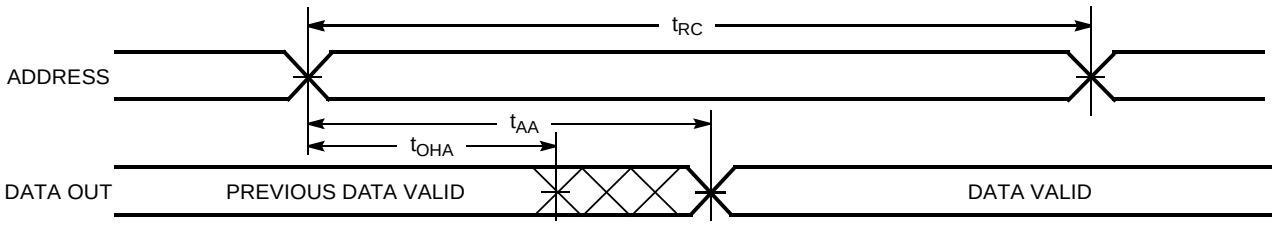
6. Full Device AC operation requires linear $V_{CC}$ ramp from $V_{DR}$ to $V_{CC(min.)}$ > 100 µs or stable at $V_{CC(min.)}$ > 100 µs.
7. $\overline{BHE}.\overline{BLE}$ is the AND of both $\overline{BHE}$ and $\overline{BLE}$. Chip can be deselected by either disabling the chip enable signals or by disabling both $\overline{BHE}$ and $\overline{BLE}$.
8. Test conditions assume signal transition time of 5 ns or less, timing reference levels of $V_{CC(typ.)}/2$, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified $I_{OL}/I_{OH}$ and 30-pF load capacitance.
9. At any given temperature and voltage condition, $t_{HZCE}$ is less than $t_{LZCE}$, $t_{HZBE}$ is less than $t_{LZBE}$, $t_{HZOE}$ is less than $t_{LZOE}$, and $t_{HZWE}$ is less than $t_{LZWE}$ for any given device.
10. If both byte enables are toggled together this value is 10 ns.
11. $t_{HZOE}$, $t_{HZCE}$, $t_{HZBE}$, and $t_{HZWE}$ transitions are measured when the outputs enter a high impedance state.
12. The internal write time of the memory is defined by the overlap of $\overline{WE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$ and/or $\overline{BLE}$ = $V_{IL}$. All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the write.

## Switching Characteristics Over the Operating Range (continued)[8]

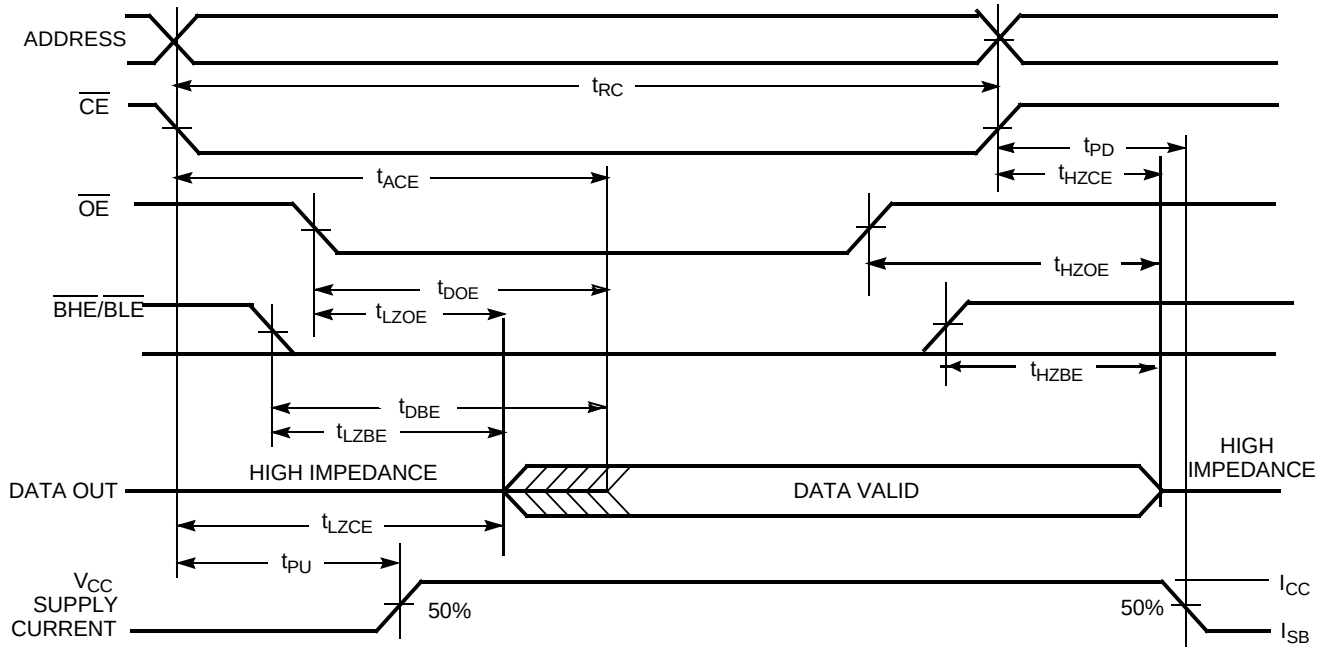
| Parameter | Description | 55 ns | | 70 ns | | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Max. | Min. | Max. | |
| $t_{AW}$ | Address Set-Up to Write End | 45 | | 60 | | ns |
| $t_{HA}$ | Address Hold from Write End | 0 | | 0 | | ns |
| $t_{SA}$ | Address Set-Up to Write Start | 0 | | 0 | | ns |
| $t_{PWE}$ | $\overline{WE}$ Pulse Width | 40 | | 50 | | ns |
| $t_{BW}$ | $\overline{BHE}$ / $\overline{BLE}$ Pulse Width | 45 | | 60 | | ns |
| $t_{SD}$ | Data Set-Up to Write End | 25 | | 30 | | ns |
| $t_{HD}$ | Data Hold from Write End | 0 | | 0 | | ns |
| $t_{HZWE}$ | $\overline{WE}$ LOW to High Z[9, 11] | | 25 | | 25 | ns |
| $t_{LZWE}$ | $\overline{WE}$ HIGH to Low Z[9] | 5 | | 5 | | ns |

## Switching Waveforms

### Read Cycle No. 1 (Address Transition Controlled)[13, 14]



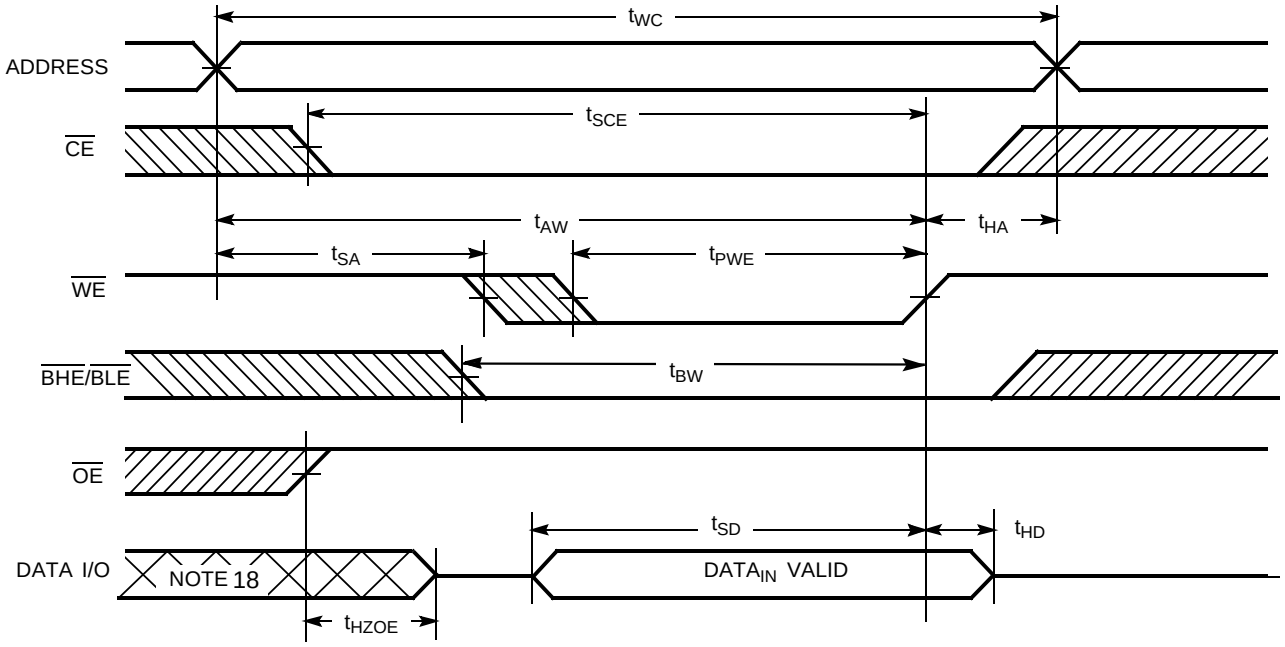

### Read Cycle No. 2 ($\overline{OE}$ Controlled)[14, 15]



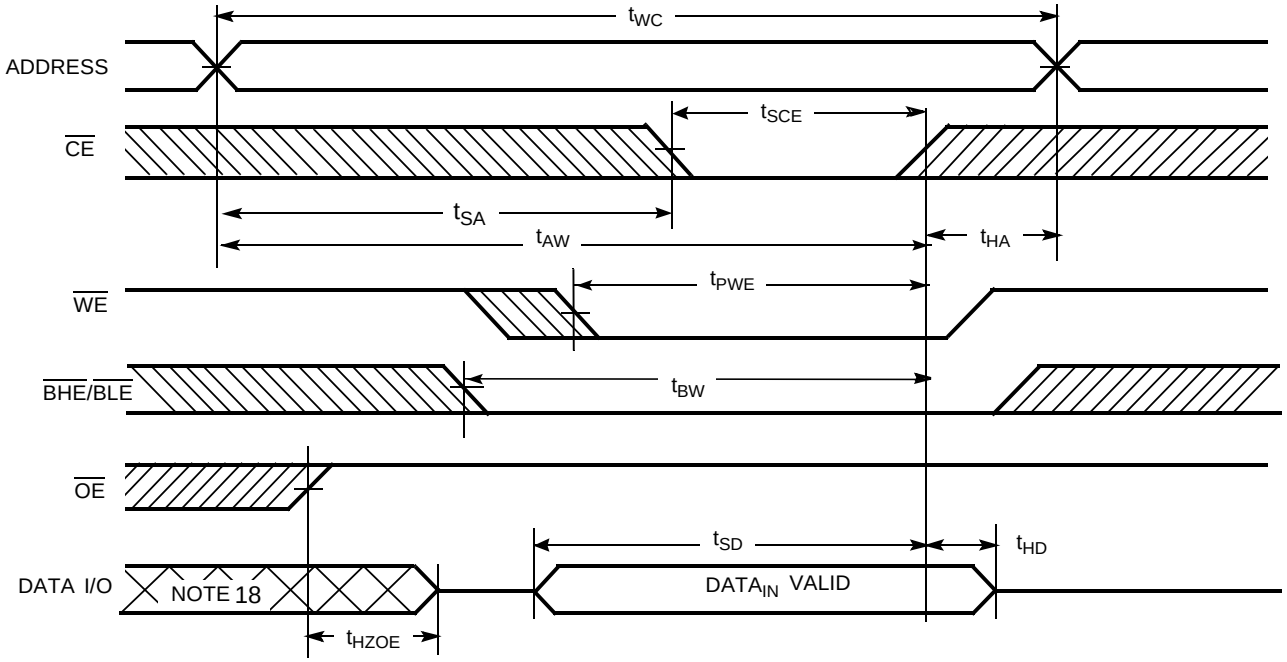

**Notes:**
13. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = $V_{IL}$, $\overline{BHE}$, $\overline{BLE}$ = $V_{IL}$.
14. $\overline{WE}$ is HIGH for read cycle.
15. Address valid prior to or coincident with $\overline{CE}$, $\overline{BHE}$, $\overline{BLE}$ transition LOW.

## Switching Waveforms (continued)

### Write Cycle No. 1 (WE Controlled) [12, 16, 17]



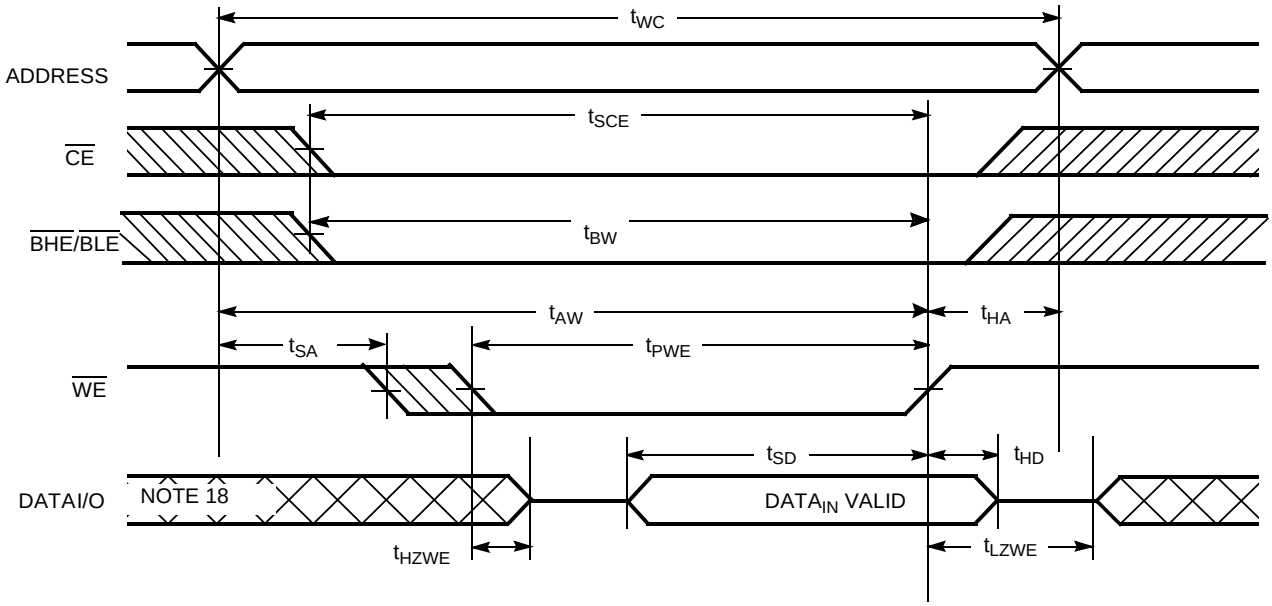

### Write Cycle No. 2 (CE Controlled) [12, 16, 17]



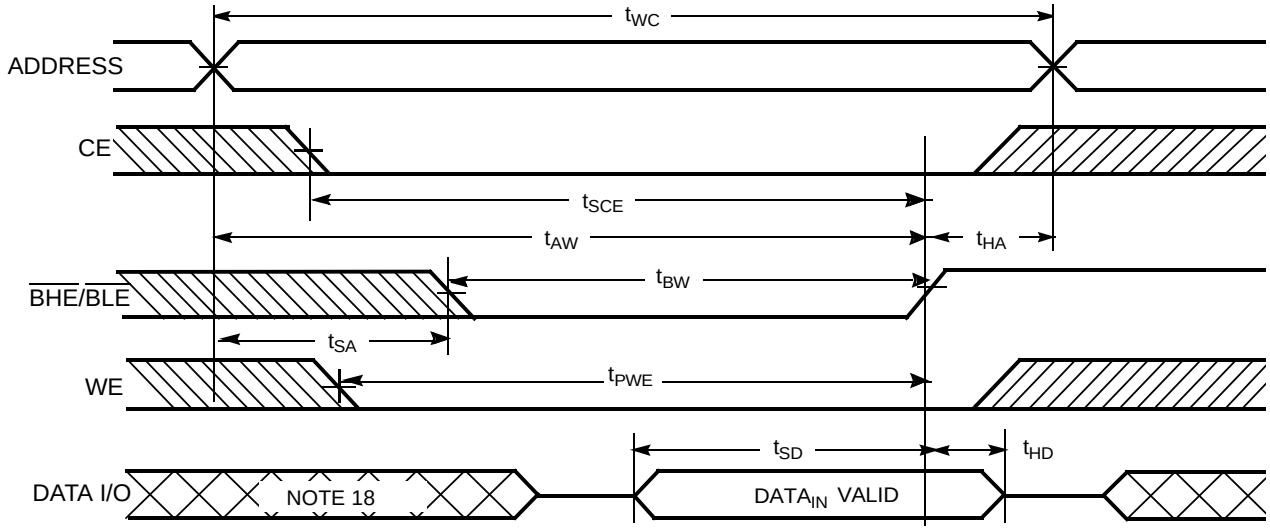

**Notes:**
16. Data I/O is high-impedance if $\overline{OE} = V_{IH}$.
17. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
18. During this period, the I/Os are in output state and input signals should not be applied.

## Switching Waveforms (continued)

**Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)** [17]




**Write Cycle No. 4 ($\overline{BHE}$/$\overline{BLE}$ Controlled, $\overline{OE}$ LOW)** [17]




## Truth Table

| $\overline{CE}$ | $\overline{WE}$ | $\overline{OE}$ | $\overline{BHE}$ | $\overline{BLE}$ | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|---|---|
| H | X | X | X | X | High Z | Deselect/Power-Down | Standby ($I_{SB}$) |
| X | X | X | H | H | High Z | Deselect/Power-Down | Standby ($I_{SB}$) |
| L | H | L | L | L | Data Out ($I/O_O$–$I/O_{15}$) | Read | Active ($I_{CC}$) |
| L | H | L | H | L | Data Out ($I/O_O$–$I/O_7$); $I/O_8$–$I/O_{15}$ in High Z | Read | Active ($I_{CC}$) |
| L | H | L | L | H | Data Out ($I/O_8$–$I/O_{15}$); $I/O_0$–$I/O_7$ in High Z | Read | Active ($I_{CC}$) |
| L | H | H | L | L | High Z | Output Disabled | Active ($I_{CC}$) |
| L | H | H | H | L | High Z | Output Disabled | Active ($I_{CC}$) |

## Truth Table (continued)

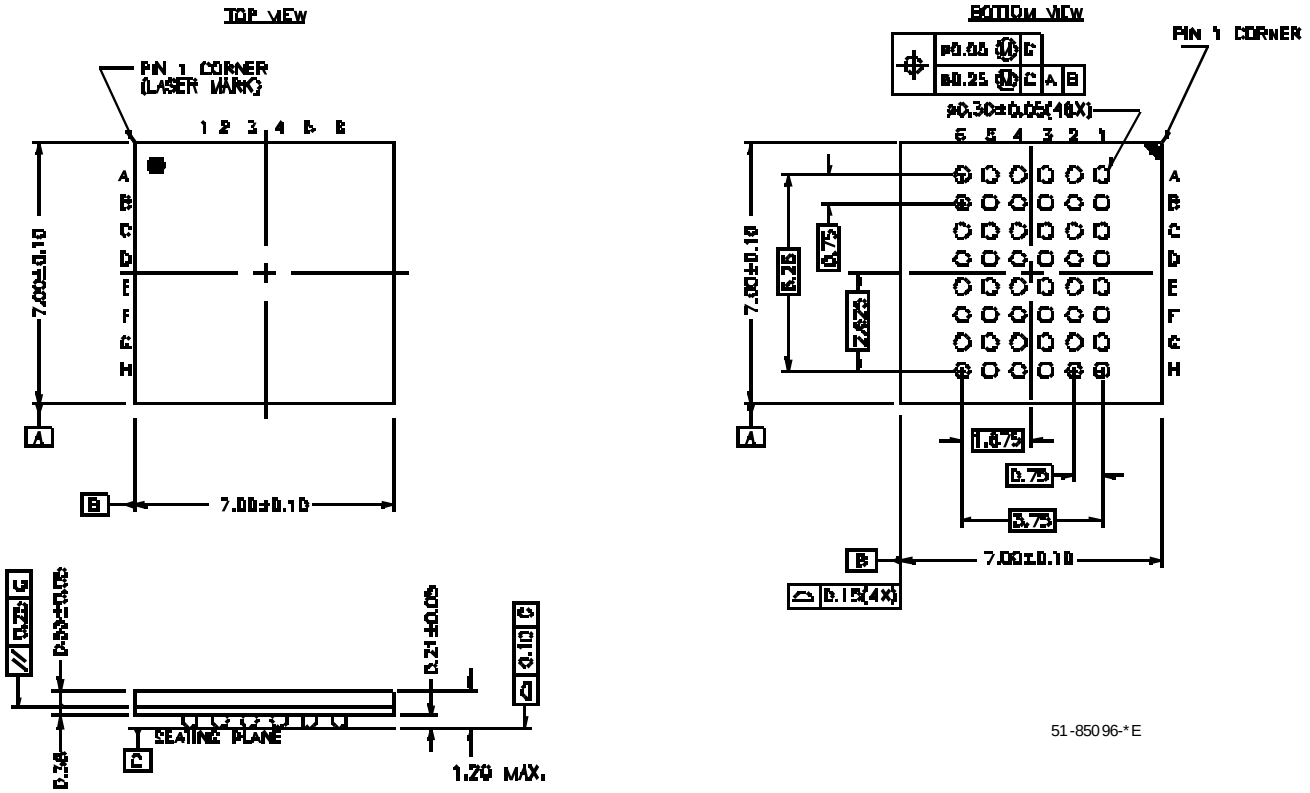
| CE | WE | OE | BHE | BLE | Inputs/Outputs | Mode | Power |
|---|---|---|---|---|---|---|---|
| L | H | H | L | H | High Z | Output Disabled | Active ($I_{CC}$) |
| L | L | X | L | L | Data In ($I/O_O$–$I/O_{15}$) | Write | Active ($I_{CC}$) |
| L | L | X | H | L | Data In ($I/O_O$–$I/O_7$) | Write Lower Byte Only | Active ($I_{CC}$) |
| L | L | X | L | H | Data In ($I/O_8$–$I/O_{15}$) | Write Upper Byte Only | Active ($I_{CC}$) |

## Ordering Information

| Speed (ns) | Ordering Code | Package Name | Package Type | Operating Range |
|---|---|---|---|---|
| 55 | CY62127BVLL-55ZI | Z44 | 44-lead TSOP II | Industrial |
| 70 | CY62127BVLL-70ZI | | | |
| | CY62127BVLL-70BAI | BA48A | 48-ball Fine Pitch BGA (7 mm x 7 mm x 1.2 mm) | |
| | CY62127BVLL-70BVI | BV48A | 48-ball Fine Pitch BGA (6 mm x 8 mm x 1 mm) | |

## Package Diagrams

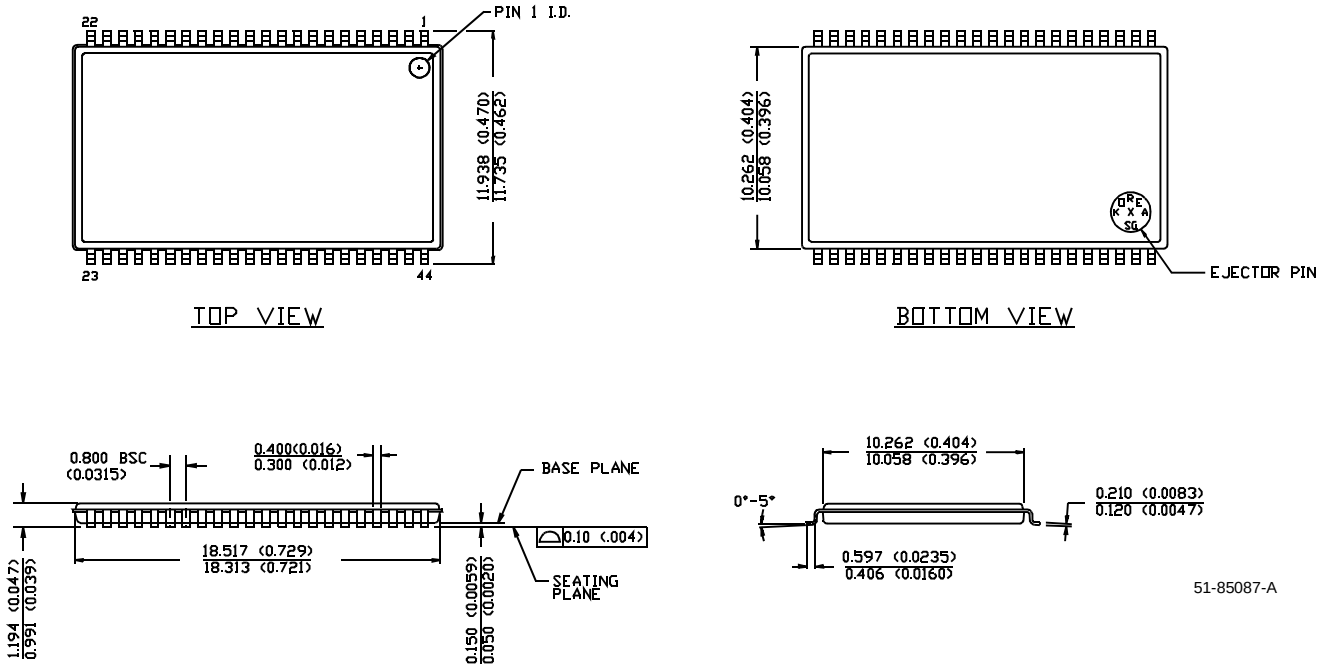
**48-Ball (7.00 mm x 7.00 mm x 1.2 mm) FBGA BA48A**



**Package Diagrams** (continued)

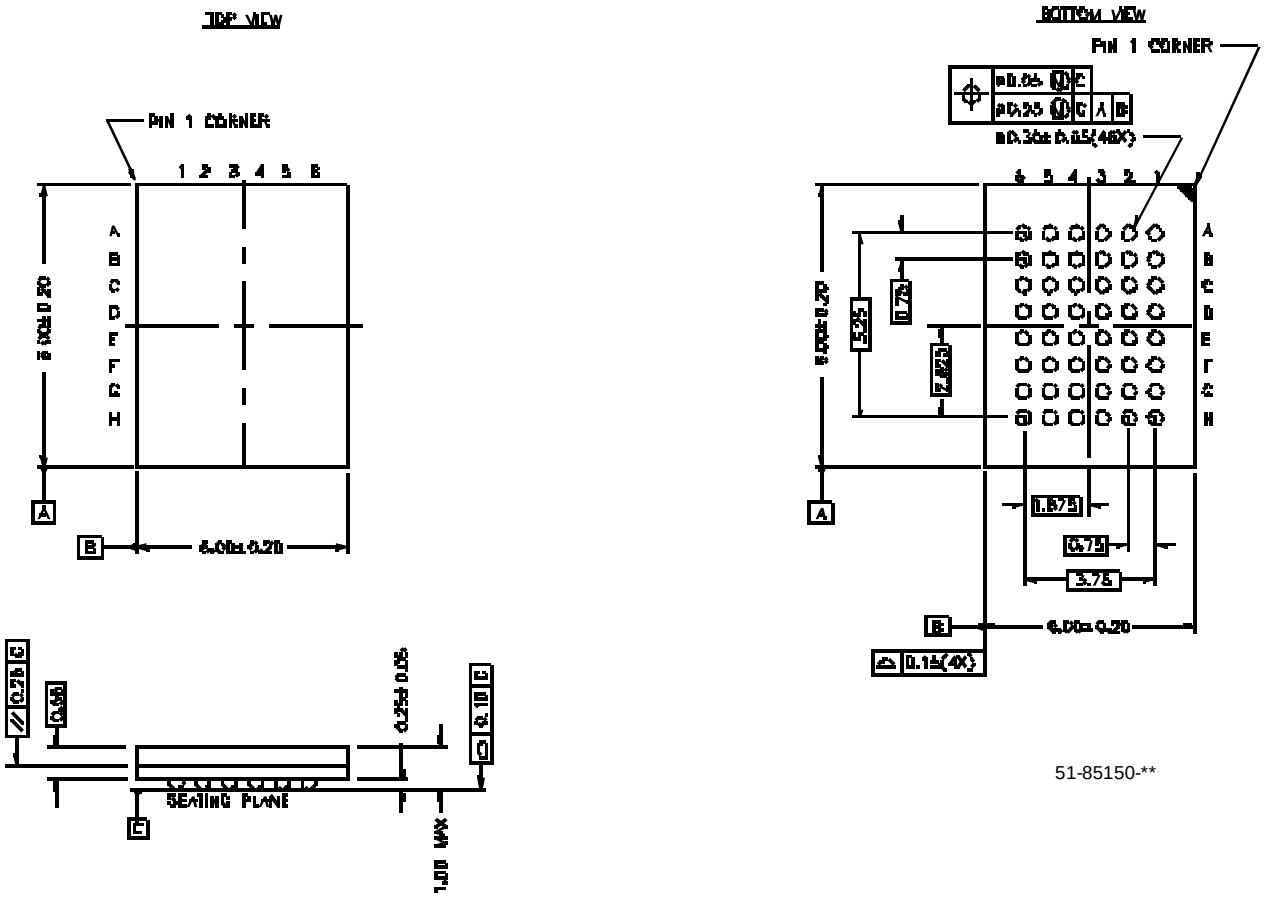
**44-pin TSOP II Z44**

DIMENSION IN MM (INCH)
MAX
MIN.



**Package Diagrams** (continued)

**48-Lead VFBGA (6 x 8 x 1 mm) BV48A**

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| Document Title: CY62127BV MoBL® 1M (64K x 16) Static RAM<br>Document Number: 38-05155 | | | | |
|---|---|---|---|---|
| **REV.** | **ECN NO.** | **Issue Date** | **Orig. of Change** | **Description of Change** |
| ** | 109899 | 10/02/01 | SZV | Change from Spec number: 38-01018 to 38-05155 |
| *A | 113307 | 03/01/02 | MGN | Format standardization & update ordering information |
| *B | 116362 | 09/04/02 | GBI | Add footnote 1 and BV Package. |