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Fax: 886-2-29174598
URL: http://www.princeton.com.tw

Programmable Encoder IC **PT2241**

DESCRIPTION

PT2241 is a tri-state programmable encoder utilizing CMOS Technology specially designed for remote control applications. It encodes address and data codes into a coded waveform suitable for RF modulation and can provide up to 3^{11} Address which may be designed by a one-time programmable process. PT2241 can support up to 4 Data Bits, thereby reducing inventory pressures. It is housed in 8 or 16-pin DIP or SOP Package. The pin assignments and application circuit are optimized for easy PCB Layout and cost saving advantage.

FEATURES

- CMOS technology
- Low power consumption
- Least external components
- High noise immunity
- Single resistor oscillator
- Operating voltage: 1.8~15V
- Up to 4 data pins
- Up to 3^{11} address codes
- One-time programmable process
- Available in SOP or DIP package
- Reduction of inventory pressures

APPLICATIONS

- Burglar alarm system
- Car security system
- Car/Garage door controller
- Home/Office security system
- Personal alarm system

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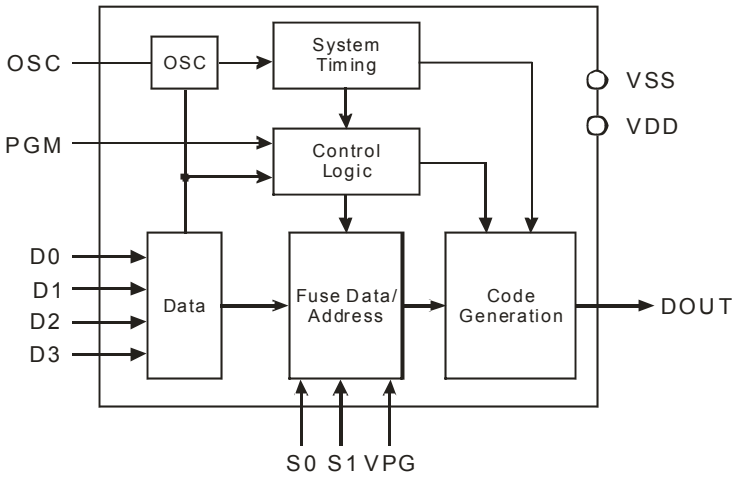
BLOCK DIAGRAM



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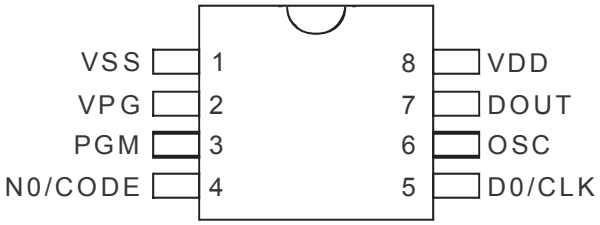
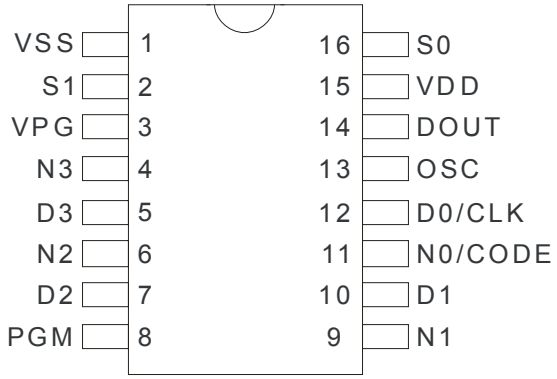
PIN CONFIGURATION

8 PINS



PT2241P

16 PINS



PT2241P-16

PIN DESCRIPTION

Pin Name	I/O	Description	Pin No.	
			8 pins	16 pins
VSS	-	Negative power supply	1	1
S1, S0	I	Select pin Normal="High" When these pins are set to "Low", they are used to select the number of data pins	-	16, 2
VPG	I	Voltage program pin Normal="Floating" When this pin is set to "Low", the programmed "Low" bits can be burnt-out	2	3
D0/CLK	I	Data/Clock input pin Normal="Low" (Internal pull-low resistor) When PGM="High", this pin functions as a Clock input terminal When the PGM="Low", this pin functions as a Data input terminal	5	12
D1, D2, D3	I	Data pins (Internal pull-low resistor) These pins are determined by the state of S1 and S0	-	10, 7, 5
N0/CODE	I	Normal="Low" (Internal pull-low resistor) When PGM="High", this pin functions as a Code input terminal	4	11
N1, N2, N3	I	Normally connected to D1~D3 (Internal pull-low resistor)	-	9, 6, 4
PGM	I	Program pin Normal="Low" (Internal pull-low resistor) When this pin is set to "High", PT2241 can be programmed	3	8
OSC	I	Oscillator pin	6	13
DOUT	O	Data output pin Normal="Low" When PGM is "High", this pin shows the programming status of PT2241	7	14
VDD	-	Positive power supply	8	15

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FUNCTION DESCRIPTION

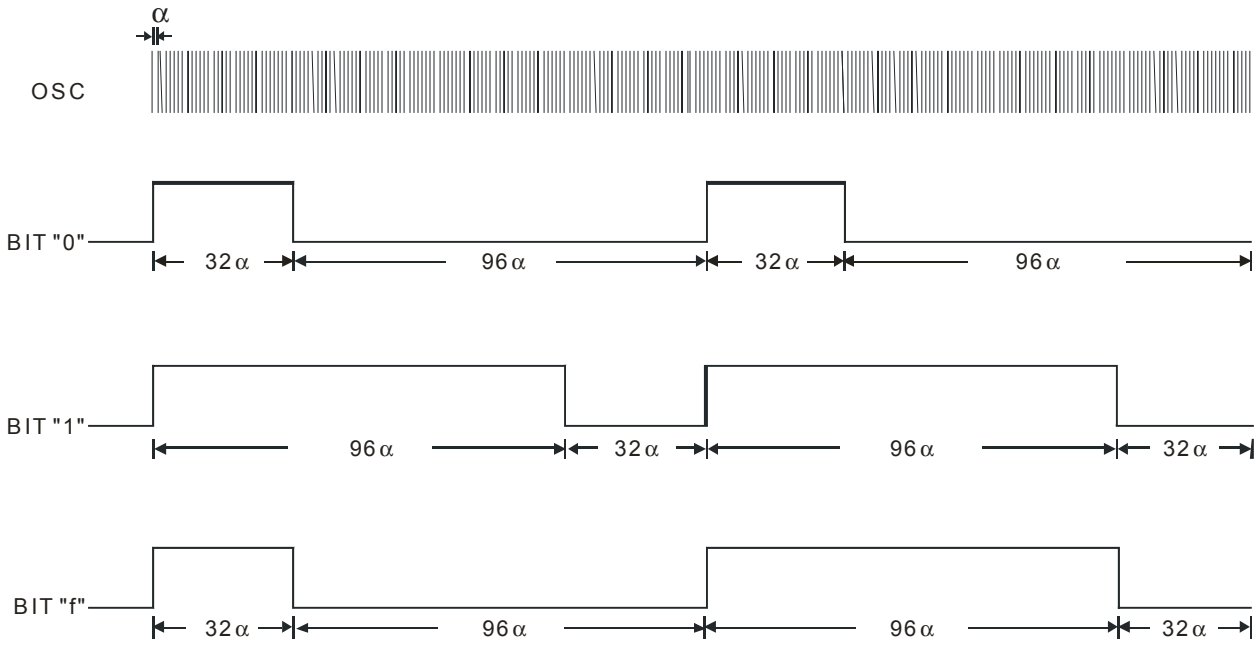
PT2241 encodes the address code (which are one-time programmable) and data into a special waveform and outputs it to the DOUT. This waveform is fed to the RF modulator for transmission. The transmitted radio frequency is received by the RF demodulator and reshaped into the special waveform. PT2270 is then used to decode the waveform and set the corresponding output pin(s). Thus, completing a remote control encoding and decoding function.

CODE BITS

A Code Bit is the basic component of the encoded waveform, and can be classified as either an (Address/Data) Bit or a SYNC (Synchronous) Bit.

DATA BIT WAVEFORM

Data Bit can be designated as either Bit “0”, “1” or “f” if it is in “Low”, “High” or “Floating” State respectively. One bit waveform consists of two pulse cycles and each pulse cycle has 128 oscillating time periods. For further details, please refer to the diagram below:



where: the oscillating time period, α =1/f and (f is the oscillation frequency)

As you can see in the diagram above, Bit “0” consists of 2 pulse cycles. Each Bit “0” pulse cycle goes “High“ for 32 α (where α = oscillating time period) then changes to “Low” for 96 α. Likewise, Bit “1” has 2 pulse cycles and each Bit “1” pulse cycle consists of a “High” pulse for 96 α is followed by “Low” Pulse for 32 α. For simplicity, let us designate one Bit “0” pulse cycle as a “Short Pulse” and one Bit “1” Pulse Cycle as a “Long Pulse”. Then, we can say that a Bit “F” or a floating bit consists of a “Short Pulse” followed by a “Long Pulse”.

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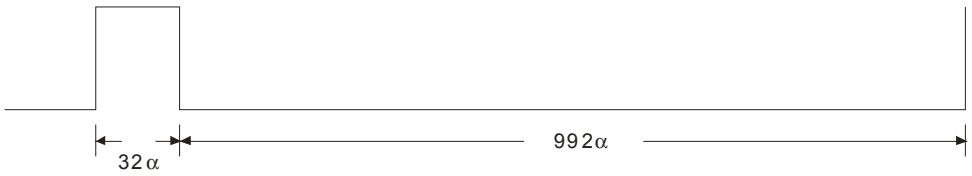
SYNCHRONOUS (SYNC.) BIT WAVEFORM

The Synchronous Bit Waveform is 4 bits long. It exhibits a high pulse for 32α followed by a low pulse for 992α. Please refer to the diagram below:



CODE WORD

A group of Code Bits is called a Code Word. A Code Word consists of 11 Address, 1 Data Bit followed by one Sync Bit. Please refer to the diagram below:

A0	A1	·····	A7	D3/A8	D2/A9	S1/A10	D0	Sync. bit

First bit transmitted

Notes:
1. AN=Address Bits
2. DN=Data Bits

PT2241 provides (four) data selections, namely: 1/2/3/4 Data Type which may be defined by the S0 and S1 Pins. Up to 4 data bits may be selected. Please refer to the diagram below:

1 Data Type: S0=”1” and S1=”1”

A0	A1	·····	A7	A8	A9	A10	D0	Sync. bit

2 Data Type: S0=”1” and S1=”0”

A0	A1	·····	A7	A8	A9	D1	D0	Sync. bit

3 Data Type: S0=”0” and S1=”1”

A0	A1	·····	A7	A8	D2	D1	D0	Sync. bit

4 Data Type: S0=”0” and S1=”0”

A0	A1	·····	A7	D3	D2	D1	D0	Sync. bit

PROGRAMMING

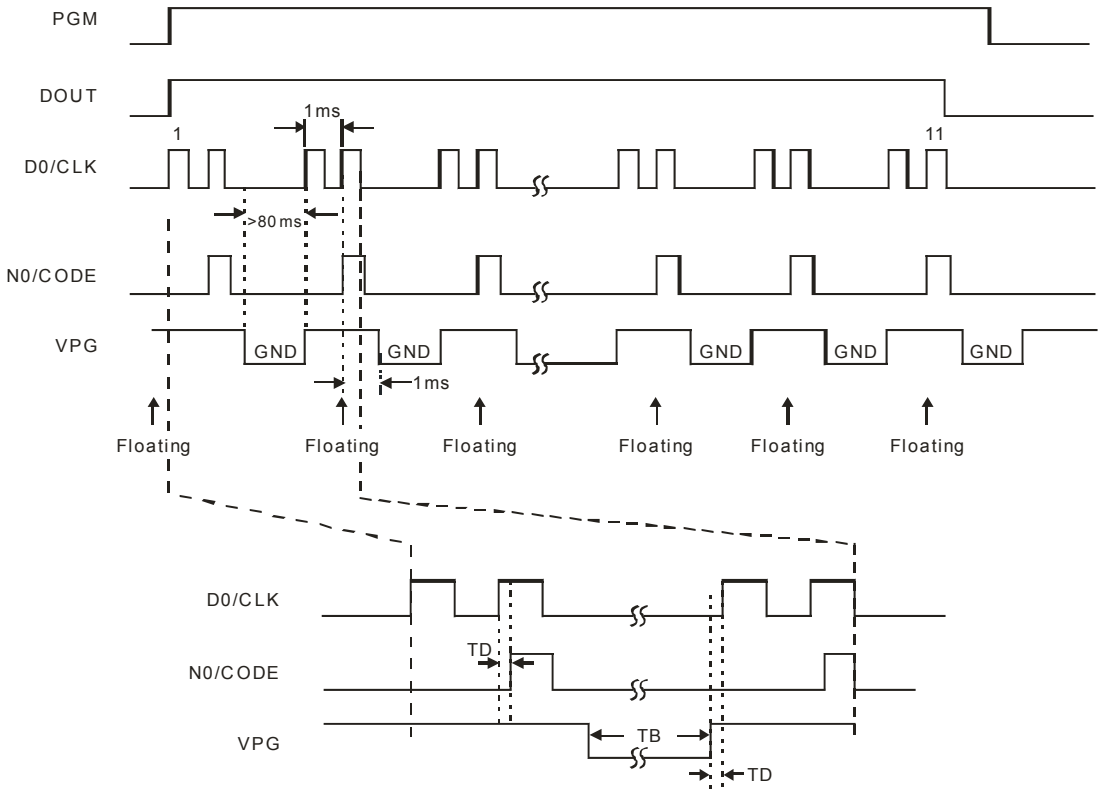
Address Bits of PT2241 are programmable only once and the Output Code Word contains 11 Address Bits, one Data Bit, and one Sync Bit.

WRITE

When PGM is set to “High” Level, the WRITE is activated and DOUT changes from “Low” to “High”. The PT2241 is now ready to be programmed. It must be noted that the first to receive programming instruction is A0 followed by A1 and so forth.
In the WRITE Mode, N0 signal determines the value of the Address Bit. When N0 is “HIGH”, the corresponding Address Bit is set to “1”. Conversely, when N0 is “Low” (or floating), the corresponding Address Bit is set to “0”. After the 11th clock (1 clock consist of 2 pulses), DOUT changes from “High” to “Low” indicating that the address programming has been completed.

DATA PROGRAMMING IN PT2241

When VPG is “Low”, at least 80ms is needed to burn out the fuse so that data may be programmed into the PT2241.



Notes: In this diagram:
1. all addresses are programmed to “F” (“Floating”) State
2. TD=Delay Time and cannot be less than 0.1ms
3. TB=Burn-Out Time and cannot be less than 80ms.

In the Programming Technique used by PT2241, data are written/programmed into the chip two bits at a time. The Clock contains 2 pulses and the burn-out time. Each pulse should be more than 1ms and burn-out time should be greater than 80ms.

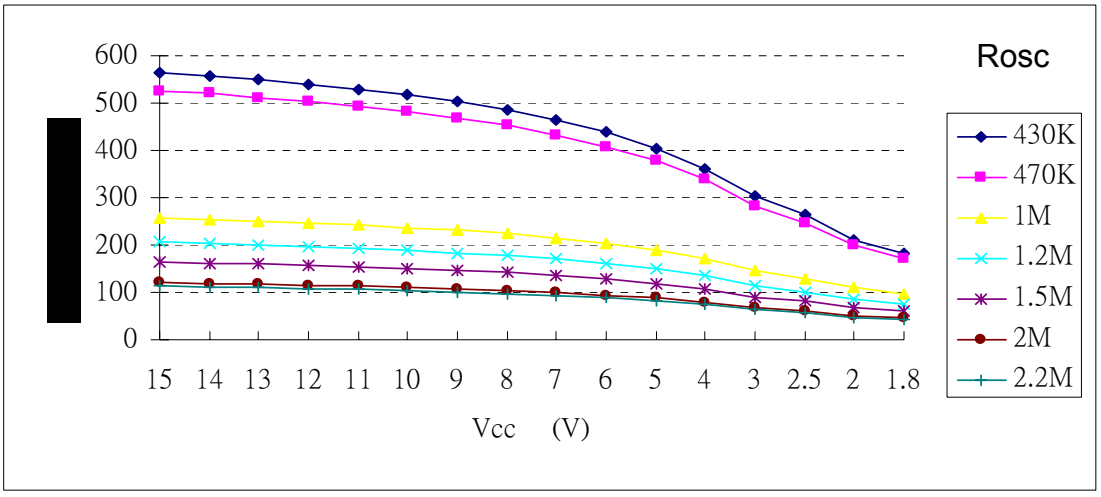
Please refer to the PT2241 Application Notes and the PT2241 Programming Manual.

SINGLE RESISTOR OSCILLATOR

The built-in oscillator circuit of PT2241 allows a precision oscillator to be constructed by connecting an external resistor (Rosc) to the OSC Pin. For the PT2270 to decode correctly the received waveform, the oscillator frequency of PT2270 must be 0.2 ~ 3.2 times that of the transmitting PT2241. The typical oscillator frequency with various resistor values for both PT2241 and PT2270 are given below:

PT2241	PT2270
620KΩ	1.0KΩ
2.0MΩ	1.2MΩ
3.3MΩ	2.0MΩ

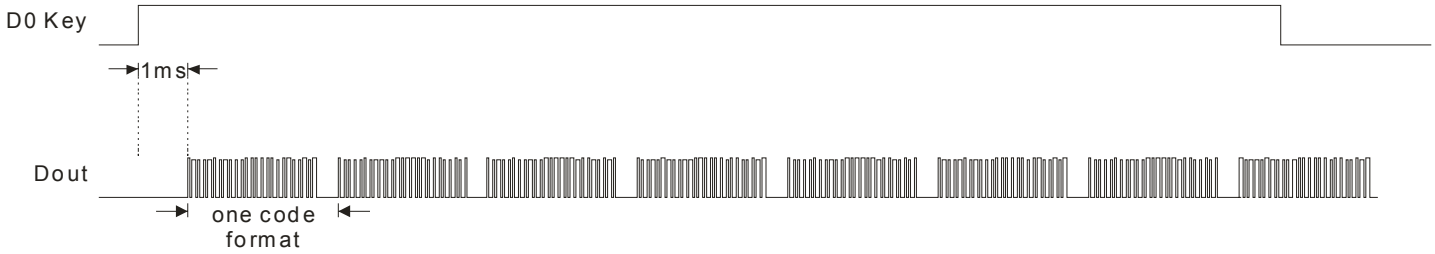
ENCODER (PT2241) OSCILLATION FREQUENCY



OUTPUT PIN (DOUT)

While programming PT2241, the state of the IC may be determined by DOUT. During the PROGRAM Mode, DOUT changes from “Low” to “High”. When the signal inputted from the D0 Pin‘s reaches the 11th falling edge of the CLK, the DOUT state changes to “Low”. During the rising edge of the 12th CLK, DOUT goes to “High”. It must be noted that PT2241 can only be programmed once.

Under normal condition, the DOUT Output Code Format does not include a carrier. Please refer to the diagram below:



DATA PINS

PT2241 can support up to a maximum of 4 data pins which can be determined by the S1 and S0 Pins. Please refer to table below:

Data bits	Address bits	S0	S1	Data pins
1	11	1	1	D0
2	10	1	0	D0, D1
3	9	0	1	D0, D1, D2
4	8	0	0	D0, D1, D2, D3

Data Bits, D1 ~ D3 can de defined by S0 and S1. Address Bits - A10 ~ A8 - may be set to “1”, “0” or “f” and does not affect the outputs of D1 ~ D3. If the data bits are all set to “High”, they do not conflict with each other, and the Output Data Bits are all “High”.

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Condition	Rating	Unit
Operating voltage	VDD		-0.3 ~ 15	V
Input voltage	VIN	VDD=12V All outputs not connected	VSS-0.3 ~ VDD+0.3	V
Operating temperature	Topr	VDD=12V	-40 ~ +85	℃
Storage temperature	Tstg		-65 ~ +150	℃

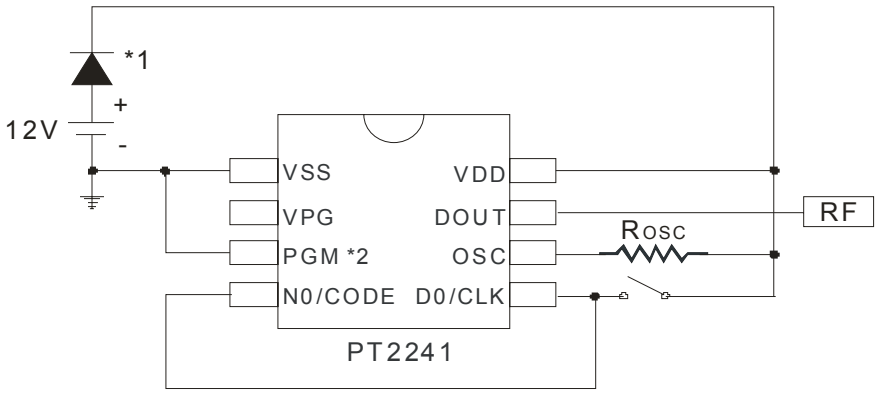
DC ELECTRICAL CHARACTERISTICS

(Unless otherwise specified, Ta=25℃, VDD=12V)

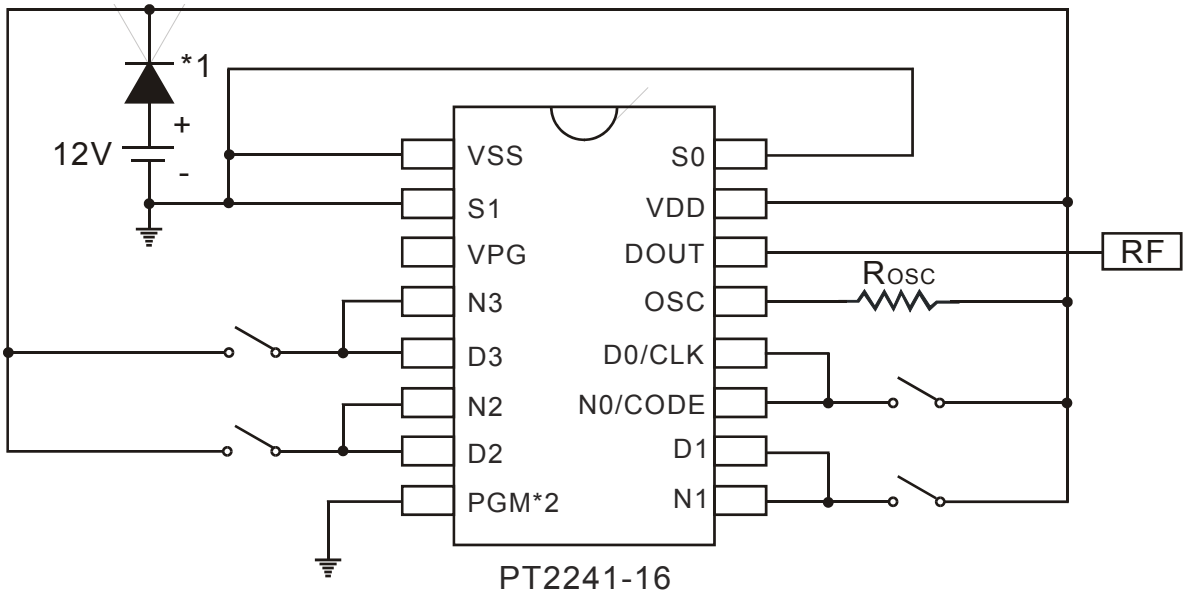
Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	VDD		1.8	12	15	V
Stand-by current	ISB	OSC connected to “Low” other pins floating	-	-	1	μA
Operating current	IOP	Connect one data pin to “high”	-*	-	5	mA
DOUT output current	IOH	VDD=12V, VOH=5V	30	25	-	mA
		VDD=9V, VOH=4.5V	12	15	-	
		VDD=3V, VOH=1.5V	1.2	1.4	-	

APPLICATION CIRCUIT

8 PIN-1 DATA



16 PIN-4 DATA



Notes:

1. In order that IC protection is assured, please make sure that a diode is connected between the battery and the VDD. If the diode is not connected and the battery polarity was inverted, the IC will fail.
2. In order to avoid unexpected programming, we suggest PGM pin connects with ground (VSS) to avoid PGM pin changed to “High level” and cause into “Programming mode”

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ORDER INFORMATION

Valid Part Number	Package Type	Top Code	Address Codes
PT2241P	8 Pins, DIP, 300mil	PT2241P	Programmed
PT2241P-S	8 Pins, SOP, 150mil	PT2241P-S	Programmed
PT2241P-16	16 Pins, DIP, 300mil	PT2241P-16	Programmed
PT2241P-16S	16 Pins, SOP, 150mil	PT2241P-16S	Programmed

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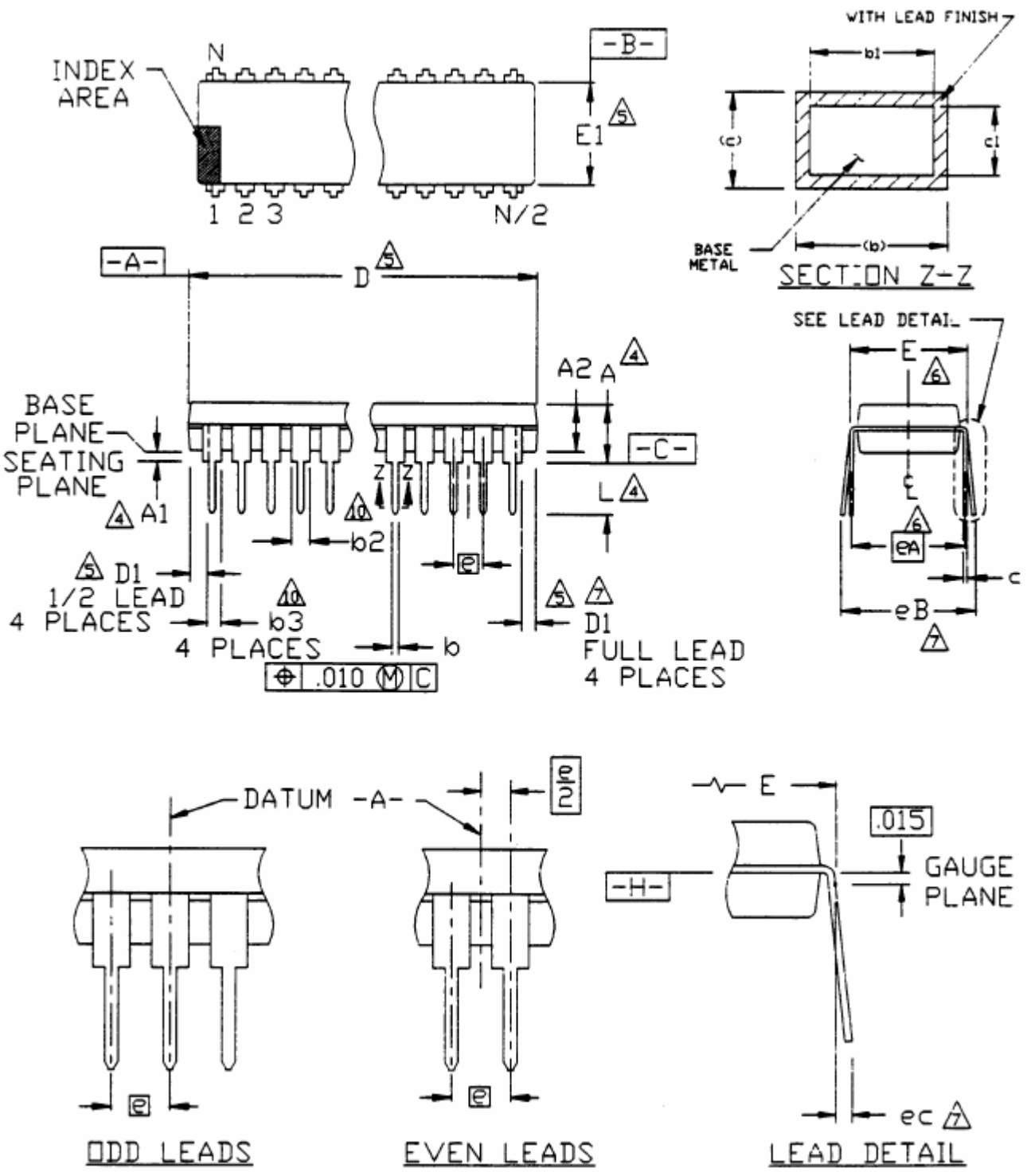
PACKAGE INFORMATION

8 PINS, DIP, 300MIL



Symbol	Dimensions in Inches		
	Min.	Nom.	Max.
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.355	0.365	0.400
D1	0.005	-	-
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e	0.100 bsc.		
eA	0.300 bsc.		
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

Notes:
1. All dimensions are in INCHS.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimensions “A”, “A1” and “L” are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
4. “D”, “D1” and “E1” dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
5. “E” and “eA” measured with the leads constrained to be perpendicular to datum -c-.
6. “eB” and “eC” are measured at the lead tips with the loads unconstrained.
7. “N” is the number of terminal positions. (N=8)
8. Pointed or rounded lead tips are preferred to ease insertion.
9. “b2” and “b3” maximum dimensions are not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25 mm).
10. Variation BA has a b3 dimension and is 1/2 lead package.
11. Distance between leads including dambar protrusions to be 0.005 inch minimum.
12. Datum plane -H- coincident with the bottom of lead, where lead exits body.
13. Refer to JEDEC MS-001 Variation BA.

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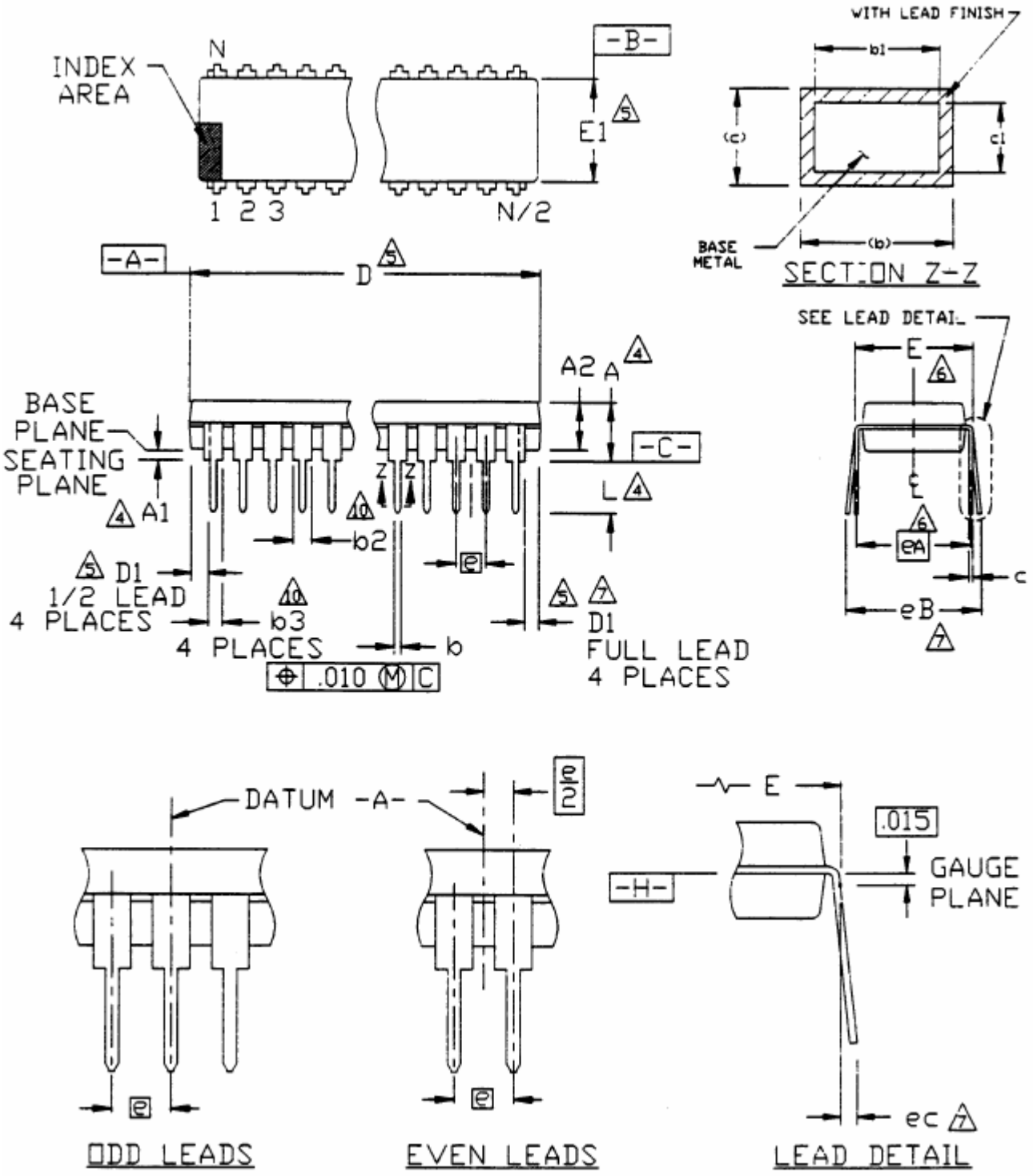
16 PINS, DIP, 300MIL



Symbol	Dimensions in Inches		
	Min.	Nom.	Max.
A	-	-	0.210
A1	0.015	-	-
A2	0.115	0.130	0.195
b	0.014	0.018	0.022
b1	0.014	0.018	0.020
b2	0.045	0.060	0.070
b3	0.030	0.039	0.045
c	0.008	0.010	0.014
c1	0.008	0.010	0.011
D	0.735	0.755	0.775
D1	0.005	-	-
E	0.300	0.310	0.325
E1	0.240	0.250	0.280
e	0.100 bsc.		
eA	0.300 bsc.		
eB	-	-	0.430
eC	0.000	-	0.060
L	0.115	0.130	0.150

Notes:
1. All dimensions are in INCHS.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimensions “A”, “A1” and “L” are measured with the package seated in JEDEC Seating Plane Gauge GS-3.
4. “D”, “D1” and “E1” dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch.
5. “E” and “eA” measured with the leads constrained to be perpendicular to datum -c-.
6. “eB” and “eC” are measured at the lead tips with the loads unconstrained.
7. “N” is the number of terminal positions. (N=16)
8. Pointed or rounded lead tips are preferred to ease insertion.
9. “b2” and “b3” maximum dimensions are not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25 mm).
10. Variation BA has a b3 dimension and is 1/2 lead package.
11. Distance between leads including dambar protrusions to be 0.005 inch minimum.
12. Datum plane -H- coincident with the bottom of lead, where lead exits body.
13. Refer to JEDEC MS-001 Variation BB.

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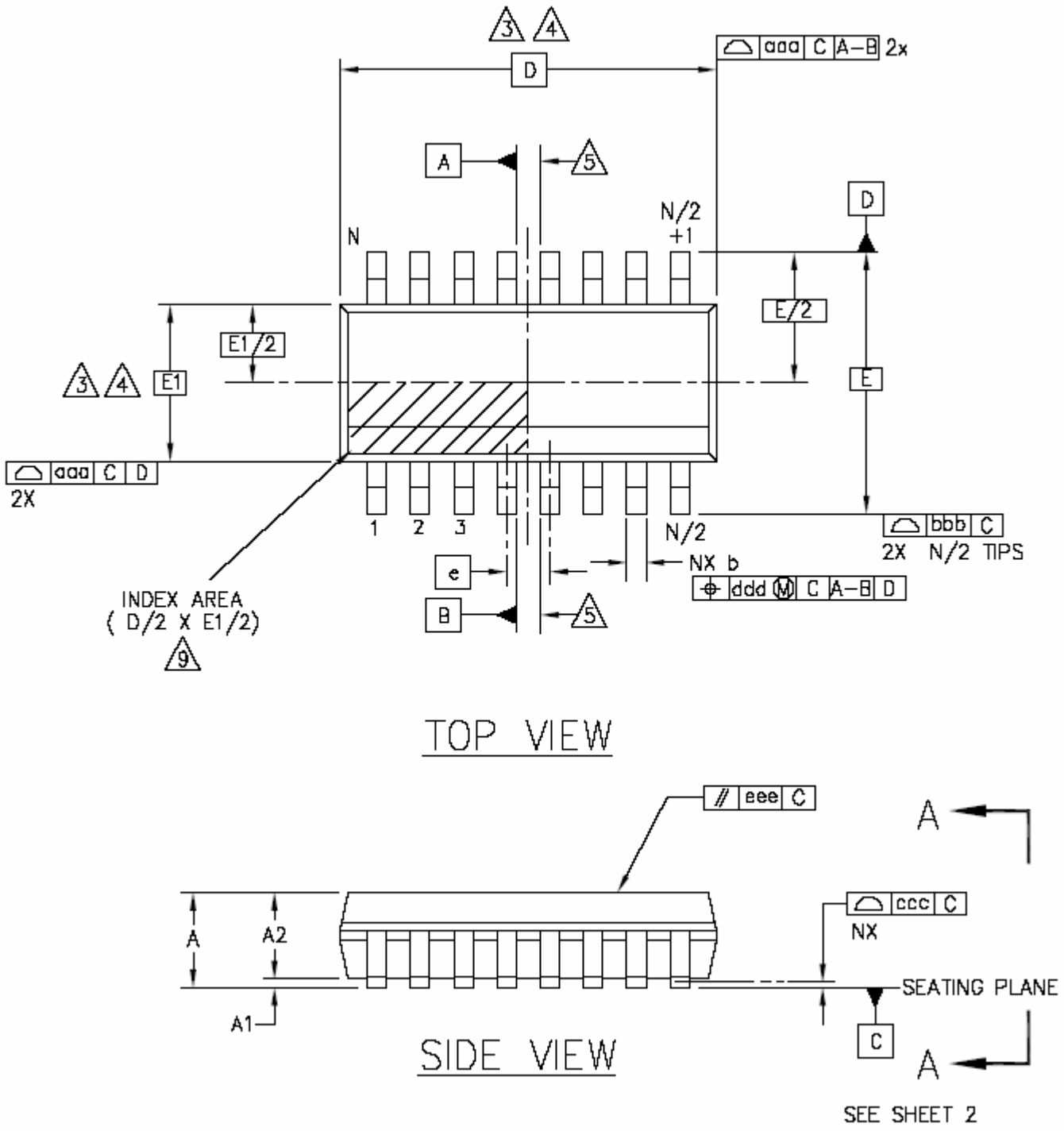
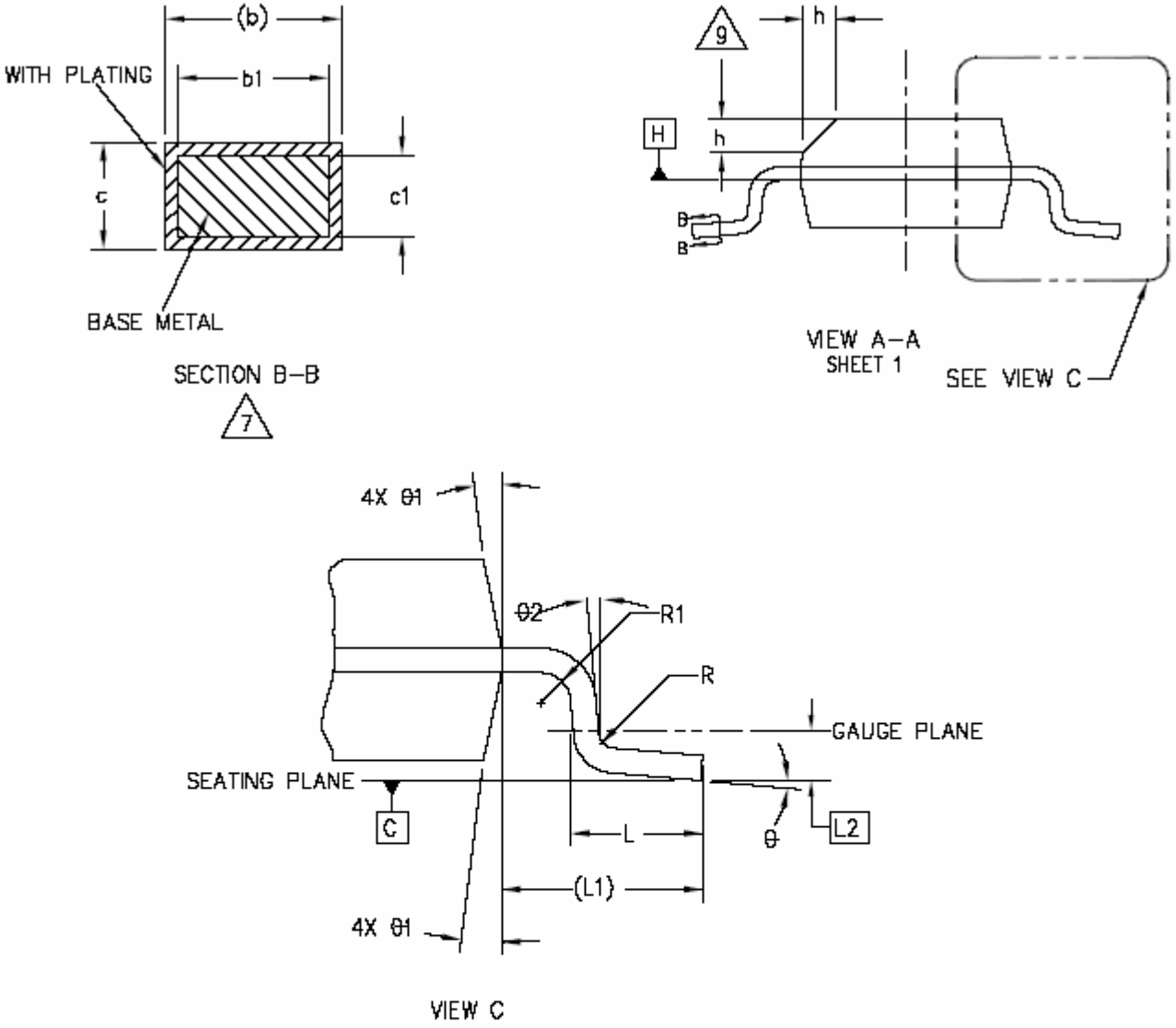
8 PINS, SOP, 150MIL




(b)
WITH PLATING
b1
c
c1
BASE METAL
SECTION B–B
7
g
h
H
h
B
B
VIEW A–A
SHEET 1
SEE VIEW C
4X θ1
θ2
R1
R
GAUGE PLANE
SEATING PLANE
C
L
θ
L2
(L1)
4X θ1
VIEW C
(b)
5
B
X
X = A &/or B
ODD LEAD SIDES
TOPVIEW
5
e/2
X
X = A &/or B
EVEN LEAD SIDES
TOPVIEW

Symbol	Min.	Typ.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.17	-	0.25
c1	0.17	-	0.23
D	4.90 BSC.		
E	6.00 BSC.		
E1	3.90 BSC.		
e	1.27 BSC.		
L	0.40	-	1.27
L1	1.04 REF.		
L2	0.25 BSC.		
R	0.07	-	-
R1	0.07		-
h	0.25	-	0.50
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

Notes:
1. Dimensioning and tolerancing per ANSI Y 14.5M-1994
2. Controlling Dimension: MILLIMETERS.
3. Dimension D does not include mold flash protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 in) per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side. D and E1 dimensions are determined at datum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
5. Datums A & B to be determined at datum H.
6. N is the number of terminal positions. (N=8)
7. The dimensions apply to the flat section of the lead between 0.10 to 0.25mm from the lead tip.
8. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of the “b” dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.
9. This chamfer feature is optional. If it is not present, then a pin 1 identifier must be located within the index area indicated.
10. Refer to JEDEC MS-012, Variation AA.

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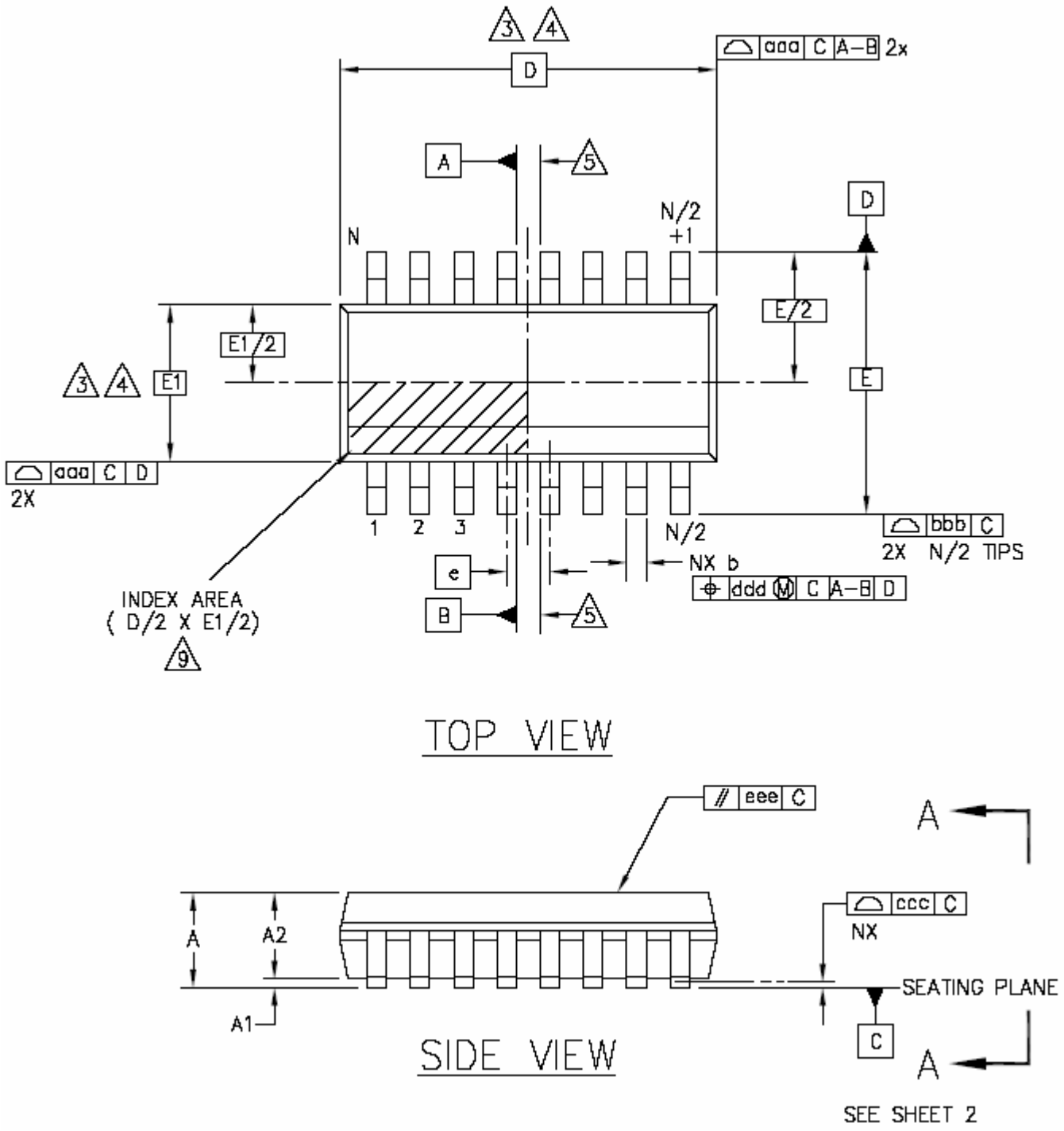
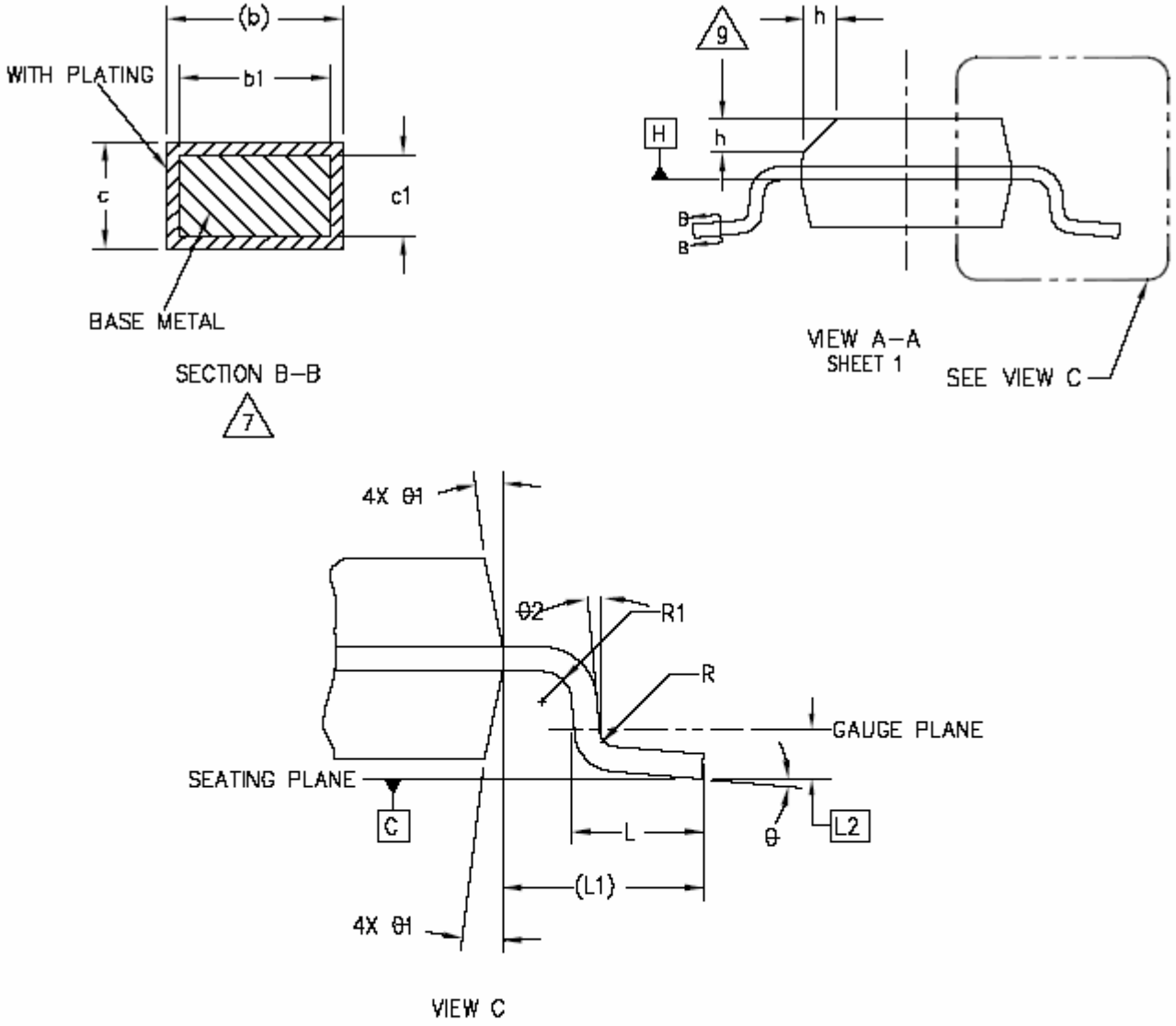
16 PINS, SOP, 150MIL




(b)
WITH PLATING
b1
c
c1
BASE METAL
SECTION B–B
7
g
h
H
h
B
B
VIEW A–A
SHEET 1
SEE VIEW C
4X θ1
θ2
R1
R
GAUGE PLANE
SEATING PLANE
C
L
θ
L2
(L1)
4X θ1
VIEW C
(b)
5
B
X
X = A &/or B
ODD LEAD SIDES
TOPVIEW
5
e/2
X
X = A &/or B
EVEN LEAD SIDES
TOPVIEW

Symbol	Min.	Typ.	Max.
A	1.35	-	1.75
A1	0.10	-	0.25
A2	1.25	-	1.65
b	0.31	-	0.51
b1	0.28	-	0.48
c	0.17	-	0.25
c1	0.17	-	0.23
D	9.90 BSC.		
E	6.00 BSC.		
E1	3.90 BSC.		
e	1.27 BSC.		
L	0.40	-	1.27
L1	1.04 REF.		
L2	0.25 BSC.		
R	0.07	-	-
R1	0.07		-
h	0.25	-	0.50
θ	0°	-	8°
θ1	5°	-	15°
θ2	0°	-	-

Notes:
1. Dimensioning and tolerancing per ANSI Y 14.5M-1994
2. Controlling Dimension: MILLIMETERS.
3. Dimension D does not include mold flash protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15 mm (0.006 in) per end. Dimension E1 does not include interlead flash or protrusion. Interlead flash or protrusion shall not exceed 0.25mm per side. D and E1 dimensions are determined at datum H.
4. The package top may be smaller than the package bottom. Dimensions D and E1 are determined at the outermost extremes of the plastic body exclusive of mold flash, tie bar burrs, gate burrs and interlead flash, but including any mismatch between the top and bottom of the plastic body.
5. Datums A & B to be determined at datum H.
6. N is the number of terminal positions. (N=8)
7. The dimensions apply to the flat section of the lead between 0.10 to 0.25mm from the lead tip.
8. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.10mm total in excess of the “b” dimension at maximum material condition. The dambar cannot be located on the lower radius of the foot.
9. This chamfer feature is optional. If it is not present, then a pin 1 identifier must be located within the index area indicated.
10. Refer to JEDEC MS-012, Variation AC

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