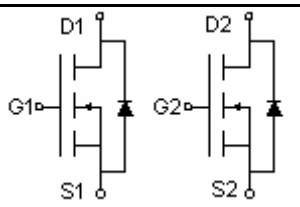
DESCRIPTION

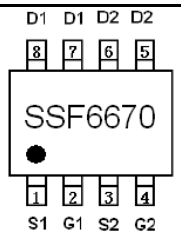
The SSF6670 uses advanced trench technology to provide excellent $R_{DS(ON)}$ and low gate charge .



Schematic diagram

GENERAL FEATURES

- V_{DS} = 60V,I_D =3.5A
  $R_{DS(ON)}$ <120mΩ @ V_{GS}=4.5V
  $R_{DS(ON)}$ <90mΩ @ V_{GS}=10V
- High Power and current handing capability
- Lead free product is acquired
- Surface Mount Package



Marking and pin Assignment

Application

- PWM applications
- Load switch
- Power management

SOP-8 top view

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Device Package	Reel Size	Tape width	Quantity
SSF6670	SSF6670	SOP-8	Ø330mm	12mm	2500 units

ABSOLUTE MAXIMUM RATINGS(TA=25℃unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	60	V
Gate-Source Voltage	V_{GS}	±25	V
Drain Current-Continuous@ Current-Pulsed (Note 1)	I_D(25℃)	3.5	A
	I_D(70℃)	2.8	A
	I_{DM}	20	A
Maximum Power Dissipation	P_D	2.0	W
Operating Junction and Storage Temperature Range	T_J,T_{STG}	-55 To 150	℃

THERMAL CHARACTERISTICS

Thermal Resistance,Junction-to-Ambient (Note 2)	$R_{\theta JA}$	62.5	℃/W

ELECTRICAL CHARACTERISTICS (TA=25℃unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-Source Breakdown Voltage	BV_{DSS}	V_{GS}=0V I_D=250μA	60			V

Zero Gate Voltage Drain Current	I_{DSS}	V_{DS}=60V,V_{GS}=0V			10	μA
Gate-Body Leakage Current	I_{GSS}	V_{GS}=±25V,V_{DS}=0V			±100	nA
ON CHARACTERISTICS (Note 3)						
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS}=V_{GS},I_D=250μA	1		3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS}=4.5V, I_D=2A		80	120	mΩ
		V_{GS}=10V, I_D=3A		65	90	mΩ
Forward Transconductance	g_{FS}	V_{DS}=10V,I_D=3A	3			S
DYNAMIC CHARACTERISTICS (Note4)						
Input Capacitance	C_{lss}	V_{DS}=25V,V_{GS}=0V, F=1.0MHz		500		PF
Output Capacitance	C_{oss}			50		PF
Reverse Transfer Capacitance	C_{rss}			40		PF
SWITCHING CHARACTERISTICS (Note 4)						
Turn-on Delay Time	$t_{d(on)}$	V_{DS}=30V,V_{GS}=10V,R_{GEN}=3Ω I_D=1A		6		nS
Turn-on Rise Time	t_r			5		nS
Turn-Off Delay Time	$t_{d(off)}$			16		nS
Turn-Off Fall Time	t_f			3		nS
Total Gate Charge	Q_g	V_{DS}=48V,I_D=3A,V_{GS}=4.5V		7		nC
Gate-Source Charge	Q_{gs}			2		nC
Gate-Drain Charge	Q_{gd}			3		nC
Body Diode Reverse Recovery Time	T_{rr}	I_F=4A, dI/dt=100A/μs		27		nS
Body Diode Reverse Recovery Charge	Q_{rr}			32		nC
DRAIN-SOURCE DIODE CHARACTERISTICS						
Diode Forward Voltage (Note 3)	V_{SD}	V_{GS}=0V,I_S=1.7A			1.2	V

NOTES:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on 1in^2 FR4 Board, t ≤ 10 sec.
3. Pulse Test: Pulse Width ≤ 300μs, Duty Cycle ≤ 2%.
4. Guaranteed by design, not subject to production testing.

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

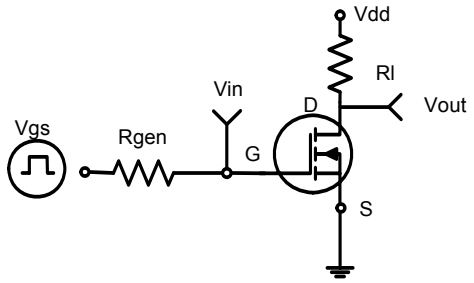


Figure 1:Switching Test Circuit

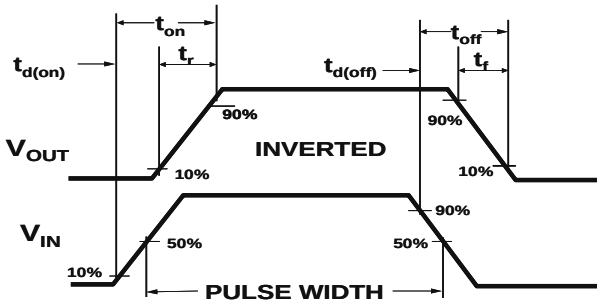


Figure 2:Switching Waveforms

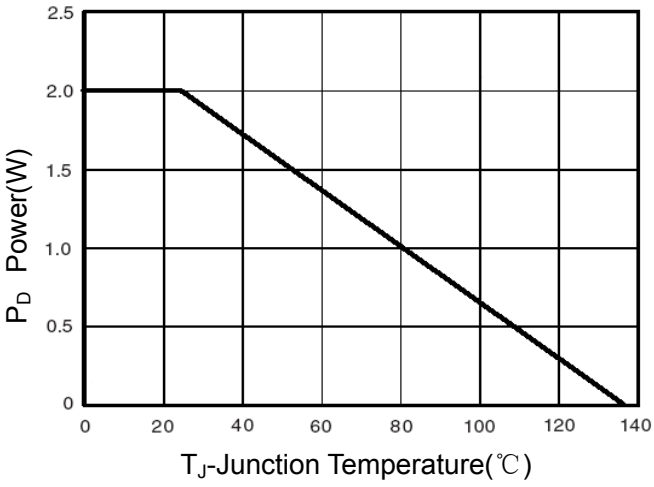


Figure 3 Power Dissipation

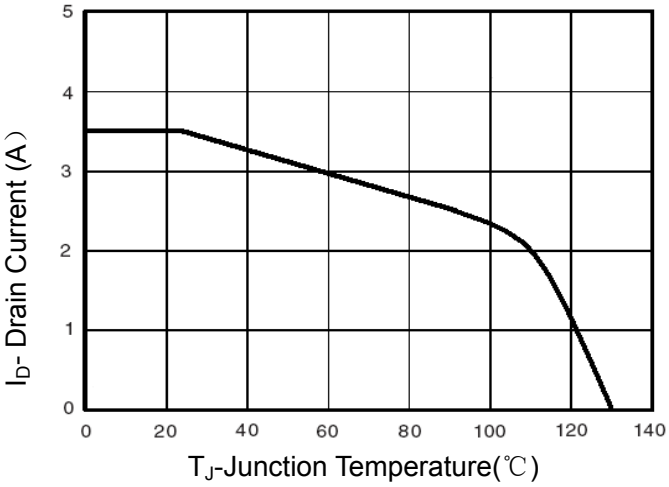


Figure 4 Drain Current

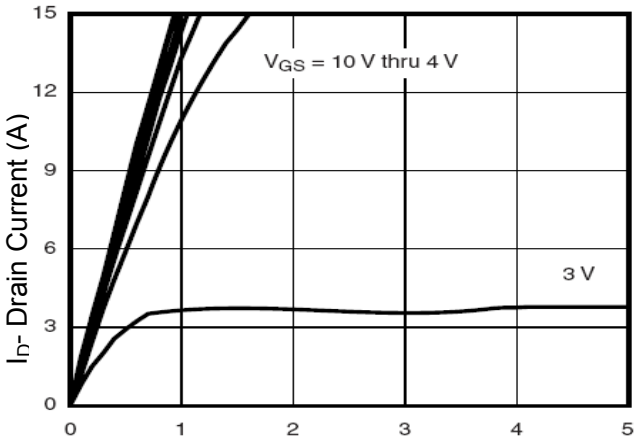


Figure 5 Output CHARACTERISTICS

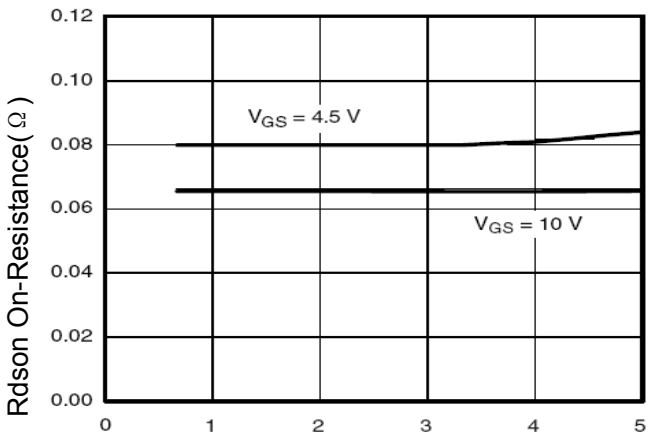


Figure 6 Drain-Source On-Resistance

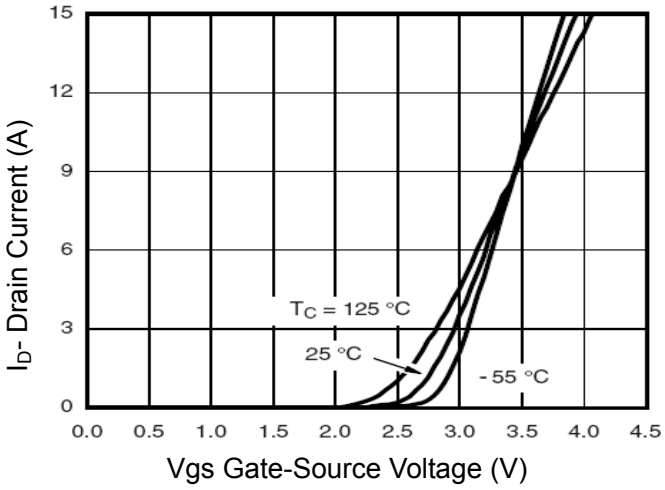


Figure 7 Transfer Characteristics

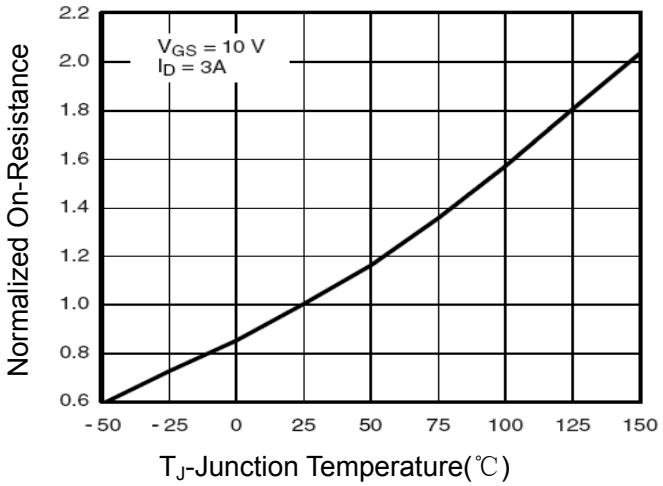


Figure 8 Drain-Source On-Resistance

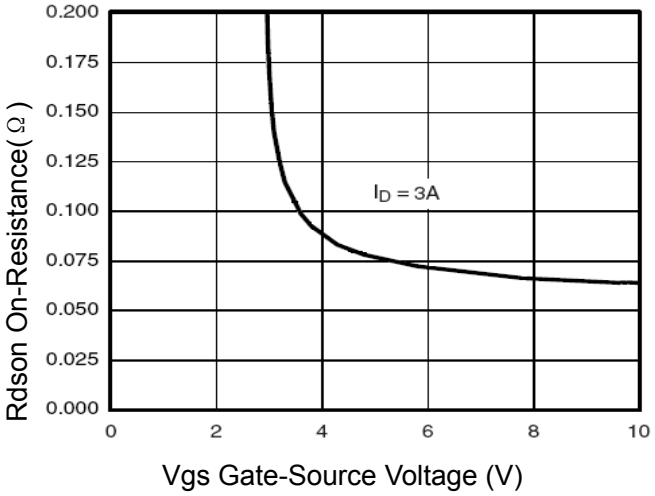


Figure 9 Rdson vs Vgs

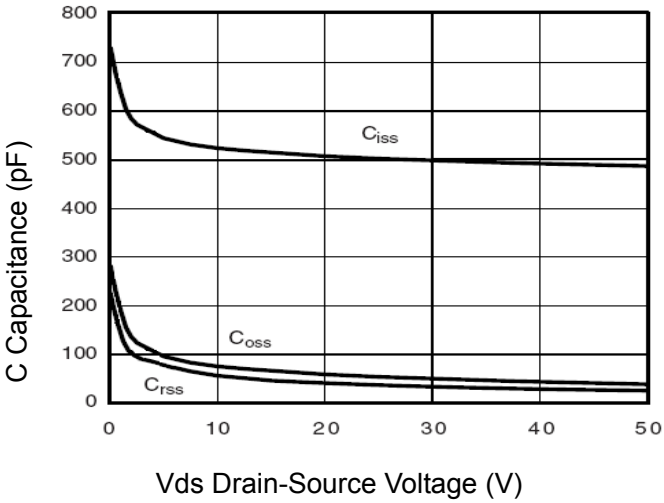


Figure 10 Capacitance vs Vds

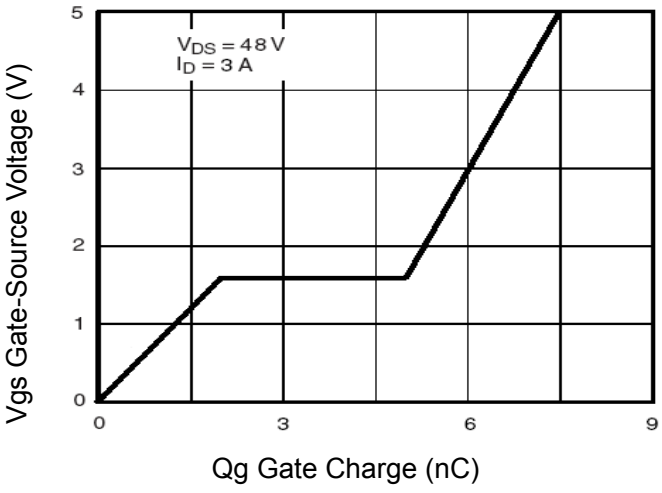


Figure 11 Gate Charge

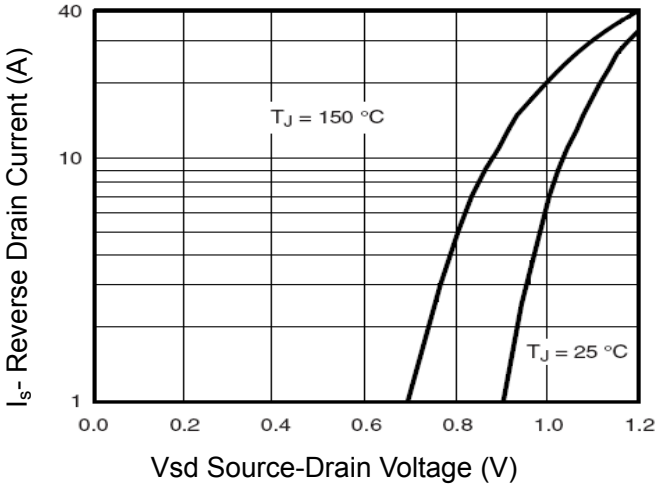


Figure 12 Source- Drain Diode Forward

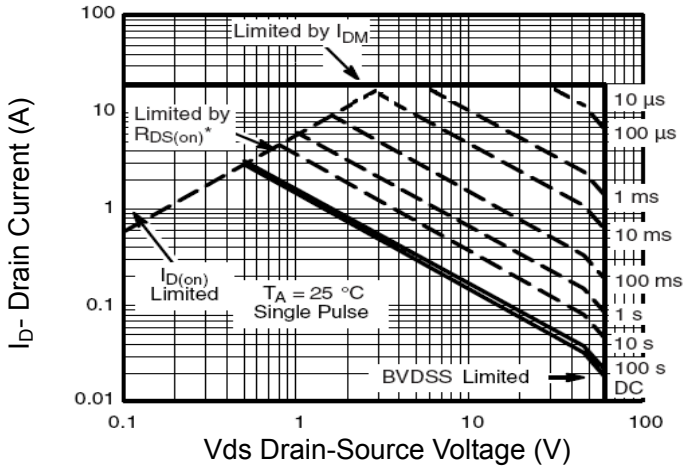


Figure 13 Safe Operation Area

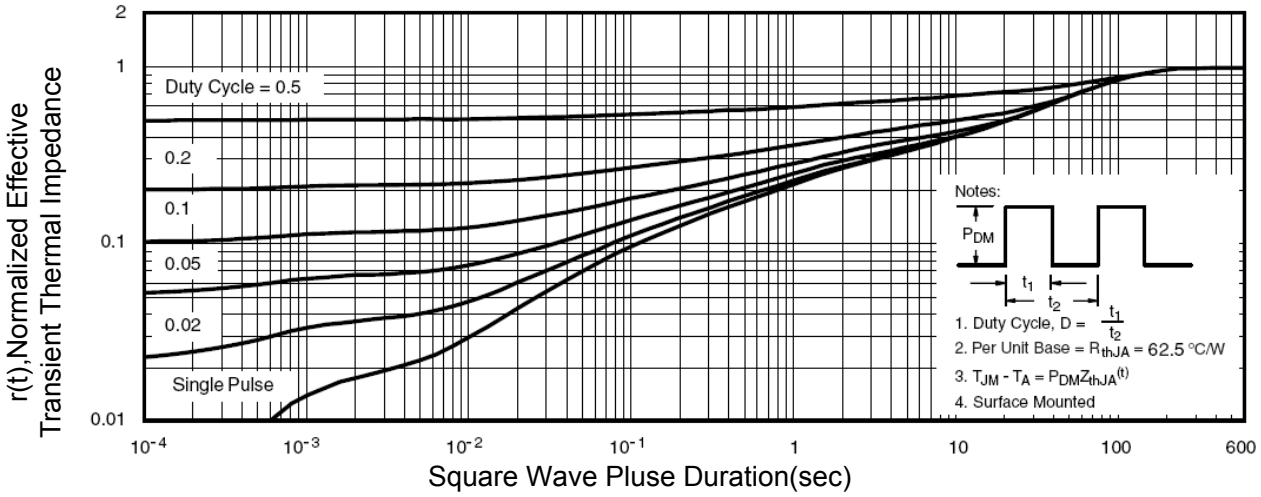
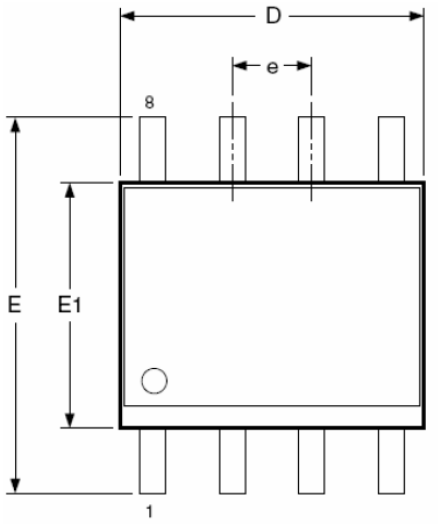
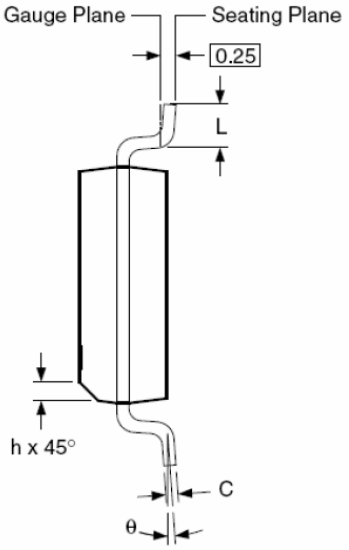
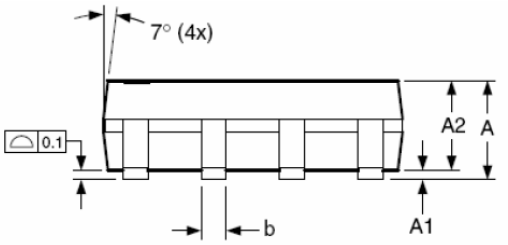


Figure 14 Normalized Maximum Transient Thermal Impedance

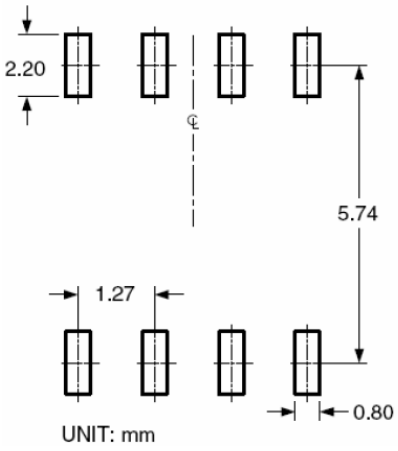
SOP-8 PACKAGE INFORMATION







RECOMMENDED LAND PATTERN



Dimensions in millimeters

Symbols	Min.	Nom.	Max.
A	1.35	1.65	1.75
A1	0.10	—	0.25
A2	1.25	1.50	1.65
b	0.31	—	0.51
c	0.17	—	0.25
D	4.80	4.90	5.00
E1	3.80	3.90	4.00
e	1.27 BSC		
E	5.80	6.00	6.20
h	0.25	—	0.50
L	0.40	—	1.27
θ	0°	—	8°

Dimensions in inches

Symbols	Min.	Nom.	Max.
A	0.053	0.065	0.069
A1	0.004	—	0.010
A2	0.049	0.059	0.065
b	0.012	—	0.020
c	0.007	—	0.010
D	0.189	0.193	0.197
E1	0.150	0.154	0.157
e	0.050 BSC		
E	0.228	0.236	0.244
h	0.010	—	0.020
L	0.016	—	0.050
θ	0°	—	8°

NOTES:

1. Dimensions are inclusive of plating
2. Package body sizes exclude mold flash and gate burrs. Mold flash at the non-lead sides should be less than 6 mils.
3. Dimension L is measured in gauge plane.
4. Controlling dimension is millimeter, converted inch dimensions are not necessarily exact.

ATTENTION:

- Any and all Silikron products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your Silikron representative nearest you before using any Silikron products described or contained herein in such applications.
- Silikron assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all Silikron products described or contained herein.
- Specifications of any and all Silikron products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- Silikron Semiconductor CO.,LTD. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives, that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- In the event that any or all Silikron products(including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of Silikron Semiconductor CO.,LTD.
- Information (including circuit diagrams and circuit parameters) herein is for example only ; it is not guaranteed for volume production. Silikron believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.
- Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the Silikron product that you intend to use.
- This catalog provides information as of Dec, 2008. Specifications and information herein are subject to change without notice.