✓RoHS

RF Power Field Effect Transistor
## N‑Channel Enhancement‑Mode Lateral MOSFET

Designed for broadband commercial and industrial applications with frequencies up to 1000 MHz. The high gain and broadband performance of this device make it ideal for large‑signal, common‑source amplifier applications in 26 volt base station equipment.

- Typical Two‑Tone Performance at 945 MHz, 26 Volts
    Output Power — 30 Watts PEP
    Power Gain — 19 dB
    Efficiency — 41.5%
    IMD — -32.5 dBc
- Capable of Handling 10:1 VSWR, @ 26 Vdc, 945 MHz, 30 Watts CW Output Power

Features

- Integrated ESD Protection
- Designed for Maximum Gain and Insertion Phase Flatness
- Excellent Thermal Stability
- Characterized with Series Equivalent Large‑Signal Impedance Parameters
- Low Gold Plating Thickness on Leads. L Suffix Indicates 40μ″ Nominal.
- RoHS Compliant
- In Tape and Reel. R1 Suffix = 500 Units per 32 mm, 13 inch Reel.

MRF9030LR1

**945 MHz, 30 W, 26 V
LATERAL N‑CHANNEL
BROADBAND
RF POWER MOSFET**

**CASE 360B‑05, STYLE 1
NI‑360**
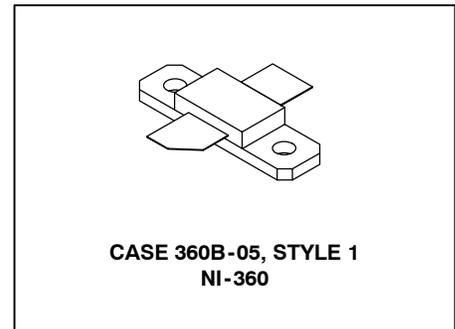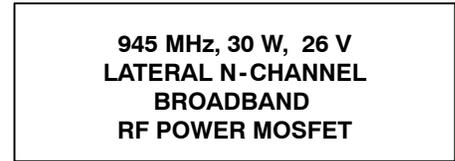
Table 1. Maximum Ratings

Rating	Symbol	Value	Unit
Drain‑Source Voltage	V_{DSS}	- 0.5, +68	Vdc
Gate‑Source Voltage	V_{GS}	- 0.5, +15	Vdc
Total Device Dissipation @ T_C = 25°C Derate above 25°C	P_D	92 0.53	W W/°C
Storage Temperature Range	T_{stg}	- 65 to +150	°C
Case Operating Temperature	T_C	150	°C
Operating Junction Temperature	T_J	200	°C

Table 2. Thermal Characteristics

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.9	°C/W

Table 3. ESD Protection Characteristics

Test Conditions	Class
Human Body Model	1 (Minimum)
Machine Model	M1 (Minimum)

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Table 4. Electrical Characteristics (T_C = 25°C unless otherwise noted)

| Characteristic	Symbol	Min	Typ	Max	Unit
Off Characteristics					
Zero Gate Voltage Drain Leakage Current (V_{DS} = 68 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	10	μAdc
Zero Gate Voltage Drain Leakage Current (V_{DS} = 26 Vdc, V_{GS} = 0 Vdc)	I_{DSS}	—	—	1	μAdc
Gate-Source Leakage Current (V_{GS} = 5 Vdc, V_{DS} = 0 Vdc)	I_{GSS}	—	—	1	μAdc
On Characteristics					
Gate Threshold Voltage (V_{DS} = 10 Vdc, I_D = 100 μAdc)	$V_{GS(th)}$	2	2.9	4	Vdc
Gate Quiescent Voltage (V_{DS} = 26 Vdc, I_D = 250 mAdc)	$V_{GS(Q)}$	—	3.8	—	Vdc
Drain-Source On-Voltage (V_{GS} = 10 Vdc, I_D = 0.7 Adc)	$V_{DS(on)}$	—	0.19	0.4	Vdc
Forward Transconductance (V_{DS} = 10 Vdc, I_D = 2 Adc)	g_{fs}	—	3	—	S
Dynamic Characteristics					
Input Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{iss}	—	49.5	—	pF
Output Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{oss}	—	26.5	—	pF
Reverse Transfer Capacitance (V_{DS} = 26 Vdc ± 30 mV(rms)ac @ 1 MHz, V_{GS} = 0 Vdc)	C_{rss}	—	1	—	pF

(continued)

Table 4. Electrical Characteristics (T$_C$ = 25°C unless otherwise noted) **(continued)**

Characteristic	Symbol	Min	Typ	Max	Unit
Functional Tests (In Freescale Test Fixture, 50 ohm system)					
Two-Tone Common-Source Amplifier Power Gain (V$_{DD}$ = 26 Vdc, P$_{out}$ = 30 W PEP, I$_{DQ}$ = 250 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	G$_{ps}$	18	19	—	dB
Two-Tone Drain Efficiency (V$_{DD}$ = 26 Vdc, P$_{out}$ = 30 W PEP, I$_{DQ}$ = 250 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	η	37	41.5	—	%
3rd Order Intermodulation Distortion (V$_{DD}$ = 26 Vdc, P$_{out}$ = 30 W PEP, I$_{DQ}$ = 250 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	IMD	—	-32.5	-28	dBc
Input Return Loss (V$_{DD}$ = 26 Vdc, P$_{out}$ = 30 W PEP, I$_{DQ}$ = 250 mA, f1 = 945.0 MHz, f2 = 945.1 MHz)	IRL	—	-15.5	-9	dB
Two-Tone Common-Source Amplifier Power Gain (V$_{DD}$ = 26 Vdc, P$_{out}$ = 30 W PEP, I$_{DQ}$ = 250 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	G$_{ps}$	—	19	—	dB
Two-Tone Drain Efficiency (V$_{DD}$ = 26 Vdc, P$_{out}$ = 30 W PEP, I$_{DQ}$ = 250 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	η	—	41.5	—	%
3rd Order Intermodulation Distortion (V$_{DD}$ = 26 Vdc, P$_{out}$ = 30 W PEP, I$_{DQ}$ = 250 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	IMD	—	-33	—	dBc
Input Return Loss (V$_{DD}$ = 26 Vdc, P$_{out}$ = 30 W PEP, I$_{DQ}$ = 250 mA, f1 = 930.0 MHz, f2 = 930.1 MHz and f1 = 960.0 MHz, f2 = 960.1 MHz)	IRL	—	-14	—	dB
Power Output, 1 dB Compression Point (V$_{DD}$ = 26 Vdc, P$_{out}$ = 30 W CW, I$_{DQ}$ = 250 mA, f1 = 945.0 MHz)	P$_{1dB}$	—	30	—	W
Common-Source Amplifier Power Gain (V$_{DD}$ = 26 Vdc, P$_{out}$ = 30 W CW, I$_{DQ}$ = 250 mA, f1 = 945.0 MHz)	G$_{ps}$	—	19	—	dB
Drain Efficiency (V$_{DD}$ = 26 Vdc, P$_{out}$ = 30 W CW, I$_{DQ}$ = 250 mA, f1 = 945.0 MHz)	η	—	60	—	%

MRF9030LR1

V_GG B1 C7 C8 V_DD B2 C14 C15 C16 C17

L1 C5 C9 L2

RF INPUT Z1 Z2 Z3 Z4 Z5 Z6 Z7 DUT Z8 Z9 Z10 Z11 Z12 Z13 RF OUTPUT

C1 C2 C3 C4 C6 C10 C11 C12 C13

B1	Short Ferrite Bead
B2	Long Ferrite Bead
C1, C8, C13, C14	47 pF Chip Capacitors
C2, C4	0.8 pF to 8.0 pF Trim Capacitors
C3	3.9 pF Chip Capacitor
C5, C6	7.5 pF Chip Capacitors
C7, C15, C16	10 µF, 35 V Tantalum Capacitors
C9, C10	10 pF Chip Capacitors
C11	9.1 pF Chip Capacitor
C12	0.6 pF to 4.5 pF Trim Capacitor
C17	220 µF, 50 V Electrolytic Capacitor
L1, L2	12.5 nH Surface Mount Inductors
Z1	0.260″ x 0.060″ Microstrip
Z2	0.240″ x 0.060″ Microstrip
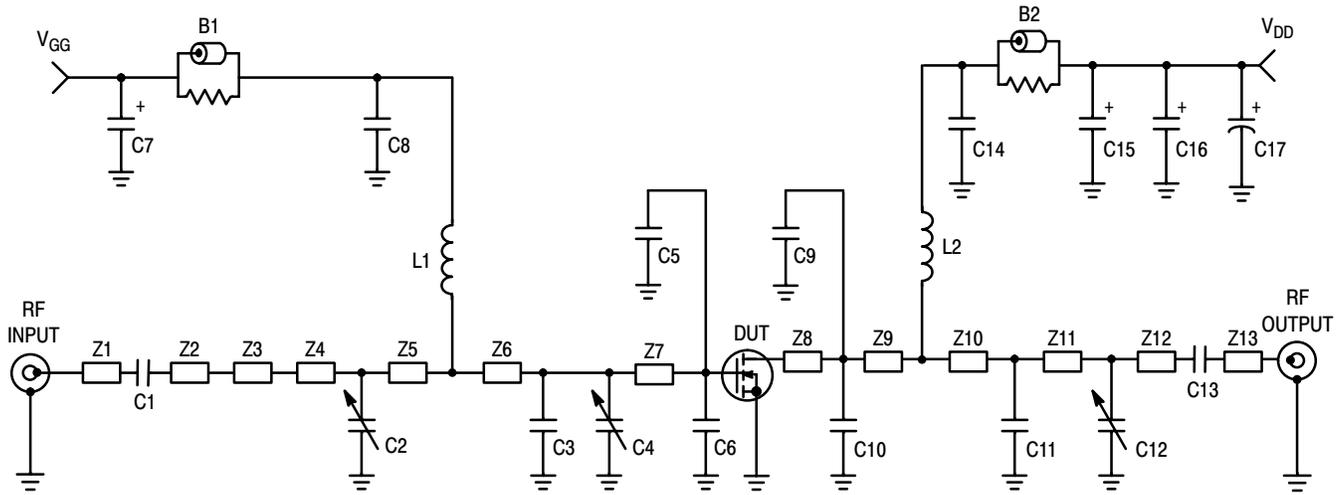
Z3	0.500″ x 0.100″ Microstrip
Z4	0.215″ x 0.270″ Microstrip
Z5	0.315″ x 0.270″ Microstrip
Z6	0.160″ x 0.270″ x 0.520″, Taper
Z7	0.285″ x 0.520″ Microstrip
Z8	0.450″ x 0.270″ Microstrip
Z9	0.140″ x 0.270″ Microstrip
Z10	0.250″ x 0.060″ Microstrip
Z11	0.720″ x 0.060″ Microstrip
Z12	0.490″ x 0.060″ Microstrip
Z13	0.290″ x 0.060″ Microstrip
PCB	Taconic RF-35-0300, 30 mil, $\varepsilon_r = 3.55$

Figure 1. 945 MHz Broadband Test Circuit Schematic

C7 C17 V_GG V_DD C8 C9 C14 C15 C16 L1 L2 C5 RF INPUT C1 C2 C3 C4 C6 C10 C11 C12 C13 RF OUTPUT CUT OUT AREA

MOTOROLA

MRF9030
900 MHz
Rev-02
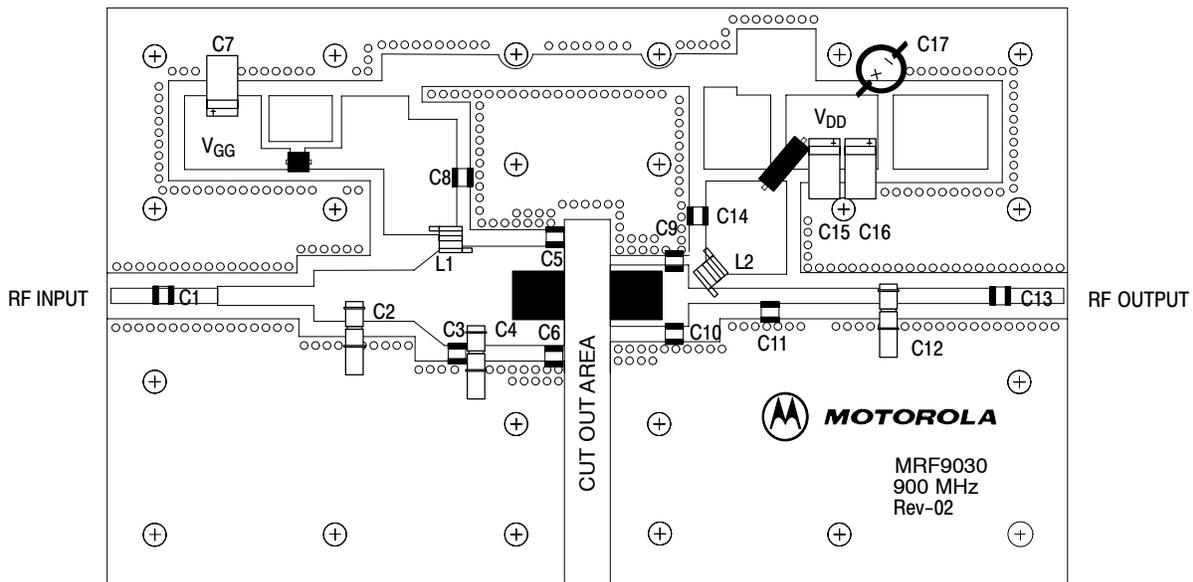
Freescale has begun the transition of marking Printed Circuit Boards (PCBs) with the Freescale Semiconductor signature/logo. PCBs may have either Motorola or Freescale markings during the transition period. These changes will have no impact on form, fit or function of the current product.

Figure 2. 945 MHz Broadband Test Circuit Component Layout

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TYPICAL CHARACTERISTICS
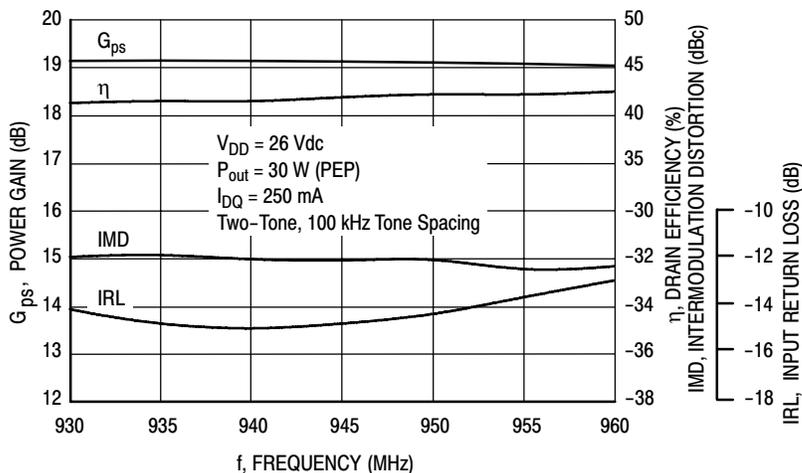
Figure 3. Class AB Broadband Circuit Performance

V_{DD} = 26 Vdc
P_{out} = 30 W (PEP)
I_{DQ} = 250 mA
Two–Tone, 100 kHz Tone Spacing
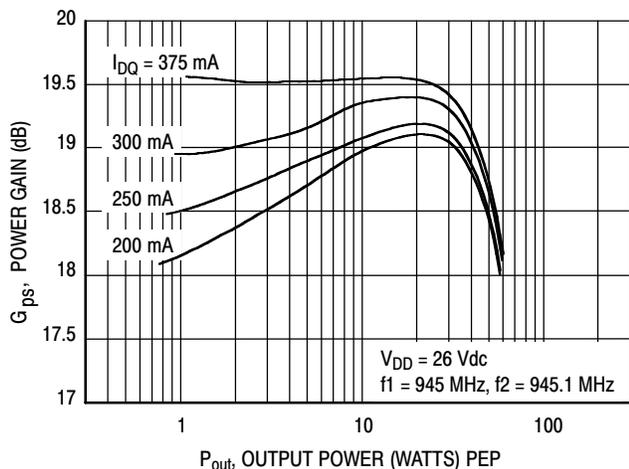
**Figure 4. Power Gain versus Output Power**
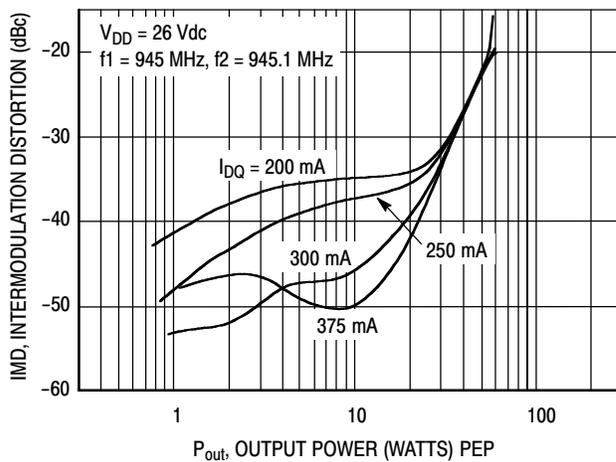

Figure 5. Intermodulation Distortion versus Output Power
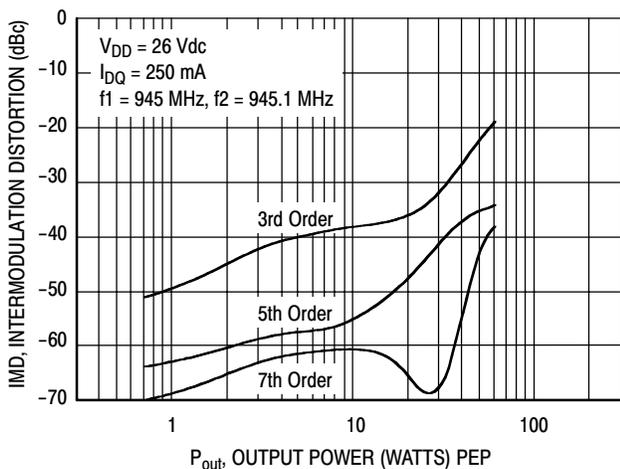
**Figure 6. Intermodulation Distortion Products versus Output Power**
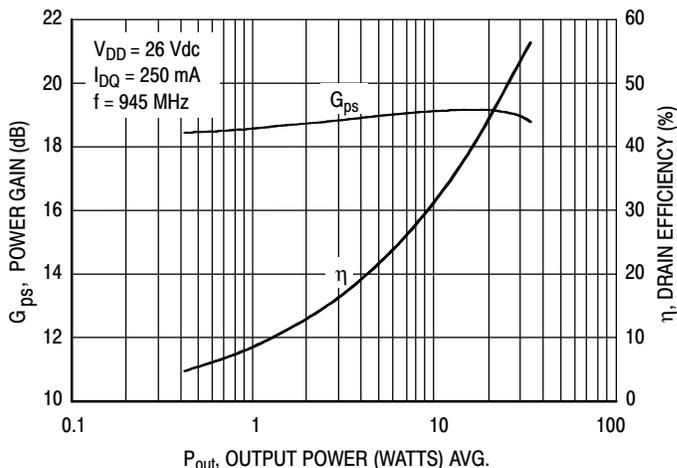


Figure 7. Power Gain and Efficiency versus Output Power

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TYPICAL CHARACTERISTICS
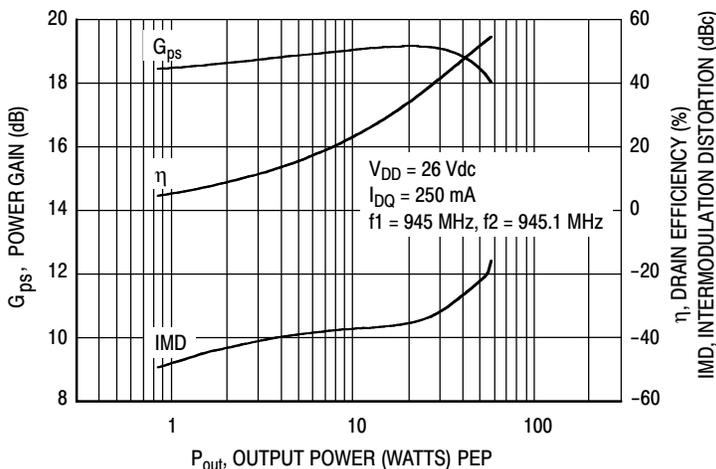
Figure 8. Power Gain, Efficiency and IMD versus Output Power

V_{DD} = 26 Vdc
I_{DQ} = 250 mA
f1 = 945 MHz, f2 = 945.1 MHz
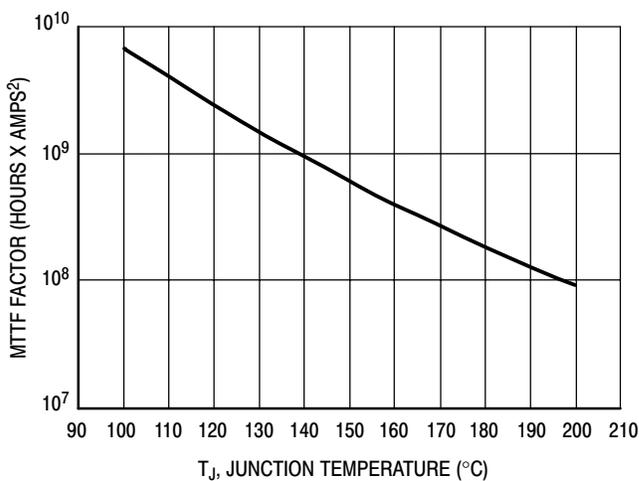
This above graph displays calculated MTTF in hours x ampere^2 drain current. Life tests at elevated temperatures have correlated to better than ±10% of the theoretical prediction for metal failure. Divide MTTF factor by $I_D{}^2$ for MTTF in a particular application.

Figure 9. MTTF Factor versus Junction Temperature

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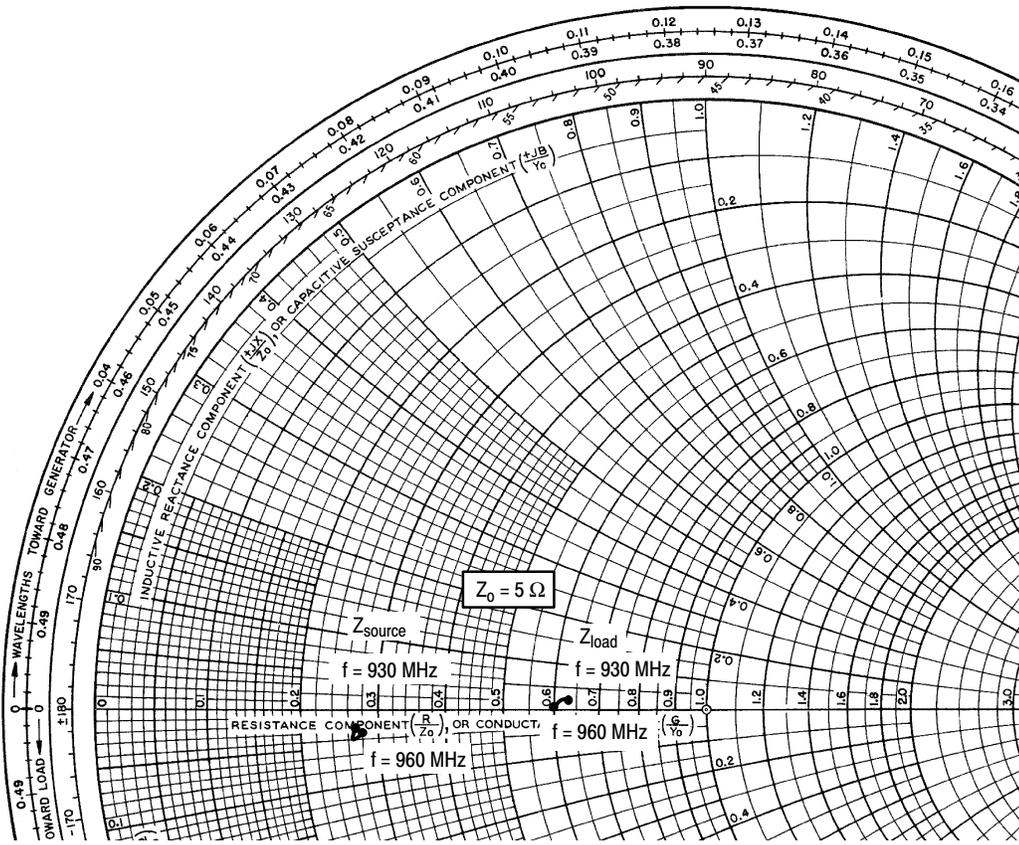
V_{DD} = 26 V, I_{DQ} = 250 mA, P_{out} = 30 W PEP

f MHz	Z_{source} Ω	Z_{load} Ω
930	1.34 - j0.1	3.175 + j0.09
945	1.36 - j0.2	3.1 + j0.08
960	1.4 - j0.14	3.0 + j0.05

Z_{source} = Test circuit impedance as measured from gate to ground.

Z_{load} = Test circuit impedance as measured from drain to ground.
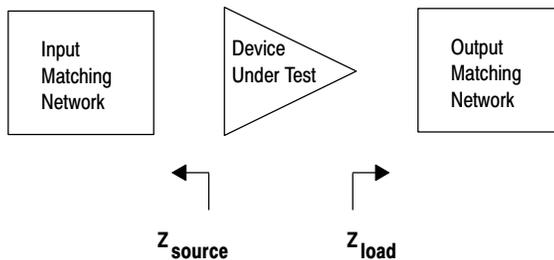
Figure 10. Series Equivalent Source and Load Impedance

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RF Device Data
Freescale Semiconductor

PACKAGE DIMENSIONS
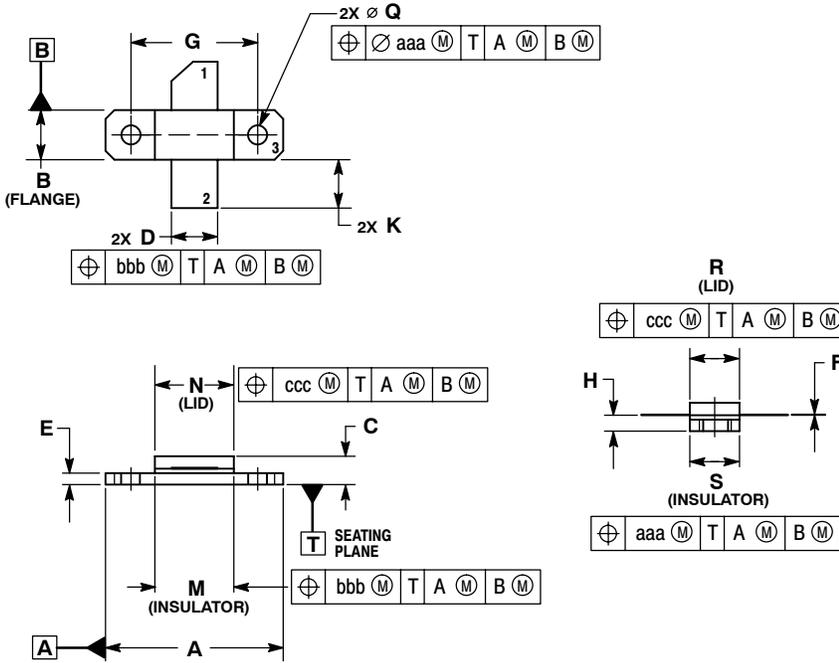
NOTES:
1. INTERPRET DIMENSIONS AND TOLERANCES PER ASME Y14.5M−1994.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION H IS MEASURED 0.030 (0.762) AWAY FROM PACKAGE BODY.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.795	0.805	20.19	20.45
B	0.225	0.235	5.72	5.97
C	0.125	0.175	3.18	4.45
D	0.210	0.220	5.33	5.59
E	0.055	0.065	1.40	1.65
F	0.004	0.006	0.10	0.15
G	0.562 BSC		14.28 BSC	
H	0.077	0.087	1.96	2.21
K	0.220	0.250	5.59	6.35
M	0.355	0.365	9.02	9.27
N	0.357	0.363	9.07	9.22
Q	0.125	0.135	3.18	3.43
R	0.227	0.233	5.77	5.92
S	0.225	0.235	5.72	5.97
aaa	0.005 REF		0.13 REF	
bbb	0.010 REF		0.25 REF	
ccc	0.015 REF		0.38 REF	

STYLE 1:
PIN 1. DRAIN
    2. GATE
    3. SOURCE

CASE 360B-05
ISSUE G
NI-360
MRF9030LR1

PRODUCT DOCUMENTATION

Refer to the following documents to aid your design process.

Engineering Bulletins

- EB212: Using Data Sheet Impedances for RF LDMOS Devices

REVISION HISTORY

The following table summarizes revisions to this document.

Revision	Date	Description
8	Sept. 2008	• Data sheet revised to reflect part status change, p. 1, including use of applicable overlay. • Added Product Documentation and Revision History, p. 9

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