Speaker /Headphone Amplifier Series

# 1W+1W Stereo Speaker / Headphone Amplifier

## BH7884EFV

Pb Free ROHM Electronic Components

RoHS Directive Compliance

**●Description**

The BH7884EFV is a low voltage, low noise, high output speaker and headphone amplifier drive, in which a BiCMOS process is used. This IC supports: headphone amplifier gain adjustment, active/suspend switching, speaker amplifier stereo/monaural switching, and amplifier mute switching. All functions are controllable from a microcontroller. Built-in digital noise reduction circuits eliminate digital noise and BEEP sounds.

**●Features**

1) Built-in 1W+1W stereo speaker amplifier (Vcc=5V, RL=8Ω, THD=10%)
2) Built-in stereo headphone amplifier
3) Built-in bass boost function for speaker amplifier
4) Built-in low noise VCA (electronic volume) for headphone
5) Built-in mute circuit
6) Built-in standby circuit
7) Low current consumption specifications (9 mA TYP. in ACTIVE mode, 0.2 μA TYP. in SUSPEND mode)

**●Applications**

Notebook computers, LCD TVs, etc.

**●Absolute maximum ratings**(Ta=25°C)

| Parameter | Limits | Unit |
|---|---|---|
| Supply voltage | +6.0 | V |
| Power dissipation | 1100 *1 | mW |
| Storage temperature | -55 ～ +125 | °C |
| Operating temperature | -10 ～ +70 | °C |

*1 Reduced by 11 mW/°C at 25°C or higher, when mounting on a 70mmX70mmX1.6mm PCB board).

**●Operating range** (Ta=25°C)

| Parameter | Limits | Unit |
|---|---|---|
| Supply voltage | +3.0~+5.5 | V |

* This IC is not designed to be radiation-resistant.

●**Electrical characteristics** (Unless otherwise noted, Vcc=3.3V, Ta=25°C, f=1kHz)

| Parameter | Symbol | Specifications | | | Unit | Condition |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| ■1 CHIP | | | | | | |
| Circuit current ACTV | $I_A$ | - | 9.0 | 18.0 | mA | No signal ACTIVE |
| Circuit current SPND | Is | - | 0.2 | 10.0 | μA | No signal SUSPEND |
| ■SP AMP | | | | | | |
| Voltage gain1 | $G_{SP}1$ | 9.0 | 12.0 | 15.0 | dB | SE, Vin=-18dBV,$R_L$=8Ω |
| Voltage gain2 | $G_{SP}2$ | 15.2 | 18.2 | 21.2 | dB | BTL, Vin=-18dBV |
| Distortion | $D_{SP}$ | - | 0.1 | 1.0 | % | BTL, Vin=-18dBV |
| Maximum output level | $V_{OSP}$ | 2.2 | 5.2 | - | dBV | BTL, $D_{SP}$=1% |
| Output noise level | $V_{NSP}$ | - | -97 | -80 | dBV | SE, DIN-Audio |
| Cross talk | $CT_{SP}$ | - | -90 | -80 | dBV | SE, Vin=-18dBV, DIN-Audio |
| Output level on mute | $MT_{SP}$ | - | -102 | -80 | dBV | BTL, Vin=-18dBV |
| ■HP AMP | | | | | | |
| Voltage gain 3 | $G_{HP}$ | 2.6 | 5.6 | 8.6 | dB | VOL:MAX, $R_L$=10kΩ,Vin=-12dBV |
| Voltage gain 4 | $G_{HP}$ | -10 | -7 | -4 | dB | VOL:MAX, $R_L$=32Ω,Vin=-12dBV |
| Distortion | $D_{HP}$ | - | 0.025 | 0.1 | % | VOL:MAX, $R_L$=32Ω,Vin=-8dBV |
| Variable width of volume | $\Delta G_{HP}$ | 70 | 100 | - | dB | VOL:MIN～MAX, $R_L$=32Ω |
| Maximum output level | $Vo_{HP}$ | -2.0 | 1.0 | - | dBV | VOL:MAX, $D_{HP}$=1%, $R_L$=10kΩ |
| Output noise level | $V_{NHP}$ | - | -98 | -80 | dBV | VOL:MAX, $R_L$=32Ω, DIN-Audio |
| Cross talk | $CT_{HP}$ | - | -98 | -80 | dBV | VOL:MAX, $R_L$=32Ω,Vin=-12dBV DIN-Audio |
| Output level on mute | $MT_{HP}$ | - | -110 | -80 | dBV | VOL:MAX, $R_L$=32Ω,Vin=-12dBV DIN-Audio |
| ■BEEP AMP | | | | | | |
| Output voltage level | $V_{BP}$ | 0.8 | 1.25 | - | Vpp | Vin=1.3dBV, f=1kHz, 20MHzLPF |
| ■BIAS | | | | | | |
| Output voltage level | $V_{BIAS}$ | 1.4 | 1.7 | 2.0 | V | No Signal |
| ■CTRL | | | | | | |
| ACTIVE mode | $V_{11H}$ | VCC -0.3 | - | VCC | V | Active mode. Hold Voltage of 11pin. |
| SUSPEND mode | $V_{11L}$ | GND | - | 0.3 | V | Suspend mode. Hold Voltage of 11pin. |
| SP/ON mode | $V_{2H}$ | VCC -0.3 | - | VCC | V | SP/ON mode. Hold Voltage of 2pin. |
| SP/OFF mode | $V_{2L}$ | GND | - | 0.3 | V | SP/OFF mode. Hold Voltage of 2pin. |
| BASS-BOOST/ON mode | $V_{4H}$ | VCC -0.7 | - | VCC | V | SP/BassBoost mode. Hold Voltage of 4pin. |
| BASS-BOOST/OFF mode | $V_{4L}$ | GND | - | 0.7 | V | SP/NonBoost mode. Hold Voltage of 4pin. |
| STEREO mode | $V_{3H}$ | VCC -0.7 | - | VCC | V | SP/STEREO mode. Hold Voltage of 3pin. |
| MONO mode | $V_{3L}$ | GND | - | 0.7 | V | SP/MONO mode. Hold Voltage of 3pin. |
| ACTIVE mode | $V_{10H}$ | VCC -0.7 | - | VCC | V | HP/Active mode. Hold Voltage of 10pin. |
| MUTE mode | $V_{10L}$ | GND | - | 0.7 | V | HP/MUTE mode. Hold Voltage of 10pin. |
| ■PSRR | | | | | | |
| Ripple rejection ratio | $G_{PR}$ | - | -64 | - | dBV | f=100Hz, 0.3Vpp, SIN Input SPOUT monitor, DIN-Audio |

●**Block diagram**

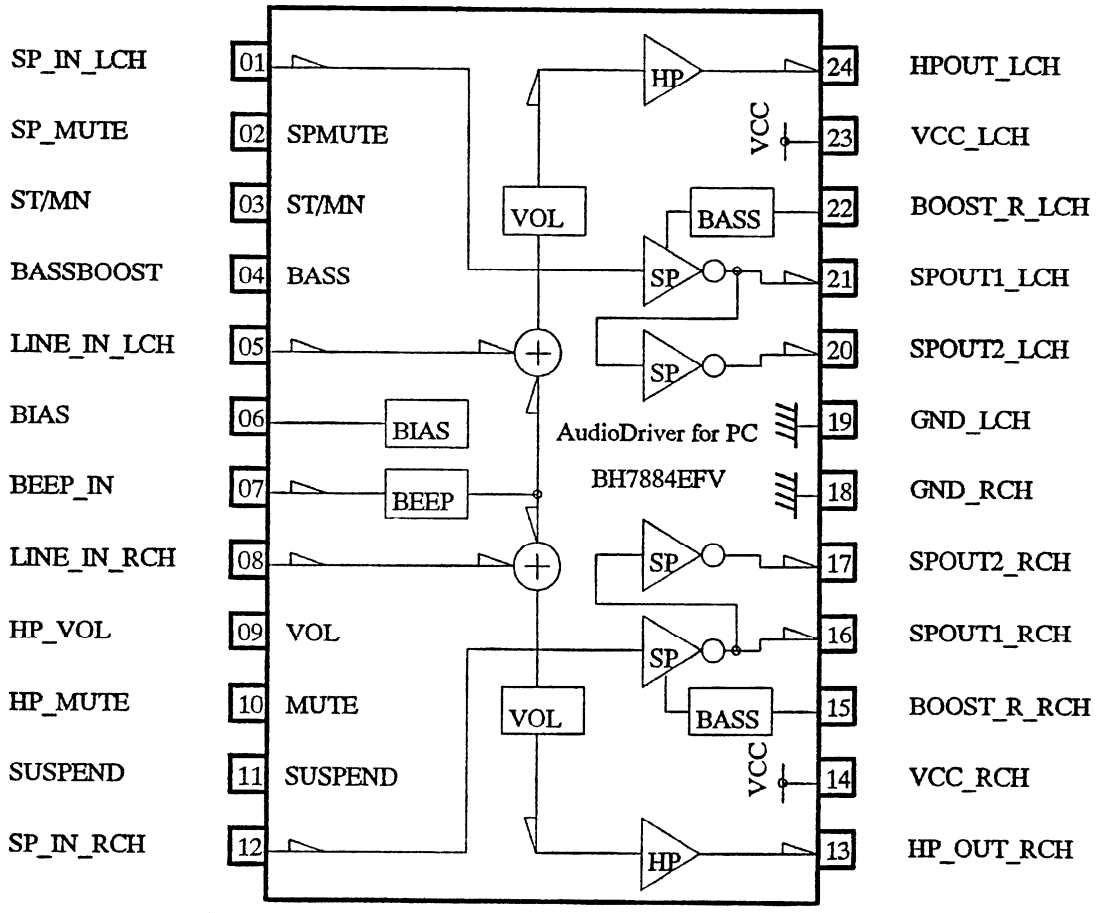
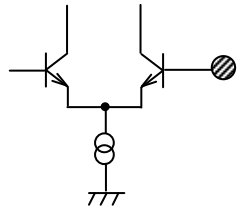
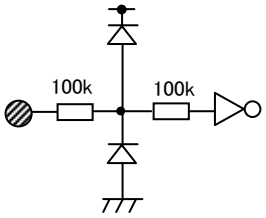
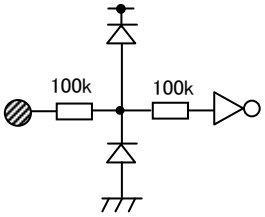
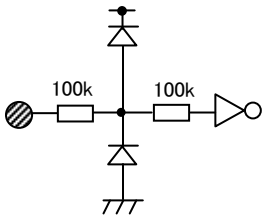
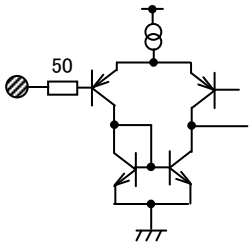
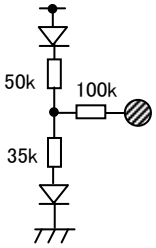
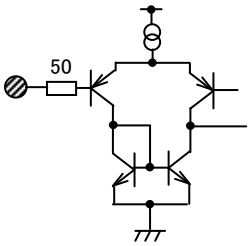
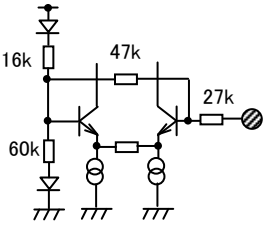
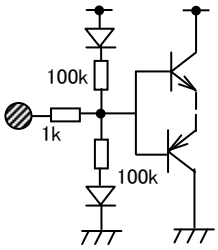
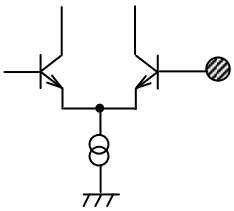
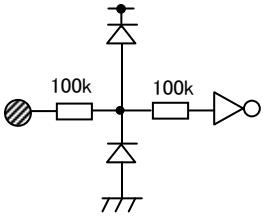
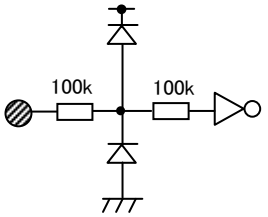
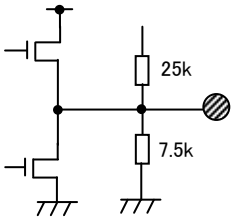
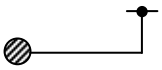
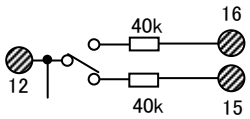
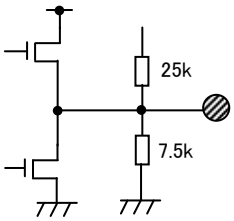



Fig.1

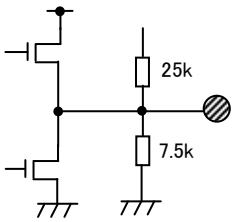
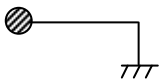
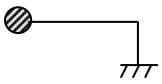
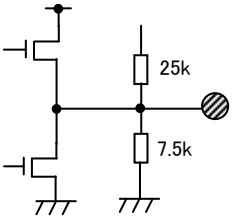
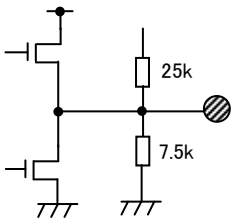
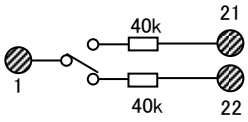
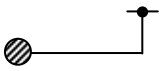
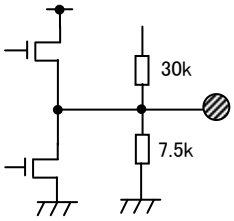
●**Control pin settings**

| | | |
|---|---|---|
| SP MUTE PIN:2PIN | | |
| H | SP ACTIVE | SPAMP is in active state |
| L | SP MUTE | SPAMP is in suspend state |
| STEREO/MONO PIN:3PIN | | |
| H | STEREO | For SPAMP, LCH and RCH both are in active state |
| L | MONO | For SPAMP, LCH is in active state and RCH is in suspend state |
| BASSBOOST PIN:4PIN | | |
| H | BASS BOOST | For SPAMP, bass is boosted |
| L | NON -BOOST | For SPAMP, bass is not boosted |
| MUTE PIN:10PIN<br>(The SPAMP mute function is realized by connecting HP_OUT to SP_IN) | | |
| H | ACTIVE | HPAMP is in active state |
| L | MUTE | HPAMP is in mute state |
| SUSPEND PIN:11PIN | | |
| H | ACTIVE | The IC is in active state |
| L | SUSPEND | The IC is in suspend state |

●**Equivalent circuit** (1 of 2)

| PIN1 | SP_IN_LCH | PIN2 | SP__MUTE | PIN3 | ST/MN | PIN4 | BASS BOOST |
|---|---|---|---|---|---|---|---|
|  | |  | |  | |  | |
| PIN5 | LINE_IN_LCH | PIN6 | BIAS | PIN7 | BEEP_IN | PIN8 | LIHE_IN_RCH |
|  | |  | |  | |  | |
| PIN9 | HP_VOL | PIN10 | HP_MUTE | PIN11 | SUSPEND | PIN12 | SP_IN_RCH |
|  | |  | |  | |  | |
| PIN13 | HP_OUT_RCH | PIN14 | VCC_RCH | PIN15 | BOOST_R_RCH | PIN16 | SPOUT1_RCH |
|  | |  | |  | |  | |

●**Equivalent circuit** (2 of 2)

| PIN17 | SPOUT2_RCH | PIN18 | GND_RCH | PIN19 | GND_LCH | PIN20 | SPOUT2_LCH |
|---|---|---|---|---|---|---|---|
|  | |  | |  | |  | |
| PIN21 | SPOUT1_LCH | PIN22 | BOOST_R_LCH | PIN23 | VCC_LCH | PIN24 | HP_OUT_LCH |
|  | |  | |  | |  | |

●Application circuit

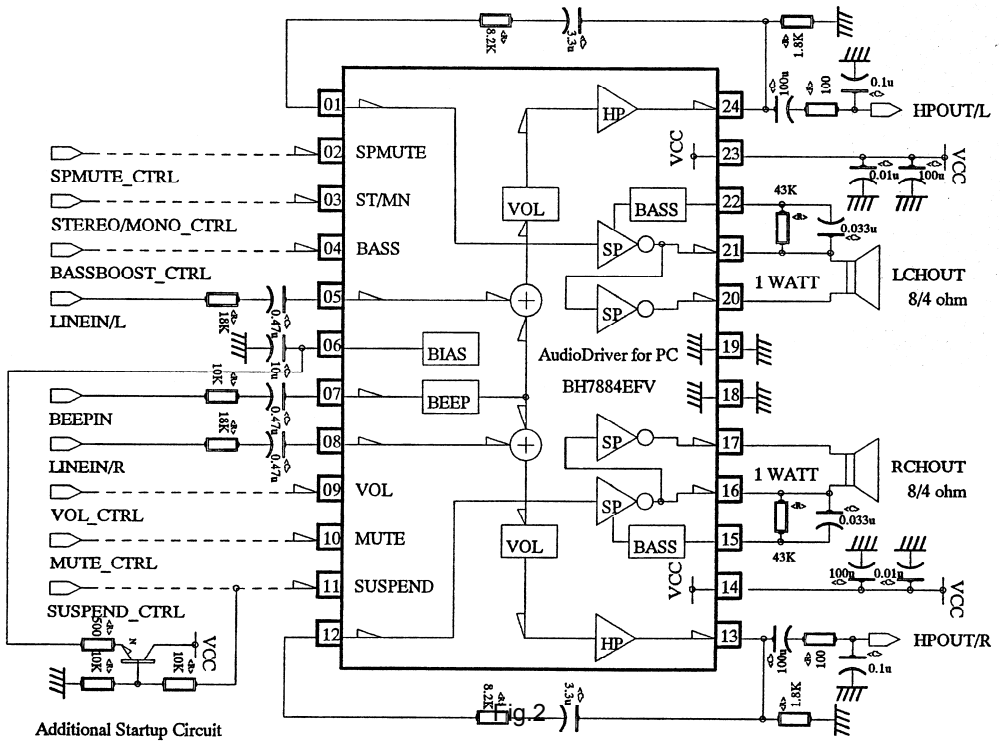



Fig.2

**●Description of operations**

1) LINEIN (5,8PIN)～HPOUT (13,24PIN) voltage gain

The voltage gain at EVRMAX is generally calculated by the following equation:

$$G_{HP} = 20 \times \log \frac{40k}{R_5 (\text{or } R_8)} \text{ (dB)}$$

The above gain attenuates according to the DC voltage of the VOL pin (9PIN).

By connecting multiple resistances (R), mixing input can be handled.

2) BEEPIN(7PIN)～HPOUT(13,24PIN)

When a pulse waveform is input at the BEEPIN pin, a pulse wave is output at HPOUT (24,13PIN).

The output level, determined by the resistance of 7PIN, has default values as follows:

| HP OUT level | Vcc=5V | Vcc=4V | Vcc=3.3V |
|---|---|---|---|
| 1Vpp< | <56k | <91k | <120k |
| 0.5Vpp | 68k | 110k | 160k |
| 0.25Vpp | 75k | 130k | 200k |

Unit: Ω

To obtain the default setting output (approx. 1.2 Vpp output), make R7=10 kΩ.

The variation in output levels is small.

Signals below a certain level are determined to be noise, by IC internals, and are not output at HPOUT.

3) SP IN (1,12PIN)～SP OUT (21,20,16,17PIN) voltage gain

The voltage gain in BASSBOOST is generally calculated by the following equation:

$$G_{SPB} = 20 \times \log \frac{40k + R_{21-22} (\text{or } R_{16-15})}{R_1 (\text{or } R_{12})} \text{(dB)}$$

The cut-off frequency in BASSBOOST is generally calculated by the following equation:

$$f_{CB} = \frac{1}{2\pi C_{21-22} (\text{or } C_{16-15}) \times R_{21-22} (\text{or } R_{16-15})} (H_Z)$$

The voltage gain in NONBOOST is generally calculated by the following equation:

$$G_{SP} = 20 \times \log \frac{40k}{R_1 (\text{ or } R_{12})} \text{(dB)}$$

4) EVR control characteristic

HP AMP gain is controlled by the ratio of voltage to resistance between VCC and GND.

Note: A resistance ($R_N$), shown above, is the resistance that is connected to pin N.
A capacitance ($C_N$), shown above, is the capacitance that is connected to pin N.
The numeric values above are design reference values, whose values are not guaranteed.

**●Operation Notes**

1. Numbers and data in entries are representative design values and are not guaranteed values of the items.
2. Although ROHM is confident that the example application circuit reflects the best possible recommendations, be sure to verify circuit characteristics for your particular application. Modification of constants for other externally connected circuits may cause variations in both static and transient characteristics for external components as well as this Rohm IC. Allow for sufficient margins when determining circuit constants.
3. Absolute maximum ratings
   Use of the IC in excess of absolute maximum ratings, such as the applied voltage or operating temperature range (Topr), may result in IC damage. Assumptions should not be made regarding the state of the IC (short mode or open mode) when such damage is suffered. A physical safety measure, such as a fuse, should be implemented when using the IC at times where the absolute maximum ratings may be exceeded.
4. GND potential
   Ensure a minimum GND pin potential in all operating conditions. Make sure that no pins are at a voltage below the GND at any time, regardless of whether it is a transient signal or not.
5. Thermal design
   Perform thermal design, in which there are adequate margins, by taking into account the permissible dissipation (Pd) in actual states of use.
6. Short circuit between terminals and erroneous mounting
   Pay attention to the assembly direction of the ICs. Wrong mounting direction or shorts between terminals, GND, or other components on the circuits, can damage the IC.
7. Operation in strong electromagnetic field
   Using the ICs in a strong electromagnetic field can cause operation malfunction.
8. Pop noise when switching power ON/OFF
   To prevent pop noise when switching VCC ON/OFF or switching SUSPEND ON/OFF, use SUSPEND (11PIN=L), HP MUTE (10PIN=L), and SUSPEND (2PIN=L) for noise control, as shown below.

{VCC OFF→ON}

| VCC | SPND | HPMT | SPMT |
|---|---|---|---|
| 1) OFF | L | L | L |
| 2) ON | L | L | L |
| 3) ON | H | L | L |
| 4) ON | H | H | L |
| 5) ON | H | H | H |

{VCC ON→OFF}

| VCC | SPND | HPMT | SPMT |
|---|---|---|---|
| 1) OFF | H | H | H |
| 2) ON | H | H | L |
| 3) ON | H | L | L |
| 4) ON | L | L | L |
| 5) ON | L | L | L |

9. Power supply bypass capacitor
   Place the bypass capacitor close to the VCC～GND pins.
10. Mode switching
    Do not apply a voltage that exceeds VCC or a voltage that is less than GND, at a control pin.
11. Power package
    Ensure a heat dissipation by connecting the heatsink to the back of the IC and to the GND board. Ensure that the GND area is large.
12. HPOUT
    Connect resistance (100 Ω is recommended) to the output for SPAMP input level adjustment and to prevent HPAMP oscillation.
13. Capacitive load
    Do not connect a capacitive load to SPAMP or HPAMP output as it may cause oscillation.
14. Startup time at low temperature and reduced power
    Use the following methods to eliminate longer start up time at low temperatures (less than about -10°C) and reduced power (less than about 3.0 V):
    1) Start in SPMUTE state and then cancel SPMUTE.
    2) Add to transistor and resistance, as shown in the application circuit diagram.

●Selection of order type

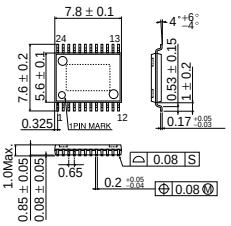
| B | H | 7 | 8 | 8 | 4 | E | F | V | — | E | 2 |
|---|---|---|---|---|---|---|---|---|---|---|---|

Part No.
BH7884EFV

Tape and Reel information

## HTSSOP-B24

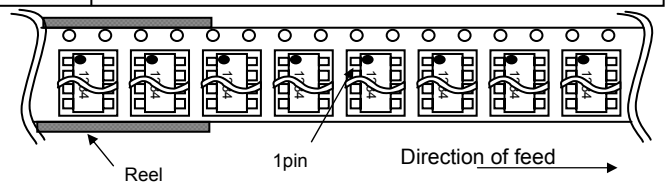
<Dimension>




(Unit:mm)

<Tape and Reel information>

| Tape | Embossed carrier tape |
|---|---|
| Quantity | 2000pcs |
| Direction of feed | E2<br>(The direction is the 1pin of product is at the upper left when you hold reel on the left hand and you pull out the tape on the right hand) |




※When you order , please order in times the amount of package quantity.



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