19-5228; Rev 0; 6/10

3V/5V Low-Power, Low-Noise, CMOS, Rail-to-Rail I/O Op Amps

General Description

The MAX9636/MAX9637/MAX9638 are single-supply, CMOS input op amps featuring wide bandwidth at low quiescent current, making them suitable for a broad range of battery-powered applications such as portable medical instruments, portable media players, and smoke detectors. A combination of extremely low input bias currents, low input current noise and low input voltage noise allows interface to high-impedance sources such as photodiode and piezoelectric sensors. These devices are also ideal for general-purpose signal processing functions such as filtering and amplification in a broad range of portable, battery-powered applications.

The ICs feature a maximized ratio of gain bandwidth (GBW) to supply current. The devices operate from a single 2.1V to 5.5V supply at a typical quiescent supply current of 36µA. For additional power conservation, the MAX9636 and MAX9638 offer a low-power shutdown mode that reduces supply current to 1µA and places the amplifiers' outputs into a high-impedance state.

The ICs are specified over the automotive operating temperature range (-40°C to +125°C). The single is offered in a space-saving, 6-pin SC70 package, while the dual is offered in tiny, 8-pin SC70 and 10-pin UTQFN packages.

Applications

- Portable Medical Instruments
- Piezoelectric Transducer Amplifiers
- Smoke Detectors
- Battery-Powered Devices
- General-Purpose Signal Conditioning
- Notebooks
- Portable Media Players

Features

- ♦ **Low Input Voltage-Noise Density: 38nV/$\sqrt{Hz}$**
- ♦ **Low Input Current-Noise Density: 50fA/$\sqrt{Hz}$**
- ♦ **Ultra-Low 0.1pA Bias Current**
- ♦ **Low 36µA Quiescent Current**
- ♦ **1µA Quiescent Current in Shutdown**
- ♦ **Wide 1.5MHz Bandwidth**
- ♦ **Single-Supply Operation V_{DD} = 2.1V to 5.5V**
- ♦ **Available in Tiny 6-Pin SC70, 8-Pin SC70, and 10-Pin UTQFN Packages**
- ♦ **-40°C to +125°C Operating Temperature Range**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX9636AXT+	-40°C to +125°C	6 SC70
MAX9637AXA+*	-40°C to +125°C	8 SC70
MAX9638AVB+*	-40°C to +125°C	10 UTQFN

+Denotes a lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.
**Future product—contact factory for availability.*

3V/5V Low-Power, Low-Noise, CMOS, Rail-to-Rail I/O Op Amps

ABSOLUTE MAXIMUM RATINGS

V_{DD}, $\overline{SHDN}$ to V_{SS} ....-0.3V to +6V
IN+, IN-, OUT ....GND - 0.3V to V_{DD} + 0.3V
Continuous Input Current (any pins).................... ±20mA
Output Short Circuit to V_{DD} or V_{SS} Duration 5s
Thermal Limits (Note 1)
Multiple Layer PCB
Continuous Power Dissipation (T_A = +70°C)
6-Pin SC70 (derate 3.1mW/°C above +70°C) 245mW
θ_{JA} ....326.5°C/W
θ_{JC} ....115°C/W
8-Pin SC70 (derate 3.1mW/°C above +70°C).............245mW
θ_{JA} ....326°C/W
θ_{JC} ....115°C/W
10-Pin UTQFN (derate 7mW/°C above +70°C)........558.7mW
θ_{JA} ....143.2°C/W
θ_{JC}....................20.1°C/W
Operating Temperature Range.................... -40°C to +125°C
Junction Temperature ....+150°C
Lead Temperature (soldering 10s) ....+300°C
Soldering Temperature (reflow) ....+260°C

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maxim-ic.com/thermal-tutorial**.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{CM} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, $\overline{SHDN}$ = V_{DD}, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC CHARACTERISTICS							
Input Voltage Range	V_{IN+}, V_{IN-}	Guaranteed by CMRR		V_{SS} - 0.1		V_{DD} + 0.1	V
Input Offset Voltage	V_{OS}	T_A = +25°C			0.01	2.2	mV
		T_A = -40°C to +125°C				3.5	
Input Offset Voltage Drift	TCV_{OS}	(Note 3)				7	µV/°C
Input Bias Current (Note 3)	I_B	T_A = +25°C			±0.1	±0.8	pA
		T_A = -40°C to +85°C				±50	
		T_A = -40°C to +125°C				±800	
Common-Mode Rejection Ratio	CMRR	V_{SS} < V_{CM} < (V_{DD} - 1.4V)	T_A = +25°C	72	86		dB
			T_A = -40°C to +125°C	68			
		(V_{SS} - 0.1V) < V_{CM} < (V_{DD} + 0.1V)		58	77		
Open-Loop Gain	A_{OL}	V_{OUT} = 0.25V from rails		104	124		dB
		V_{OUT} = 0.4V from rails, R_L = 600Ω		100	120		
Output Short-Circuit Current	I_{SC}	Short to V_{DD}			10		mA
		Short to V_{SS}			40		
Output Voltage Low	VOL	V_{OUT}	R_L = 10kΩ		0.014	0.03	V
			R_L = 600Ω		0.044	0.08	
Output Voltage High	V_{OH}	V_{DD} - V_{OUT}	R_L = 10kΩ		0.019	0.04	V
			R_L = 600Ω		0.057	0.1	
Output Leakage in Shutdown (MAX9636, MAX9638 Only)		SHDN = V_{SS}, V_{OUT} = 0V to V_{DD}			0.01	1	µA

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{CM} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, $\overline{SHDN}$ = V_{DD}, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
AC CHARACTERISTICS							
Input Voltage Noise Density	e_N	f = 1kHz			38		nV/√Hz
Input Voltage Noise		0.1Hz ≤ f ≤ 10Hz			5		µV_{P-P}
Input Current Noise Density	I_N	f = 1kHz			50		fA/√Hz
Input Capacitance	C_{IN}				2		pF
Gain Bandwidth	GBW				1.5		MHz
Slew Rate	SR				0.9		V/µs
Capacitive Loading	C_{LOAD}	No sustained oscillations			300		pF
Distortion	THD	f = 10kHz, V_O = 2V_{P-P}, A_V = 1V/V			-68		dB
		f = 10kHz, V_O = 2V_{P-P}, A_V = 1V/V, V_{DD} = 5.5V			-74		
Settling Time		To 0.1%, V_{OUT} = 2V step, A_V = 1V/V			11.5		µs
POWER-SUPPLY CHARACTERISTICS							
Power-Supply Range	V_{DD}	Guaranteed by PSRR		2.1		5.5	V
Power-Supply Rejection Ratio	PSRR	V_{IN+} = V_{IN-} = V_{SS}, V_{DD} - V_{SS} = 2.1V to 5.5V	T_A = +25°C	72	100		dB
			T_A = -40°C to +125°C	69			
Quiescent Current	I_{DD}	Per amplifier	T_A = +25°C		36	55	µA
			T_A = -40°C to +125°C			60	
Shutdown Supply Current (MAX9636, MAX9638 Only)	I_{DD_SHDN}	V_{SHDN} ≤ V_{IL}				1	µA
Shutdown Input Low (MAX9636, MAX9638 Only)	V_{IL}	Over the power-supply range				0.5	V
Shutdown Input High (MAX9636, MAX9638 Only)	V_{IH}	Over the power-supply range		1.4			V
Shutdown Input Bias Current (MAX9636, MAX9638 Only)	I_{SHDN}	(Note 3)			1	100	nA
Turn-On Time (MAX9636, MAX9638 Only)	t_{ON}	V_{SHDN} = 0V to 3V			60		µs
Power-Up Time	t_{UP}	V_{DD} = 0V to 3.3V			18		µs

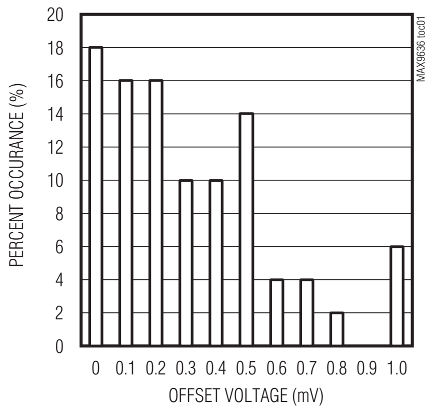
Note 2: All devices are 100% production tested at T_A = +25°C. Temperature limits are guaranteed by design.
Note 3: Parameter is guaranteed by design.

3V/5V Low-Power, Low-Noise, CMOS, Rail-to-Rail I/O Op Amps

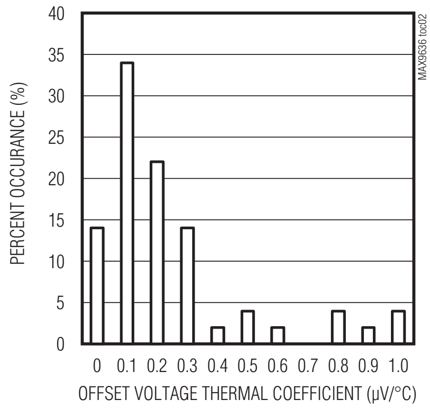
Typical Operating Characteristics

(V_{DD} = 3.3V, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{CM} = $V_{DD}/2$, R_L = 10kΩ to $V_{DD}/2$, $\overline{SHDN}$ = V_{DD}, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.)

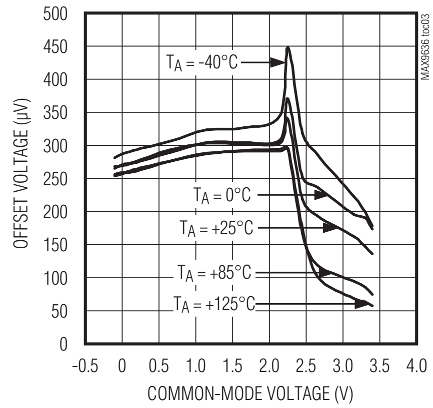
OFFSET VOLTAGE HISTOGRAM



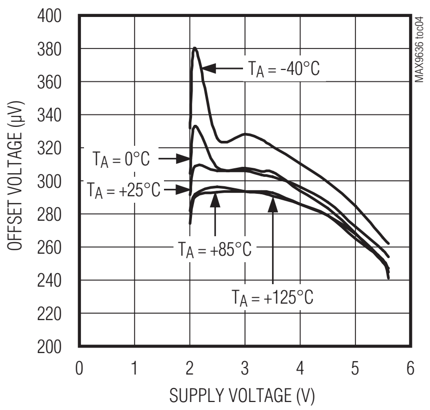
OFFSET VOLTAGE THERMAL COEFFICIENT HYSTOGRAM



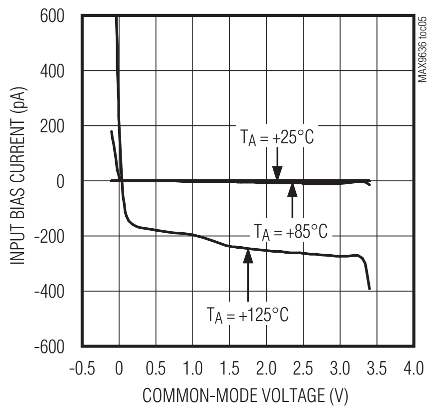
INPUT OFFSET VOLTAGE vs. COMMON-MODE VOLTAGE



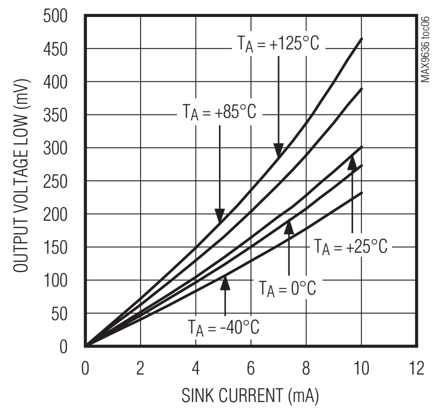
INPUT OFFSET VOLTAGE vs. SUPPLY VOLTAGE $V_{CM} = V_{DD}/2$



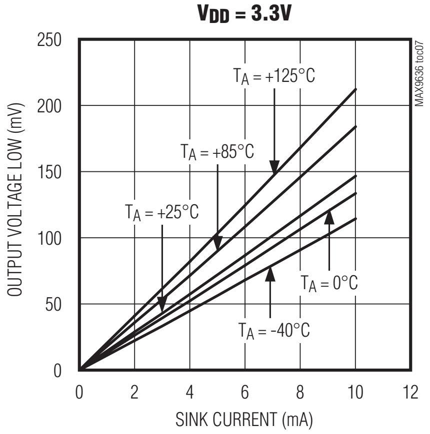
INPUT BIAS CURRENT vs. COMMON-MODE VOLTAGE



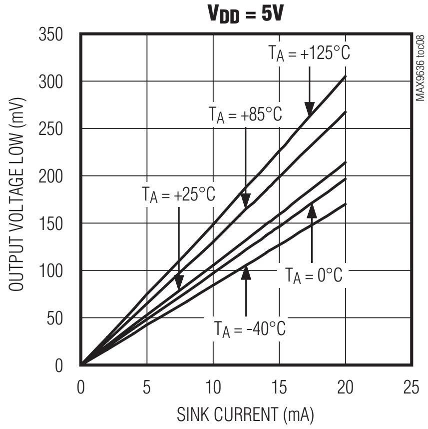
OUTPUT VOLTAGE LOW vs. SINK CURRENT V_{DD} = 2.1V



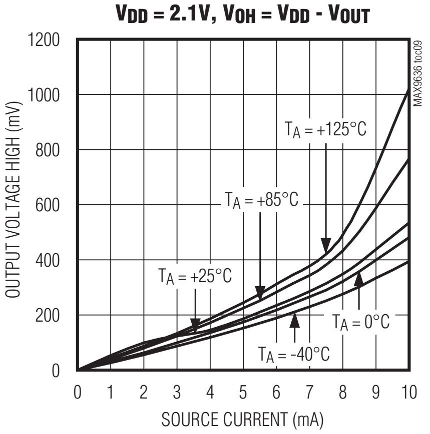
OUTPUT VOLTAGE LOW vs. SINK CURRENT V_{DD} = 3.3V



OUTPUT VOLTAGE LOW vs. SINK CURRENT V_{DD} = 5V



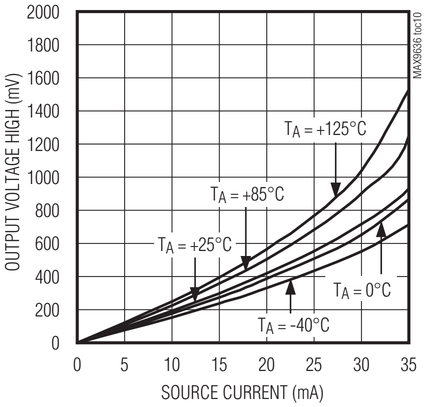
OUTPUT VOLTAGE HIGH vs. SOURCE CURRENT V_{DD} = 2.1V, V_{OH} = V_{DD} - V_{OUT}



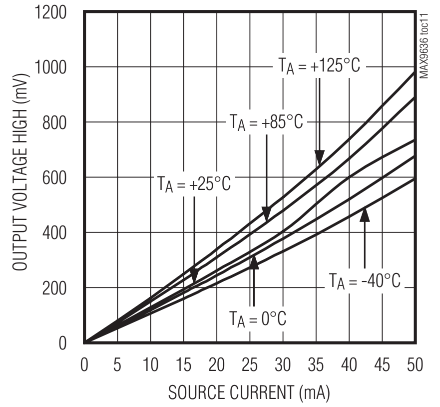
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{CM} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, $\overline{SHDN}$ = V_{DD}, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.)

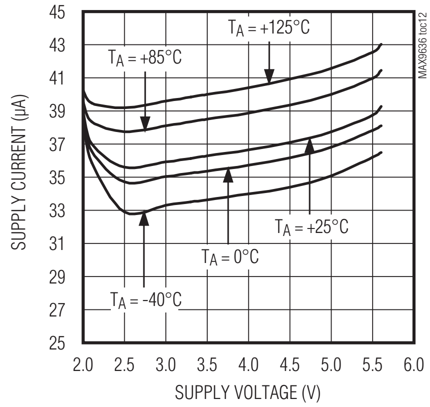
OUTPUT VOLTAGE HIGH vs. SOURCE CURRENT
V_{DD} = 3.3V, V_{OH} = V_{DD} - V_{OUT}



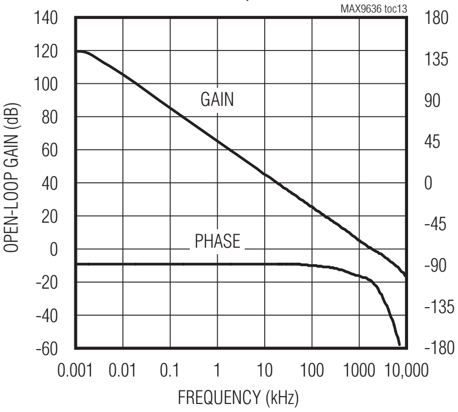
OUTPUT VOLTAGE HIGH vs. SOURCE CURRENT
V_{DD} = 5V, V_{OH} = V_{DD} - V_{OUT}



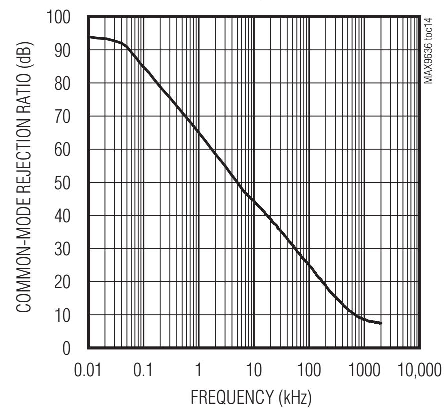
SUPPLY CURRENT vs. SUPPLY VOLTAGE



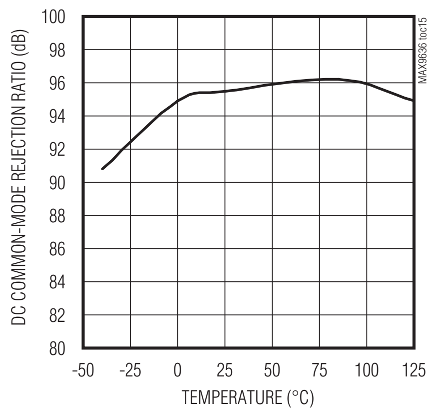
OPEN-LOOP GAIN AND PHASE vs. FREQUENCY



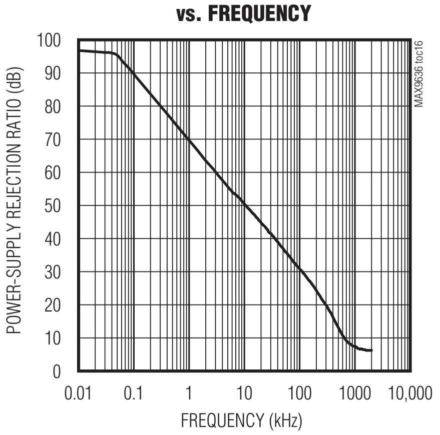
COMMON-MODE REJECTION RATIO vs. FREQUENCY



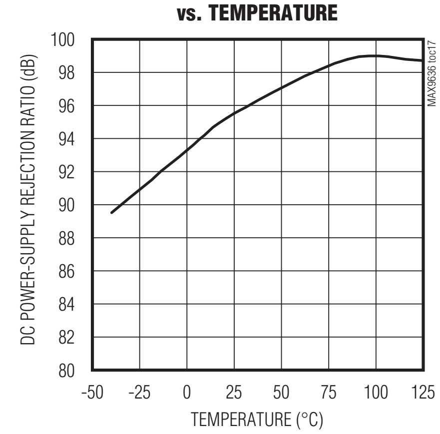
DC COMMON-MODE REJECTION RATIO vs. TEMPERATURE



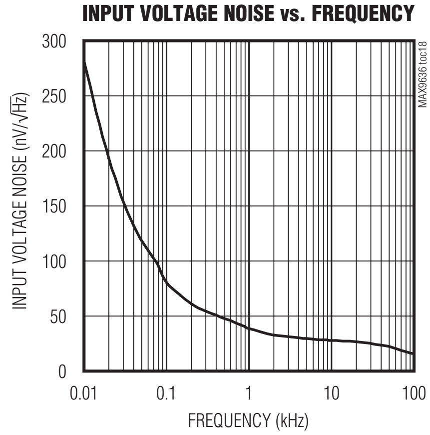
POWER-SUPPLY REJECTION RATIO vs. FREQUENCY



DC POWER-SUPPLY REJECTION RATIO vs. TEMPERATURE



INPUT VOLTAGE NOISE vs. FREQUENCY

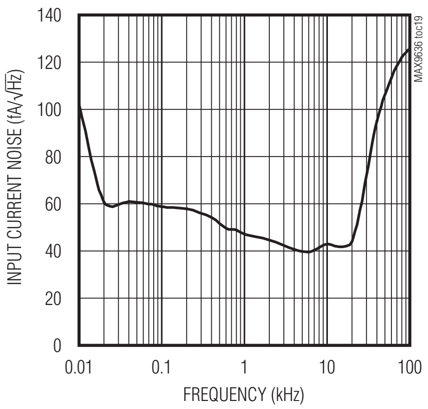


3V/5V Low-Power, Low-Noise, CMOS, Rail-to-Rail I/O Op Amps

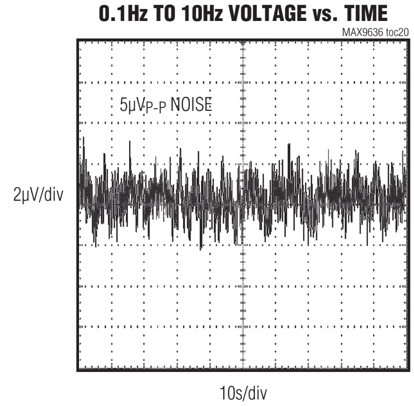
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{CM} = V_{DD}/2, R_L = 10kΩ to V_{DD}/2, $\overline{SHDN}$ = V_{DD}, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.)

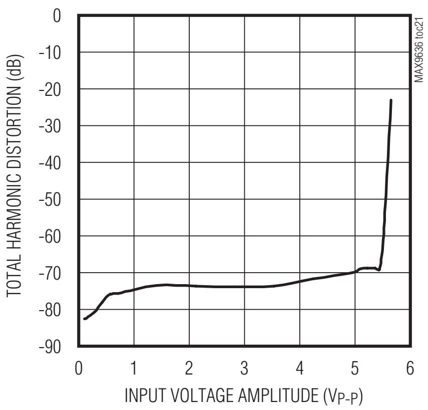
INPUT CURRENT NOISE vs. FREQUENCY



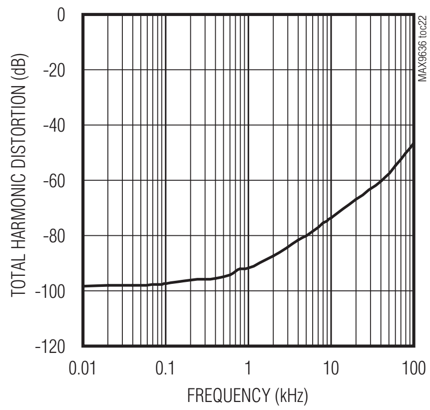
0.1Hz TO 10Hz VOLTAGE vs. TIME



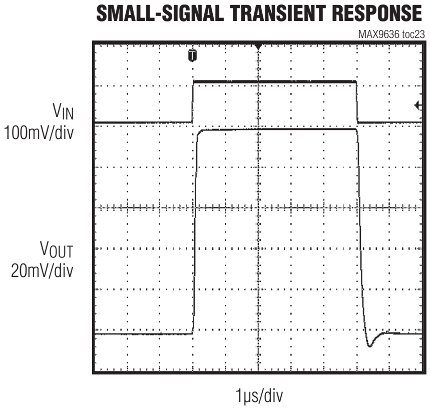
TOTAL HARMONIC DISTORTION vs. INPUT VOLTAGE AMPLITUDE V_{DD} = 5.5V, A_O = 1V/V



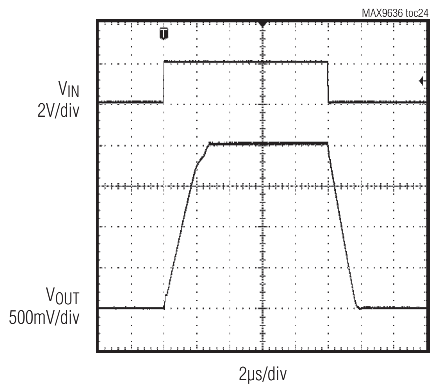
TOTAL HARMONIC DISTORTION vs. FREQUENCY V_{DD} = 5.5V, A_O = 1V/V, V_{OUT} = $2V_{P-P}$, R_L = 10kΩ to V_{DD}/2



SMALL-SIGNAL TRANSIENT RESPONSE



LARGE-SIGNAL TRANSIENT RESPONSE

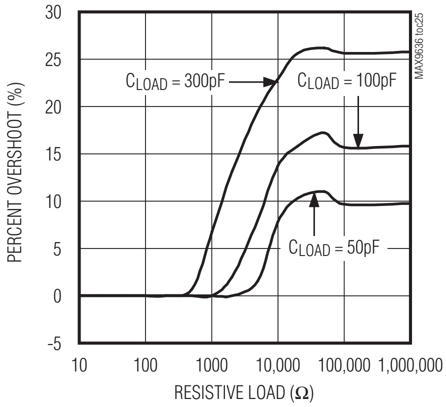


3V/5V Low-Power, Low-Noise, CMOS, Rail-to-Rail I/O Op Amps

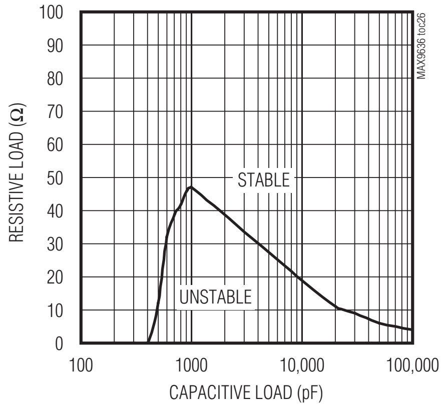
Typical Operating Characteristics (continued)

(V_{DD} = 3.3V, V_{SS} = 0V, V_{IN+} = V_{IN-} = V_{CM} = $V_{DD}/2$, R_L = 10kΩ to $V_{DD}/2$, $\overline{SHDN}$ = V_{DD}, T_A = -40°C to +125°C. Typical values are at T_A = +25°C, unless otherwise noted.)

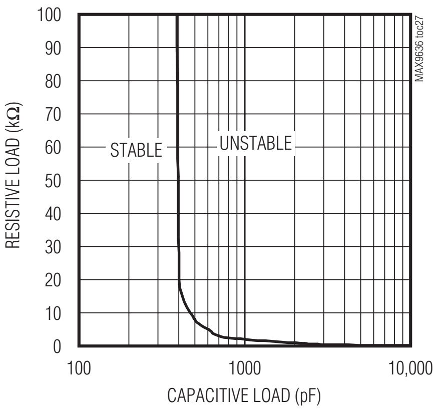
PERCENT OVERSHOOT vs. RESISTIVE LOAD



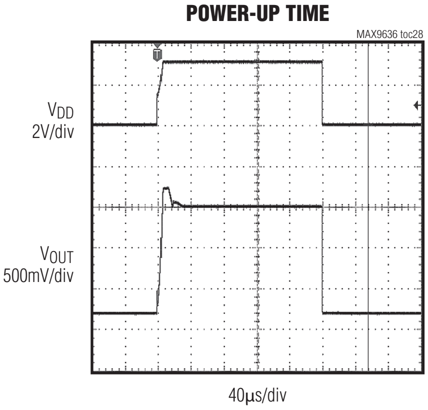
STABILITY vs. CAPACITIVE AND RESISTIVE LOAD R_{ISO} IN SERIES WITH C_{LOAD}



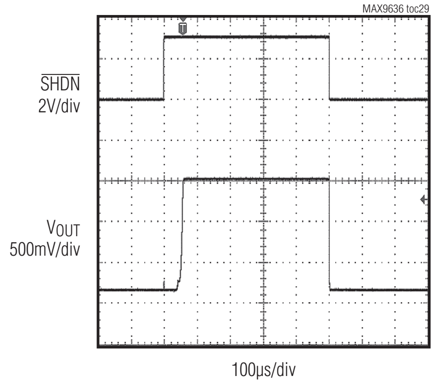
STABILITY vs. CAPACITIVE AND RESISTIVE LOAD R_P IN PARALLEL WITH C_L



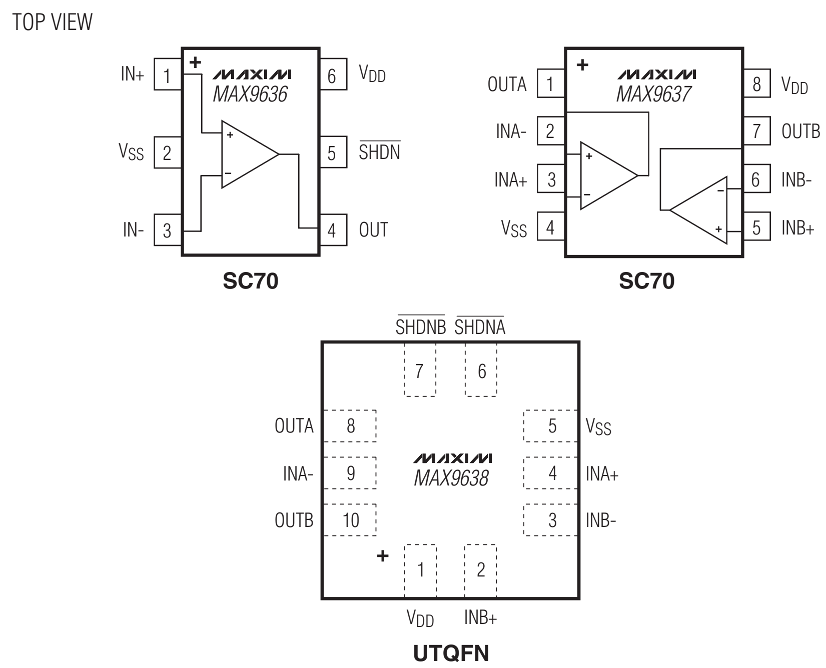
POWER-UP TIME



TURN-ON TIME



Pin Configurations



Pin Description

MAX9636 (6 SC70)	MAX9637 (8 SC70)	MAX9638 (10 UTQFN)	NAME	FUNCTION
1	—	—	IN+	Positive Input
—	3	4	INA+	Positive Input A
—	5	2	INB+	Positive Input B
2	4	5	V_{SS}	Negative Power Supply. Bypass with a 0.1µF capacitor to ground.
3	—	—	IN-	Negative Input
—	2	9	INA-	Negative Input A
—	6	3	INB-	Negative Input B
4	—	—	OUT	Output
—	1	8	OUTA	Output A
—	7	10	OUTB	Output B
—	—	6	$\overline{SHDNA}$	Active-Low Shutdown A
—	—	7	$\overline{SHDNB}$	Active-Low Shutdown B
5	—	—	$\overline{SHDN}$	Active-Low Shutdown
6	8	1	V_{DD}	Positive Power Supply. Bypass with a 0.1µF capacitor to ground.

Detailed Description

The MAX9636/MAX9637/MAX9638 are single-supply, CMOS input op amps. They feature wide bandwidth at low quiescent current, making them suitable for a broad range of battery-powered applications such as portable medical instruments, portable media players, and smoke detectors. A combination of extremely low input bias currents, low input current noise, and low input voltage noise allows interface to high-impedance sources such as photodiode and piezoelectric sensors. These devices are also ideal for general-purpose signal processing functions such as filtering and amplification in a broad range of portable, battery-powered applications.

The devices' operational common-mode range extends 0.1V beyond the supply rails, allowing for a wide variety of single-supply applications.

The ICs also feature low quiescent current and a shutdown mode that greatly reduces quiescent current while the device is not operational. This makes the device suitable for portable applications where power consumption must be minimized.

Rail-to-Rail Input Stage

The operational amplifiers have parallel-connected n- and p-channel differential input stages that combine to accept a common-mode range extending 100mV beyond the supply rails. The n-channel stage is active for common-mode input voltages typically greater than (V_{DD} - 1.2V), and the p-channel stage is active for common-mode input voltages typically less than (V_{DD} - 1.4V). A small transition region exists, typically V_{DD} - 1.4 to V_{DD} - 1.2V, during which both pairs are on.

Rail-to-Rail Output Stage

The maximum output voltage swing is load dependent. However, it is guaranteed to be within 100mV of the positive rail even with 3mA of load current. To maximize the output current sourcing capability, these parts do not come with built-in short-circuit protection. If loads heavier than 600Ω must be driven, then ensure that the maximum allowable power dissipation is not exceeded (see the *Absolute Maximum Ratings* section).

Low Input Bias Current

This op-amp family features ultra-low 0.1pA (typ) input bias current and guaranteed maximum current of ±50pA over -40°C to +85°C when the input common-mode voltage is at midrail. For the -40°C to +85°C temperature range, the variation in the input bias current is small with changes in the input voltage due to very high input impedance (in the order of 100GΩ).

Power-Up Time

The ICs typically require a power-up time of 18µs. Supply settling time depends on the supply voltage, the value of the bypass capacitor, the output impedance of the incoming supply, and any lead resistance or inductance between components. Op amp settling time depends primarily on the output voltage and is slew-rate limited. The output settles in approximately 11.5µs for V_{DD} = 3V and V_{OUT} = V_{DD}/2V (see the Power-Up Time graph in the *Typical Operating Characteristics* section).

3V/5V Low-Power, Low-Noise, CMOS, Rail-to-Rail I/O Op Amps

Driving Capacitive Loads

The ICs have a high tolerance for capacitive loads. In unity-gain configuration, the op amps can typically drive up to 300pF pure capacitive load. Increasing the gain enhances the amplifier's ability to drive greater capacitive loads. In unity-gain configurations, capacitive load drive can be improved by inserting a small (5Ω to 30Ω) isolation resistor, R_{ISO}, in series with the output, as shown in Figure 1. This significantly reduces ringing while maintaining DC performance for purely capacitive loads. However, if the load also has a resistive component then a voltage-divider is created, introducing a direct current (DC) error at the output. The error introduced is proportional to the ratio RISO/RL, which is usually negligible in most cases. Applications that cannot tolerate this slight DC error can use an alternative approach of providing stability by placing a suitable resistance in parallel with the capacitive load as shown in Figure 2 (see the *Typical Operating Characteristics* section for graphs of the stable operating region for various capacitive loads vs. resistive loads). While this approach of adding a resistor parallel to the load does not introduce DC error, it nevertheless reduces the output swing proportionally.

High-Impedance Sensor Front-Ends

The ICs interface to both current-output sensors, such as photodiodes (Figure 3), and high-impedance voltage sources, such as piezoelectric sensors. For current-output sensors, a transimpedance amplifier is the most noise-efficient method for converting the input signal to a voltage. High-value feedback resistors are commonly chosen to create large gains, while feedback capacitors help stabilize the amplifier by cancelling any poles introduced in the feedback function by the highly capacitive sensor or cabling. A combination of low-current noise and low-voltage noise is important for these applications. Take care to calibrate out photodiode dark current if DC accuracy is important. The high bandwidth and slew rate also allows AC signal processing in certain medical photodiode sensor applications such as pulse oximetry.

For voltage-output sensors, a noninverting amplifier is typically used to buffer and/or apply a small gain to the input voltage signal. Due to the extremely high impedance of the sensor output, a low input bias current with minimal temperature variation is very important for these applications.

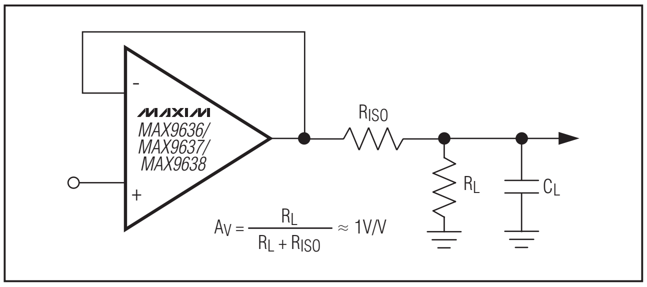


Figure 1. Using a Series Resistor to Isolate the Capacitive Load from the Op Amp

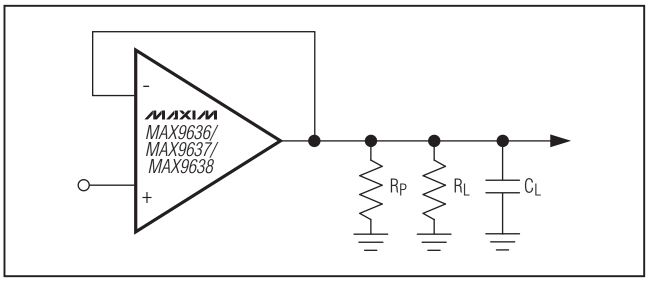


Figure 2. Using a Parallel Resistor to Degenerate the Effect of the Capacitive Load and Increase Stability

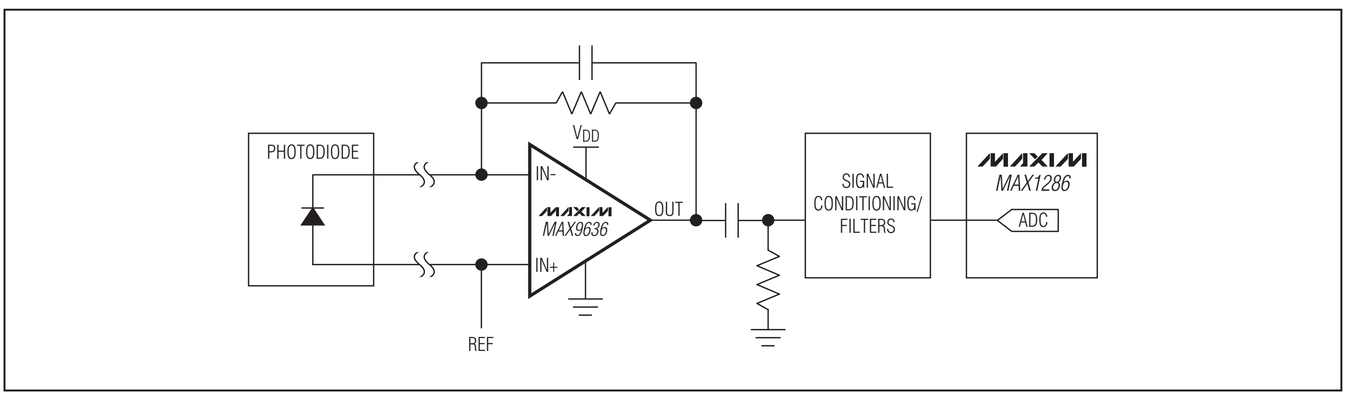


Figure 3. MAX9636 in a Sensor Preamp Configuration

For best performance, follow standard high-impedance layout techniques, which include the following:

- Using shielding techniques to guard against parasitic leakage paths. For example, put a trace connected to the noninverting input around the inverting input.
- Minimizing the amount of stray capacitance connected to op amp's inputs to improve stability. To achieve this, minimize trace lengths and resistor leads by placing external components as close as possible to the package.
- Use separate analog and digital power supplies.

Applications Information

Shutdown Operation

The MAX9636/MAX9638 feature an active-low shutdown mode that sends the inputs and output into high impedance and substantially lowers the quiescent current.

Active-Low Input

The shutdown active-low (V_{IL}) and high (V_{IH}) threshold voltages are designed for ease of integration with digital controls, such as microcontroller outputs. These thresholds are independent of supply, eliminating the need for external pulldown circuitry.

Output During Shutdown

The MAX9638 output is in a high-impedance state while $\overline{SHDN}$ is low. The device structure limits the output leakage current in this state to 0.01µA when the output is between 0V to V_{DD}.

ADC Driver

The MAX9636/MAX9637/MAX9638 are low-power amplifiers ideal for driving high to medium-resolution ADCs. Figure 3 shows how the MAX9636 is connected to a photodiode, with the amplifier output connected to additional signal conditioning/filtering, or directly to the ADC. The MAX1286–MAX1289 family of low-power, 12-bit ADCs are ideal for connecting to the MAX9636/MAX9637/MAX9638.

The MAX1286–MAX1289 ADCs offer sample rates up to 150ksps, with 3V and 5V supplies, as well as 1- and 2-channel options. These ADCs dissipate just 15µA when sampling at 10ksps and 0.2µA in shutdown. Offered in tiny 8-pin SOT23 and 3mm x 3mm TDFN packages, the MAX1286–MAX1289 ADCs are an ideal fit to pair with the MAX9636/MAX9637/MAX9638 amplifiers in portable applications.

Similarly, the MAX1086–MAX1089 is a family of 10-bit pin-compatible low-power ADCs with the same 3V/5V, 1- and 2-channel options. Table 1 details the amplifier and ADC pairings for single- and dual-channel applications.

Chip Information

PROCESS: BiCMOS

Table 1. Recommended Amplifiers/ADCs

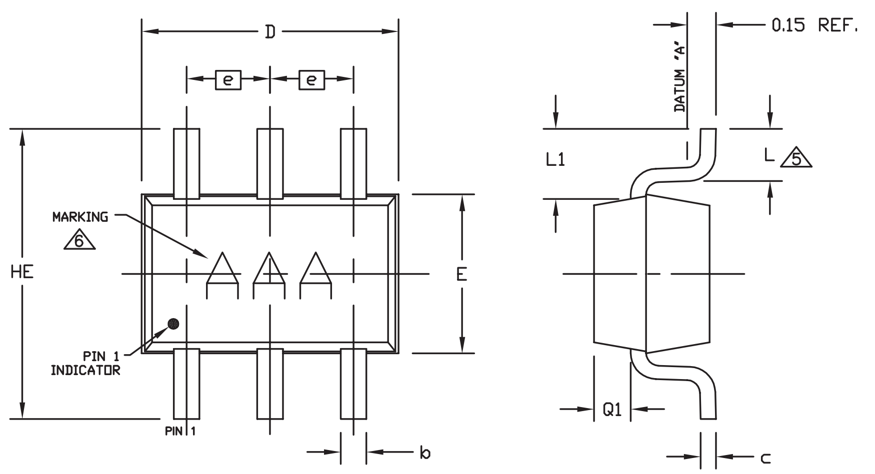
CHANNELS	AMPLIFIER	ADC			
		3V, 10 BIT	3V, 12 BIT	5V, 10 BIT	5V, 12 BIT
1	MAX9636	MAX1089	MAX1289	MAX1088	MAX1288
2	MAX9637	MAX1087	MAX1287	MAX1086	MAX1286
2	MAX9638	MAX1087	MAX1287	MAX1086	MAX1286

Package Information

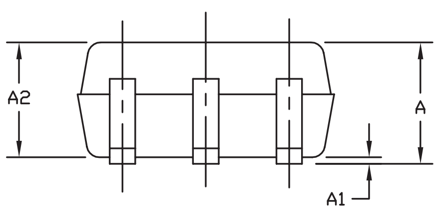
For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	DOCUMENT NO.
6 SC70	X6SN+1	21-0077
8 SC70	X8CN+1	21-0460
10 UTQFN	V101A1CN+1	21-0028

SC70, 6L.EPS



COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	0.80	0.95	1.10
A1	0.00	0.07	0.10
A2	0.80	0.90	1.00
b	0.15	0.22	0.30
c	0.10	0.14	0.18
D	1.80	2.00	2.20
e	0.65 BSC.		
E	1.15	1.25	1.35
HE	1.80	2.20	2.40
L	0.26	0.34	0.46
L1	0.425 TYP.		
Q1	0.10	0.25	0.40
PKG. CODES	X6SN-1		



NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COPLANARITY 4 MILS. MAX.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM 'A' AND LEAD SURFACE.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
8. ALL DIMENSIONS COMPLY TO JEDEC MO-203.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

MAXIM

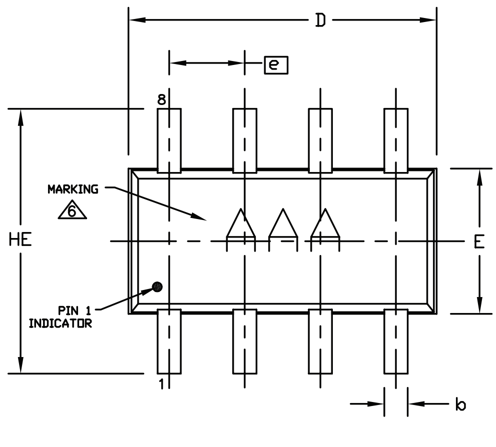
TITLE: PACKAGE OUTLINE, 6L SC70

APPROVAL | DOCUMENT CONTROL NO. 21-0077 | REV. G | 1/1

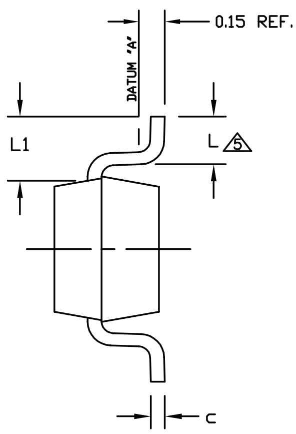
-DRAWING NOT TO SCALE-

Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

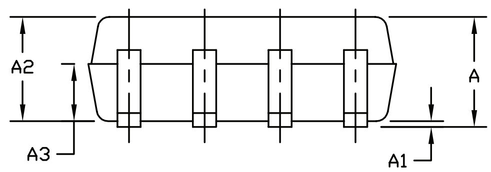


TOP VIEW



SIDE VIEW

COMMON DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	0.80	0.95	1.10
A1	0.00	0.07	0.10
A2	0.80	0.90	1.00
A3	0.40	0.47	0.55
b	0.15	0.21	0.27
c	0.10	0.14	0.18
D	1.80	2.00	2.20
e	0.50 BSC.		
E	1.15	1.25	1.35
HE	1.80	2.20	2.40
L	0.26	0.34	0.46
L1	0.425 TYP.		
PKG. CODE	X8CN-1		



SIDE VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONS ARE INCLUSIVE OF PLATING.
3. DIMENSIONS ARE EXCLUSIVE OF MOLD FLASH & METAL BURR.
4. COPLANARITY 4 MILS. MAX.
5. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM 'A' AND LEAD SURFACE.
6. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
7. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
8. ALL DIMENSIONS COMPLY TO JEDEC MO-203.
9. ALL DIMENSIONS APPLY TO BOTH LEADED (-) AND LEAD FREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-

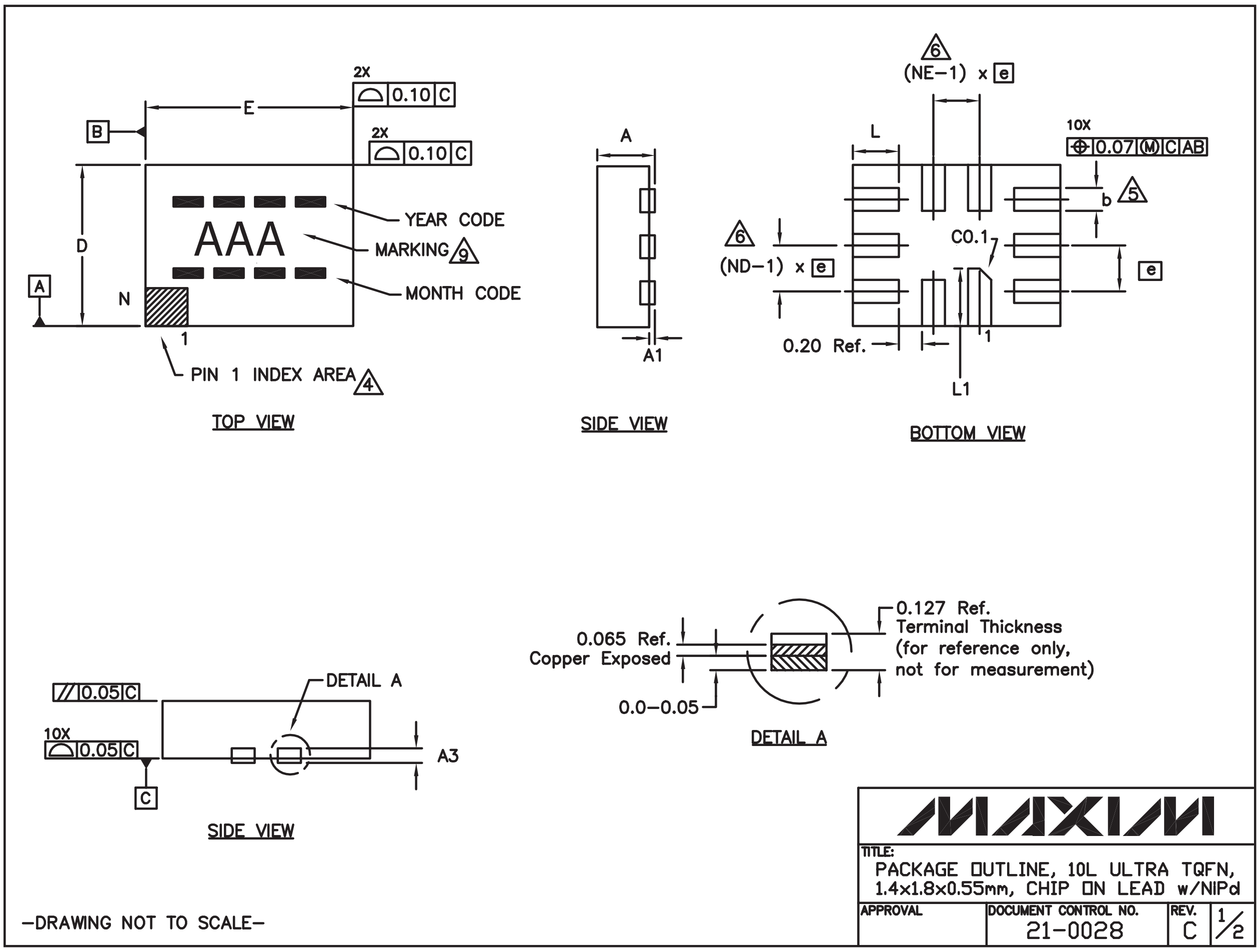
TITLE: PACKAGE OUTLINE, 8L SC70, COL PKG., NiPd

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0460	B	1/1

3V/5V Low-Power, Low-Noise, CMOS, Rail-to-Rail I/O Op Amps

Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages.** Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.



Package Information (continued)

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.25mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. REFER TO JEDEC MO-248 AND MO-236.
8. WARPAGE SHALL NOT EXCEED 0.05mm.
9. MARKING IS PACKAGE ORIENTATION PURPOSE ONLY.
10. DIMENSIONS APPLY TO PbFREE (+) PRODUCTS ONLY.
11. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.05mm.

PKG	10L 1.4x1.8			NOTE
REF.	MIN.	NOM.	MAX.	
A	0.45	0.50	0.55	
A1	0	-	0.05	
A3	0.127 REF			
b	0.15	0.20	0.25	
D	1.30	1.40	1.50	
E	1.70	1.80	1.90	
e	0.40 BSC.			
L	0.35	0.40	0.45	
L1	0.45	0.50	0.55	
N	10			
ND	3			
NE	2			
PKG. CODE	V101A1CN-1			

TABLE 1

Translation Table for Calendar Year Code

2008	■	□	□	□
2009	■	□	□	■
2010	■	□	■	□
2011	□	□	□	■
2012	□	□	■	□
2013	□	□	■	■
2014	□	■	□	□
2015	□	■	□	■
2016	□	■	■	□
2017	□	■	■	■

TABLE 2

Translation Table for Calendar Month Code

Jan	□	□	□	■
Feb	□	□	■	□
Mar	□	□	■	■
Apr	□	■	□	□
May	□	■	□	■
Jun	□	■	□	□
Jul	□	■	■	■
Aug	■	□	□	□
Sep	■	□	□	■
Oct	■	□	■	□
Nov	■	□	■	■
Dec	■	■	□	□

Legend: ■ Marked with bar □ Blank space - no bar required

-DRAWING NOT TO SCALE-

MAXIM

TITLE: PACKAGE OUTLINE, 10L ULTRA TQFN, 1.4x1.8x0.55mm, CHIP ON LEAD w/NIPd

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0028	C	2/2

3V/5V Low-Power, Low-Noise, CMOS, Rail-to-Rail I/O Op Amps

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/10	Initial release	—