



# SOT23 Power-Supply Sequencers

MAX6819/MAX6820

## General Description

The MAX6819/MAX6820 are power-supply sequencers for dual-voltage microprocessors ( $\mu$ Ps) and multivoltage systems. These devices monitor a primary supply voltage and enable/disable an external n-channel MOSFET switch for a secondary supply voltage. The MAX6819/MAX6820 control local component voltage sequencing when system power-on/power-off characteristics cannot be guaranteed (supplies come from a multivoltage system bus, silver box, or must be sequenced in different modes for components on the same board). These small power-supply sequencers improve system reliability.

The MAX6819/MAX6820 include an internal voltage reference/comparator with externally adjustable thresholds to monitor the primary power supply. When the primary supply is below the desired threshold, an external secondary supply MOSFET switch is disabled. When the primary supply exceeds the threshold, an internal charge pump is activated and the external MOSFET switch is enabled to connect the secondary supply to the load. The charge pump fully enhances the n-channel MOSFET switch to provide a very low  $R_{DS-ON}$  voltage drop. The devices can be connected to support various supply sequencing priorities such as  $V_{I/O}$  before  $V_{CORE}$  or  $V_{CORE}$  before  $V_{I/O}$ .

The MAX6819 features a logic-driven EN input to enable/disable the external MOSFET drive and includes an internally fixed 200ms enable timeout period ( $V_{PRIMARY\ GOOD}$  to  $V_{SECONDARY\ ENABLE}$ ). The MAX6820 allows the enable timeout period to be adjusted with a single external capacitor. Both devices are specified over the automotive temperature range ( $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$ ) and are available in space-saving 6-pin SOT23 packages.

## Applications

- Dual-Voltage Microprocessors
- Multivoltage Systems
- Digital Signal Processors
- Power PC™ Series Processors

**Pin Configurations and Typical Operating Circuits** continued at end of data sheet.

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## Features

- ◆ Adjustable Primary Supply Voltage Monitor (Monitors Down to 0.62V)
- ◆ Internal Charge Pump to Enhance External Secondary Supply n-Channel MOSFET Switch
- ◆ Delay from Primary Supply Good to Secondary Supply Enabled  
Factory Fixed 200ms (MAX6819)  
Capacitor Adjustable (MAX6820)
- ◆ Logic Driven ENABLE Input (MAX6819)
- ◆ Immune to Short Voltage Transients
- ◆ Few External Components
- ◆  $-40^{\circ}\text{C}$  to  $+125^{\circ}\text{C}$  Operating Temperature Range
- ◆ Small 6-Pin SOT23 Package

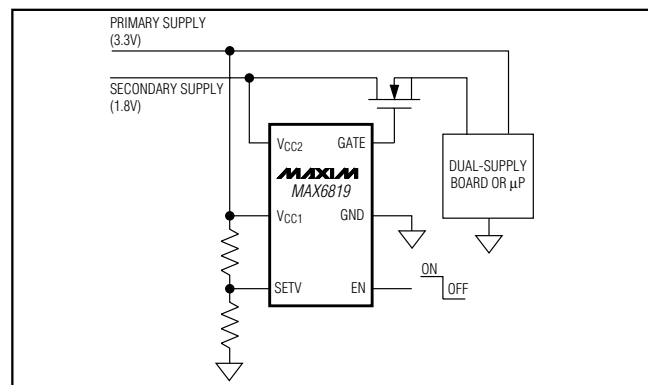
## Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	TOP MARK
MAX6819UT-T	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	6 SOT23-6	AARF
MAX6820UT-T	$-40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$	6 SOT23-6	AARG

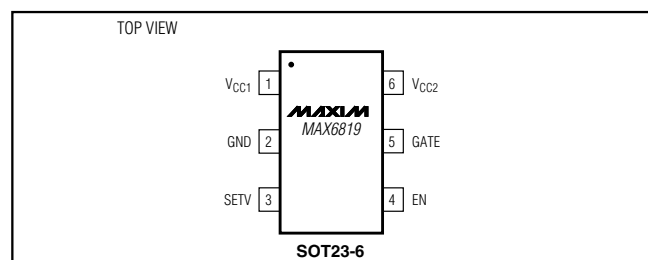
Products must be ordered in 2,500 piece increments.

Devices are available in both leaded and lead-free packaging. Specify lead-free by replacing "-T" with "+T" when ordering.

## Typical Operating Circuits



## Pin Configurations



# SOT23 Power-Supply Sequencers

## ABSOLUTE MAXIMUM RATINGS

Referenced to GND

V<sub>CC1</sub>, V<sub>CC2</sub>, EN .....-0.3V to +6.0V  
 SETV, SETD .....-0.3V to the higher of (V<sub>CC1</sub> + 0.3V) and  
 (V<sub>CC2</sub> + 0.3V)  
 GATE .....-0.3V to +12.0V  
 Input Current/Output Current (all pins) .....20mA

Continuous Power Dissipation (T<sub>A</sub> = +70°C)

6-Pin SOT23 (derate 8.7mW/°C above +70°C) .....696mW  
 Operating Temperature Range .....-40°C to +125°C  
 Junction Temperature .....+150°C  
 Storage Temperature Range .....-65°C to +150°C  
 Lead Temperature (soldering 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

## ELECTRICAL CHARACTERISTICS

(V<sub>CC1</sub> or V<sub>CC2</sub> > +2.125V to +5.5V, T<sub>A</sub> = -40°C to +125°C, unless otherwise specified. Typical values are at T<sub>A</sub> = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage Range	V <sub>CC1</sub> , V <sub>CC2</sub>	(Note 2)	0.9		5.5	V
V <sub>CC1</sub> , V <sub>CC2</sub> Supply Current	I <sub>CC</sub>	V <sub>CC1</sub> = V <sub>CC2</sub> = +3.3V		60	120	μA
V <sub>CC1</sub> , V <sub>CC2</sub> Disable Mode Current		V <sub>CC1</sub> = V <sub>CC2</sub> = +3.3V, EN = GND		20		μA
V <sub>CC1</sub> , V <sub>CC2</sub> Slew Rate (Note 3)		MAX6819		6		V/s
		MAX6820 (Note 4)		1.2 / t <sub>DELAY</sub>		
Undervoltage Lockout (UVLO)	V <sub>UVLO</sub>		1.875	2.0	2.125	V
SETV Threshold	V <sub>TH</sub>	V <sub>SETV</sub> rising, enables GATE	0.602	0.618	0.634	V
SETV Input Current		(Note 3)		10	100	nA
SETV Threshold Hysteresis		V <sub>SETV</sub> falling, disables GATE		-1		%
SETV to GATE Delay	t <sub>DELAY</sub>	V <sub>SETV</sub> > V <sub>TH</sub> , V <sub>EN</sub> ≥ 2V (MAX6819)	140	200	280	ms
SETD Ramp Current (MAX6820)	I <sub>SETD</sub>	V <sub>CC1</sub> or V <sub>CC2</sub> > +2.125V	400	500	600	nA
SETD Voltage (MAX6820)	V <sub>SETD</sub>	V <sub>CC1</sub> or V <sub>CC2</sub> > +2.125V	1.210	1.242	1.273	V
SETD Threshold Hysteresis (MAX6820)		V <sub>SETD</sub> falling		-62		mV
GATE Turn-On Time	t <sub>ON</sub>	C <sub>GATE</sub> = 1500pF, V <sub>CC2</sub> = +3.3V, V <sub>GATE</sub> = +7.8V	0.5	1.5	10	ms
GATE Turn-Off Time	t <sub>OFF</sub>	C <sub>GATE</sub> = 1500pF, V <sub>CC2</sub> = +3.3V, V <sub>GATE</sub> = +0.5V		30		μs
GATE Voltage	V <sub>GATE</sub>	With respect to V <sub>CC2</sub> (Note 2) R <sub>GATE</sub> > 50MΩ to V <sub>CC2</sub>	4.5	5.5	6.0	V
		With respect to V <sub>CC2</sub> (Note 2) R <sub>GATE</sub> > 5MΩ to V <sub>CC2</sub>	4.0		6.0	
EN Input Voltage	V <sub>IL</sub>	V <sub>CC1</sub> or V <sub>CC2</sub> > +2.125V to +5.5V			0.4	V
	V <sub>IH</sub>		2.0			

**Note 1:** 100% production tested at T<sub>A</sub> = +25°C. Specifications over temperature limit are guaranteed by design.

**Note 2:** Either V<sub>CC1</sub> or V<sub>CC2</sub> must be > 2.125V. The other supply can go to 0.

**Note 3:** Guaranteed by design, not production tested.

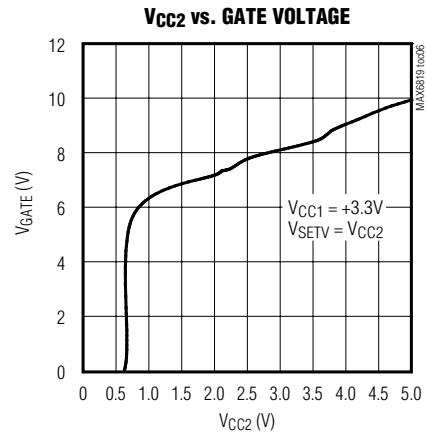
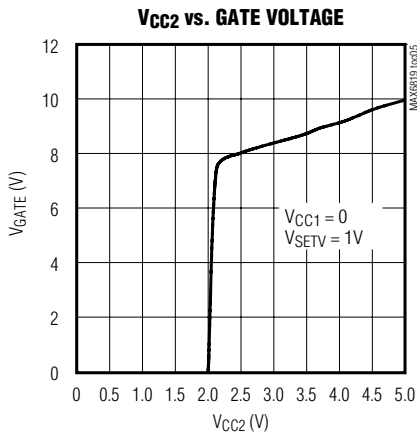
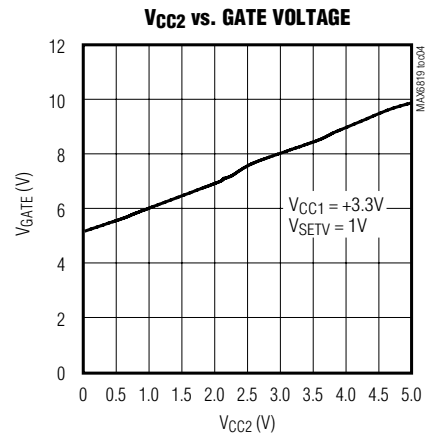
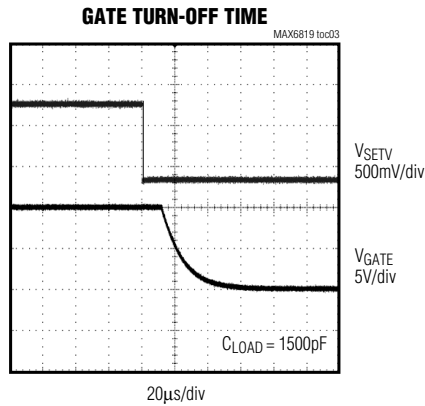
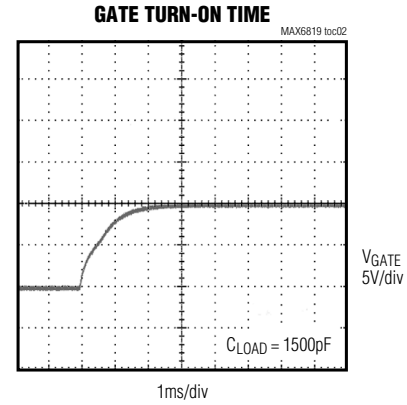
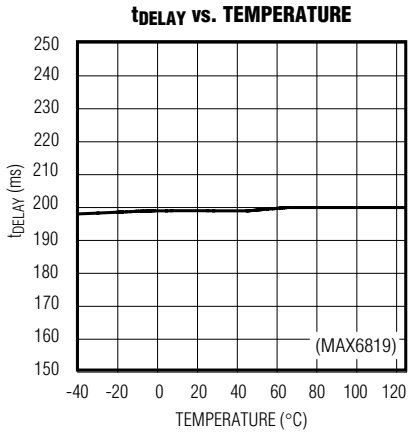
**Note 4:** t<sub>DELAY</sub> (s) = 2.48 × 10<sup>6</sup> × C<sub>SET</sub>

# SOT23 Power-Supply Sequencers

## Typical Operating Characteristics

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)

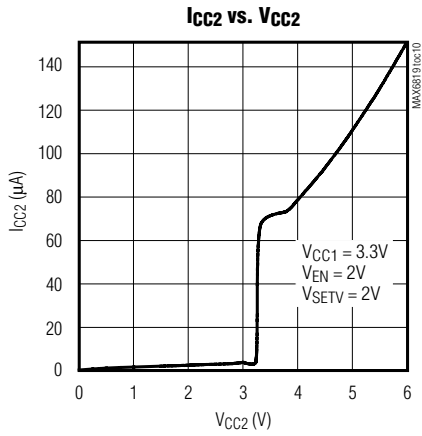
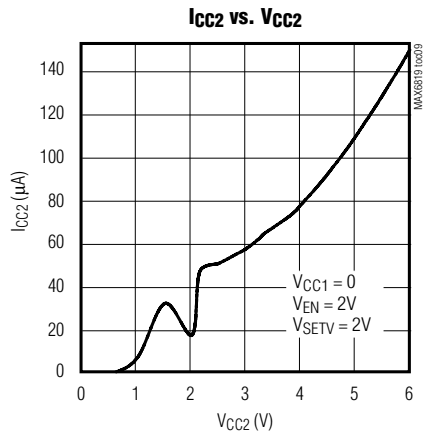
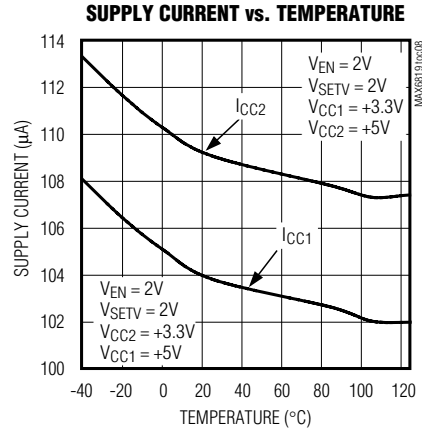
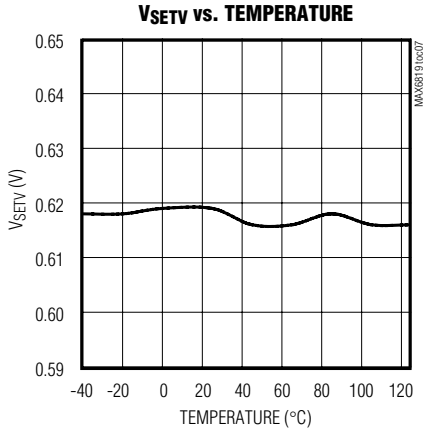
MAX6819/MAX6820



# SOT23 Power-Supply Sequencers

## Typical Operating Characteristics (continued)

( $T_A = +25^\circ\text{C}$ , unless otherwise noted.)



# SOT23 Power-Supply Sequencers

## Pin Description

MAX6819/MAX6820

PIN		NAME	FUNCTION
MAX6819	MAX6820		
1	1	V <sub>CC1</sub>	Supply Voltage 1. Either V <sub>CC1</sub> or V <sub>CC2</sub> must be greater than the UVLO to enable external MOSFET drive.
2	2	GND	Ground
3	3	SETV	Sequence Threshold Set. Connect to an external resistor-divider network to set the V <sub>CC1</sub> threshold that enables GATE turn-on. The internal reference is 0.618V.
4	—	EN	Active-High Enable. GATE drive is enabled t <sub>DELAY</sub> after EN is driven high. GATE drive is immediately disabled when EN is driven low. Connect to the higher of V <sub>CC1</sub> and V <sub>CC2</sub> if not used.
—	4	SETD	GATE Delay Set Input. Connect an external capacitor from SETD to GND to adjust the delay from SETV > V <sub>TH</sub> to GATE turn-on. t <sub>DELAY</sub> (s) = 2.484 × 10 <sup>6</sup> × C <sub>SET</sub> (F).
5	5	GATE	GATE Drive Output. GATE drives an external n-channel MOSFET to connect V <sub>CC2</sub> to the load. GATE drive enables t <sub>DELAY</sub> after SETV exceeds V <sub>TH</sub> and ENABLE is driven high. GATE drive is immediately disabled when SETV drops below V <sub>TH</sub> or ENABLE is driven low. When enabled, an internal charge pump drives GATE to V <sub>CC2</sub> + 5.5V to fully enhance the external n-channel MOSFET.
6	6	V <sub>CC2</sub>	Supply Voltage 2. Either V <sub>CC1</sub> or V <sub>CC2</sub> must be greater than the UVLO to enable external MOSFET drive.

## Detailed Description

Many dual-supply processors or multivoltage boards require one power supply to rise to the proper operating voltage before another supply is applied. Improper sequencing can lead to chip latchup, incorrect device initiation, or long-term reliability degradation. If the various supply voltages are not locally generated (coming from a main system bus, an externally purchased silver box, or a nonsequenced power management chip), power-on and power-off sequencing can be difficult to control or predict. Supply loading can affect turn-on/turn-off times from board to board.

The MAX6819/MAX6820 provide proper local voltage sequencing in multisupply systems. The sequencers use an external n-channel MOSFET to switch the secondary supply to the load only when the primary supply is above a desired operating voltage threshold. The n-channel MOSFET operates in a default off mode when the primary supply is below the desired threshold or if neither supply exceeds the sequencer's UVLO level.

When the primary supply voltage is above the set threshold, the external MOSFET is driven on. An internal charge pump fully enhances the external MOSFET by providing a gate-to-source voltage (V<sub>GS</sub>) of +5.5V (typ). The charge pump fully enhances the MOSFET to yield a low drain-to-source impedance (R<sub>DS(ON)</sub>) for reduced switch voltage drop. The MOSFET is never dri-

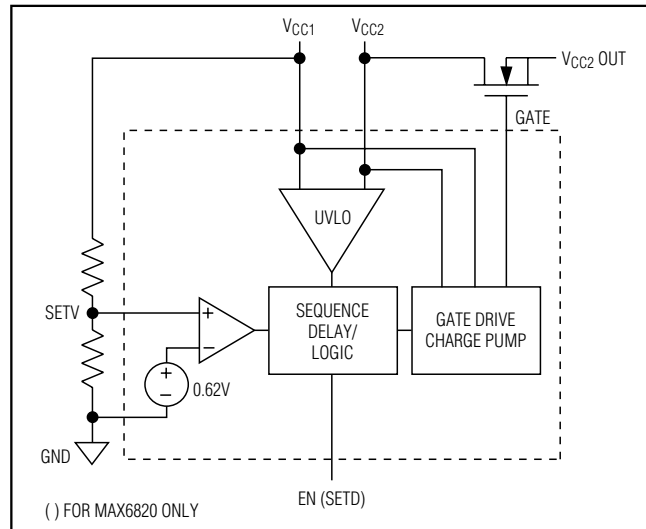


Figure 1. Functional Diagram

ven on unless the sequencer can provide a minimum V<sub>GS</sub> enhancement, ensuring that the switch MOSFET never operates in its higher impedance linear range.

Either supply may act as the primary source, regardless of the voltage level, provided that V<sub>CC1</sub> or V<sub>CC2</sub> is greater than 2.125V (Figure 1 and Figure 2).

# SOT23 Power-Supply Sequencers

## Applications Information

### Adjusting $t_{DELAY}$

The MAX6820 features a capacitor adjustable sequence delay. The adjustable delay provides power sequencing for a wide range of devices with different power-supply delay requirements. Connect a capacitor ( $C_{SET}$ ) between SETD and GND to adjust the delay time (Figure 2). Calculate the sequence delay time as follows:

$$t_{DELAY} (s) = 2.48 \times 10^6 \times C_{SET}$$

### Setting Threshold Voltage at SETV

The threshold voltage is the minimum  $V_{CC1}$  voltage at which  $V_{CC2}$  turn-on is acceptable. To monitor voltages higher than the threshold voltage, connect external resistors as a voltage-divider to SETV, and calculate the minimum  $V_{CC}$  turn-on voltage as follows:

$$R1 = R2 ((V_{TRIP} / V_{TH}) - 1)$$

where  $V_{TRIP}$  is the minimum turn-on voltage at  $V_{CC1}$  and  $V_{TH} = 0.618V$  (Figure 2).

Since SETV input current is 10nA (typ), high value resistors can be used.

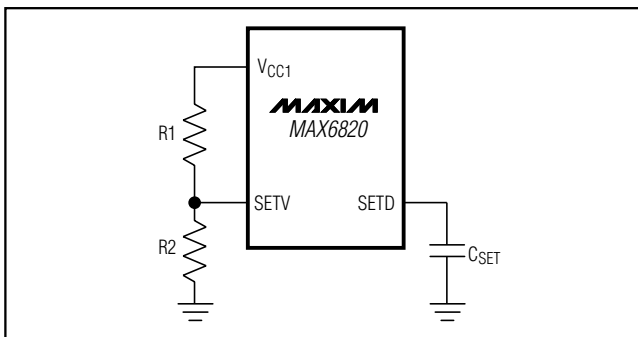


Figure 2.  $t_{DELAY}$  (MAX6820 ONLY) and  $V_{TH}$  Adjust

### Selecting the Pass MOSFET

The external pass MOSFET is connected in series with the sequenced power-supply source. Since the load current and the MOSFET drain-to-source impedance ( $R_{DS}$ ) determine the voltage drop, the on characteristics of the MOSFET affect the load supply accuracy. The MAX6819/MAX6820 fully enhance the external MOSFET out of its linear range to ensure the lowest drain-to-source on impedance. For highest supply accuracy/lowest voltage drop, select a MOSFET with an appropriate drain-to-source on impedance for a gate-to-source bias of 4.5V to 6.0V.

### Gate Drive Characteristics

The MAX6819/MAX6820 internal charge pump drives the n-channel MOSFET with a gate-to-source voltage ( $V_{GS}$ ) of 5.5V, ensuring low MOSFET on-resistance  $R_{DS(ON)}$ . The charge pump drives the high-impedance capacitive load of a MOSFET gate input.

Loading the GATE output resistively adds load current and reduces gate drive capability. The internal charge pump does not require external capacitors.

The external pass MOSFET is disabled, and charge pump circuitry is turned off when neither  $V_{CC1}$  nor  $V_{CC2}$  are above the 1.875V UVLO or EN is low.

### Logic Driven Supply Sequencing

The MAX6819 offers a logic-compatible enable input (EN) that allows digital devices to control sequencing. When the TTL/CMOS-compatible EN input is logic-low, the GATE output is low. When the EN input is logic-high (and SETV is above the monitor threshold), the GATE output is enabled after an internally fixed 200ms delay. For a logic-controlled sequencer when voltage monitoring is not desired, connect SETV to  $V_{CC1}$  or  $V_{CC2} > 0.62V$  (Figure 3).

### Sequencing Three or More Supplies

Cascade multiple MAX6819/MAX6820 to sequence more than two supplies. Daisy-chaining devices allows one sequencer to monitor the passed voltage of an upstream sequencer through the SETV comparator inputs. EN allows any sequencer to be shut down independent of the SETV levels. Figure 4 shows an example of a three-supply system in which the first supply must come up before the second supply and the third supply must yield for both supplies.

### Negative-Going Voltage Transient Immunity

The MAX6819/MAX6820 power-supply voltage sequencers are relatively immune to short-duration (pulse width), negative-going voltage transients (Figure 5). However, the amplitude of the transient is inversely proportional to its pulse width.

## Chip Information

TRANSISTOR COUNT: 638

PROCESS: BiCMOS

# SOT23 Power-Supply Sequencers

MAX6819/MAX6820

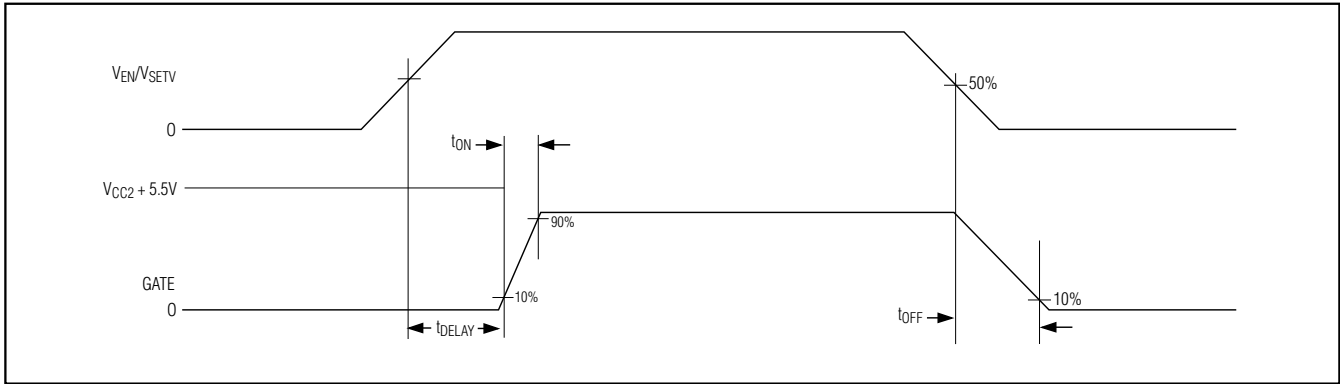


Figure 3. Timing Diagram

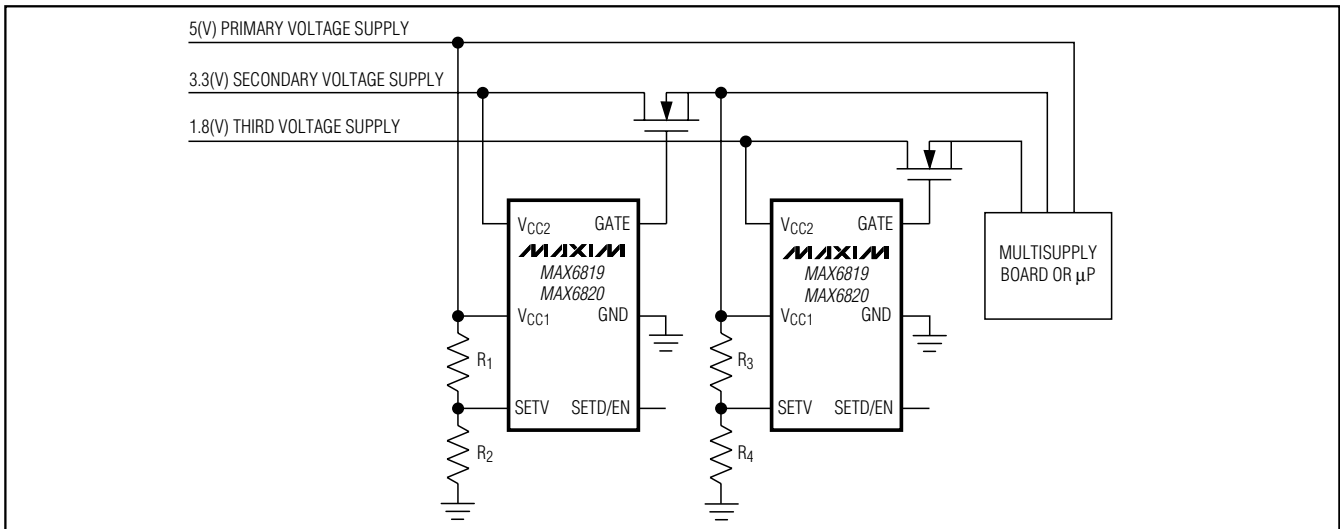


Figure 4. Sequencing Three Power Supplies

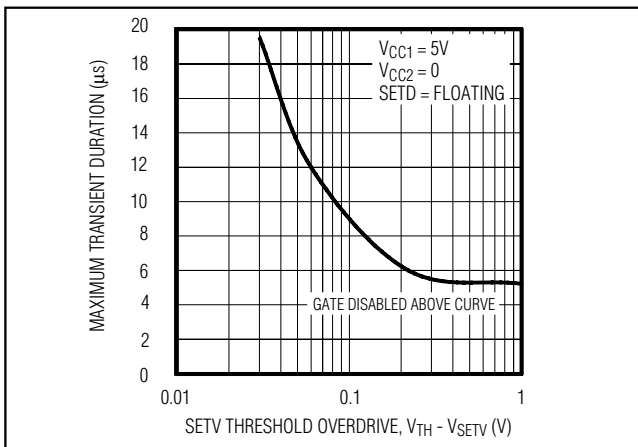
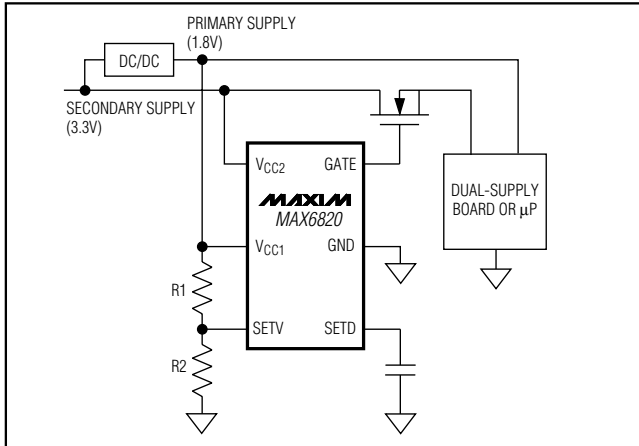


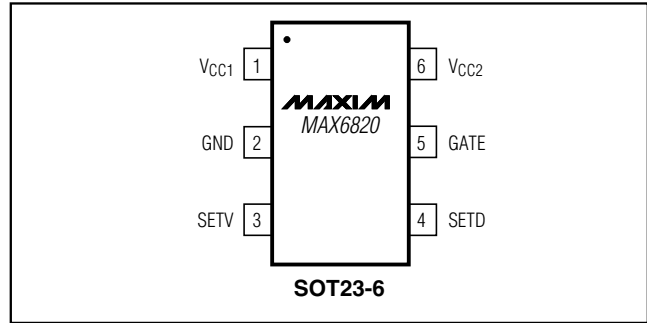
Figure 5. Maximum Transient Duration vs. SETV Threshold in Overdrive

# SOT23 Power-Supply Sequencers

## Typical Operating Circuits (continued)



## Pin Configurations (continued)



## Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to [www.maxim-ic.com/packages](http://www.maxim-ic.com/packages).)

SEE NOTE 5  
EXAMPLE  
TOP MARK

PIN 1  
I.D. DOT  
(SEE NOTE 6)

PIN #1

SYMBOL	MIN	MAX
A	0.90	1.45
A1	0.00	0.15
A2	0.90	1.30
b	0.35	0.50
C	0.08	0.20
D	2.80	3.00
E	2.60	3.00
E1	1.50	1.75
L	0.35	0.60
L1	0.60	REF.
e1	1.90	BSC.
e	0.95	BSC.
alpha	0°	10°

NOTES:  
 1. ALL DIMENSIONS ARE IN MILLIMETERS.  
 2. FOOT LENGTH MEASURED AT INTERCEPT POINT BETWEEN DATUM A & LEAD SURFACE.  
 3. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASH & METAL BURR. MOLD FLASH, PROTRUSION OR METAL BURR SHOULD NOT EXCEED 0.25 MM.  
 4. PACKAGE OUTLINE INCLUSIVE OF SOLDER PLATING.  
 5. PIN 1 IS LOWER LEFT PIN WHEN READING TOP MARK.  
 6. PIN 1 I.D. DOT IS 0.3 MM Ø MIN. LOCATED ABOVE PIN 1.  
 7. MEETS JEDEC MOL78, VARIATION A3.  
 8. SOLDER THICKNESS MEASURED AT FLAT SECTION OF LEAD BETWEEN 0.08mm AND 0.15mm FROM LEADTIP.  
 9. LEAD TO BE COPLANAR WITHIN 0.1 MM.

6LSOT23EFS

-DRAWING NOT TO SCALE-

TITLE: PACKAGE OUTLINE, SOT 6L BODY

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