ANALOG DEVICES

Low Distortion Ultrahigh Speed Differential ADC Driver

Preliminary Technical Data

ADA4960-1

FEATURES

Adjustable output common-mode voltage
Externally adjustable gain
–3 dB bandwidth of 3GHz, (all gains)
Low harmonic distortion (H2/H3 SE->DIFF)
- **-77/-67 dBc @ 250 MHz**
- **-69/-63 dBc @ 500 MHz**
- **-52/-63 dBc @ 1GHz**

IMD3 @ 1GHz = 67dBc
Slew rate 8000 V/µs
Fast overdrive recovery of 1 ns
Low input voltage noise of 3.6 nV/√Hz
Low power dissipation: 60 mA quiescent current
0.1 dB gain flatness to TBD MHz
Available in 16-Lead and 24-Lead LFSCP packages

APPLICATIONS

ADC drivers for giga-sample ADCs
Single-ended-to-differential converters
RF/IF gain block
Line drivers
Oscilloscopes
Satellite Communications
Data Acquisition
Electronic Surveillance and Countermeasures

PIN CONFIGURATION

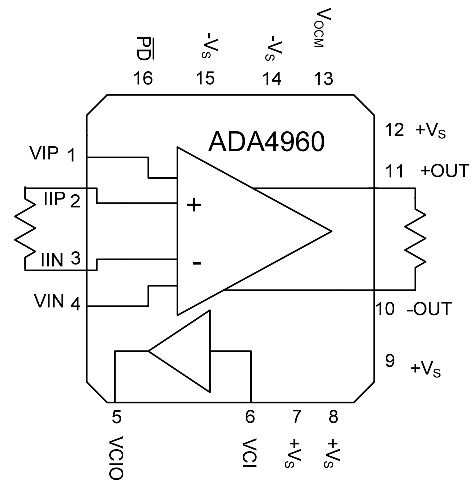

Figure 1.

GENERAL DESCRIPTION

The ADA4960-1 is a high performance differential amplifier optimized for RF and IF applications. It achieves better than 63dB SFDR performance at frequencies up to 500 MHz, and 52dB up to 1GHz, making it an ideal driver for high speed 8-bit to 10-bit giga-sample analog-to-digital converters (ADCs).

Unlike other wideband differential amplifiers, the ADA4960-1 has buffered inputs that isolate the gain-setting resistor (RG) from the signal inputs. As a result, the ADA4960-1 maintains a constant 10 kΩ differential input resistance for gains of 6 dB to 15 dB, easing matching and input drive requirements. The ADA4960-1 has a nominal 150 Ω differential output resistance.

The device is optimized for wideband, low distortion performance at frequencies up to and beyond 1 GHz. These attributes, together with its wide gain adjust capability make this device the amplifier of choice for general-purpose IF and broadband applications where low distortion, noise, and power are critical.

The device also includes a unity gain buffer, for the buffering of DC signals such as the common-mode-input to the amplifier. This buffer is found between pins 6 (input) and pin5 (output). If this buffer is not used, the output can be left disconnected and the input can be grounded.

It is ideally suited for driving not only ADCs, but also mixers, pin diode attenuators, SAW filters, and multi-element discrete devices, as well as buffering high frequency DACs. The device will be available in a single channel version in 3 mm ×3 mm, 16-lead LFCSP package or a dual channel version in 4 mm x 4 mm, 24-lead LFSCP. The device operates over a temperature range of –40°C to +105°C.

Rev. PrB

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

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REVISION HISTORY

12/09—Revision PrA: Preliminary Version

SPECIFICATIONS

V_S = +5V, V_{OCM} = +2.5V, $R_{L,\,dm}$ = 100Ω, @ 25°C, unless otherwise noted. T_{MIN} to T_{MAX} = −40°C to +105°C.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
DIFFERENTIAL INPUT PERFORMANCE					
DYNAMIC PERFORMANCE					
−3 dB Small Signal Bandwidth	$V_{O,\,dm}$ = 0.1 V p-p		3000		MHz
Bandwidth for 0.1 dB Flatness	$V_{O,\,dm}$ = 0.1 V p-p				MHz
Slew Rate	$V_{O,\,dm}$ = 2 V Step		8000		V/μs
Settling Time to 0.1%	$V_{O,\,dm}$ = 2 V Step				ns
Overdrive Recovery Time	G = 2, $V_{IN,\,dm}$ = 7 V p-p Triangle Wave				ns
NOISE/HARMONIC PERFORMANCE					
H2/H3 (Av = 12dB) SE->DIFF	$V_{O,\,dm}$ = 1 V p-p, f_C = 250 MHz		-77/-67		dBc
	$V_{O,\,dm}$ = 1 V p-p, f_C = 500 MHz		-69/63		dBc
	$V_{O,\,dm}$ = 1 V p-p, f_C = 1000 MHz		-52/-63		dBc
H2/H3 (Av= 12dB) DIFF->DIFF	$V_{O,\,dm}$ = 1 V p-p, f_C = 250 MHz		-80/-67		dBc
	$V_{O,\,dm}$ = 1 V p-p, f_C = 500 MHz		-70/-63		dBc
	$V_{O,\,dm}$ = 1 V p-p, f_C = 1000 MHz		-58/-69		dBc
Third-Order IMD	$V_{O,\,dm}$ = 1 V p-p, f_C = 1005 MHz ± 0.05 MHz		67		dBc
Input Voltage Noise	f = 100 kHz		3.6		nV/√Hz
Input Current Noise	f = 100 kHz		3		pA/√Hz
DC PERFORMANCE					
Input Offset Voltage	V_{IP} = V_{IN} = V_{OCM} =0 V				μV
Input Offset Voltage Drift	T_{MIN} to T_{MAX}				μV/ºC
Input Bias Current	T_{MIN} to T_{MAX}				μA
Input Offset Current					μA
Open-Loop Gain					dB
INPUT CHARACTERISTICS					
Input Common-Mode Voltage Range		Vs/2-0.25	Vs/2	Vs/2+ 0.25	V
Input Resistance	Differential (DC≤ Fin ≤ 1GHz)		10		KΩ
	Common-Mode				MΩ
Input Capacitance	Common-Mode				pF
CMRR	ΔV_{ICM} = ±1 V dc				dB
OUTPUT CHARACTERISTICS					
Output Voltage Swing			3.5		V pk-pk Differential
	Each Single-Ended Output, $R_{L,\,dm}$ = Open Circuit				V
Output Impedance	Each Single-Ended Output		150		Ω
V_{OCM} to $V_{O,\,cm}$ PERFORMANCE					
V_{OCM} DYNAMIC PERFORMANCE					
−3 dB Bandwidth	$V_{O,\,cm}$ = 0.1 V p-p				MHz
Slew Rate	$V_{O,\,cm}$ = 2 V p-p				V/μs
Gain					V/V
V_{OCM} INPUT CHARACTERISTICS					
Input Voltage Range					V
Input Resistance					MΩ
Input Offset Voltage	$V_{OS,\,cm}$ = $V_{O,\,cm}$ − V_{OCM}; V_{IP} = V_{IN} = V_{OCM} = 2.5 V				mV
Input Voltage Noise	f = 100 KHz				nV/√Hz
Input Bias Current					μA
CMRR	$\Delta V_{OCM}/\Delta V_O$(dm), ΔV_{OCM} = ±1 V				dB

Parameter	Conditions	Min	Typ	Max	Unit
POWER SUPPLY					
Operating Range			5		V
Quiescent Current			60		mA
+PSRR	Change in $+V_S = \pm1$ V				dB
−PSRR	Change in $-V_S = \pm1$ V				dB
OPERATING TEMPERATURE RANGE		−40		+105	°C

PIN CONFIGURATION AND FUNCTION DESCRIPTION

TBD

Figure 2. Pin Configuration

Table 2. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VIP	Balanced Differential Input. Biased to VCOM.
2	IIP	Gain setting input, positive side. A resistor from this pin to pin 3 sets the gain for the device.
3	IIN	Gain setting input, negative side. A resistor from this pin to pin 3 sets the gain for the device..
4	VIN	Balanced Differential Input. Biased to VCOM.
5	VCIO	Common Mode buffer output.
6	VCI	Common Mode buffer input
7, 8, 9, 12	+Vs	Positive Supply.
10	VON	Balanced Differential Output. Biased to VCOM, typically ac-coupled.
11	VOP	Balanced Differential Output. Biased to VCOM, typically ac-coupled.
13	VC0M	Common-Mode Voltage. A voltage applied to this pin sets the common-mode voltage of the input and output. Typically decoupled to ground with a 0.1 μF capacitor. With no reference applied, input and output common mode floats to midsupply (VCC/2).
16	PD	Enable. Apply positive voltage (1.3 V < ENB < VCC) to activate device.
13, 14, 15, 16	GND	Ground. Connect to low impedance GND.

OUTLINE DIMENSIONS

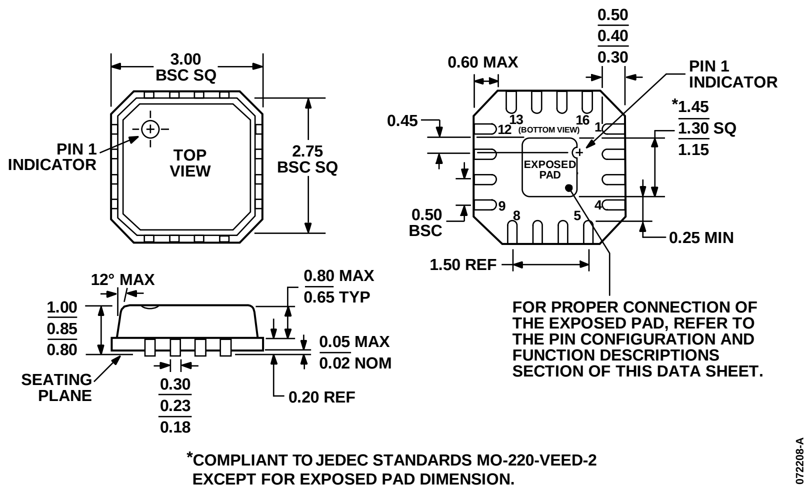

Figure 3. 16-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
3 mm × 3 mm Body, Very Thin Quad (CP-16-2)
Dimensions shown in millimeters