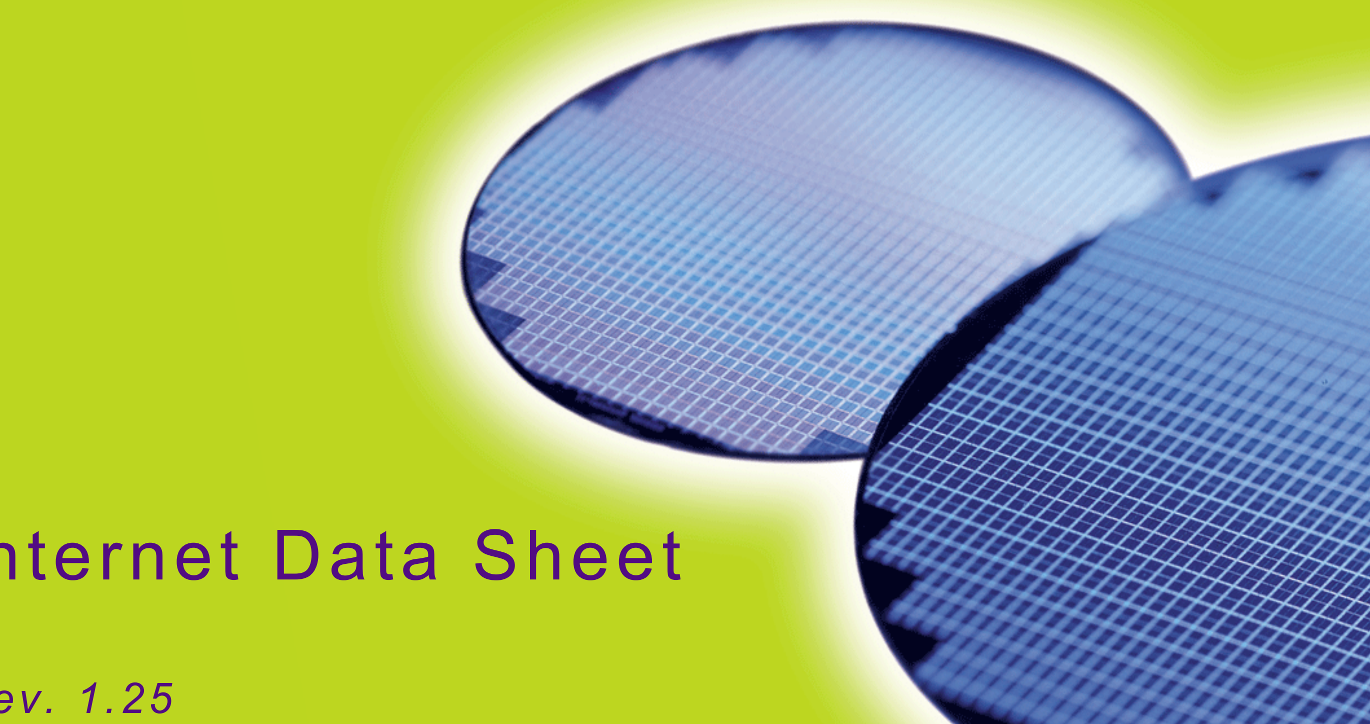
June 2007

HYB39SC256[80/16]0FE
HYI39SC256[80/16]0FF

256-MBit Synchronous DRAM
Green Product
SDRAM



Internet Data Sheet

Rev. 1.25

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HYB39SC256[80/16]0FE, HYI39SC256[80/16]0FF

Revision History: 2007-06, Rev. 1.25

Page	Subjects (major changes since last revision)
All	Adapted internet edition
41	Corrected in figure 28 (auto refresh) tRC to tRFC
Previous Revision: 2007-06, Rev. 1.24	
8	Corrected figure 1
11,12	Corrected block diagram
Previous Revision: 2007-06, Rev. 1.23	
18	Added text for Auto Refresh Command (CBR)
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6	Corrected ball DQ0 to 2,8A for data signals x16 organization
6	Corrected data Data Signal Bus [7:0] for data signals x8 organization
Previous Revision: 2007-06, Rev. 1.21	
13	Corrected operation command "Power Down / Clock suspend ...” in truth table
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13	Corrected operation command "Power Down Exit" to X (WE#)
15	Corrected text to "After the mode register is set a NOP command is required" , chapter 3.2
19	Corrected text to "One clock delay is required for mode entry and exit", chapter 3.4
21	Corrected the line "Input Capacitances: CK" in table 10, chapter 4
21	Corrected to A0-A12 in table 10, chapter 4
22	Corrected tCK MIN in table 13
22	Corrected CLE setup time in table 13
Previous Revision: 2007-05, Rev. 1.11	
6	Corrected A6 position from H to 3H in table 3
Previous Revision: 2006-09, Rev. 1.1	

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1 Overview

This chapter lists all main features of the product family HY[B/I]39SC256[80/16]0F[E/F] and the ordering information.

1.1 Features

- Fully Synchronous to Positive Clock Edge
- 0 to 70 °C Operating Temperature for HYB...
- -40 to 85 °C Operating Temperature for HYI...
- Four Banks controlled by BA0 & BA1
- Programmable CAS Latency: 2 & 3
- Programmable Wrap Sequence: Sequential or Interleave
- Programmable Burst Length: 1, 2, 4, 8 and full page
- Multiple Burst Read with Single Write Operation
- Automatic and Controlled Precharge Command
- Data Mask for Read / Write control (x8, x16)
- Data Mask for Byte Control (x16)
- Auto Refresh (CBR) and Self Refresh
- Power Down and Clock Suspend Mode
- 8192 refresh cycles / 64 ms (7.8 µs)
- Random Column Address every CLK (1-N Rule)
- Single 3.3 V ± 0.3 V Power Supply
- LVTTL Interface
- Plastic Packages
  – PG-TSOPII-54 (400mil width)
  – PG-TFBGA-54 (12 mm x 8 mm)
- RoHS compliant product

TABLE 1
Performance

Product Type Speed Code			**–6**	**–7**	**Unit**
Speed Grade			PC166–333	PC143–333 PC133–222[1)]	—
Max. Clock Frequency	@CL3	f_{CK3}	166	143	MHz
		t_{CK3}	6	7	ns
		t_{AC3}	5.4	5.4	ns
	@CL2	t_{CK2}	7.5	7.5	ns
		t_{AC2}	5.4	5.4	ns

1) Max. Frequency CL/t_{RCD} / t_{RP}

1.2 Description

The HY[B/I]39SC256[80/16]0F[E/F] are four bank Synchronous DRAM's organized as 16 MBit ×8 and 8 Mbit x16 respectively. These synchronous devices achieve high speed data transfer rates for CAS latencies by employing a chip architecture that prefetches multiple bits and then synchronizes the output data to a system clock. The chip is fabricated with Qimonda advanced 0.11 μm 256-MBit DRAM process technology.

The device is designed to comply with all industry standards set for synchronous DRAM products, both electrically and mechanically. All of the control, address, data input and output circuits are synchronized with the positive edge of an externally supplied clock.

Operating the four memory banks in an interleave fashion allows random access operation to occur at a higher rate than is possible with standard DRAMs. A sequential and gapless data rate is possible depending on burst length, CAS latency and speed grade of the device.

Auto Refresh (CBR) and Self Refresh operation are supported. These devices operate with a single 3.3 V ± 0.3 V power supply. All 256-Mbit components are available in PG–TSOPII–54 and PG-TFBGA-54 packages.

TABLE 2
Ordering Information for RoHS Compliant Products

Product Type[1]	Speed Grade	Description	Package	Note
Standard Operating Temperature (0 to 70 °C)				
HYB39SC256800FE-6	PC166–333	166MHz 16M ×8 SDRAM	PG-TSOPII-54	2)
HYB39SC256160FE-6		166MHz 8M ×16 SDRAM		
HYB39SC256800FE-7	PC133–222	143MHz 16M ×8 SDRAM		
HYB39SC256800FEH-7				
HYB39SC256160FE-7		143MHz 8M ×16 SDRAM		
HYB39SC256160FEH-7				
HYB39SC256160FF-6	PC166–333	166MHz 8M ×16 SDRAM	PG-TFBGA-54	2)
HYB39SC256160FF-7	PC133–222	143MHz 8M ×16 SDRAM		
HYB39SC256800FF-7		143MHz 8M ×8SDRAM		
Industrial Operating Temperature (-40 to 85 °C)				
HYI39SC256800FE-6	PC166–333	166MHz 16M ×8 SDRAM	PG-TSOPII-54	2)
HYI39SC256160FE-6		166MHz 8M ×16 SDRAM		
HYI39SC256800FE-7	PC133–222	143MHz 16M ×8 SDRAM		
HYI39SC256160FE-7		143MHz 8M ×16 SDRAM		

1) Please check with your Qimonda representative that leadtime and availability of your preferred device and version meet your project requirements.
2) RoHS Compliant Product: Restriction of the use of certain hazardous substances (RoHS) in electrical and electronic equipment as defined in the directive 2002/95/EC issued by the European Parliament and of the Council of 27 January 2003. These substances include mercury, lead, cadmium, hexavalent chromium, polybrominated biphenyls and polybrominated biphenyl ethers.

Note: For product nomenclature see ***Chapter 6*** *of this data sheet*

2 Configuration

This chapter contains the pin configuration table, the TSOP and FBGA package drawing, and the block diagrams for the ×8, ×16 organization of the SDRAM.

2.1 Pin Configuration

Listed below are the pin configurations sections for the various signals of the SDRAM

TABLE 3
Pin Configuration of the SDRAM

Pin No.	Name	Pin Type	Buffer Type	Function
Clock Signals x8/x16 Organization				
38,2F	CLK	I	LVTTL	**Clock Signal CK**
37,3F	CKE	I	LVTTL	**Clock Enable**
Control Signals x8/x16 Organization				
18, 8F	$\overline{RAS}$	I	LVTTL	**Row Address Strobe (RAS), Column Address Strobe (CAS), Write Enable (WE)**
17, 7F	$\overline{CAS}$	I	LVTTL	
16, 9F	$\overline{WE}$	I	LVTTL	
19, 9G	$\overline{CS}$	I	LVTTL	**Chip Select**
Address Signals x8/x16 Organization				
20, 7G	BA0	I	LVTTL	**Bank Address Signals 1:0**
21, 8G	BA1	I	LVTTL	
23, 7H	A0	I	LVTTL	**Address Signal, Address Signal 10/Auto precharge**
24, 8H	A1	I	LVTTL	
25, 8J	A2	I	LVTTL	
26, 7J	A3	I	LVTTL	
29, 3J	A4	I	LVTTL	
30, 2J	A5	I	LVTTL	
31, 3H	A6	I	LVTTL	
32, 2H	A7	I	LVTTL	
33, 1H	A8	I	LVTTL	
34, 3G	A9	I	LVTTL	
22, 9H	A10	I	LVTTL	
35, 2G	A11	I	LVTTL	
36, 1G	A12	I	LVTTL	

Pin No.	Name	Pin Type	Buffer Type	Function
Data Signals x8 Organization				
2, 8A	DQ0	I/O	LVTTL	**Data Signal Bus [7:0]**
5, 8B	DQ1	I/O	LVTTL	
8, 8C	DQ2	I/O	LVTTL	
11, 8D	DQ3	I/O	LVTTL	
44, 2D	DQ4	I/O	LVTTL	
47, 2C	DQ5	I/O	LVTTL	
50, 2B	DQ6	I/O	LVTTL	
53, 2A	DQ7	I/O	LVTTL	
Data Signals x16 Organization				
2, 8A	DQ0	I/O	LVTTL	**Data Signal Bus [15:0]**
4, 9B	DQ1	I/O	LVTTL	
5, 8B	DQ2	I/O	LVTTL	
7, 9C	DQ3	I/O	LVTTL	
8, 8C	DQ4	I/O	LVTTL	
10, 9D	DQ5	I/O	LVTTL	
11, 8D	DQ6	I/O	LVTTL	
13, 9E	DQ7	I/O	LVTTL	
42, 1E	DQ8	I/O	LVTTL	
44, 2D	DQ9	I/O	LVTTL	
45, 1D	DQ10	I/O	LVTTL	
47, 2C	DQ11	I/O	LVTTL	
48, 1C	DQ12	I/O	LVTTL	
50, 2B	DQ13	I/O	LVTTL	
51, 1B	DQ14	I/O	LVTTL	
53, 2A	DQ15	I/O	LVTTL	
Data Mask x8 Organization				
39, 1F	DQM	I/O	LVTTL	**Data Mask**
Data Mask x16 Organization				
39, 1F	UDQM	I/O	LVTTL	**Data Mask Upper Byte**
15, 8E	LDQM	I/O	LVTTL	**Data Mask Lower Byte**
Power Supplies x8/x16 Organization				
3B, 3D, 7A, 7C	VDDQ	PWR	—	**Power Supply**
7E, 9A, 9J	VDD	PWR	—	**Power Supply**
3A, 3C, 7B, 7D	VSSQ	PWR	—	**Power Supply Ground for DQs**
1J, 1A, 3E	VSS	PWR	—	**Power Supply Ground**

Pin No.	Name	Pin Type	Buffer Type	Function
Not connected x8 Organization				
7, 10, 13, 15, 40, 42, 45, 48, 51, 1B, 1C, 1D, 1E, 2E, 8E, 9B, 9C, 9D, 9E	NC	NC	—	**Not connected**
Not connected x16 Organization				
40, 2E	NC	NC	—	**Not connected**

FIGURE 1
Pin Configuration PG–TSOPII–54

x16	x8	Pin	Pin	x8	x16
V_{DD}	V_{DD}	1	54	V_{SS}	V_{SS}
DQ0	DQ0	2	53	DQ7	DQ15
V_{DDQ}	V_{DDQ}	3	52	V_{SSQ}	V_{SSQ}
DQ1	N.C.	4	51	N.C.	DQ14
DQ2	DQ1	5	50	DQ6	DQ13
V_{SSQ}	V_{SSQ}	6	49	V_{DDQ}	V_{DDQ}
DQ3	N.C.	7	48	N.C.	DQ12
DQ4	DQ2	8	47	DQ5	DQ11
V_{DDQ}	V_{DDQ}	9	46	V_{SSQ}	V_{SSQ}
DQ5	N.C.	10	45	N.C.	DQ10
DQ6	DQ3	11	44	DQ4	DQ9
V_{SSQ}	V_{SSQ}	12	43	V_{DDQ}	V_{DDQ}
DQ7	N.C.	13	42	N.C.	DQ8
V_{DD}	V_{DD}	14	41	V_{SS}	V_{SS}
LDQM	N.C.	15	40	N.C.	N.C.
WE	WE	16	39	DQM	UDQM
CAS	CAS	17	38	CLK	CLK
RAS	RAS	18	37	CKE	CKE
CS	CS	19	36	A12	A12
BA0	BA0	20	35	A11	A11
BA1	BA1	21	34	A9	A9
A10/AP	A10/AP	22	33	A8	A8
A0	A0	23	32	A7	A7
A1	A1	24	31	A6	A6
A2	A2	25	30	A5	A5
A3	A3	26	29	A4	A4
V_{DD}	V_{DD}	27	28	V_{SS}	V_{SS}

TSOPII-54 (400 mil x 875 mil, 0.8 mm pitch)

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FIGURE 2

Ballout for ×16 Components, PG-TFBGA-54 (top view)

	1	2	3	4	5	6	7	8	9
A	V_{SS}	DQ15	V_{SSQ}		A		V_{DDQ}	DQ0	V_{DD}
B	DQ14	DQ13	V_{DDQ}		B		V_{SSQ}	DQ2	DQ1
C	DQ12	DQ11	V_{SSQ}		C		V_{DDQ}	DQ4	DQ3
D	DQ10	DQ9	V_{DDQ}		D		V_{SSQ}	DQ6	DQ5
E	DQ8	NC	V_{SS}		E		V_{DD}	LDQM	DQ7
F	UDQM	CLK	CKE		F		$\overline{CAS}$	$\overline{RAS}$	$\overline{WE}$
G	A12	A11	A9		G		BA0	BA1	$\overline{CS}$
H	A8	A7	A6		H		A0	A1	A10
J	V_{SS}	A5	A4		J		A3	A2	V_{DD}

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FIGURE 3
Ballout for ×8 components, PG-TFBGA-54 (top view)

	1	2	3	4	5	6	7	8	9
A	V_{SS}	DQ7	V_{SSQ}				V_{DDQ}	DQ0	V_{DD}
B	NC	DQ6	V_{DDQ}				V_{SSQ}	DQ1	NC
C	NC	DQ5	V_{SSQ}				V_{DDQ}	DQ2	NC
D	NC	DQ4	V_{DDQ}				V_{SSQ}	DQ3	NC
E	NC	NC	V_{SS}				V_{DD}	NC	NC
F	DQM	CLK	CKE				$\overline{CAS}$	$\overline{RAS}$	$\overline{WE}$
G	A12	A11	A9				BA0	BA1	$\overline{CS}$
H	A8	A7	A6				A0	A1	A10
J	V_{SS}	A5	A4				A3	A2	V_{DD}

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3 Functional Description

This chapter lists all defined commands and their usage for this Synchronous DRAM.

TABLE 4
Truth Table: Operation Command

Operation	Device State	CKE n-1[1][2]	CKE n[1][2]	DQM[1][2]	BA0 BA1[1][2]	AP= A10[1][2]	Addr.[1][2]	$\overline{CS}$[1][2]	$\overline{RAS}$[1][2]	$\overline{CAS}$[1][2]	$\overline{WE}$[1][2]
Bank Active	Idle[3]	H	X	X	V	V	V	L	L	H	H
Bank Precharge	Any	H	X	X	V	L	X	L	L	H	L
Precharge All	Any	H	X	X	X	H	X	L	L	H	L
Write	Active[3]	H	X	X	V	L	V	L	H	L	L
Write with Auto precharge	Active[3]	H	X	X	V	H	V	L	H	L	L
Read	Active[3]	H	X	X	V	L	V	L	H	L	H
Read with Auto precharge	Active[3]	H	X	X	V	H	V	L	H	L	H
Mode Register Set	Idle	H	X	X	V	V	V	L	L	L	L
No Operation	Any	H	X	X	X	X	X	L	H	H	H
Burst Stop	Active	H	X	X	X	X	X	L	H	H	L
Device Deselect	Any	H	X	X	X	X	X	H	X	X	X
Auto Refresh	Idle	H	H	X	X	X	X	L	L	L	H
Self Refresh Entry	Idle	H	L	X	X	X	X	L	L	L	H
Self Refresh Exit	Idle (Self Refr.)	L	H	X	X	X	X	H	X	X	X
								L	H	H	X
Power Down/ Clock Suspend Entry	Active or Idle or Burst	H	L	X	X	X	X	H	X	X	X
								L	H	H	H
Power Down/ Clock Suspend Exit	Active or Idle or Burst	L	H	X	X	X	X	H	X	X	X
								L	H	H	H
Data Write/ Output Enable	Active	H	X	L	X	X	X	X	X	X	X
Data Write/ Output Disable	Active	H	X	H	X	X	X	X	X	X	X

1) V = Valid, x = Don’t Care, L = Low Level, H = High Level
2) CKEn signal is input level when commands are provided, CKEn-1 signal is input level one clock before the commands are provided.
3) This is the state of the banks designated by BA0, BA1 signals.

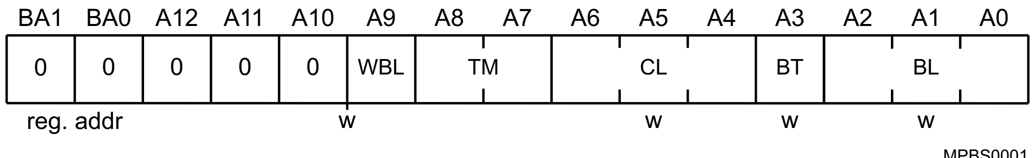

TABLE 5
Mode Register Definition (BA[1:0] = 00_B)

Field	Bits	Type	Description
BL	[2:0]	w	**Burst Length** Number of sequential bits per DQ related to one read/write command, see **Table 6** *Note: All other bit combinations are RESERVED* 000_B **1** 001_B **2** 010_B **4** 011_B **8** 111_B **Full Page (Sequential burst type only)**
BT	3		**Burst Type** 0_B **Sequential** 1_B **Interleaved**
CL	[6:4]		**CAS Latency** Number of full clocks from read command to first data valid window. *Note: All other bit combinations are RESERVED.* 010_B **2** 011_B **3**
TM	[8:7]		**Test Mode** *Note: All other bit combinations are RESERVED.* 00_B **Mode register set**
WBL	9		**Write Burst Length** 0_B **Burst write** 1_B **Single bit write**
	[12:10]		Reserved, set to zero

TABLE 6
Burst Length and Sequence

Burst Length	Starting Column Address			Order of Accesses Within a Burst	
	A2	A1	A0	Type=Sequential	Type=Interleaved
2			0	0–1	0–1
			1	1–0	1–0
4		0	0	0–1–2–3	0–1–2–3
		0	1	1–2–3–0	1–0–3–2
		1	0	2–3–0–1	2–3–0–1
		1	1	3–0–1–2	3–2–1–0
8	0	0	0	0–1–2–3–4–5–6–7	0–1–2–3–4–5–6–7
	0	0	1	1–2–3–4–5–6–7–0	1–0–3–2–5–4–7–6
	0	1	0	2–3–4–5–6–7–0–1	2–3–0–1–6–7–4–5
	0	1	1	3–4–5–6–7–0–1–2	3–2–1–0–7–6–5–4
	1	0	0	4–5–6–7–0–1–2–3	4–5–6–7–0–1–2–3
	1	0	1	5–6–7–0–1–2–3–4	5–4–7–6–1–0–3–2
	1	1	0	6–7–0–1–2–3–4–5	6–7–4–5–2–3–0–1
	1	1	1	7–0–1–2–3–4–5–6	7–6–5–4–3–2–1–0
FullPage	n			Cn, Cn+1, Cn+2	Not supported

Notes

1. *For a burst length of two, A1-Ai selects the two-data-element block; A0 selects the first access within the block.*
2. *For a burst length of four, A2-Ai selects the four-data-element block; A0-A1 selects the first access within the block.*
3. *For a burst length of eight, A3-Ai selects the eight-data- element block; A0-A2 selects the first access with in the block.*
4. *Whenever a boundary of the block is reached within a given sequence above, the following access wraps within the block.*

4 Electrical Characteristics

4.1 Operating Conditions

TABLE 7
Absolute Maximum Ratings

Parameter	Symbol	Limit Values		Unit	Note/ Test Condition
		Min.	Max.		
Input / Output voltage relative to V_{SS}	V_{IN}, V_{OUT}	–1.0	+4.6	V	
Voltage on V_{DD} supply relative to V_{SS}	V_{DD}	–1.0	+4.6	V	
Voltage on V_{DDQ} supply relative to V_{SS}	V_{DDQ}	–1.0	+4.6	V	
Operating Temperature for HYB...	T_A	0	+70	°C	
Operating Temperature for HYI...	T_A	-40	+85	°C	
Storage temperature range	T_{STG}	–55	+150	°C	
Power dissipation per SDRAM component	P_D	—	1	W	
Data out current (short circuit)	I_{OUT}	—	50	mA	

***Attention:** Stresses above the max. values listed here may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Maximum ratings are absolute ratings; exceeding only one of these values may cause irreversible damage to the integrated circuit.*

TABLE 8
DC Characteristics

Parameter	Symbol	Values		Unit	Note/ Test Condition
		Min.	Max.		
Supply Voltage	V_{DD}	3.0	3.6	V	1)
I/O Supply Voltage	V_{DDQ}	3.0	3.6	V	1)
Input high voltage	V_{IH}	2.0	V_{DDQ} + 0.3	V	1)2)
Input low voltage	V_{IL}	–0.3	+0.8	V	1)2)
Output high voltage (I_{OUT} = – 4.0 mA)	V_{OH}	2.4	—	V	1)
Output low voltage (I_{OUT} = 4.0 mA)	V_{OL}	—	0.4	V	1)
Input leakage current, any input (0 V < V_{IN} < V_{DD}, all other inputs = 0 V)	I_{IL}	–5	+5	µA	
Output leakage current (DQs are disabled, 0 V < V_{OUT} < V_{DDQ})	I_{OL}	–5	+5	µA	

1) All voltages are referenced to V_{SS}
2) V_{IH} may overshoot to V_{DDQ} + 2.0 V for pulse width of < 4ns with 3.3 V. V_{IL} may undershoot to -2.0 V for pulse width < 4.0 ns with 3.3 V. Pulse width measured at 50% points with amplitude measured peak to DC reference.

TABLE 9
Input and Output Capacitances

Parameter	Symbol	Values		Unit	Note
		Min.	Max.		
Input Capacitances: CK	C_{I1}	2.5	3.5	pF	1)2)
Input Capacitance (A0-A12, BA0, BA1, $\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$, $\overline{CS}$, CKE, DQM)	C_{I2}	2.5	3.8	pF	1)2)
Input/Output Capacitance (DQ)	C_{IO}	4.0	6.0	pF	1)2)

1) V_{DD},V_{DDQ} = 3.3 V ± 0.3 V, f = 1 MHz, T_A see **Table 7**
2) Capacitance values are shown for TSOP-54 packages. Capacitance values for TFBGA packages are lower by 0.5 pF

TABLE 10
I_{DD} Conditions

Parameter		Symbol
Operating Current	One bank active, Burst length = 1	I_{DD1}
Precharge Standby Current	Power down mode	I_{DD2P}
	Non-power down mode	I_{DD2N}
No Operating Current	Active state (max. 4 banks)	I_{DD3N}
		I_{DD3P}
Burst Operating Current	Read command cycling	I_{DD4}
Auto Refresh Current	Auto Refresh command cycling	I_{DD5}
Self Refresh Current	Self Refresh Mode, CKE=0.2 V, t_{CK}=infinity	I_{DD6}

TABLE 11
I_{DD} Specifications and Conditions

Symbol	Test Condition	–6	–7	Unit	Note [1]
I_{DD1}	$t_{RC} = t_{RC(min)}$, I_O = 0 mA	100	80	mA	[2][3]
I_{DD2P}	$\overline{CS} = V_{IH\ (min.)}$, CKE $\leq V_{IL(max)}$	2	2	mA	[1]
I_{DD2N}	$\overline{CS} = V_{IH\ (min.)}$, CKE$\geq V_{IH(min)}$	26	22	mA	[1]
I_{DD3N}	CS = $V_{IH(min)}$, CKE $\geq V_{IH(min.)}$	40	35	mA	[1]
I_{DD3P}	CS = $V_{IH(min)}$, CKE $\leq V_{IL(max.)}$	5	5	mA	[1]
I_{DD4}	—	65	57	mA	[1][3]
I_{DD5}	$t_{RFC} = t_{RFC(min)}$	168	142	mA	[4]
	t_{RFC}= 15.6 µs	25	25	mA	
I_{DD6}	—	3	3	mA	

1) V_{SS} = 0 V; V_{DD}, V_{DDQ} = 3.3 V ± 0.3 V, T_A see **Table 7**
2) These parameters depend on the cycle rate. All values are measured at 133 MHz for -7 with the outputs open. Input signals are changed once during t_{CK}.
3) These parameters are measured with continuous data stream during read access and all DQ toggling. CL=3 and BL=4 is assumed and the V_{DDQ} current is excluded.
4) $t_{RFC} = t_{RFC(min)}$ "burst refresh", t_{RFC}= 15.6 µs "distributed refresh".

4.2 AC Characteristics

TABLE 12
AC Timing - Absolute Specifications

Parameter	Symbol	–7		–6		Unit	Note[1)2)3)]
		PC143–333		PC166–333			
		Min.	Max.	Min.	Max.		
Clock and Clock Enable							
Clock Frequency	t_{CK}	7 7.5	— —	6 7.5	— —	ns ns	CL3 CL2
Access Time from Clock	t_{AC}	— —	5.4 5.4	— —	5.4 5.4	ns ns	CL3 CL2 3)4)5)
Clock High Pulse Width	t_{CH}	2.5	—	2	—	ns	
Clock Low Pulse Width	t_{CL}	2.5	—	2	—	ns	
Transition time	t_{T}	0.3	1.2	0.3	1.2	ns	
Setup and Hold Times							
Input Setup Time	t_{IS}	1.5	—	1.5	—	ns	6)
Input Hold Time	t_{IH}	0.8	—	0.8	—	ns	6)
CKE Setup Time	t_{CKS}	1.5	—	1.5	—	ns	6)
CKE Hold Time	t_{CKH}	0.8	—	0.8	—	ns	6)
Mode Register Set-up to Active delay	t_{RSC}	2	—	2	—	t_{CK}	
Power Down Mode Entry Time	t_{SB}	0	7	0	6	ns	
Common Parameters							
Row to Column Delay Time	t_{RCD}	15	—	15	—	ns	7)
Row Precharge Time	t_{RP}	15	—	15	—	ns	7)
Row Active Time	t_{RAS}	37	100k	36	100k	ns	7)
Row Cycle Time	t_{RC}	60	—	60	—	ns	7)
Row Cycle Time during Auto Refresh	t_{RFC}	63	—	60	—	ns	
Activate(a) to Activate(b) Command period	t_{RRD}	14	—	12	—	ns	7)
$\overline{CAS}$(a) to $\overline{CAS}$(b) Command period	t_{CCD}	1	—	1	—	t_{CK}	
Refresh Cycle							
Refresh Period (8192 cycles)	t_{REF}	–	64	–	64	ms	
Self Refresh Exit Time	t_{SREX}	1	—	1	—	t_{CK}	
Data Out Hold Time	t_{OH}	3	—	2.5	—	ns	3)5)
Read Cycle							
Data Out to Low Impedance Time	t_{LZ}	0	—	0	—	ns	
Data Out to High Impedance Time	t_{HZ}	3	7	3	6	ns	
DQM Data Out Disable Latency	t_{DQZ}	—	2	—	2	t_{CK}	

Parameter	Symbol	–7		–6		Unit	Note[1)2)3)]
		PC143–333		PC166–333			
		Min.	Max.	Min.	Max.		
Write Cycle							
Last Data Input to Precharge (Write without Auto Precharge)	t_{WR}	14	—	12	—	ns	8)
Last Data Input to Activate (Write with Auto Precharge)	$t_{DAL(min.)}$	—	—	—	—	t_{CK}	9)
DQM Write Mask Latency	t_{DQW}	0	—	0	—	t_{CK}	

1) T_A = 0 to 70 °C; V_{SS} = 0 V; V_{DD}, V_{DDQ} = 3.3 V ± 0.3 V, t_T = 1 ns
2) For proper power-up see the operation section of this data sheet.
3) AC timing tests for LV-TTL versions have V_{IL} = 0.4 V and V_{IH} = 2.4 V with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL}. All AC measurements assume t_T = 1 ns with the AC output load circuit shown in figure below. Specified t_{AC} and t_{OH} parameters are measured with a 50 pF only, without any resistive termination and with an input signal of 1V / ns edge rate between 0.8 V and 2.0 V.
4) If clock rising time is longer than 1 ns, a time (t_T/2 - 0.5) ns has to be added to this parameter.
5) Access time from clock t_{ac} is 4.6 ns for PC133 components with no termination and 0 pF load, Data out hold time t_{oh} is 1.8 ns for PC133 components with no termination and 0 pF load.
6) If t_T is longer than 1 ns, a time (t_T - 1) ns has to be added to this parameter.
7) These parameter account for the number of clock cycles and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing period (counted in fractions as a whole number)
8) It is recommended to use two clock cycles between the last data-in and the precharge command in case of a write command without Auto-Precharge. One clock cycle between the last data-in and the precharge command is also supported, but restricted to cycle times t_{CK} greater or equal the specified t_{WR} value, where t_{ck} is equal to the actual system clock time.
9) When a Write command with Auto Precharge has been issued, a time of $t_{DAL(min)}$ has be fullfilled before the next Activate Command can be applied. For each of the terms, if not already an integer, round up to the next highest integer. t_{CK} is equal to the actual system clock time.

FIGURE 4
Measurement conditions for t_{AC} and t_{OH}

5 Package Outlines

FIGURE 5
Package Outline PG-TSOPII-54 (top view)

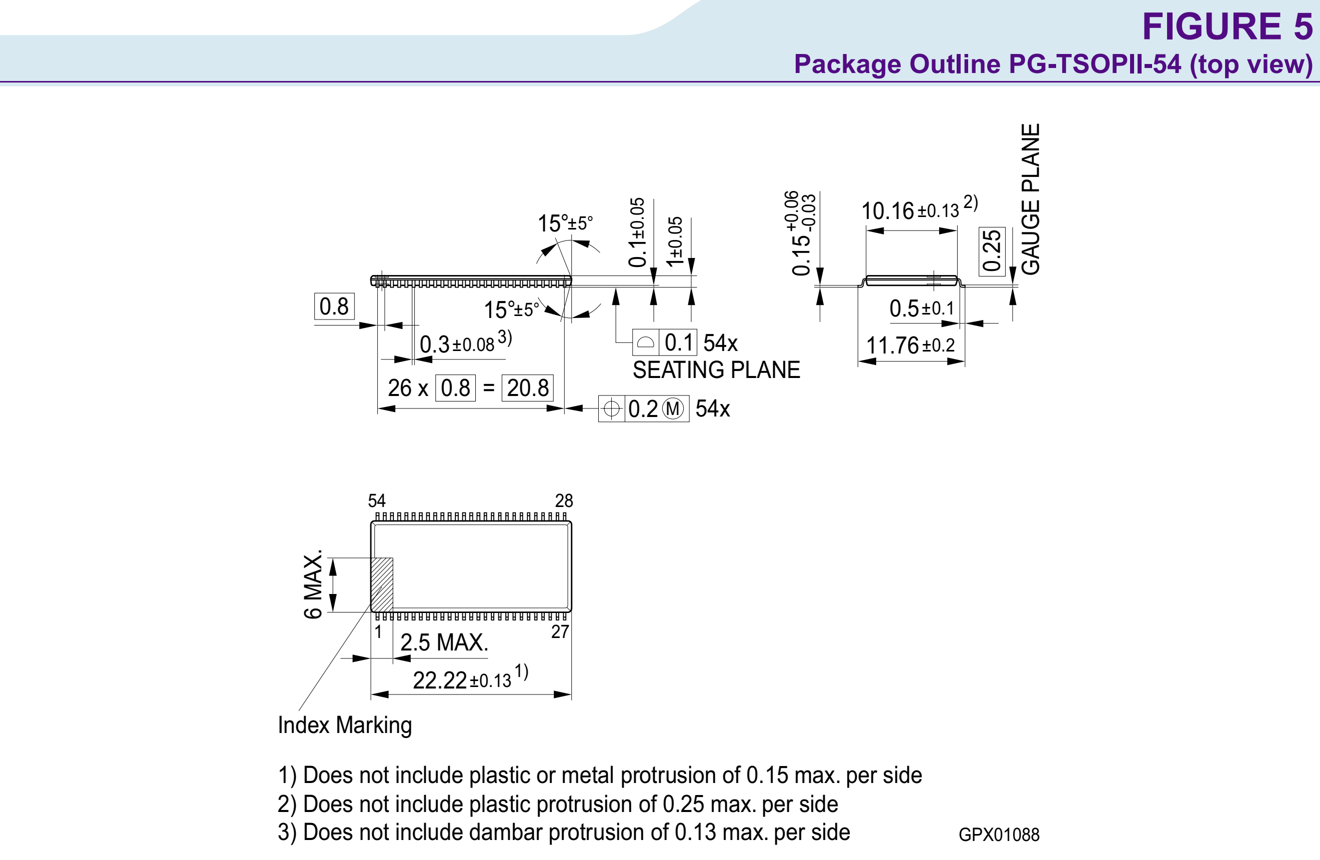

FIGURE 6
Package Outline PG-TFBGA-54-15

Notes

1. *Drawing according to ISO 8015*
2. *Dimensions in mm*
3. *General tolerances +/- 0.15*

6 Product Nomenclature

For reference the Qimonda SDRAM component nomenclature is enclosed in this chapter.

TABLE 13
Examples for Nomenclature Fields

Example for	Field Number										
	1	2	3	4	5	6	7	8	9	10	11
SDRAM	HYB	39	SC	256	80		0	F	F	—	–6
SDRAM	HYI	39	SC	256	16		0	F	E	—	–7

TABLE 14
Memory Components

Field	Description	Values	Coding
1	Qimonda Component Prefix	HYB	Memory components
		HYI	Memory components, industrial temperature range (-40 °C – +85 °C)
2	Interface Voltage [V]	39	3.3 V
3	DRAM Technology	SC	Single Data Rate SDRAM Consumer Product
4	Component Density [Mbit]	128	128 Mbit
		256	256 Mbit
		512	512 Mbit
5+6	Number of I/Os	40	×4
		80	×8
		16	×16
7	Product Variations	0 .. 9	look up table
8	Die Revision	C	Third
		D	Fourth
		F	Fifth
9	Package, Lead-Free Status	E	TSOP, lead- and halogen-free
		F	FBGA, lead- and halogen-free
10	Power	–	Standard power product
11	Speed Grade	–6	PC166-333
		–7	PC143-333, PC133-222

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