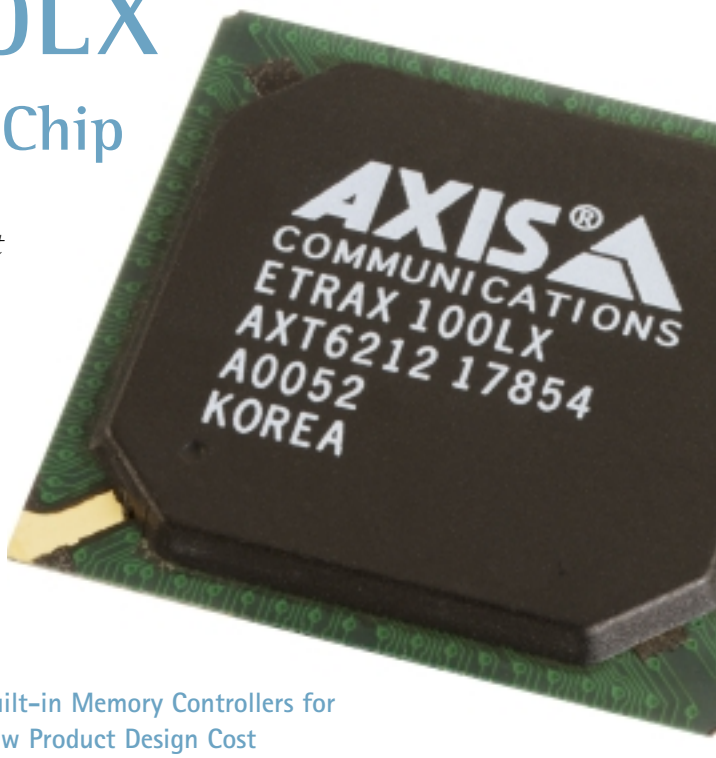
AXIS ETRAX 100LX

Network Device System-on-Chip



Designed to Simplify Embedded Linux Development

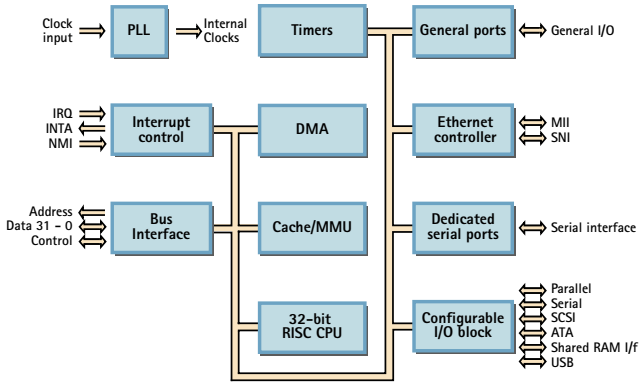
The ETRAX 100LX with a powerful CPU, MMU (Memory Management Unit), integrated Ethernet (10/100), and many device interfaces, is a price competitive hardware option for designers of embedded Linux appliances such as internet gateways, access control equipment, industry automation controllers, *Bluetooth™* appliances etc. Combined with the latest available Linux kernel, and the strong support and design help provided by Axis' engineers, product development teams are able to quickly get to market with competitive products by using the AXIS ETRAX 100LX.

High Performance at Low Power Consumption

The innovative 100 MIPS 32-bit RISC design delivers compact code and exceptional price/performance with low power consumption. An 8-kbyte on-chip cache takes full advantage of the CPU performance.

Feature Rich Integrated I/O for Device Attachment

Several integrated intelligent DMA-driven ports: 2 synchronous serial ports, 4 asynchronous serial ports, 2 parallel ports (fully compatible with IEEE 1284), SCSI-2 and SCSI-3, EIDE/ATA-2, USB (host and device mode), 10/100 full duplex Ethernet controller.



Built-in Memory Controllers for Low Product Design Cost

The ETRAX 100LX has 4 GB of address space and supports SDRAM, EDO DRAM, SRAM, EPROM, EEPROM, and Flash PROM without external logic, which lowers cost and makes design easy.

Linux Kernel Source Code and Development Environment

All you need in terms of software source code and tools for the ETRAX 100LX chip can be downloaded for free from the Axis developer site http://developer.axis.com/. There you will also find the extensive documentation for the ETRAX 100LX chip.

Partnership Development

Axis is committed to open-source development and fully supporting its customers. Reference designs and advanced technical support are available, as well as open discussion forums to facilitate communication between the wide range of ETRAX system developers.

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Technical Specification - AXIS ETRAX 100LX

32-Bit RISC CPU

- RISC CPU with a 32-bit data and address format. 15 general 32-bit registers. Instruction set optimized for compact code and high speed with 16/32-bit bus width. Runs on a 100 MHz clock. User and Supervisor mode for restricted access and selection of appropriate address mapping by the MMU.

Memory Management Unit (MMU)

- MMU featuring 4 GB of virtual uniformed address space for each user process with address space protection so that user applications do not have access to data of other applications or the operating system. Supports zero-copy shared memory schemes and includes a 64-entry on-chip Translation Look-aside Buffer (TLB).

Cache Memory

- 8 Kbytes on-chip direct mapped unified instruction/data cache memory.

Ethernet Controller

- Ethernet controller supporting 100 Mbit and 10 Mbit (compatible with IEEE 802.3 and Fast Ethernet standards). ETRAX 100LX interfaces to Media Independent Interface and Serial Network Interface.

Direct Memory Access (DMA)

- 10 DMA channels each with a 64 byte FIFO for low latency and high throughput data transfer to and from internal and external units (200 MBytes/sec total peek bandwidth to share between the 10 DMA channels). Address range of 31 bits, DMA and cache cooperation to keep memory and cache coherent, and burst access to and from memory to take full advantage of SDRAM and EDO DRAM performance.

4 Asynchronous Serial Ports

- Internal baudrate programmable from 48 Hz to 1.5625 MHz, or external baudrate up to 3.125 MHz. Fixed baudrates from 300 Hz to 1843.2 kHz, and a non-standard baudrate at 6.25 MHz.

2 Synchronous Serial Ports

- Master or Slave synchronous serial mode with codec clock between 32 kHz and 4.096 MHz.

2 USB Ports

- Universal Serial Bus 1.1 Host (control and bulk traffic only) and Device mode operation. Lists 31 endpoints with full performance in Host mode. Hardware support for dynamic connect/disconnect, suspend/resume and remote wakeup.

2 Parallel I/O Ports

- The ports can be used through register access or internal DMA access, and can be configured to support various protocols, including:
  - IBM XT/AT compatible Centronics
  - IBM PS/2 compatible Centronics
  - Hewlett-Packard Fast Mode
  - IBM Fastbyte
  - Compatible with IEEE 1284 - byte, nibble, ECP, and EPP mode.
  - Parallel port wide, supporting 16-bit data transmission, with a transmission rate of up to 12 MByte/s.

SCSI

- Initiator (host) mode SCSI controller that supports either two 8-bit wide or one 16-bit wide SCSI interface. Synchronous and asynchronous data transfer is supported, including SCSI-3 and FAST-20. External bus drivers are required. The SCSI interface is multiplexed on the same pins as the EIDE/ATA-2 ports, the parallel ports and two of the serial ports.

EIDE/ATA-2

- Configuration of up to 4 EIDE/ATA-2 ports for up to 8 IDE disk drives. The EIDE/ATA-2 interfaces are multiplexed on the same pins as the SCSI, parallel ports and two of the serial ports.

Bus Interface and Memory Controllers

- Built-in memory controllers for SDRAM, EDO DRAM, SRAM, EPROM, parallel EEPROM, and FlashPROM. Bus width configurable to 16 or 32 bits. Support for 64 bit SDRAM DIMM and SO-DIMM modules, Double Data Rate SDRAM, and power save mode.

Bootstrap Program Download

- Support for initial loading to internal cache memory from parallel port, serial port and network. Code, loaded to cache, can be designed to enable download of program to initially empty Flash PROM or other external memory.

Timers and Watchdog

- Two eight-bit timers with programmable clock from 381 Hz to 12.5 MHz. Fixed timer clocks from 300 Hz to 1843.2 kHz, and a non-standard baudrate at 6.25 MHz. Additional watchdog timer.

General Purpose Ports

- Two general-purpose ports that each contains 8 bits of individually controlled I/O-pins.

Clock Generator

- Internal 100 MHz operating frequency, generated by a PLL from an external 20 MHz clock signal.

Interrupt Control

- Vectorized interrupt; internal (I/O ports, network interface, DMA, and timer) and external (IRQ and NMI).

Software and Development Tools

- The Linux kernel 2.4 or subsequent for ETRAX 100LX, including device drivers for all ETRAX ports, is available for download from the Axis developer Web site **http://developer.axis.com**. Also available at the site is the GNU CC for ETRAX 100LX including compiler, debugger, and other tools, and extensive documentation: for example Programmer's Manual and Designer's Reference. All downloads and documentation is free of charge. An ETRAX 100LX lab platform, the AXIS Developer Board, can be ordered on-line at **http://developer.axis.com/order/**.

Compatibility with ETRAX 100

- The ETRAX 100LX is code and pin compatible with Axis' renowned ETRAX 100, which has shipped in several million units. The ETRAX 100LX extends the applicability for embedded Linux designs through an added MMU and device interfaces.

Package

- 256-pin Plastic Ball Grid Array package, 27 x 27 x 2.15 mm

Power

- Power dissipation (outputs open): 350mW typ., 610 mW max.

Operating Conditions

- Supply voltage: 3.0 - 3.6V
- Ambient temperature range: 0 - 70 °C.

For more information, visit: **developer.axis.com**

www.axis.com

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