Si4313-B1

Si4313 LOW-COST ISM RECEIVER

Features

- Frequency range = 240–960 MHz
- Sensitivity = –118 dBm
- Low power consumption
- Data rate = 0.2 to 128 kbps
- FSK, GFSK, and OOK modulation schemes
- Power supply = 1.8 to 3.6 V
- Ultra low power shutdown mode
- Digital RSSI
- Wake-up timer
- Auto Frequency Calibration (AFC)
- Clear channel assessment

- Programmable RX BW 2.6–620 kHz
- Preamble detector
- RX 64 byte FIFO
- –40 to +85 °C temperature range
- Integrated voltage regulators
- Frequency hopping capability
- On-chip crystal tuning
- 20-pin QFN package
- Low BOM
- Single capacitor matching network
- Power-On-Reset (POR)
- Single-ended antenna configuration

Applications

- Remote control
- Weather station
- Personal data logging
- Health monitors
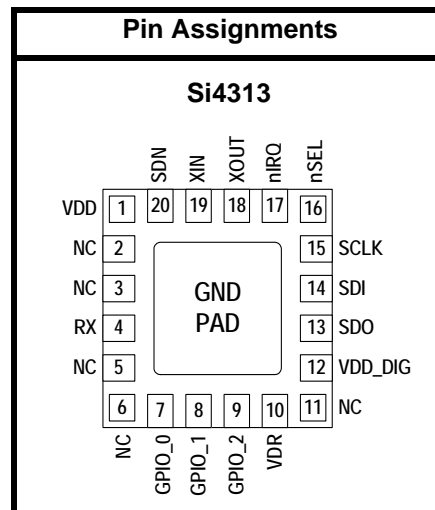
Description

The Si4313 is a single-ended universal ISM receiver for cost-sensitive applications featuring technology developed for the EZRadioPRO® product family.

The Si4313 offers a simple, single-ended radio implementation over the 240–960 MHz frequency range. A receive sensitivity of up to –118 dBm allows for the creation of communication links with an extended range. The Si4313 offers excellent receiver performance in cost-sensitive radio applications.

The Si4313 provides designers with advanced features to enable low system power consumption by offloading a number of RF-related activities from the system MCU allowing for extended MCU sleep periods. Additional features, such as an automatic wake-up timer, 64-byte RX FIFO, and a preamble detection circuit, are available.
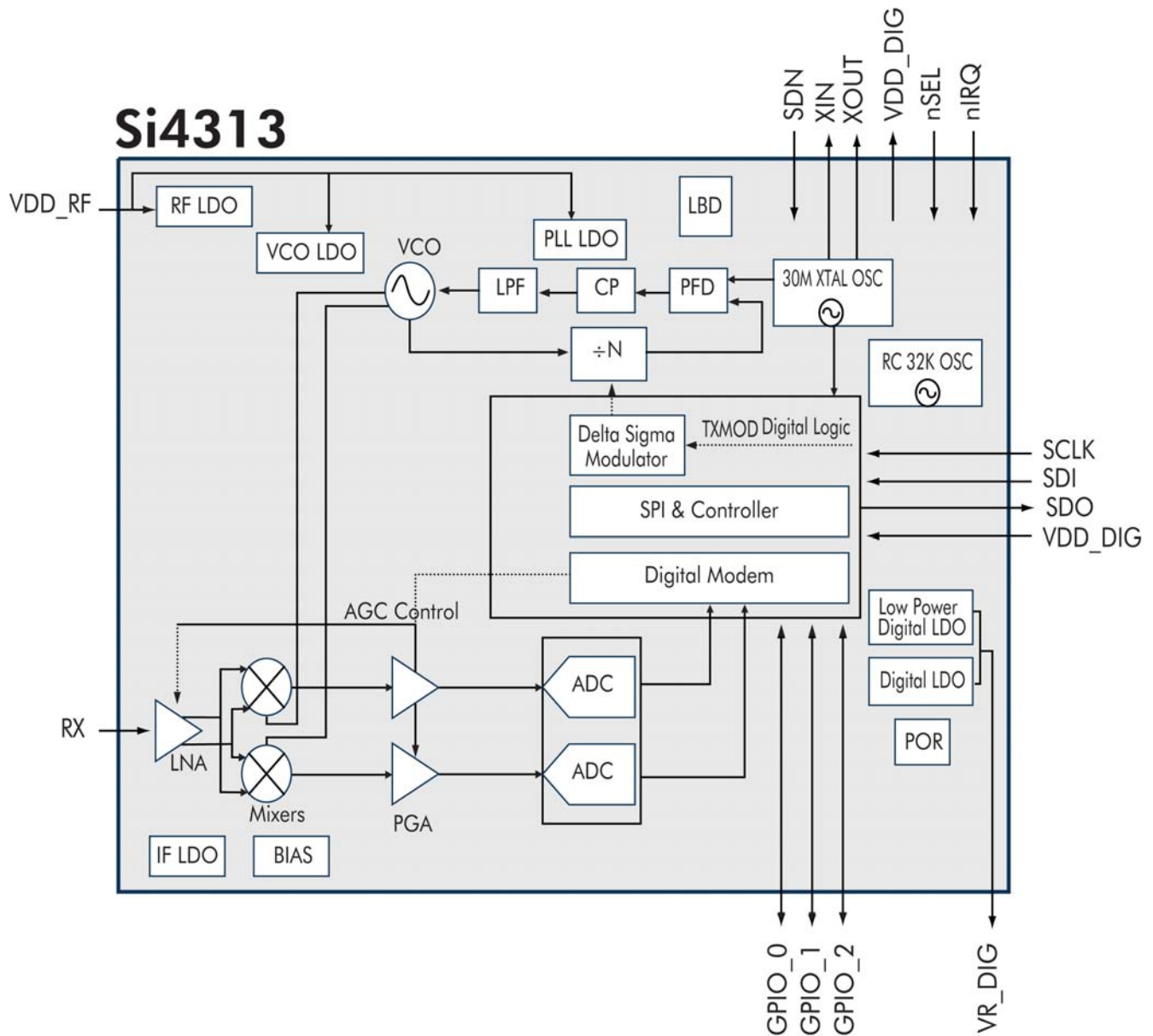
The Si4313's digital receive architecture features an ADC and DSP based modem that performs the radio demodulation and filtering for increased performance.

Ordering Information:
See page 46.

Pin Assignments

Si4313

Pin	Signal
1	VDD
2	NC
3	NC
4	RX
5	NC
6	NC
7	GPIO_0
8	GPIO_1
9	GPIO_2
10	VDR
11	NC
12	VDD_DIG
13	SDO
14	SDI
15	SCLK
16	nSEL
17	nIRQ
18	XOUT
19	XIN
20	SDN

Patents pending

This information applies to a product under development. Its characteristics and specifications are subject to change without notice.

Functional Block Diagram

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1. Electrical Specifications

Table 1. DC Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Supply Voltage Range	V_{DD}		1.8	3.0	3.6	V
Power Saving Modes	$I_{SHUTDOWN}$	RC Oscillator, Main Digital Regulator, and Low Power Digital Regulator OFF[2]	—	15	50	nA
	$I_{STANDBY}$	Low Power Digital Regulator ON (Register values retained) and Main Digital Regulator, and RC Oscillator OFF	—	450	800	nA
	I_{SLEEP}	RC Oscillator and Low Power Digital Regulator ON (Register values retained) and Main Digital Regulator OFF	—	1	—	µA
	$I_{SENSOR-LBD}$	Main Digital Regulator and Low Battery Detector ON, Crystal Oscillator and all other blocks OFF[2]	—	1	—	µA
	$I_{SENSOR-TS}$	Main Digital Regulator and Temperature Sensor ON, Crystal Oscillator and all other blocks OFF[2]	—	1	—	µA
	I_{READY}	Crystal Oscillator and Main Digital Regulator ON, all other blocks OFF. Crystal Oscillator buffer disabled	—	800	—	µA
Tune Mode Current	I_{TUNE}	Synthesizer and regulators enabled	—	8.5	—	mA
RX Mode Current	I_{RX}		—	18.5	—	mA

Notes:
1. All specifications guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in "1.1.1. Production Test Conditions" on page 14.
2. Guaranteed by qualification. Qualification test conditions are listed in "1.1.1. Production Test Conditions" on page 14.

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Table 2. Synthesizer AC Electrical Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Synthesizer Frequency Range	$F_{SYNTH-LB}$	Low Band	240	—	480	MHz
	$F_{SYNTH-HB}$	High Band	480	—	960	MHz
Synthesizer Frequency Resolution[2]	F_{RES-LB}	Low Band	—	156.25	—	Hz
	F_{RES-HB}	High Band	—	312.5	—	Hz
Reference Frequency Input Level[2]	f_{REF_LV}	When using external reference signal driving XOUT pin, instead of using crystal. Measured peak-to-peak (V_{PP})	0.7	—	1.6	V
Synthesizer Settling Time[2]	t_{LOCK}	Measured from leaving Ready mode with XOSC running to any frequency including VCO Calibration	—	200	—	µs
Notes:						
1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in "1.1.1. Production Test Conditions" on page 14.						
2. Guaranteed by qualification. Qualification test conditions are listed in "1.1.1. Production Test Conditions" on page 14.						

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Table 3. Receiver AC Electrical Characteristics[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Synthesizer Frequency Range	F_{RX}		240	—	960	MHz
RX Sensitivity	P_{RX_2}	(BER < 0.1%) (2 kbps, GFSK, BT = 0.5, Δf = ±5 kHz)[2]	—	−118	—	dBm
	P_{RX_40}	(BER < 0.1%) (40 kbps, GFSK, BT = 0.5, Δf = ±20 kHz)[2]	—	−105	—	dBm
	P_{RX_100}	(BER < 0.1%) (100 kbps, GFSK, BT = 0.5, Δf = ±50 kHz)[2]	—	−101	—	dBm
	P_{RX_125}	(BER < 0.1%) (125 kbps, GFSK, BT = 0.5, Δf = ±62.5 kHz)[1]	—	−98	—	dBm
	P_{RX_OOK}	(BER < 0.1%) (4.8 kbps, 350 kHz BW, OOK)[2]	—	−107	—	dBm
		(BER < 0.1%) (40 kbps, 400 kHz BW, OOK)[1]	—	−99	—	dBm
RX Bandwidth[2]	BW		2.6	—	620	kHz
RSSI Resolution	RES_{RSSI}		—	±0.5	—	dB
±1-Ch Offset Selectivity[2]	$C/I_{1\text{-}CH}$	Desired Ref Signal 3 dB above sensitivity, BER <0.1%. Interferer and desired modulated with 40 kbps ΔF = 20 kHz GFSK with BT = 0.5, channel spacing = 150 kHz	—	−31	—	dB
±2-Ch Offset Selectivity[2]	$C/I_{2\text{-}CH}$		—	−35	—	dB
≥±3-Ch Offset Selectivity[2]	C/I3-CH		—	−40	—	dB
Blocking at 1 MHz offset[2]	$1M_{BLOCK}$	Desired Ref Signal 3 dB above sensitivity. Interferer and desired modulated with 40 kbps ΔF = 20 kHz GFSK with BT = 0.5	—	−52	—	dB
Blocking at 4 MHz offset [2]	$4M_{BLOCK}$		—	−56	—	dB
Blocking at 8 MHz offset [2]	$8M_{BLOCK}$		—	−63	—	dB
Image Rejection[2]	Im_{REJ}	IF = 937 kHz	—	−30	—	dB
Spurious Emissions[2]	P_{OB_RX1}		—	—	−54	dBm

Notes:
1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in "1.1.1. Production Test Conditions" on page 14.
2. Guaranteed by qualification. Qualification test conditions are listed in "1.1.1. Production Test Conditions" on page 14.

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Table 4. Auxiliary Block Specifications[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Low Battery Detector Resolution[2]	LBD_{RES}		—	50	—	mV
Low Battery Detector Conversion Time[2]	LBD_{CT}		—	250	—	µs
Microcontroller Clock Output Frequency	F_{MC}	Configurable to 30 MHz, 15 MHz, 10 MHz, 4 MHz, 3 MHz, 2 MHz, 1 MHz, or 32.768 kHz	32.768 k	—	30 M	Hz
30 MHz XTAL Start-Up time	t_{30M}		—	600	—	µs
30 MHz XTAL Cap Resolution[2]	$30M_{RES}$		—	97	—	fF
32 kHz XTAL Start-Up Time[2]	t_{32k}		—	6	—	sec
32 kHz XTAL Accuracy[2]	$32K_{RES}$	Using 20 ppm 32 kHz Crystal.	—	100	—	ppm
32 kHz RC OSC Accuracy[2]	$32KRC_{RES}$		—	2500	—	ppm
POR Reset Time	t_{POR}		—	16	—	ms
Software Reset Time[2]	t_{soft}		—	100	—	µs
Notes:						
1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in "1.1.1. Production Test Conditions" on page 14.						
2. Guaranteed by qualification. Qualification test conditions are listed in "1.1.1. Production Test Conditions" on page 14.						

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Table 5. Digital IO Specifications (SDO, SDI, SCLK, nSEL, and nIRQ)[1]

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Rise Time[2]	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L = 5 pF	—	—	8	ns
Fall Time[2]	T_{FALL}	0.9 x V_{DD} to 0.1 x V_{DD}, C_L = 5 pF	—	—	8	ns
Input Capacitance[2]	C_{IN}		—	—	1	pF
Logic High Level Input Voltage[2]	V_{IH}		V_{DD}–0.6	—	—	V
Logic Low Level Input Voltage[2]	V_{IL}		—	—	0.6	V
Input Current[2]	I_{IN}	0<V_{IN}< V_{DD}	−100	—	100	nA
Logic High Level Output Voltage[2]	V_{OH}	I_{OH}<1 mA source, V_{DD} = 1.8 V	V_{DD}–0.6	—	—	V
Logic Low Level Output Voltage[2]	V_{OL}	I_{OL}<1 mA sink, V_{DD} = 1.8 V	—	—	0.6	V
Notes: 1. All specification guaranteed by production test unless otherwise noted. Production test conditions and max limits are listed in "1.1.1. Production Test Conditions" on page 14. 2. Guaranteed by qualification. Qualification test conditions are listed in "1.1.1. Production Test Conditions" on page 14.						

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Table 6. GPIO Specifications (GPIO_0, GPIO_1 and GPIO_2)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Rise Time[2]	T_{RISE}	0.1 x V_{DD} to 0.9 x V_{DD}, C_L = 10 pF, DRV<1:0> = HH	—	—	8	ns
Fall Time[2]	T_{FALL}	0.9 x V_{DD} to 0.1 x V_{DD}, C_L = 10 pF, DRV<1:0> = HH	—	—	8	ns
Input Capacitance[2]	C_{IN}		—	—	1	pF
Logic High Level Input Voltage[2]	V_{IH}		V_{DD}–0.6	—	—	V
Logic Low Level Input Voltage[2]	V_{IL}		—	—	0.6	V
Input Current[2]	I_{IN}	0<V_{IN}< V_{DD}	–100	—	100	nA
Input Current if pull-up activated[2]	I_{INP}	V_{IL} = 0 V	5	—	25	µA
Maximum Output Current[2]	I_{OMAXLL}	DRV<1:0> = LL	0.1	0.5	0.8	mA
	I_{OMAXLH}	DRV<1:0> = HL	0.9	2.3	3.5	mA
	I_{OMAXHL}	DRV<1:0> = HL	1.5	3.1	4.8	mA
	I_{OMAXHH}	DRV<1:0> = HH	1.8	3.6	5.4	mA
Logic High Level Output Voltage[2]	V_{OH}	I_{OH}< I_{Omax} source, V_{DD} = 1.8 V	V_{DD}–0.6	—	—	V
Logic Low Level Output Voltage[2]	V_{OL}	I_{OL}< I_{Omax} sink, V_{DD} = 1.8 V	—	—	0.6	V

Notes:
1. All specification guaranteed by production test unless otherwise noted.
2. Guaranteed by qualification. Qualification test conditions are listed in "1.1.1. Production Test Conditions" on page 14.

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Table 7. Absolute Maximum Ratings

Parameter	Value	Unit
V_{DD} to GND	−0.3, +3.6	V
Voltage on Digital Control Inputs	−0.3, V_{DD} +0.3	V
Voltage on Analog Inputs	−0.3, V_{DD} +0.3	V
RX Input Power	+10	dBm
Operating Ambient Temperature T_A	−40 to +85	°C
Thermal Impedance θ_{JA}	30	°C/W
Junction Temperature T_J	+125	°C
Storage Temperature Range T_{STG}	−55 to +125	°C
*Note: Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at or beyond these ratings in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. *This is an ESD-sensitive device*.		

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1.1. Test Condition Definitions

1.1.1. Production Test Conditions

- TA = +25 °C
- VDD = +3.3 VDC
- Sensitivity measured at 919 MHz.
- External reference signal (XOUT) = 1.0 VPP at 30 MHz, centered around 0.8 VDC.
- Production test schematic (unless noted otherwise).
- All RF input levels refer to the pins of the Si4313 (not the RF module).

1.1.2. Qualification Test Conditions

- TA = –40 to +85 °C.
- VDD = +1.8 to +3.6 VDC.
- Based upon standard reference design test cards.
- All RF input levels refer to the pins of the Si4313 (not the RF module).

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2. Functional Description

The Si4313 is an ISM wireless single-ended receiver with continuous frequency coverage over the entire 240–960 MHz band. The wide operating voltage range of 1.8–3.6 V and low current consumption make the Si4313 an ideal solution for low-cost, battery-powered applications.

The Si4313 receiver uses a low IF architecture with a digital modem that performs the signal demodulation. The demodulated signal is output to the system MCU through a programmable GPIO or via the standard SPI bus by reading the 64-byte RX FIFO.

A local oscillator (LO) is generated by an integrated VCO and $\Delta\Sigma$ Fractional-N PLL synthesizer. The synthesizer is designed to support configurable data rates, output frequency, frequency deviation, and Gaussian filtering at any frequency between 240–960 MHz.

The Si4313 is designed to work with a microcontroller, crystal, and a few passives to create a very low-cost system. Voltage regulators are integrated on-chip, which allows for a wide range of operating supply voltage conditions from +1.8 to +3.6 V. A standard 4-pin SPI bus is used to communicate with the microcontroller. Three configurable general-purpose I/Os are also available. Minimal antenna matching is required allowing the use of a single ac coupling capacitor which simplifies the system design and lowers the solution cost.

2.1. Application Example
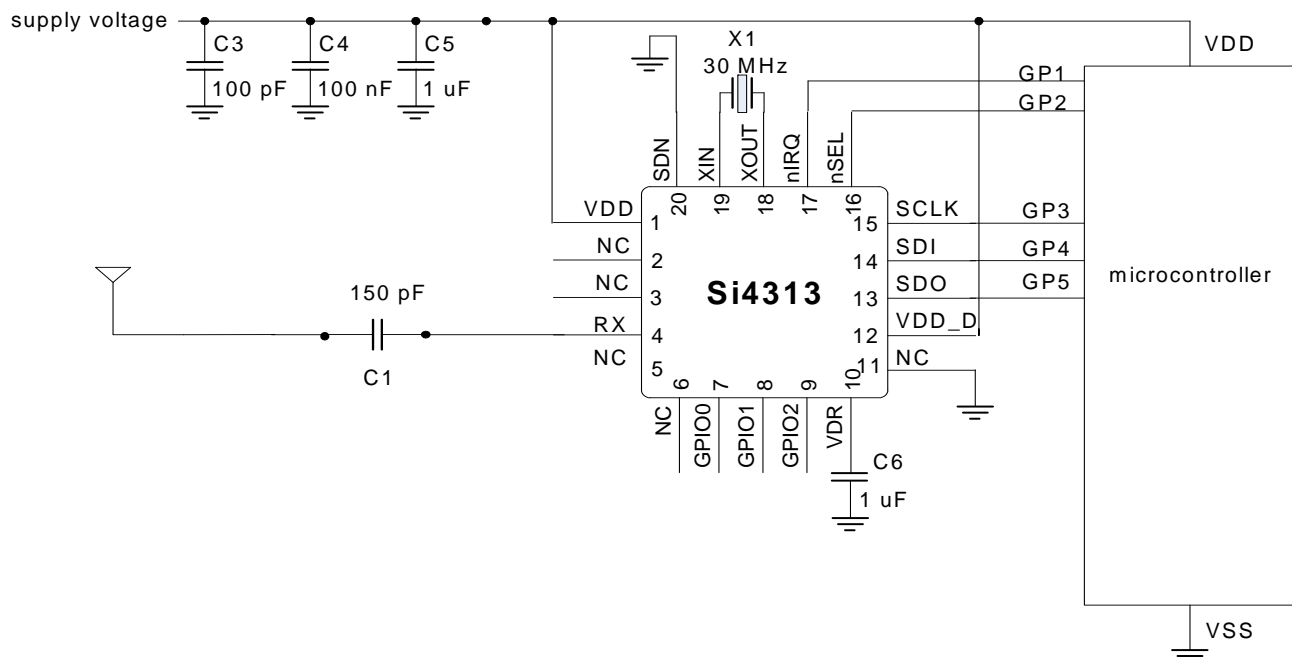
Figure 1. Application Example

2.2. Operating Modes

The Si4313 provides several operating modes, which can be used to optimize the power consumption of the receive application. Depending upon the system communication protocol, an optimal trade-off between radio wake time and power consumption can be achieved.

In general, any given operating mode may be classified as an Active mode or a Power Saving mode. Table 8 indicates which blocks are enabled (active) in each corresponding mode. With the exception of the Shutdown mode, all can be dynamically selected by sending the appropriate commands over the SPI. An "X" in any table cell means that the block can be independently programmed to be either ON or OFF (in that given operating mode) without noticeably impacting current consumption. The SPI block includes the SPI interface hardware and the register space. The 32 kHz OSC circuit block includes the 32.768 kHz RC oscillator or 32.768 kHz crystal oscillator and wake-up timer. AUX (Auxiliary Blocks) includes the temperature sensor and low-battery detector.

Table 8. Operating Modes

Mode Name	Circuit Blocks							
	Digital LDC	**SPI**	**32 kHz OSC**	**AUX**	**30 MHz XTAL**	**PLL**	**RX**	I_{VDD}
Shutdown	OFF register contents lost	OFF	OFF	OFF	OFF	OFF	OFF	15 nA
Standby	ON register contents retained	OFF	OFF	OFF	OFF	OFF	OFF	450 nA
Sleep		ON	ON	X	OFF	OFF	OFF	1 µA
Sensor		ON	X	ON	OFF	OFF	OFF	1 µA
Ready		ON	X	X	ON	OFF	OFF	800 µA
Tuning		ON	X	X	ON	ON	OFF	8.5 mA
Receive		ON	X	X	ON	ON	ON	18.5 mA

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3. Controller Interface

3.1. Serial Peripheral Interface

The Si4313 communicates with the host MCU over a standard three-wire SPI interface: SCLK, SDI, and nSEL. The host MCU can read data from the device on the SDO output pin. An SPI transaction is a 16-bit sequence which consists of a Read-Write (R/W) select bit followed by a 7-bit address field (ADDR) and an 8-bit data field (DATA). The 7-bit address field supports reading from or writing to one of the 128 8-bit control registers. The R/W select bit determines whether the SPI transaction is a read or write transaction. If R/W = 1, it signifies a WRITE transaction, while R/W = 0 signifies a READ transaction. The contents (ADDR or DATA) are latched into the Si4313 every eight clock cycles. Timing parameters are shown in Table 9. The SCLK rate is flexible with a maximum rate of 10 MHz.
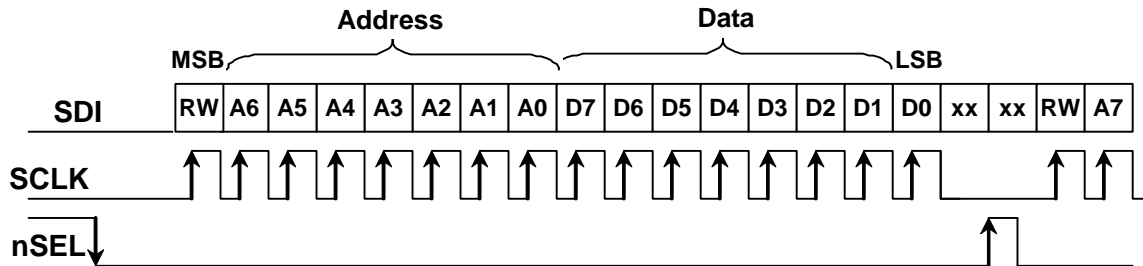
Figure 2. SPI Timing

Table 9. Serial Interface Timing Parameters

Symbol	Parameter	Min (nsec)	Diagram
t_{CH}	Clock high time	40	
t_{CL}	Clock low time	40	
t_{DS}	Data setup time	20	
t_{DH}	Data hold time	20	
t_{DD}	Output data delay time	20	
t_{EN}	Output enable time	20	
t_{DE}	Output disable time	50	
t_{SS}	Select setup time	20	
t_{SH}	Select hold time	50	
t_{SW}	Select high period	80	

To read back data from the Si4313, the R/W bit must be set to 0 followed by the 7-bit address of the register from which to read. The 8 bit DATA field following the 7-bit ADDR field is ignored on the SDI pin when R/W = 0. The next eight negative edge transitions of the SCLK signal will clock out the contents of the selected register. The data read from the selected register will be available on the SDO output pin. The READ function is shown in Figure 3. After the READ function is completed, the SDO pin will remain at either a logic 1 or logic 0 state depending on the last data bit clocked out (D0). When nSEL goes high, the SDO output pin will be pulled high by internal pull-up.

First Bit **Last Bit**

| SDI | RW =0 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D7 =X | D6 =X | D5 =X | D4 =X | D3 =X | D2 =X | D1 =X | D0 =X |

SCLK

First Bit **Last Bit**

| SDO | | | | | | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |
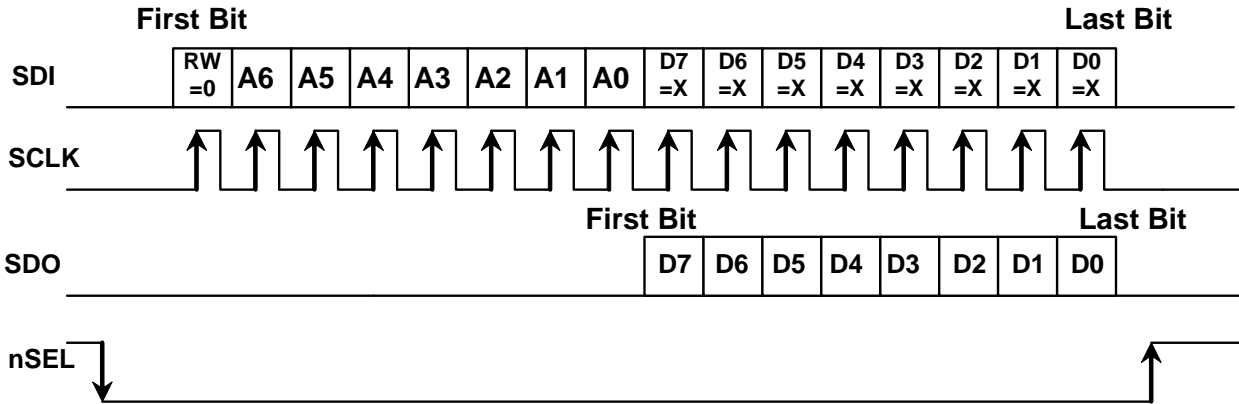
nSEL

Figure 3. SPI Timing—READ Mode

The SPI interface contains a burst read/write mode, which allows for reading/writing sequential registers without having to resend the SPI address. When the nSEL bit is held low while continuing to send SCLK pulses, the SPI interface will automatically increment the ADDR and read from/write to the next address. An example burst write transaction is shown in Figure 4, and a burst read is shown in Figure 5. As long as nSEL is held low, input data will be latched into the Si4313 every eight SCLK cycles.

First Bit **Last Bit**

| SDI | RW =1 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D7 =X | D6 =X | D5 =X | D4 =X | D3 =X | D2 =X | D1 =X | D0 =X | D7 =X | D6 =X | D5 =X | D4 =X | D3 =X | D2 =X | D1 =X | D0 =X |

SCLK

nSEL
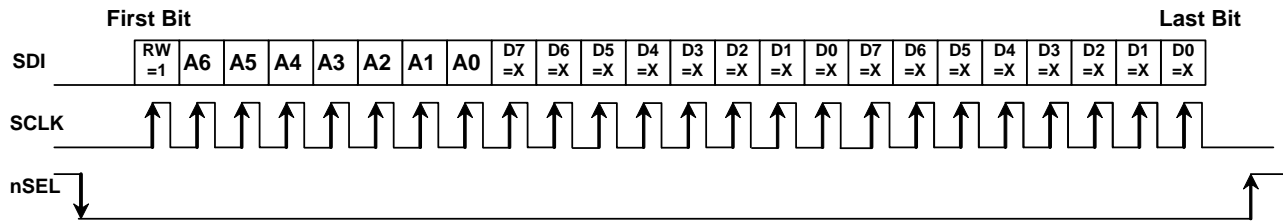
Figure 4. SPI timing—Burst Write Mode

First Bit **Last Bit**

| SDI | RW =0 | A6 | A5 | A4 | A3 | A2 | A1 | A0 | D7 =X | D6 =X | D5 =X | D4 =X | D3 =X | D2 =X | D1 =X | D0 =X |

SCLK

First Bit

| SDO | | | | | | | | | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 |

nSEL
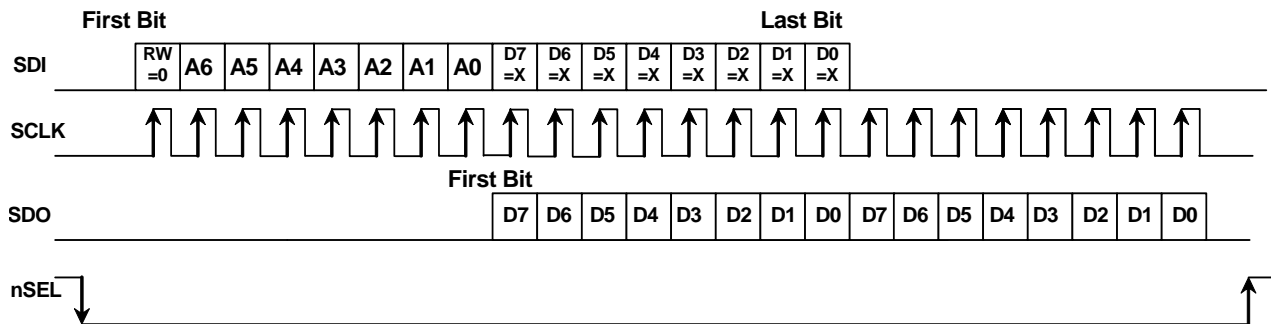
Figure 5. SPI timing—Burst Read Mode

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3.2. Operating Mode Control

There are three primary states in the Si4313 radio state machine: SHUTDOWN, IDLE, and RECEIVE. The SHUTDOWN state is designed to completely shut down the radio to minimize current consumption. There are five different configurations/options for the IDLE state that can be selected to optimize the Si4313 for the application requirements.

"Register 07h. Operating Mode and Function Control 1" controls which operating mode/state is selected. The RX state may be reached automatically from any of the IDLE states by setting the rxon bit in "Register 07h. Operating Mode and Function Control 1". Table 10 shows each of the operating modes with the time required to reach RX mode as well as the current consumption of each mode.

The Si4313 includes a low-power digital regulated supply (LPLDO), which is internally connected in parallel to the output of the main digital regulator (and is available externally at the VR_DIG pin); this common digital supply voltage is connected to all digital circuit blocks, including the digital modem, crystal oscillator, SPI, and register space. The LPLDO has extremely low quiescent current consumption but limited current supply capability; it is used only in the IDLE-STANDBY and IDLE-SLEEP modes.
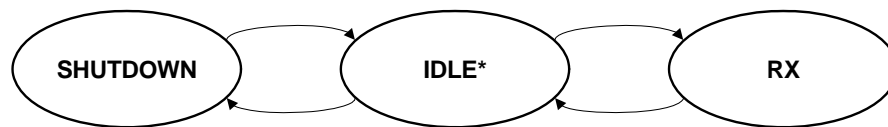
*Five different options for IDLE

Figure 6. State Machine Diagram

Table 10. Operating Modes Response Time

State Mode	Response Time to RX	Current in State/Mode (µA)
Shut Down State	16.8 ms	15 nA
Idle States		
Standby Mode	800 µs	450 nA
Sleep Mode	800 µs	1 µA
Sensor Mode	800 µs	1 µA
Ready Mode	200 µs	800 µA
Tune Mode	200 µs	8.5 mA
RX State	N/A	18.5 mA

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3.2.1. SHUTDOWN State

The SHUTDOWN state is the lowest current consumption state of the device with nominally less than 15 nA of current consumption. The shutdown state may be entered by driving the SDN pin (Pin 20) high. The SDN pin should be held low in all states except the SHUTDOWN state. In the SHUTDOWN state, the contents of the registers are lost and there is no SPI access.

When the chip is connected to the power supply, a POR will be initiated after the falling edge of SDN.

3.2.2. IDLE State

There are fivefour different modes in the IDLE state which may be selected by "Register 07h. Operating Mode and Function Control 1". All modes have a tradeoff between current consumption and response time to TX/RX mode. This tradeoff is shown in Table 10. After the POR event, SWRESET, or exiting from the SHUTDOWN state the chip will default to the IDLE-READY mode. After a POR event the interrupt registers must be read to properly enter the SLEEP, SENSOR, or STANDBY mode and to control the 32 kHz clock correctly.

3.2.2.1. STANDBY Mode

STANDBY mode has the lowest current consumption of the five IDLE states with only the LPLDO enabled to maintain the register values. In this mode the registers can be accessed in both read and write mode. The STANDBY mode can be entered by writing 0h to "Register 07h. Operating Mode and Function Control 1". If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption. Additionally, the ADC should not be selected as an input to the GPIO in this mode as it will cause excess current consumption.

3.2.2.2. SLEEP Mode

In SLEEP mode the LPLDO is enabled along with the Wake-Up-Timer, which can be used to accurately wake-up the radio at specified intervals. See "8.4. Wake-Up Timer and 32 kHz Clock Source" on page 36 for more information on the Wake-Up-Timer. SLEEP mode is entered by setting enwt = 1 (40h) in "Register 07h. Operating Mode and Function Control 1". If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption. Also, the ADC should not be selected as an input to the GPIO in this mode as it will cause excess current consumption.

3.2.2.3. SENSOR Mode

In SENSOR mode the Low Battery Detector may be enabled in addition to the LPLDO and Wake-Up-Timer. The Low Battery Detector can be enabled by setting enlbd = 1 in "Register 07h. Operating Mode and Function Control 1". See "8.3. Low Battery Detector" on page 34 for more information on this feature. If an interrupt has occurred (i.e., the nIRQ pin = 0) the interrupt registers must be read to achieve the minimum current consumption.

3.2.2.4. READY Mode

READY Mode is designed to give a fast transition time to TXRX mode with reasonable current consumption. In this mode the Crystal oscillator remains enabled reducing the time required to switch to TX or RX mode by eliminating the crystal start-up time. READY mode is entered by setting xton = 1 in "Register 07h. Operating Mode and Function Control 1". To achieve the lowest current consumption state the crystal oscillator buffer should be disabled in "Register 62h. Crystal Oscillator Control and Test." To exit READY mode, bufovr (bit 1) of this register must be set back to 0.

3.2.2.5. TUNE Mode

In TUNE mode the PLL remains enabled in addition to the other blocks enabled in the IDLE modes. This will give the fastest response to TXRX mode as the PLL will remain locked but it results in the highest current consumption. This mode of operation is designed for frequency hopping spread spectrum systems (FHSS). TUNE mode is entered by setting pllon = 1 in "Register 07h. Operating Mode and Function Control 1". It is not necessary to set xton to 1 for this mode, the internal state machine automatically enables the crystal oscillator.

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3.2.3. RX State

The RX state may be entered from any of the Idle modes when the rxon bit is set to 1 in 'Register 07h. Operating Mode and Function Control 1'. A built-in sequencer takes care of all the actions required to transition from one of the IDLE modes to the RX state. The following sequence of events will occur automatically to get the chip into RX mode when going from STANDBY mode to RX mode by setting the rxon bit:

1. Enable the main digital LDO and the Analog LDOs.

2. Start up crystal oscillator and wait until ready (controlled by internal timer).

3. Enable PLL.

4. Calibrate VCO (this action is skipped when the vcocal bit is "0", default value is "1").

5. Wait until PLL settles to required receive frequency (controlled by internal timer).

6. Enable receive circuits: LNA, mixers, and ADC.

7. Calibrate ADC (RC calibration).

8. Enable receive mode in the digital modem.

Depending on the configuration of the radio all or some of the following functions will be performed automatically by the digital modem: AGC, AFC (optional), update status registers, bit synchronization, packet handling (optional) including sync word, header check, and CRC.

3.2.4. Device Status

Add	R/W	Func/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def
02	R	Device Status	ffovfl	ffunfl	rxffem	headerr	freqerr		cps[1]	cps[2]	—

The operational status of the Si4313 can be read from the Device Status register, 'Register 02h'

3.3. Interrupts

The Si4313 is capable of generating an interrupt signal when certain events occur. The chip notifies the microcontroller that an interrupt event has occurred by setting the nIRQ output pin LOW = 0. This interrupt signal will be generated when any one (or more) of the interrupt events (corresponding to the Interrupt Status bits) shown below occur. The nIRQ pin will remain low until the microcontroller reads the Interrupt Status Register(s) (Registers 03h-04h) containing the active Interrupt Status bit. The nIRQ output signal will then be reset until the next change in status is detected. The interrupts must be enabled by the corresponding enable bit in the Interrupt Enable Registers (Registers 05h-06h). All enabled interrupt bits will be cleared when the microcontroller reads the interrupt status register. If the interrupt is not enabled when the event then it will not trigger the nIRQ pin, but the status may still be read at anytime in the Interrupt Status registers.

Add	R/W	Func/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def
03	R	Interrupt Status 1	ifferr	Reserved	Reserved	irxffafull	iext	Reserved	ipkvalid	icrcerror	—
04	R	Interrupt Status 2	iswdet	ipreaval	ipreainval	irssi	iwut	ilbd	ichiprdy	ipor	—
05	R/W	Interrupt Enable 1	enfferr	Reserved	Reserved	enrxffafull	enext	Reserved	enpkvalid	encrcerror	00h
06	R/W	Interrupt Enable 1	enswdet	enpreaval	enpreainval	enrssi	enwut	enlbd	enchiprdy	enpor	01h

3.4. System Timing
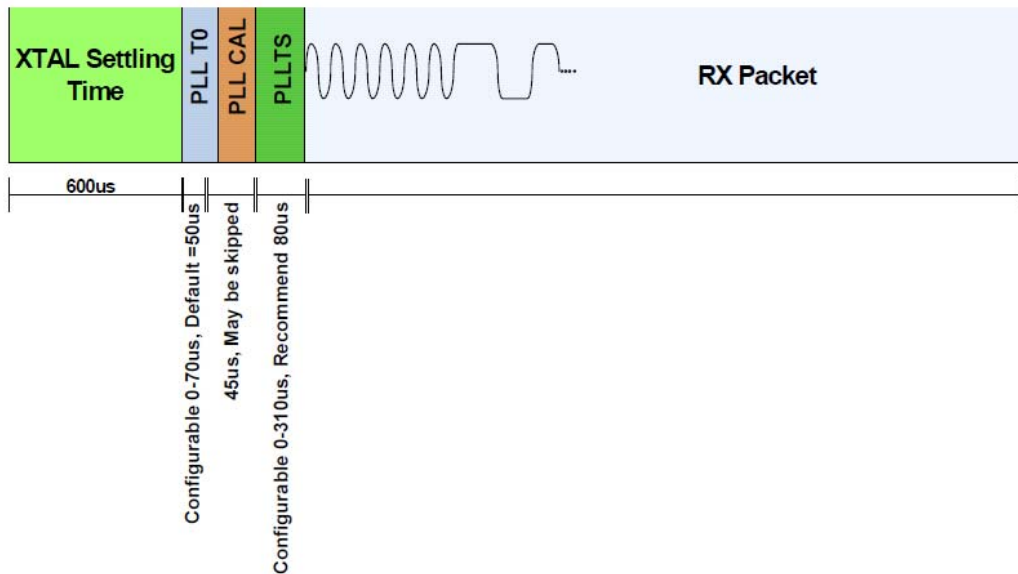
Figure 7. RX Timing

The VCO will automatically calibrate at every frequency change or power-up. The PLL T0 time is to allow for bias settling of the VCO. The PLL TS time is for the settling time of the PLL, which has a default setting of 100 µs. The total time for PLL T0, PLL CAL, and PLL TS under all conditions is 200 µs. In certain applications, the PLL T0 time and the PLL CAL may be skipped for faster turnaround time. Contact applications support if faster turnaround time is desired.

3.5. Frequency Control

To calculate the necessary frequency register settings, use the Silicon Labs' Wireless Design Suite (WDS) or Excel Calculator available from the product web page. These methods offer a simple, quick interface to determine the correct settings based on the application requirement.

Add	R/W	Function/Description	Data								POR Default
			D7	D6	D5	D4	D3	D2	D1	D0	
75	R/W	Frequency Band Select		sbsel	hbsel	fb[4]	fb[3]	fb[2]	fb[1]	fb[0]	35h
76	R/W	Nominal Carrier Frequency 1	fc[15]	fc[14]	fc[13]	fc[12]	fc[11]	fc[10]	fc[9]	fc[8]	BBh
77	R/W	Nominal Carrier Frequency 0	fc[7]	fc[6]	fc[5]	fc[4]	fc[3]	fc[2]	fc[1]	fc[0]	80h

3.5.1. Automatic State Transition for Frequency Change

If registers 79h or 7Ah are changed in RX mode, the state machine will automatically transition the chip back to tune and change the frequency. This feature is useful to reduce the number of SPI commands required in a Frequency Hopping System. In turn, this reduces microcontroller activity, thereby reducing current consumption.

3.5.2. Frequency Offset Adjustment

When the AFC is disabled, the frequency offset can be adjusted manually by fo[9:0] in registers 73h and 74h. The frequency offset adjustment and the AFC are both implemented by shifting the Synthesizer Local Oscillator frequency. This register is a signed register; so, in order to get a negative offset, it is necessary to take the twos

complement of the positive offset number. The offset can be calculated with the following formula:

$$\text{Desired Offset} = 156.25 \text{ Hz} \times (\text{hbsel} + 1) \times \text{fo}[9:0]$$

$$\text{fo}[9:0] = \frac{\text{Desired Offset}}{156.25 \text{ Hz} \times (\text{hbsel} + 1)}$$

The adjustment range is ±160 kHz in high band and ±80 kHz in low band. For example, to compute an offset of +50 kHz in high band mode, fo[9:0] should be set to 0A0h. For an offset of –50 kHz in high band mode, the fo[9:0] register should be set to 360h.

Add	R/W	Func/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def
73	R/W	Frequency Offset	fo[7]	fo[6]	fo[5]	fo[4]	fo[3]	fo[2]	fo[1]	fo[0]	00h
74	R/W	Frequency Offset	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	Rsvd	fo[9]	fo[8]	00h

3.5.3. Auto Frequency Control (AFC)

All AFC settings can be easily obtained from the excel settings calculator or by using the WDS Chip Configurator All AFC settings can be easily obtained from the settings calculator. This is the recommended method to program all AFC settings. This section is intended to describe the operation of the AFC in more detail to help understand the trade-offs of using AFC.The receiver supports automatic frequency control (AFC) to compensate for frequency differences between the transmitter and receiver reference frequencies. These differences can be caused by the absolute accuracy and temperature dependencies of the reference crystals. Due to frequency offset compensation in the modem, the receiver is tolerant to frequency offsets up to ±0.25 times the IF bandwidth when the AFC is disabled. When the AFC is enabled, the received signal will be centered in the pass-band of the IF filter, providing optimal sensitivity and selectivity over a wider range of frequency offsets up to ±0.35 times the IF bandwidth. The trade-off of receiver sensitivity (at 1% PER) versus carrier offset and the impact of AFC are illustrated in Figure 8.
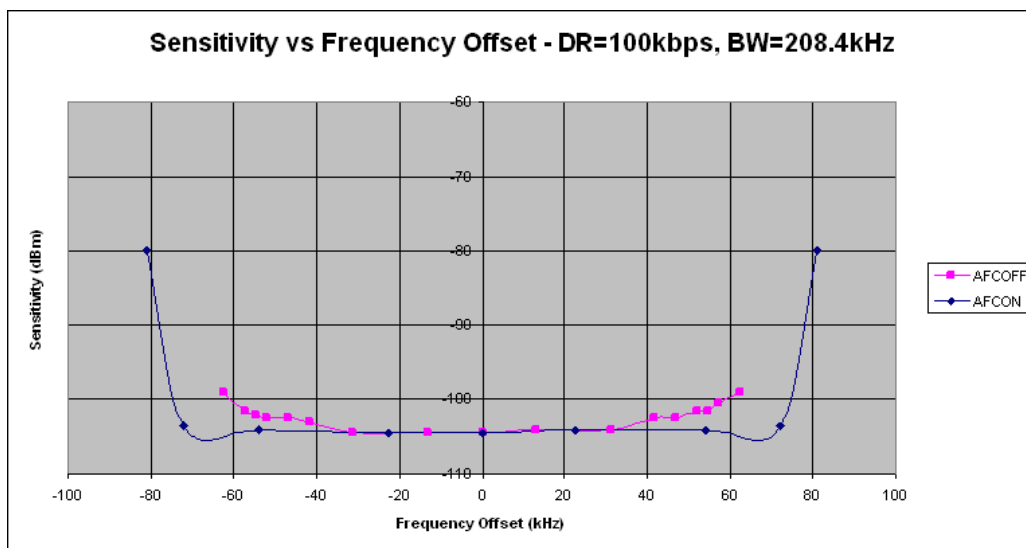
Figure 8. Sensitivity at 1% PER vs. Carrier Frequency Offset

When AFC is enabled, the preamble length needs to be long enough to settle the AFC. In general, one byte of preamble is sufficient to settle the AFC. Disabling the AFC allows the preamble to be shortened from 40 bits to 32 bits. Note that with the AFC disabled, the preamble length must still be long enough to settle the receiver and to detect the preamble (see "6.2. Preamble Length" on page 30). The AFC corrects the detected frequency offset by changing the frequency of the Fractional-N PLL. When the preamble is detected, the AFC will freeze for the remainder of the packet. In multi-packet mode the AFC is reset at the end of every packet and will re-acquire the frequency offset for the next packet. The AFC loop includes a bandwidth limiting mechanism improving the

rejection of out of band signals. When the AFC loop is enabled, its pull-in-range is determined by the bandwidth limiter value (AFCLimiter) which is located in register 2Ah.

$$AFC\_pull\_in\_range = \pm AFCLimiter[7:0] \times (hbsel+1) \times 625\ Hz$$

The AFC Limiter register is an unsigned register and its value can be obtained from the EZRadioPRO Register Calculator spreadsheet.

The amount of error correction feedback to the Fractional-N PLL before the preamble is detected is controlled from afcgearh[2:0]. The default value 000 relates to a feedback of 100% from the measured frequency error and is advised for most applications. Every bit added will half the feedback but will require a longer preamble to settle.

The AFC operates as follows. The frequency error of the incoming signal is measured over a period of two bit times, after which it corrects the local oscillator via the Fractional-N PLL. After this correction, some time is allowed to settle the Fractional-N PLL to the new frequency before the next frequency error is measured. The duration of the AFC cycle before the preamble is detected can be programmed with shwait[2:0]. It is advised to use the default value 001, which sets the AFC cycle to 4 bit times (2 for measurement and 2 for settling). If shwait[2:0] is programmed to 3'b000, there is no AFC correction output. It is advised to use the default value 001, which sets the AFC cycle to 4 bit times (2 for measurement and 2 for settling).

The AFC correction value may be read from register 2Bh. The value read can be converted to kHz with the following formula:

$$AFC\ Correction = 156.25Hz \times (hbsel +1) \times afc\_corr[7:0]$$

	Frequency Correction	
	RX	**TX**
AFC disabled	Freq Offset Register	Freq Offset Register
AFC enabled	AFC	Freq Offset Register

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4. Modulation Options

All modulation options are programmed in "Register 71h. Modulation Mode Control 2."

4.1. Modulation Type

The Si4313 can be configured to support three alternative modulation options: Gaussian Frequency Shift Keying (GFSK), Frequency Shift Keying (FSK), and On-Off Keying (OOK). The type of modulation is selected with the modtyp[1:0] bits in "Register 71h. Modulation Mode Control 2".

modtyp[1:0]	Modulation Source
00	Reserved
01	OOK
10	FSK
11	GFSK

4.2. FIFO Mode

In FIFO mode, the integrated FIFO is used to receive the data. The FIFO is accessed via "Register 7Fh. FIFO Access" with burst read capability. The FIFO may be configured specific to the application packet size, etc. (see "6. Data Handling" on page 29 for further information).

When in FIFO mode, the chip will automatically exit the RX State when the ipkvalid interrupt occurs. The chip will return to the IDLE mode state programmed in "Register 07h. Operating Mode and Function Control 1".

In RX mode, the rxon bit will only be cleared if ipkvalid occurs and the rxmpk bit (Address 08h bit [4]) is 0. When the rxmpk bit is set to 1, the part will remain in RX mode after successfully receiving a packet. A CRC, Header, or Sync error will generate an interrupt, and the microcontroller will need to decide on the next action.

In RX mode, the preamble detection threshold and sync needs to be programmed so that the modem knows when to start filling data into the FIFO. When the FIFO is being used, the data being loaded into or out of the FIFO can still be observed by configuring the GPIO, which can be useful during development.

4.3. Direct Mode

In many system implementations, it may not be desirable to use a FIFO, and, for this scenario, a "Direct Mode", which bypasses the FIFOs entirely, is provided. In Direct Mode, the RX data and RX clock are programmed directly to the GPIO and used by the microcontroller to process the data without using the FIFO. In direct mode, the preamble detection threshold (Reg 35h) still needs to be programmed. Once the preamble is detected, algorithms internal to the modem change. It is not required that the sync be programmed when direct mode is used for RX.

4.3.1. Direct Mode using SPI or nIRQ Pins

In certain applications, it may be desirable to minimize the connections to the microcontroller or to preserve the GPIOs for other uses. For these cases, it is possible to use the SPI pins and nIRQ as the modulation clock and data. The SDO pin can be configured to be the data clock by programming trclk = 10. If the nSEL pin is LOW, then the function of the pin will be SPI data output. If the pin is high and trclk is 10, then, during the RX mode, the data clock will be available on the SDO pin. If trclk[1:0] is set to 11 and no interrupts are enabled in registers 05 or 06h, the nIRQ pin can also be used as the RX data clock.

The SDI pin can be configured to be the data source for RX if dtmod = 01. Similarly, if nSEL is LOW, the pin will function as SPI data-in; if nSEL is HIGH, it will be the received demodulated data.

5. Internal Functional Blocks

This section provides an overview of some of the key blocks of the internal radio architecture.

5.1. RX LNA

The input frequency range for the LNA is 240–960 MHz. The LNA provides gain with a noise figure low enough to suppress the noise of the following stages. The LNA has one step of gain control that is controlled by the analog gain control (AGC) algorithm. The AGC algorithm adjusts the gain of the LNA and PGA so the receiver can handle signal levels from sensitivity to +5 dBm with optimal performance.

5.2. RX I-Q Mixer

The output of the LNA is fed internally to the input of the receive mixer. The receive mixer is implemented as an I-Q mixer that provides both I and Q channel outputs to the programmable gain amplifier. The mixer consists of two double-balanced mixers whose RF inputs are driven in parallel. Local oscillator (LO) inputs are driven in quadrature, and separate I and Q Intermediate Frequency (IF) outputs drive the programmable gain amplifier. The receive LO signal is supplied by an integrated VCO and PLL synthesizer operating between 240 and 960 MHz. The necessary quadrature LO signals are derived from the divider at the VCO output.

5.3. Programmable Gain Amplifier

The Programmable Gain Amplifier (PGA) provides the necessary gain to boost the signal level into the dynamic range of the ADC. The PGA must also have enough gain switching to allow for large input signals to ensure a linear RSSI range up to –20 dBm. The PGA has steps of 3 dB that are controlled by the AGC algorithm in the digital modem.

5.4. ADC

The amplified IQ IF signals are digitized using an Analog-to-Digital Converter (ADC), which allows for low current consumption and high dynamic range. The band-pass response of the ADC provides exceptional rejection of out of band blockers.

5.5. Digital Modem

Using high-performance ADCs allows channel filtering, image rejection, and demodulation to be performed in the digital domain, resulting in reduced area while increasing flexibility. The digital modem performs the following functions:

- Channel selection filter
- TX modulation
- RX demodulation
- AGC
- Preamble detector
- Invalid preamble detector
- Radio signal strength indicator (RSSI)
- Automatic frequency compensation (AFC)
- Packet handling including EZMAC® features
- Cyclic redundancy check (CRC)

The digital channel filter and demodulator are optimized for ultra low power consumption and are highly configurable. Supported modulation types are GFSK, FSK, and OOK. The channel filter can be configured to support bandwidths ranging from 620 kHz down to 2.6 kHz. A large variety of data rates are supported ranging from 0.123 up to 256 kbps. The AGC algorithm is implemented digitally using an advanced control loop optimized for fast response time.

The configurable preamble detector is used to improve the reliability of the sync-word detection. The sync-word detector is only enabled when a valid preamble is detected, significantly reducing the probability of false detection.

The received signal strength indicator (RSSI) provides a measure of the signal strength received on the tuned

channel. The resolution of the RSSI is 0.5 dB. This high resolution RSSI enables accurate channel power measurements for clear channel assessment (CCA), and carrier sense (CS), and listen before talk (LBT) functionality.

Frequency mistuning caused by crystal inaccuracies can be compensated by enabling the digital automatic frequency control (AFC) in receive mode.

A comprehensive programmable packet handler including key features of Silicon Labs' EZMAC is integrated to create a variety of communication topologies ranging from peer-to-peer networks to mesh networks. The extensive programmability of the packet header allows for advanced packet filtering which in turn enables a mix of broadcast, group, and point-to-point communication.

A wireless communication channel can be corrupted by noise and interference, and it is therefore important to know if the received data is free of errors. A cyclic redundancy check (CRC) is used to detect the presence of erroneous bits in each packet. A CRC is computed and appended at the end of each transmitted packet and verified by the receiver to confirm that no errors have occurred. The packet handler and CRC can significantly reduce the load on the system microcontroller allowing for a simpler and cheaper microcontroller.

The digital modem includes the TX modulator which converts the TX data bits into the corresponding stream of digital modulation values to be summed with the fractional input to the sigma-delta modulator. This modulation approach results in highly accurate resolution of the frequency deviation. A Gaussian filter is implemented to support GFSK, considerably reducing the energy in the adjacent channels. The default bandwidth-time product (BT) is 0.5 for all programmed data rates, but it may not be adjusted to other values.

ntly reduce the load on the system microcontroller allowing for the use of a simpler and cheaper microcontroller.

5.6. Synthesizer

An integrated Sigma Delta ($\Sigma\Delta$) Fractional-N PLL synthesizer capable of operating from 240–960 MHz is provided on-chip. Using a $\Sigma\Delta$ synthesizer has many advantages; it provides flexibility in choosing data rate, deviation, channel frequency, and channel spacing.

The PLL and $\Sigma\Delta$ modulator scheme is designed to support any desired frequency and channel spacing in the range from 240–960 MHz with a frequency resolution of 156.25 Hz (Low band) or 312.5 Hz (High band).
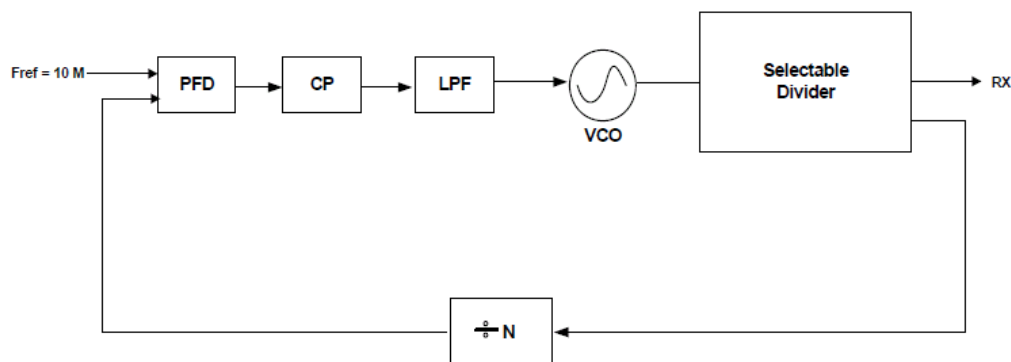
Table 11. PLL Synthesizer Block Diagram

The reference frequency to the PLL is 10 MHz. The PLL utilizes a differential L-C VCO with integrated on-chip inductors. The output of the VCO is followed by a configurable divider that divides down the signal to the desired output frequency band. The modulus of this divider stage is controlled dynamically by the output from the $\Sigma\Delta$ modulator. The tuning resolution is sufficient to tune to the commanded frequency with a maximum accuracy of 312.5 Hz anywhere in the range between 240–960 MHz.

5.6.1. VCO

The output of the VCO is automatically divided down to the correct output frequency depending on the hbsel and fb[4:0] fields in "Register 75h. Frequency Band Select". In receive mode, the LO frequency is automatically shifted downwards by the IF frequency of 937.5 kHz, allowing receive operation on the same frequency. The VCO integrates the resonator inductor and tuning varactor; so, no external VCO components are required.

The VCO uses a capacitance bank to cover the wide frequency range specified. The capacitance bank will automatically be calibrated every time the synthesizer is enabled. In certain fast hopping applications, this might not be desirable; so, the VCO calibration may be skipped by setting the appropriate register.

5.7. Crystal Oscillator

The Si4313 includes an integrated 30 MHz crystal oscillator with a fast start-up time of less than 600 μs when a suitable parallel resonant crystal is used. The design is differential with the required crystal load capacitance integrated on-chip to minimize the number of external components. By default, all that is required off-chip is the 30 MHz crystal.

The crystal load capacitance can be digitally programmed to accommodate crystals with various load capacitance requirements and to adjust the frequency of the crystal oscillator. The tuning of the crystal load capacitance is programmed through the xlc[6:0] field of "Register 09h. 30 MHz Crystal Oscillator Load Capacitance". The total internal capacitance is 12.5 pF and is adjustable in approximately 127 steps (97 fF/step). The crystal shift bit is a coarse shift in frequency but is not binary with xlc[6:0].

The crystal frequency adjustment can be used to compensate for crystal production tolerances. The typical value of the total on-chip capacitance, Cint, can be calculated as follows:

$$C_{INT} = 1.8 \text{ pF} + 0.085 \text{ pF} \times xlc[6:0] + 3.7 \text{ pF} \times xtalshift$$

Note that the coarse shift bit crystal shift is not binary with xlc[6:0]. The total load capacitance Cload seen by the crystal can be calculated by adding the sum of all external parasitic PCB capacitances Cext to Cint. If the maximum value of Cint (16.3 pF) is not sufficient, an external capacitor can be added for exact tuning.

If AFC is disabled, the synthesizer frequency may be further adjusted by programming the Frequency Offset field fo[9:0]in "Register 73h. Frequency Offset 1" and "Register 74h. Frequency Offset 2", as discussed in "3.5. Frequency Control" on page 22.

The crystal oscillator frequency is divided down internally and may be output to the microcontroller through one of the GPIO pins for use as the System Clock. In this fashion, only one crystal oscillator is required for the entire system, and the BOM cost is reduced. The available clock frequencies and the GPIO configuration are discussed further in "8.2. Microcontroller Clock" on page 33.

The Si4313 may also be driven with an external 30 MHz clock signal through the XIN pin. When driving with an external reference or using a TCXO, the crystal load capacitance register should be set to 0.

Add	R/W	Func/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def
09	R/W	Crystal Oscillator Load Capacitance	xtalshift	xlc[6]	xlc[5]	xlc[4]	xlc[3]	xlc[2]	xlc[1]	xlc[0]	7Fh

5.8. Regulators

There are a total of six regulators integrated onto the Si4313. With the exception of the digital regulator, all regulators are designed to operate with only internal decoupling. The digital regulator requires an external 1 μF decoupling capacitor. All regulators are designed to operate with an input supply voltage from +1.8 to +3.6 V.

A supply voltage should only be connected to the VDD pins. No voltage should be forced on the digital regulator outputs.

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6. Data Handling

6.1. RX FIFO

A 64 byte FIFO is integrated into the chip for RX, as shown below. "Register 7Fh. FIFO Access" is used to access the FIFO. As described in "3.1. Serial Peripheral Interface" on page 17, a burst read from address 7Fh will read data from the RX FIFO.
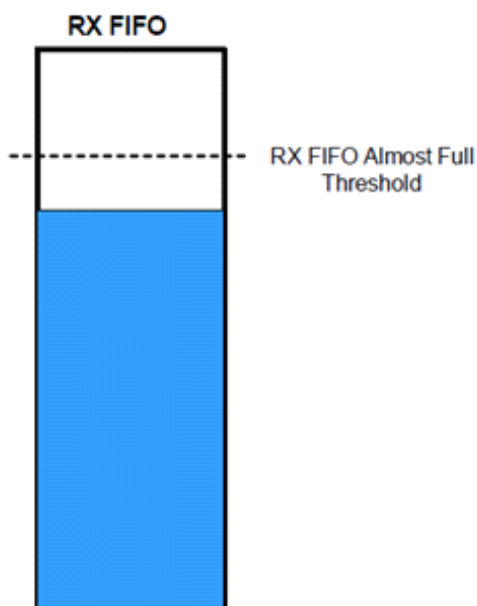
Figure 9. FIFO Threshold

The RX FIFO has one programmable threshold called the FIFO Almost Full Threshold, rxafthr[5:0]. When the incoming RX data reaches the Almost Full Threshold, an interrupt will be generated to the microcontroller via the nIRQ pin. The microcontroller will then need to read the data from the RX FIFO.

Add	R/W	Func/ Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def
08	R/W	Operating & Function Control 2	Reserved	Reserved	Reserved	rxmpk	Reserved	enldm	ffclrrx	Reserved	00h
7E	R/W	RX FIFO Control	Reserved	Reserved	rxafthr[5]	rxafthr[4]	rxafthr[3]	rxafthr[2]	rxafthr[1]	rxafthr[0]	37h

The RX FIFO may be cleared or reset with the ffclrrx bit in "Register 08h. Operating Mode and Function Control 2,". All interrupts may be enabled by setting the Interrupt Enabled bits in "Register 05h. Interrupt Enable 1" and "Register 06h. Interrupt Enable 2,". If the interrupts are not enabled, the function will not generate an interrupt on the nIRQ pin, but the bits will still be read correctly in the Interrupt Status registers.

6.2. Preamble Length

The preamble detection threshold determines the number of valid preamble bits the radio must receive to qualify a valid preamble. The preamble threshold should be adjusted depending on the nature of the application. The required preamble length threshold will depend on when receive mode is entered in relation to the start of the transmitted packet and the length of the transmit preamble. With a shorter-than-recommended preamble detection threshold, the probability of false detection is directly related to how long the receiver operates on noise before the transmit preamble is received. False detection on noise may cause the actual packet to be missed. The preamble detection threshold is programmed in register 35h. For most applications with a preamble length longer than 32 bits, the default value of 20 is recommended for the preamble detection threshold. A shorter Preamble Detection Threshold Table 12 lists the recommended preamble detection threshold and preamble length for various modes.

Table 12. Minimum Receiver Settling Time

	Approx. Receiver Settling Time	Recommended Preamble Length with 8-bit Detection Threshold	Recommended Preamble Length with 20-bit Detection Threshold
(G)FSK AFC Disabled	1 byte	20 bits	32 bits
(G)FSK AFC Enabled	2 byte	28 bits	40 bits
OOK	2 byte	3 byte	4 byte
*Note: The recommended preamble length and the preamble detection threshold may be shortened when occasional packet errors are tolerable.			

6.3. Invalid Preamble Detector

When scanning channels in a frequency hopping system it is desirable to determine if a channel is valid in the minimum amount of time. The preamble detector can output an invalid preamble detect signal. which can be used to identify the channel as invalid. After a configurable time set in Register 60h[7:4], an invalid preamble detect signal is asserted indicating an invalid channel. The period for evaluating the signal for invalid preamble is defined as (inv_pre_th[3:0] x 4) x Bit Rate Period. The preamble detect and invalid preamble detect signals are available in "Register 03h. Interrupt/Status 1" and "Register 04h. Interrupt/Status 2."

7. RX Modem Configuration

A Microsoft Excel (WDS) parameter calculator or Wireless Development Suite (WDS) calculator is provided to determine the proper settings for the modem. The calculator can be found on http://www.silabs.com or on the CD provided with the demo kits. An application note is available to describe how to use the calculator and to provide advanced descriptions of the modem settings and calculations via registers 1C-25h. The modulation index is equal to twice the peak deviation divided by the data rate (Rb).

8. Auxiliary Functions

8.1. Smart Reset

The Si4313 contains an enhanced integrated SMART RESET or POR circuit. The POR circuit contains both a classic level threshold reset as well as a slope detector, POR. This reset circuit was designed to produce a reliable reset signal under any circumstances. Reset will be initiated if any of the following conditions occurs:

- Initial power on, VDD starts from GND: reset is active till VDD reaches VRR (see table).
- When VDD decreases below VLD for any reason: reset is active till VDD reaches VRR.
- A software reset via Register 08h. "Operating Mode and Function Control 2," where reset is active for time TSWRST.
- On the rising edge of a VDD glitch when the supply voltage exceeds the time functioned limit of Figure 10.
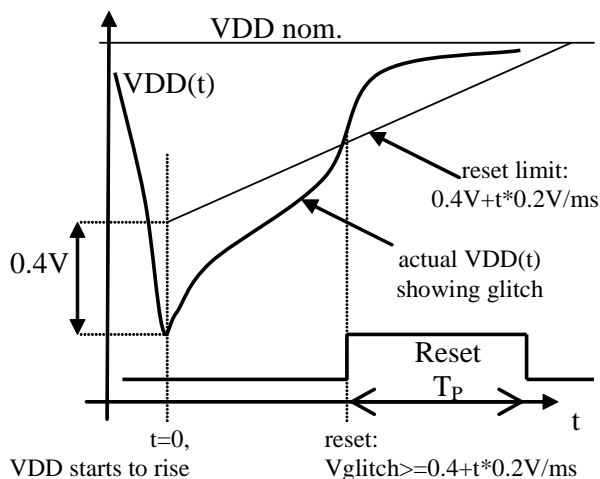
Figure 10. POR Glitch Parameters

Table 13. POR Parameters

Parameter	Symbol	Comment	Min	Typ	Max	Unit
Release Reset Voltage	VRR		0.85	1.3	1.75	V
Power-On VDD Slope	SVDD	Tested VDD Slope Region	0.03		300	V/ms
Low VDD Limit	VLD	VLD<VRR	0.7	1	1.3	V
Software Reset Pulse	T_{SWRST}		50		470	µs
Threshold Voltage	VTSD			0.4		V
Reference Slope	K			0.2		V/ms
VDD Glitch Reset Pulse	TP	Also occurs after SDN, and initial power on	5	16	40	ms

The reset will initialize all registers to their default values. The reset signal is also available for output and use by the microcontroller by using the default setting for GPIO_0. The inverted reset signal is available by default on GPIO_1.

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8.2. Microcontroller Clock

The Si4313 can divide its 30 MHz clock down internally, which can then be output to the microcontroller through GPIO2. Additionally, a 32.768 kHz clock signal can also be derived from an internal RC Oscillator or an external 32 kHz Crystal. The GPIO2 default is the microcontroller clock with a 1 MHz microcontroller clock output.

This feature is useful to lower BOM cost by using only one crystal in the system. The system clock frequency is selectable from one of eight options listed in Table 14.

Table 14. System Clock Frequency Options

mclk[2:0]	Clock Frequency
000	30 MHz
001	15 MHz
010	10 MHz
011	4 MHz
100	3 MHz
101	2 MHz
110	1 MHz
111	32.768 kHz

Add	R/W	Func/ Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def
0A	R/W	Microcontroller Output Clock			clkt[1]	clkt[0]	enlfc	mclk[2]	mclk[1]	mclk[0]	06h

Except for the 32.768 kHz option, all other frequencies are derived by dividing the Crystal Oscillator frequency. The 32.768 kHz clock signal is derived from an internal RC Oscillator or an external 32 kHz Crystal, depending on which is selected. The GPIO2 default is the microcontroller clock with a 1 MHz microcontroller clock output.

If the microcontroller clock option is being used, there may be a need for a system clock for the microcontroller while the Si4313 is in SLEEP mode. Since the crystal oscillator is disabled in SLEEP mode in order to save current, the low-power 32.768 kHz clock can be automatically switched to become the microcontroller clock. This feature is called enable low frequency clock and is enabled by the enlfc bit in Register 0Ah. Microcontroller Output Clock. When enlfc = 1 and the chip is in SLEEP mode, the 32.768 kHz clock will be provided to the microcontroller as the system clock, regardless of the setting of mclk[2:0]. For example, if mclk[2:0] = 000, 30 MHz will be provided through the GPIO output pin to the microcontroller as the system Clock in all IDLE or RX states. When the chip enters SLEEP mode, the system clock will automatically switch to 32.768 kHz from the RC oscillator or 32.768 crystal.

Another available feature for the microcontroller clock is the clock tail, clkt[1:0] in Register 0Ah. Microcontroller Output Clock. If the low frequency clock feature is not enabled (enlfc = 0), the system clock to the microcontroller is disabled in SLEEP mode. However, it may be useful to provide a few extra cycles for the microcontroller to complete its operation prior to the shutdown of the system clock signal. Setting the clkt[1:0] field will provide additional cycles of the system clock before it shuts off.

clkt[1:0]	Clock Frequency
00	0 cycles
01	128 cycles
10	256 cycles
11	512 cycles

If an interrupt is triggered, the microcontroller clock will remain enabled regardless of the selected mode. As soon as the interrupt is read, the state machine will move to the selected mode. For instance, if the chip is commanded to SLEEP mode but an interrupt has occurred, the 30 MHz crystal will be disabled until the interrupt has been cleared.

8.3. Low Battery Detector

A low battery detector (LBD) with digital readout is integrated into the chip. A digital threshold may be programmed into the lbdt[4:0] field in "Register 1Ah. Low Battery Detector Threshold". When the digitized battery voltage reaches this threshold, an interrupt will be generated on the nIRQ pin to the microcontroller. The microcontroller will then confirm the interrupt source by reading "Register 03h. Interrupt/Status 1" and "Register 04h. Interrupt/Status 2."

If the LBD is enabled while the chip is in SLEEP mode, it will automatically enable the RC oscillator, which periodically turns on the LBD circuit to measure the battery voltage. The battery voltage may also be read out through "Register 1Bh. Battery Voltage Level" at any time when the LBD is enabled. The low battery detect function is enabled by setting enlbd = 1 in "Register 07h. Operating Mode and Function Control 1".

Add	R/W	Func/ Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def
1A	R/W	Low Battery Detector Threshold				lbdt[4]	lbdt[3]	lbdt[2]	lbdt[1]	lbdt[0]	14h
1B	R	Battery Voltage Level	0	0	0	vbat[4]	vbat[3]	vbat[2]	vbat[1]	vbat[0]	—

The LBD output is digitized by a 5-bit ADC. When the LBD function is enabled (enlbd = 1 in "Register 07h.

Operating Mode and Function Control 1"), the battery voltage may be read at any time by reading "Register 1Bh. Battery Voltage Level". A battery voltage threshold may be programmed in "Register 1Ah. Low Battery Detector Threshold". When the battery voltage level drops below the battery voltage threshold, an interrupt is generated on the nIRQ pin to the microcontroller if the LBD interrupt is enabled in "Register 06h. Interrupt Enable 2". The microcontroller will then need to verify the interrupt by reading the interrupt status register, addresses 03 and 04h. The LSB step size for the LBD ADC is 50 mV, with the ADC range demonstrated in Table 15. If the LBD is enabled, the LBD and ADC will automatically be enabled every 1 s for approximately 250 μs to measure the voltage which minimizes the current consumption in Sensor mode. Before an interrupt is activated, four consecutive readings are required.

$$\text{Battery Voltage} = 1.7 + 50 \text{ mV} \times \text{ADC}_{\text{VALUE}}$$

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Table 15. LBD ADC Range

ADC Value	VDD Voltage [V]
0	<1.7
1	1.7–1.75
2	1.75–1.8
—	—
29	3.1–3.15
30	3.15–3.2
31	>3.2

8.4. Wake-Up Timer and 32 kHz Clock Source

The chip contains an integrated wake-up timer which can be used to periodically wake the chip from SLEEP mode. The wake-up timer runs from the internal 32.768 kHz RC Oscillator. The wake-up timer can be configured to run when in SLEEP mode. If enwt = 1 in "Register 07h. Operating Mode and Function Control 1" when entering SLEEP mode, the wake-up timer will count for a time specified defined in Registers 14–16h, "Wake Up Timer Period." At the expiration of this period an interrupt will be generated on the nIRQ pin if this interrupt is enabled. The microcontroller will then need to verify the interrupt by reading the Registers 03h–04h, "Interrupt Status 1 & 2". The wake-up timer value may be read at any time by the wtv[15:0] read only registers 17h–18h.

The formula for calculating the Wake-Up Period is the following:

$$WUT = \frac{4 \times M \times 2^R}{32.768} ms$$

| WUT Register	Description
wtr[4:0]	R Value in Formula
wtm[15:0]	M Value in Formula

Use of the D variable in the formula is only necessary if finer resolution is required than can be achieved by using the R value.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
14	R/W	Wake-Up Timer Period 1				wtr[4]	wtr[3]	wtr[2]	wtr[1]	wtr[0]	03h
15	R/W	Wake-Up Timer Period 2	wtm[15]	wtm[14]	wtm[13]	wtm[12]	wtm[11]	wtm[10]	wtm[9]	wtm[8]	00h
16	R/W	Wake-Up Timer Period 3	wtm[7]	wtm[6]	wtm[5]	wtm[4]	wtm[3]	wtm[2]	wtm[1]	wtm[0]	00h
17	R	Wake-Up Timer Value 1	wtv[15]	wtv[14]	wtv[13]	wtv[12]	wtv[11]	wtv[10]	wtv[9]	wtv[8]	—
18	R	Wake-Up Timer Value 2	wtv[7]	wtv[6]	wtv[5]	wtv[4]	wtv[3]	wtv[2]	wtv[1]	wtv[0]	—

There are two different methods for utilizing the wake-up timer (WUT) depending on if the WUT interrupt is enabled in "Register 06h. Interrupt Enable 2." If the WUT interrupt is enabled then nIRQ pin will go low when the timer expires. The chip will also change state so that the 30 MHz XTAL is enabled so that the microcontroller clock output is available for the microcontroller to use to process the interrupt. The other method of use is to not enable the WUT interrupt and use the WUT GPIO setting. In this mode of operation the chip will not change state until commanded by the microcontroller. The different modes of operating the WUT and the current consumption impacts are demonstrated in Figure 11.

A 32 kHz XTAL may also be used for better timing accuracy. By setting the x32 ksel bit in Register 07h "Operating & Function Control 1", GPIO0 is automatically reconfigured so that an external 32 kHz XTAL may be connected to this pin. In this mode, the GPIO0 is extremely sensitive to parasitic capacitance, so only the XTAL should be connected to this pin with the XTAL physically located as close to the pin as possible. Once the x32 ksel bit is set, all internal functions such as WUT, micro-controller clock, and LDC mode will use the 32 kHz XTAL and not the 32 kHz RC oscillator.

Interrupt Enable enwut = 1 (Reg 06h)
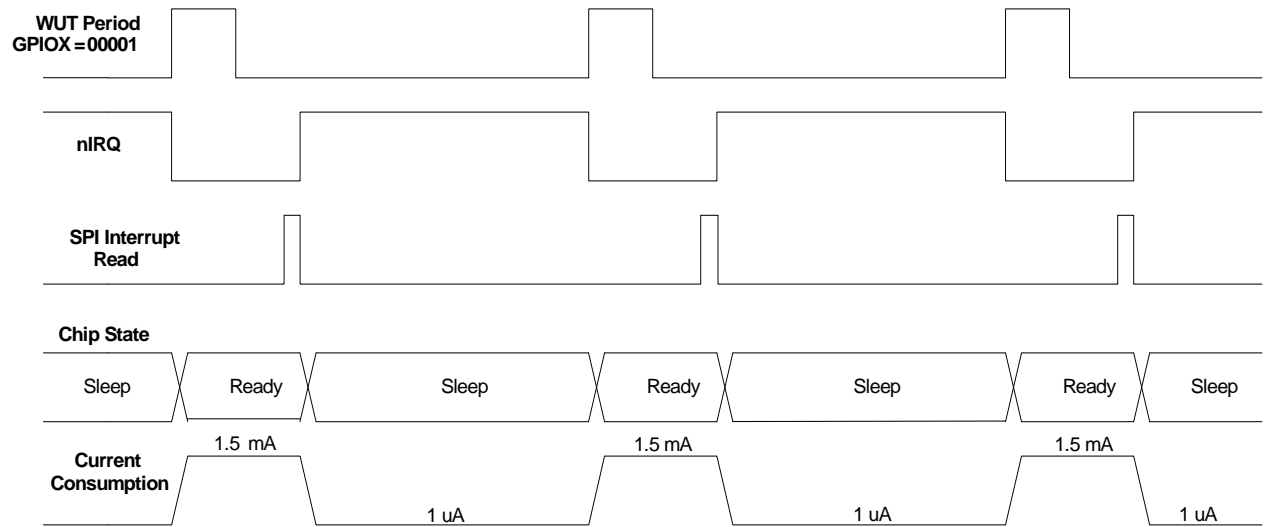
Interrupt Enable enwut = 0 (Reg 06h)
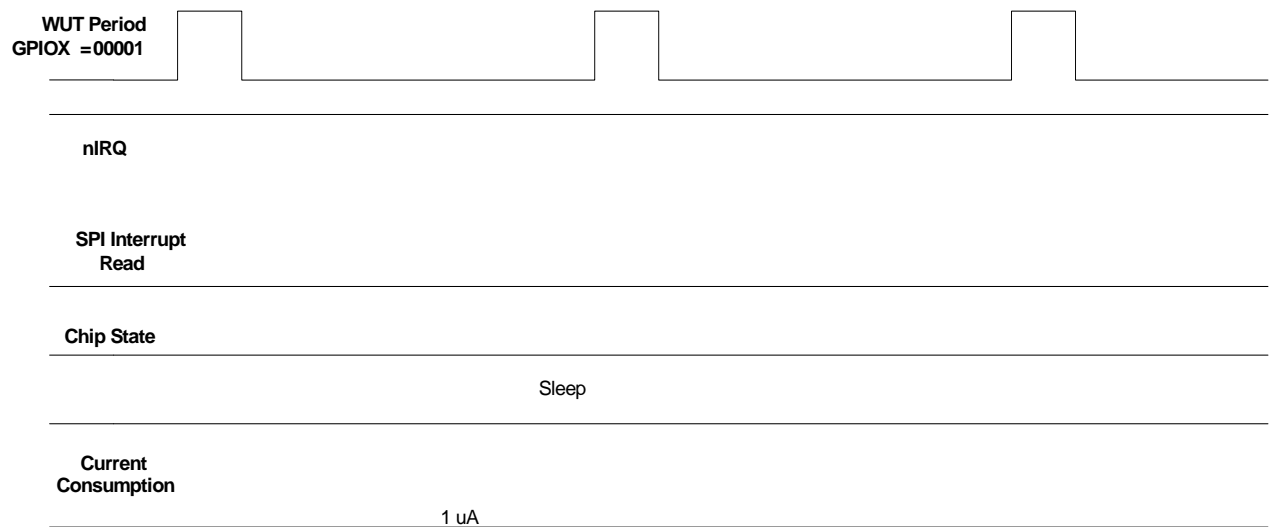
Figure 11. WUT Interrupt and WUT Operation

8.5. Low Duty Cycle Mode

The Low Duty Cycle Mode is available to automatically wake-up the receiver to check if a valid signal is available. The basic operation of the low duty cycle mode is demonstrated in the figure below. If a valid preamble or sync word is not detected the chip will return to sleep mode until the beginning of a new WUT period. If a valid preamble and sync are detected the receiver on period will be extended for the low duty cycle mode duration (TLDC) to receive all of the packet. The WUT period must be set in conjunction with the low duty cycle mode duration. The R value ("Register 14h. Wake-up Timer Period 1") is shared between the WUT and the TLDC. The ldc[7:0] bits are located in "Register 19h. Low Duty Cycle Mode Duration." The time of the TLDC is determined by the formula below:

$$TLDC = ldc\,[7:0] \times \frac{4 \times 2^{R}}{32.768}\,ms$$
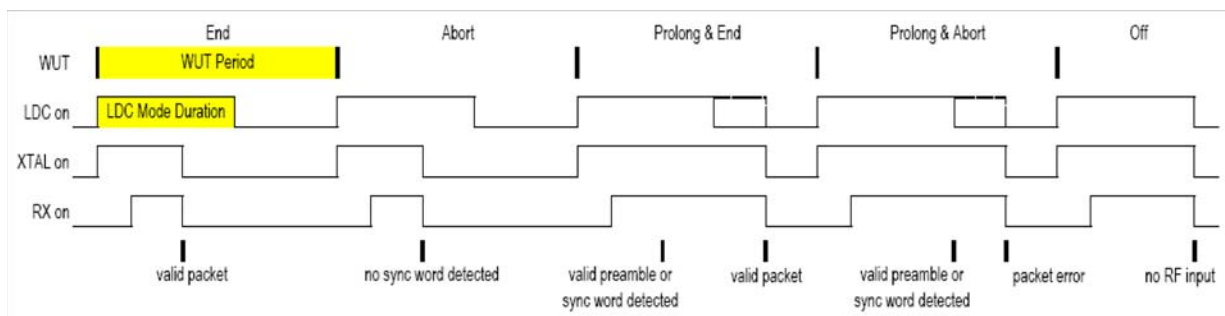
Figure 12. Low Duty Cycle Mode

8.6. GPIO Configuration

Three general purpose IOs (GPIOs) are available. Numerous functions such as specific interrupts, TRSW controlAntenna Diversity Switch control, Microcontroller Output, etc. can be routed to the GPIO pins as shown in the tables below. When in Shutdown mode all the GPIO pads are pulled low.

Note: The ADC should not be selected as an input to the GPIO in standby or sleep modes and will cause excess current consumption.

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
0B	R/W	GPIO0 Configuration	gpio0drv[1]	gpio0drv[0]	pup0	gpio0[4]	gpio0[3]	gpio0[2]	gpio0[1]	gpio0[0]	00h
0C	R/W	GPIO1 Configuration	gpio1drv[1]	gpio1drv[0]	pup1	gpio1[4]	gpio1[3]	gpio1[2]	gpio1[1]	gpio1[0]	00h
0D	R/W	GPIO2 Configuration	gpio2drv[1]	gpio2drv[0]	pup2	gpio2[4]	gpio2[3]	gpio2[2]	gpio2[1]	gpio2[0]	00h
0E	R/W	I/O Port Configuration		extitst[2]	extitst[1]	extitst[0]	itsdo	dio2	dio1	dio0	00h

The GPIO settings for GPIO1 and GPIO2 are the same as for GPIO0 with the exception of the 00000 default setting. The default settings for each GPIO are listed below:

GPIO	00000—Default Setting
GPIO0	POR
GPIO1	POR Inverted
GPIO2	Microcontroller Clock

For a complete list of the available GPIOs see "AN440: EZRadioPRO Detailed Register Descriptions".

The GPIO drive strength may be adjusted with the gpioXdrv[1:0] bits. Setting a higher value will increase the drive strength and current capability of the GPIO by changing the driver size. Special care should be taken in setting the drive strength and loading on GPIO2 when the microcontroller clock is used. Excess loading or inadequate drive may contribute to increased spurious emissions.

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8.7. RSSI and Clear Channel Assessment

Received signal strength indicator (RSSI) is an estimate of the signal strength in the channel to which the receiver is tuned. The RSSI value can be read from an 8-bit register with 0.5 dB resolution per bit. Figure 13 demonstrates the relationship between input power level and RSSI value. The absolute value of the RSSI will change slightly depending on the modem settings. The RSSI may be read at anytime, but an incorrect error may rarely occur. The RSSI value may be incorrect if read during the update period. The update period is approximately 10 ns every 4 Tb. For 10 kbps, this would result in a 1 in 40,000 probability that the RSSI may be read incorrectly. This probability is extremely low, but to avoid this, one of the following options is recommended: majority polling, reading the RSSI value within 1 Tb of the RSSI interrupt, or using the RSSI threshold described in the next paragraph for Clear Channel Assessment (CCA).

Add	R/W	Function/Description	D7	D6	D5	D4	D3	D2	D1	D0	POR Def.
26	R	Received Signal Strength Indicator	rssi[7]	rssi[6]	rssi[5]	rssi[4]	rssi[3]	rssi[2]	rssi[1]	rssi[0]	—
27	R/W	RSSI Threshold for Clear Channel Indicator	rssith[7]	rssith[6]	rssith[5]	rssith[4]	rssith[3]	rssith[2]	rssith[1]	rssith[0]	00h

For CCA, threshold is programmed into rssith[7:0] in "Register 27h. RSSI Threshold for Clear Channel Indicator." After the RSSI is evaluated in the preamble, a decision is made if the signal strength on this channel is above or below the threshold. If the signal strength is above the programmed threshold then the RSSI status bit, irssi, in "Register 04h. Interrupt/Status 2" will be set to 1. The RSSI status can also be routed to a GPIO line by configuring the GPIO configuration register to GPIOx[3:0] = 1110.

RSSI vs Input Power

Figure 13. RSSI Value vs. Input Power

9. Reference Design

Reference designs, including recommended schematics, BOM, and layouts for many common applications, are available at www.silabs.com.

Figure 14. Reference Test Card

10. Application Notes and Reference Material

- "AN414: EZRadioPRO Layout Design Guide"
- "AN415: EZRadioPRO Programming Guide"
- "AN417: Si4x3x Family Crystal Oscillators"
- "AN429: Using the DC-DC Converter on the F9xx Series MCU for Single Battery Operation with the EZRadioPRO RF Devices"
- "AN432: RX BER Measurement on EZRadioPRO with a Looped PN Sequence"
- "AN439: EZRadioPRO RF Testing QuickStart Guide"
- "AN440: EZRadioPRO Detailed Register Descriptions"
- "AN453: Advanced RX BW Calculations and Settings"
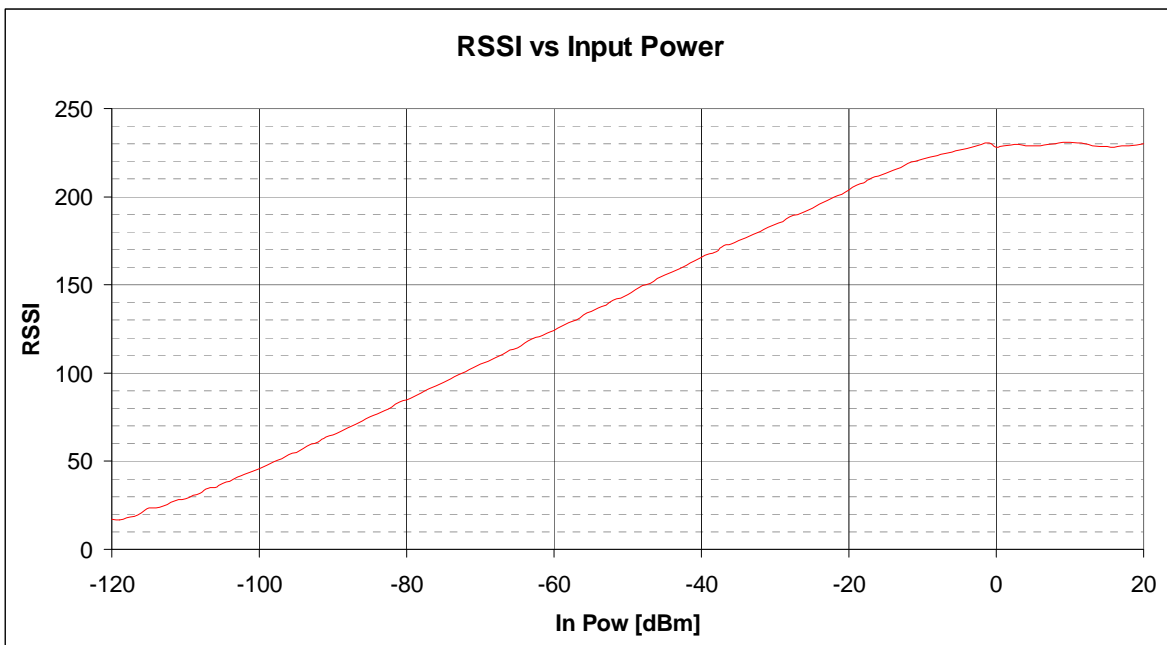
11. Customer Support

Technical support for the complete family of Silicon Labs wireless products is available by accessing the wireless section of the Silicon Labs' website at www.silabs.com/wireless. For answers to common questions please visit the wireless Knowledge Base at www.silabs.com/support/knowledgebase.

11.1. RX LNA Matching

All that is required is a 150 pF coupling capacitor between antenna and RX input.

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12. Register Table and Descriptions
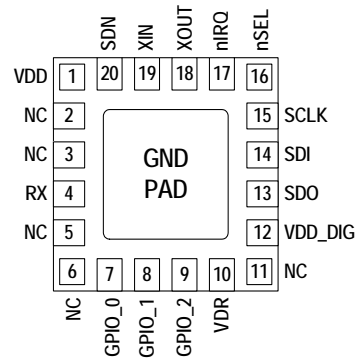
Table 16. Register Descriptions

Add	R/W	Function/Desc	D7	D6	D5	D4	D3	D2	D1	D0	POR Default
01	R	Device Version	0	0	0	vc[4]	vc[3]	vc[2]	vc[1]	vc[0]	06h
02	R	Device Status	ffovfl	ffunfl	rxffem	headerr	Reserved	Reserved	cps[1]	cps[0]	—
03	R	Interrupt Status 1	ifferr	Reserved	Reserved	irxffafull	iext	Reserved	ipkvalid	icrcerror	—
04	R	Interrupt Status 2	iswdet	ipreaval	ipreainval	irssi	iwut	ilbd	ichiprdy	ipor	—
05	R/W	Interrupt Enable 1	enfferr	Reserved	Reserved	enrxffafull	enext	Reserved	enpkvalid	encrcerror	00h
06	R/W	Interrupt Enable 2	enswdet	enpreaval	enpreainval	enrssi	enwut	enlbd	enchiprdy	enpor	03h
07	R/W	Operating & Function Control 1	swres	enlbd	enwt	x32ksel	Reserved	rxon	pllon	xton	01h
08	R/W	Operating & Function Control 2	antdiv[2]	antdiv[1]	antdiv[0]	rxmpk	Reserved	enldm	ffclrrx	Reserved	00h
09	R/W	Crystal Oscillator Load Capacitance	xtalshft	xlc[6]	xlc[5]	xlc[4]	xlc[3]	xlc[2]	xlc[1]	xlc[0]	7Fh
0A	R/W	Microcontroller Output Clock	Reserved	Reserved	clkt[1]	clkt[0]	enlfc	mclk[2]	mclk[1]	mclk[0]	06h
0B	R/W	GPIO0 Configuration	gpio0drv[1]	gpio0drv[0]	pup0	gpio0[4]	gpio0[3]	gpio0[2]	gpio0[1]	gpio0[0]	00h
0C	R/W	GPIO1 Configuration	gpio1drv[1]	gpio1drv[0]	pup1	gpio1[4]	gpio1[3]	gpio1[2]	gpio1[1]	gpio1[0]	00h
0D	R/W	GPIO2 Configuration	gpio2drv[1]	gpio2drv[0]	pup2	gpio2[4]	gpio2[3]	gpio2[2]	gpio2[1]	gpio2[0]	00h
0E	R/W	I/O Port Configuration	Reserved	extitst[2]	extitst[1]	extitst[0]	itsdo	dio2	dio1	dio0	00h
0F	R/W	ADC Configuration	adcstart/adc-done	adcsel[2]	adcsel[1]	adcsel[0]	adcref[1]	adcref[0]	adcgain[1]	adcgain[0]	00h
10	R/W	ADC Sensor Amplifier Offset	Reserved	Reserved	Reserved	Reserved	adcoffs[3]	adcoffs[2]	adcoffs[1]	adcoffs[0]	00h
11	R	ADC Value	adc[7]	adc[6]	adc[5]	adc[4]	adc[3]	adc[2]	adc[1]	adc[0]	—
12	R/W	Temperature Sensor Control	tsrange[1]	tsrange[0]	entsoffs	entstrim	tstrim[3]	tstrim[2]	tstrim[1]	tstrim[0]	20h
13	R/W	Temperature Value Offset	tvoffs[7]	tvoffs[6]	tvoffs[5]	tvoffs[4]	tvoffs[3]	tvoffs[2]	tvoffs[1]	tvoffs[0]	00h
14	R/W	Wake-Up Timer Period 1	Reserved	Reserved	Reserved	wtr[4]	wtr[3]	wtr[2]	wtr[1]	wtr[0]	03h
15	R/W	Wake-Up Timer Period 2	wtm[15]	wtm[14]	wtm[13]	wtm[12]	wtm[11]	wtm[10]	wtm[9]	wtm[8]	00h
16	R/W	Wake-Up Timer Period 3	wtm[7]	wtm[6]	wtm[5]	wtm[4]	wtm[3]	wtm[2]	wtm[1]	wtm[0]	01h
17	R	Wake-Up Timer Value 1	wtv[15]	wtv[14]	wtv[13]	wtv[12]	wtv[11]	wtv[10]	wtv[9]	wtv[8]	—
18	R	Wake-Up Timer Value 2	wtv[7]	wtv[6]	wtv[5]	wtv[4]	wtv[3]	wtv[2]	wtv[1]	wtv[0]	—
19	R/W	Low-Duty Cycle Mode Duration	ldc[7]	ldc[6]	ldc[5]	ldc[4]	ldc[3]	ldc[2]	ldc[1]	ldc[0]	00h
1A	R/W	Low Battery Detector Threshold	Reserved	Reserved	Reserved	lbdt[4]	lbdt[3]	lbdt[2]	lbdt[1]	lbdt[0]	14h
1B	R	Battery Voltage Level	0	0	0	vbat[4]	vbat[3]	vbat[2]	vbat[1]	vbat[0]	—
1C	R/W	IF Filter Bandwidth	dwn3_bypass	ndec[2]	ndec[1]	ndec[0]	filset[3]	filset[2]	filset[1]	filset[0]	01h
1D	R/W	AFC Loop Gearshift Override	afcbd	enafc	afcgearh[2]	afcgearh[1]	afcgearh[0]	1p5 bypass	matap	ph0size	40h
1E	R/W	AFC Timing Control	swait_timer[1]	swait_timer[0]	shwait[2]	shwait[1]	shwait[0]	anwait[2]	anwait[1]	anwait[0]	0Ah
1F	R/W	Clock Recovery Gearshift Override	Reserved	Reserved	crfast[2]	crfast[1]	crfast[0]	crslow[2]	crslow[1]	crslow[0]	03h
20	R/W	Clock Recovery Oversampling Ratio	rxosr[7]	rxosr[6]	rxosr[5]	rxosr[4]	rxosr[3]	rxosr[2]	rxosr[1]	rxosr[0]	64h
21	R/W	Clock Recovery Offset 2	rxosr[10]	rxosr[9]	rxosr[8]	stallctrl	ncoff[19]	ncoff[18]	ncoff[17]	ncoff[16]	01h
22	R/W	Clock Recovery Offset 1	ncoff[15]	ncoff[14]	ncoff[13]	ncoff[12]	ncoff[11]	ncoff[10]	ncoff[9]	ncoff[8]	47h
23	R/W	Clock Recovery Offset 0	ncoff[7]	ncoff[6]	ncoff[5]	ncoff[4]	ncoff[3]	ncoff[2]	ncoff[1]	ncoff[0]	AEh
24	R/W	Clock Recovery Timing Loop Gain 1	Reserved	Reserved	Reserved	rxncocomp	crgain2x	crgain[10]	crgain[9]	crgain[8]	02h
25	R/W	Clock Recovery Timing Loop Gain 0	crgain[7]	crgain[6]	crgain[5]	crgain[4]	crgain[3]	crgain[2]	crgain[1]	crgain[0]	8Fh
26	R	Received Signal Strength Indicator	rssi[7]	rssi[6]	rssi[5]	rssi[4]	rssi[3]	rssi[2]	rssi[1]	rssi[0]	—
27	R/W	RSSI Threshold for Clear Channel Indicator	rssith[7]	rssith[6]	rssith[5]	rssith[4]	rssith[3]	rssith[2]	rssith[1]	rssith[0]	1Eh

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Table 16. Register Descriptions (Continued)

Add	R/W	Function/Desc	D7	D6	D5	D4	D3	D2	D1	D0	POR Default
28	R	Antenna Diversity Register 1	adrssi1[7]	adrssia[6]	adrssia[5]	adrssia[4]	adrssia[3]	adrssia[2]	adrssia[1]	adrssia[0]	—
29	R	Antenna Diversity Register 2	adrssib[7]	adrssib[6]	adrssib[5]	adrssib[4]	adrssib[3]	adrssib[2]	adrssib[1]	adrssib[0]	—
2A	R/W	AFC Limiter	Afclim[7]	Afclim[6]	Afclim[5]	Afclim[4]	Afclim[3]	Afclim[2]	Afclim[1]	Afclim[0]	00h
2B	R	AFC Correction Read	afc_corr[9]	afc_corr[8]	afc_corr[7]	afc_corr[6]	afc_corr[5]	afc_corr[4]	afc_corr[3]	afc_corr[2]	00h
2C	R/W	OOK Counter Value 1	afc_corr[9]	afc_corr[9]	ookfrzen	peakdeten	madeten	ookcnt[10]	ookcnt[9]	ookcnt[8]	18h
2D	R/W	OOK Counter Value 2	ookcnt[7]	ookcnt[6]	ookcnt[5]	ookcnt[4]	ookcnt[3]	ookcnt[2]	ookcnt[1]	ookcnt[0]	BCh
2E	R/W	Slicer Peak Hold	Reserved	attack[2]	attack[1]	attack[0]	decay[3]	decay[2]	decay[1]	decay[0]	26h
2F-34		Reserved									
35	R/W	Preamble Detection Control	preath[4]	preath[3]	preath[2]	preath[1]	preath[0]	rssi_off[2]	rssi_off[1]	rssi_off[0]	2Ah
36	R/W	Sync Word 3	sync[31]	sync[30]	sync[29]	sync[28]	sync[27]	sync[26]	sync[25]	sync[24]	2Dh
37	R/W	Sync Word 2	sync[23]	sync[22]	sync[21]	sync[20]	sync[19]	sync[18]	sync[17]	sync[16]	D4h
38	R/W	Sync Word 1	sync[15]	sync[14]	sync[13]	sync[12]	sync[11]	sync[10]	sync[9]	sync[8]	00h
39	R/W	Sync Word 0	sync[7]	sync[6]	sync[5]	sync[4]	sync[3]	sync[2]	sync[1]	sync[0]	00h
3A-4E		Reserved									
4F	R/W	ADC8 Control	Reserved	Reserved	adc8[5]	adc8[4]	adc8[3]	adc8[2]	adc8[1]	adc8[0]	10h
50-5F		Reserved									
60	R/W	Channel Filter Coefficient Address	Inv_pre_th[3]	Inv_pre_th[2]	Inv_pre_th[1]	Inv_pre_th[0]	chfiladd[3]	chfiladd[2]	chfiladd[1]	chfiladd[0]	00h
61		Reserved									
62	R/W	Crystal Oscillator/Control Test	pwst[2]	pwst[1]	pwst[0]	clkhyst	enbias2x	enamp2x	bufovr	enbuf	24h
63-68		Reserved									
69	R/W	AGC Override 1	Reserved	sgi	agcen	lnagain	pga3	pga2	pga1	pga0	20h
6A-6C		Reserved									
70	R/W	Modulation Mode Control 1	Reserved	Reserved	txdtrtscale	enphpwdn	manppol	enmaninv	enmanch	enwhite	0Ch
71	R/W	Modulation Mode Control 2	trclk[1]	trclk[0]	dtmod[1]	dtmod[0]	eninv	fd[8]	modtyp[1]	modtyp[0]	00h
73	R/W	Frequency Offset 1	fo[7]	fo[6]	fo[5]	fo[4]	fo[3]	fo[2]	fo[1]	fo[0]	00h
74	R/W	Frequency Offset 2	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	fo[9]	fo[8]	00h
75	R/W	Frequency Band Select	Reserved	sbsel	hbsel	fb[4]	fb[3]	fb[2]	fb[1]	fb[0]	75h
76	R/W	Nominal Carrier Frequency 1	fc[15]	fc[14]	fc[13]	fc[12]	fc[11]	fc[10]	fc[9]	fc[8]	BBh
77	R/W	Nominal Carrier Frequency 0	fc[7]	fc[6]	fc[5]	fc[4]	fc[3]	fc[2]	fc[1]	fc[0]	80h
78		Reserved									
79	R/W	Frequency Hopping Channel Select	fhch[7]	fhch[6]	fhch[5]	fhch[4]	fhch[3]	fhch[2]	fhch[1]	fhch[0]	00h
7A	R/W	Frequency Hopping Step Size	fhs[7]	fhs[6]	fhs[5]	fhs[4]	fhs[3]	fhs[2]	fhs[1]	fhs[0]	00h
7B		Reserved									
7E	R/W	RX FIFO Control	Reserved	Reserved	rxafthr[5]	rxafthr[4]	rxafthr[3]	rxafthr[2]	rxafthr[1]	rxafthr[0]	37h
7F	R/W	FIFO Access	fifod[7]	fifod[6]	fifod[5]	fifod[4]	fifod[3]	fifod[2]	fifod[1]	fifod[0]	—

Note: Detailed register descriptions are available in "AN485: Si4313 Detailed Register Descriptions."

13. Pin Descriptions: Si4313

Pin	Pin Name	I/O	Description
1	VDD_RF	VDD	+1.8 to +3.6 V supply voltage input to all analog +1.7 V regulators. The recommended V_{DD} supply voltage is +3.3 V.
2	TX	O	Transmit output pin. The PA output is an open-drain connection; so, the L-C match must supply VDD (+3.3 VDC nominal) to this pin.
3	NC	—	No Connect.
4	RX	—	No Connect.
5	NC	—	No Connect. Not connected internally to any circuitry.
6	NC	O	No Connect
7	GPIO_0	I/O	General Purpose Digital I/O that may be configured through the registers to perform various functions including: Microcontroller Clock Output, FIFO status, POR, Wake-Up timer, Low Battery Detect, AntDiversity control, etc. See the SPI GPIO Configuration Registers, Address 0Bh, 0Ch, and 0Dh for more information.
8	GPIO_1	I/O	
9	GPIO_2	I/O	
10	VDR	O	Regulated Output Voltage of the Digital 1.7 V Regulator. A 1 µF decoupling capacitor is required.
11	NC	—	Internally this pin is tied to the paddle of the package. This pin should be left unconnected or connected to GND only.
12	VDD_DIG	VDD	+1.8 to +3.6 V supply voltage input to the Digital +1.7 V Regulator. The recommended V_{DD} supply voltage is +3.3 V.
13	SDO	O	0–V_{DD} V digital output that provides a serial readback function of the internal control registers.
14	SDI	I	Serial Data input. 0–V_{DD} V digital input. This pin provides the serial data stream for the 4-line serial data bus.
15	SCLK	I	Serial Clock input. 0–V_{DD} V digital input. This pin provides the serial data clock function for the 4-line serial data bus. Data is clocked into the Si4313 on positive edge transitions.
16	nSEL	I	Serial Interface Select input. 0–V_{DD} V digital input. This pin provides the Select/Enable function for the 4-line serial data bus. The signal is also used to signify burst read/write mode.
17	nIRQ	O	General Microcontroller Interrupt Status output. When the Si4313 exhibits anyone of the Interrupt Events the nIRQ pin will be set low=0. Please see the Control Logic registers section for more information on the Interrupt Events. The Microcontroller can then determine the state of the interrupt by reading a corresponding SPI Interrupt Status Registers, Address 03h and 04h. No external resistor pull-up is required, but it may be desirable if multiple interrupt lines are connected.
18	XOUT	O	Crystal Oscillator Output. Connect to an external 30 MHz crystal or leave floating if driving the Xin pin with an external signal source.
19	XIN	I	Crystal Oscillator Input. Connect to an external 30 MHz crystal or to an external source. If using an external clock source with no crystal, dc coupling with a nominal 0.8 VDC level is recommended with a minimum ac amplitude of 700 mVpp.
20	SDN	I	Shutdown input pin. 0–V_{DD} V digital input. SDN should be = 0 in all modes except Shutdown mode. When SDN =1 the chip will be completely shutdown and the contents of the registers will be lost.
PKG	PADDLE_GND	GND	The exposed metal paddle on the bottom of the Si4313 supplies the RF and circuit ground(s) for the entire chip. It is very important that a good solder connection is made between this exposed metal paddle and the ground plane of the PCB underlying the Si4313.

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14. Ordering Information

Part Number	Description	Package Type	Operating Temperature
Si4313-B1-FM	ISM Receiver	QFN-20 Pb-free	–40 to 85 °C
*Note: Add an (R) at the end of the device part number to denote tape and reel option; 2500 quantity per reel.			

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15. Package Outline: Si4313-B1

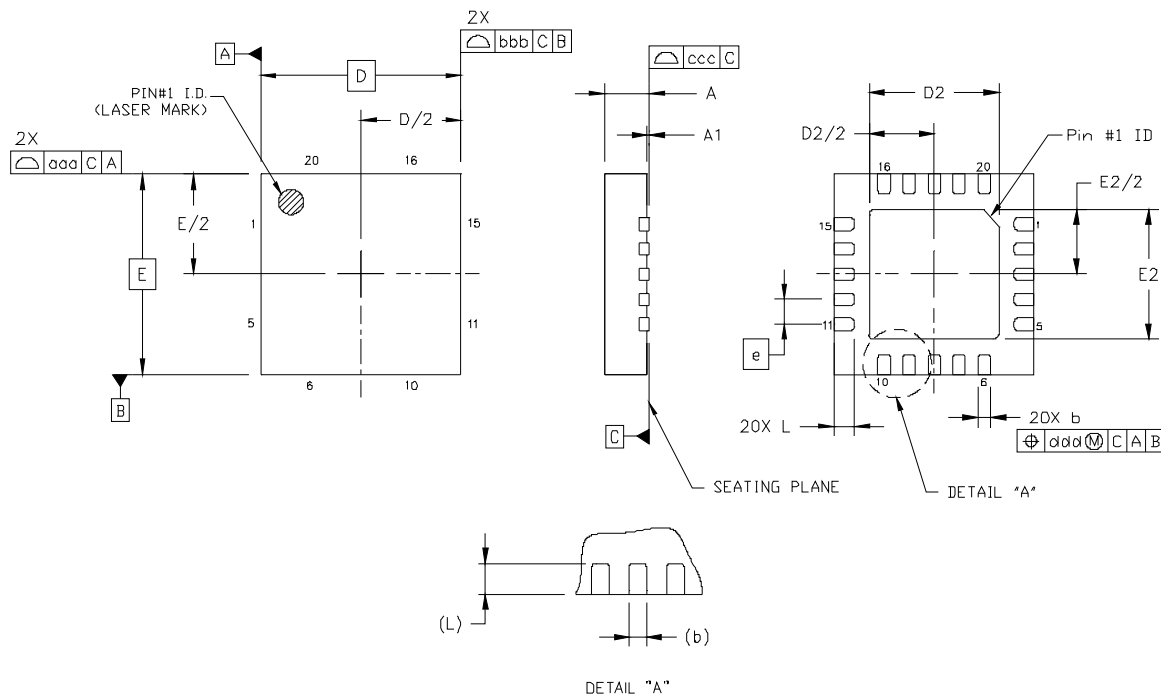Figure 15 illustrates the package details for the Si4313-B1. Table 17 lists the values for the dimensions shown in the illustration.

Figure 15. 20-Pin Quad Flat No-Lead (QFN)

Table 17. Package Dimensions

Symbol	Millimeters		
	Min	Nom	Max
A	0.80	0.85	0.90
A1	0.00	0.02	0.05
b	0.18	0.25	0.30
D	4.00 BSC		
D2	2.55	2.60	2.65
e	0.50 BSC		
E	4.00 BSC		
E2	2.50	2.60	2.70
L	0.30	0.40	0.50
aaa	—	—	0.10
bbb	—	—	0.10
ccc	—	—	0.08
ddd	—	—	0.10
eee	—	—	0.10

Notes:
1. All dimensions are shown in millimeters (mm) unless otherwise noted.
2. Dimensioning and tolerancing per ANSI Y14.5M-1994.
3. This drawing conforms to the JEDEC Solid State Outline MO-220, Variation VGGD-8.
4. Recommended card reflow profile is per the JEDEC/IPC J-STD-020C specification for Small Body Components.

16. Landing Pattern: 20-Pin QFN

Figure 16 shows the recommended landing pattern details for the Si4313-B1 in a 20-Pin QFN package. Table 18 lists the values for the dimensions shown in the illustration.
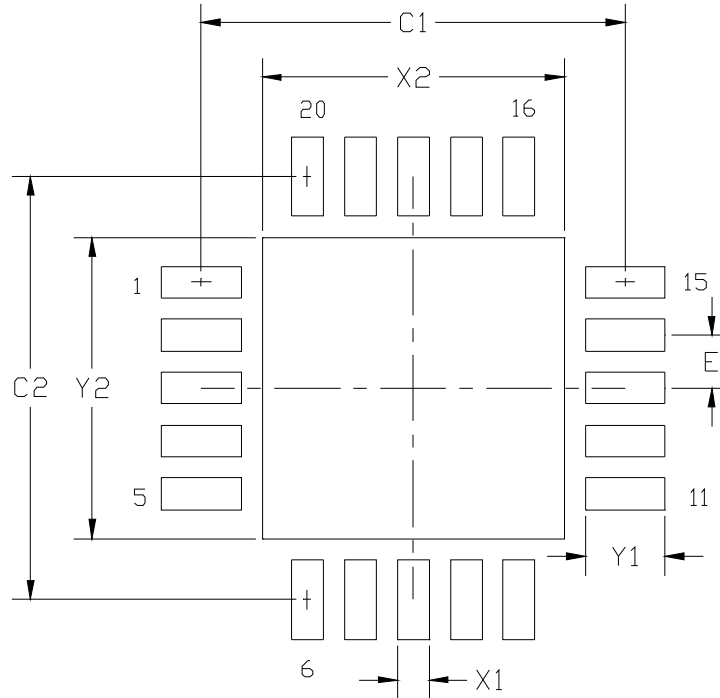
Figure 16. 20-Pin QFN Landing Pattern

Table 18. PCB Land Pattern Dimensions

Symbol	Millimeters	
	Min	**Max**
C1	3.90	4.00
C2	3.90	4.00
E	0.50 REF	
X1	0.20	0.30
X2	2.65	2.75
Y1	0.65	0.75
Y2	2.65	2.75

Notes:
General

   1. All dimensions shown are in millimeters (mm) unless otherwise noted.
   2. This land pattern design is based on IPC-7351 guidelines.

Solder Mask Design

   3. All metal pads are to be non-solder mask defined (NSMD). Clearance between the solder mask and the metal pad is to be 60 µm minimum, all the way around the pad.

Stencil Design

   4. A stainless steel, laser-cut and electro-polished stencil with trapezoidal walls should be used to assure good solder paste release.
   5. The stencil thickness should be 0.125 mm (5 mils).
   6. The ratio of stencil aperture to land pad size should be 1:1 for the perimeter pads.
   7. A 2x2 array of 1.10 x 1.10 mm openings on 1.30 mm pitch should be used for the center ground pad.

Card Assembly

   8. A No-Clean, Type-3 solder paste is recommended.
   9. The recommended card reflow profile is per the JEDEC/IPC J-STD-020 specification for small body components.

17. Top Marking: 20-Pin QFN
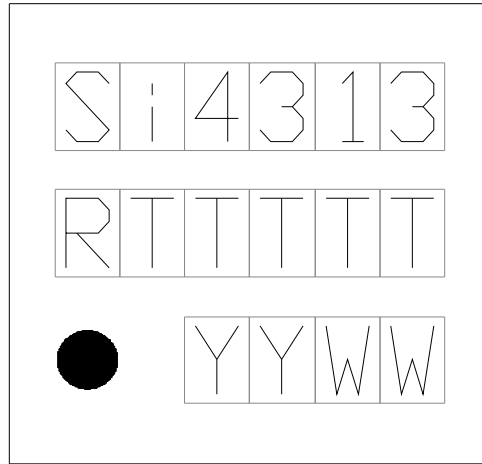
Figure 17. Si4313 Top Marking

17.1. Top Mark Explanation

Mark Method:	YAG Laser	
Line 1 Marking:	X = Part Number	0 = Si4313
Line 2 Marking:	R = Die Revision	B = Revision B1
	TTTTT = Internal Code	Internal tracking code.
Line 3 Marking:	YY = Year WW = Workweek	Assigned by the Assembly House. Corresponds to the last significant digit of the year and workweek of the mold date.

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NOTES:

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