

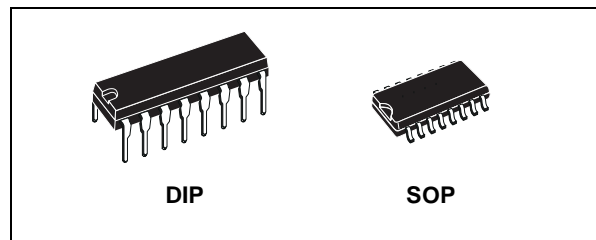


## QUAD LOW-TO-HIGH VOLTAGE LEVEL SHIFTER

- INDEPENDENCE OF POWER SUPPLY SEQUENCE CONSIDERATIONS -  $V_{CC}$  CAN EXCEED  $V_{DD}$ , INPUT SIGNALS CAN EXCEED BOTH  $V_{CC}$  AND  $V_{DD}$
- UP AND DOWN LEVEL SHIFTING CAPABILITY
- THREE-STATE OUTPUTS WITH SEPARATE ENABLE CONTROLS
- STANDARDIZED SYMMETRICAL OUTPUT CHARACTERISTICS
- QUIESCENT CURRENT SPECIFIED UP TO 20V
- 5V, 10V, AND 15V PARAMETRIC RATINGS
- INPUT LEAKAGE CURRENT  
 $I_l = 100\text{nA}$  (MAX) AT  $V_{DD} = 18\text{V}$   $T_A = 25^\circ\text{C}$
- 100% TESTED FOR QUIESCENT CURRENT
- MEETS ALL REQUIREMENTS OF JEDEC JESD13B "STANDARD SPECIFICATIONS FOR DESCRIPTION OF B SERIES CMOS DEVICES"

### DESCRIPTION

HCF40109B is a monolithic integrated circuit fabricated in Metal Oxide Semiconductor technology available in DIP and SOP packages. HCF40109B contains four low-to-high voltage level shifting circuits. Each circuit will shift a low-voltage digital-logic input signal (A, B, C, D) with logical 1 =  $V_{CC}$  and logical 0 =  $V_{SS}$  to a higher voltage output signal (E, F, G, H) with logical 1 =  $V_{DD}$  and logical 0 =  $V_{SS}$ . HCF40109B, unlike other

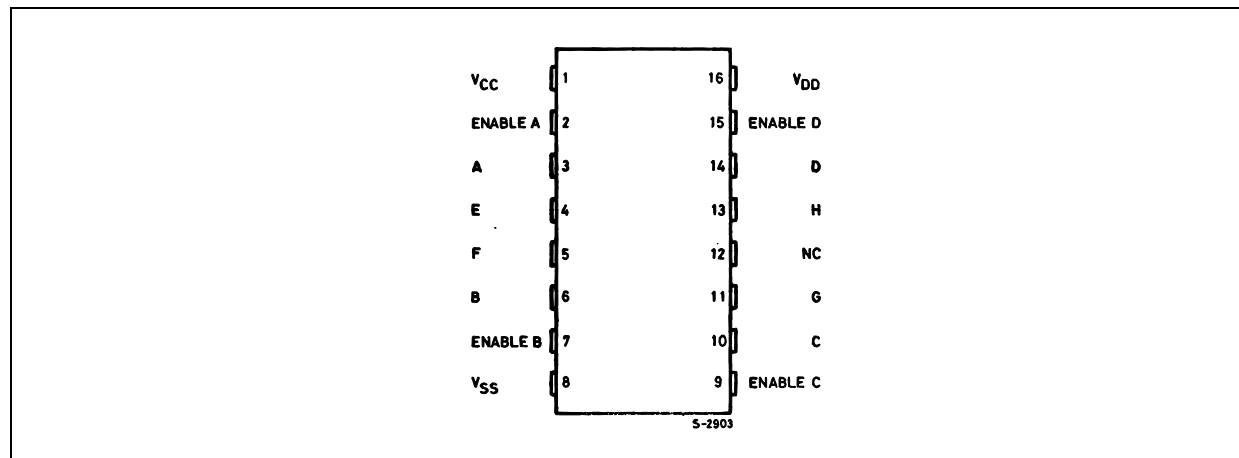


### ORDER CODES

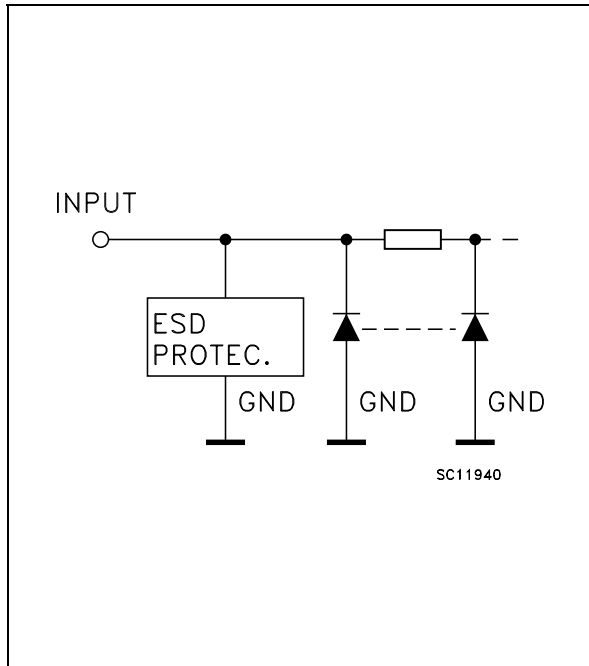
PACKAGE	TUBE	T & R
DIP	HCF40109BEY	
SOP	HCF40109BM1	HCF40109M013TR

low-to-high level-shifting circuits, does not require the presence of the high voltage supply ( $V_{DD}$ ) before the application of either the low-voltage supply ( $V_{CC}$ ) or the input signals. There are no restrictions on the sequence of application of  $V_{DD}$ ,  $V_{CC}$ , or the input signals. In addition, there are no restrictions on the relative magnitudes of the supply voltages or input signals within the device maximum ratings;  $V_{CC}$  may exceed  $V_{DD}$ , and input signals may exceed  $V_{CC}$  and  $V_{DD}$ . When operated in the mode  $V_{CC} = V_{DD}$ , HCF40109B will operate as a high-to-low level-shifter. HCF40109B also features individual three-state output capability. A low level on any of the separately enabled three-state output controls produces a high-impedance state in the corresponding output.

### PIN CONNECTION



**INPUT EQUIVALENT CIRCUIT**



**PIN DESCRIPTION**

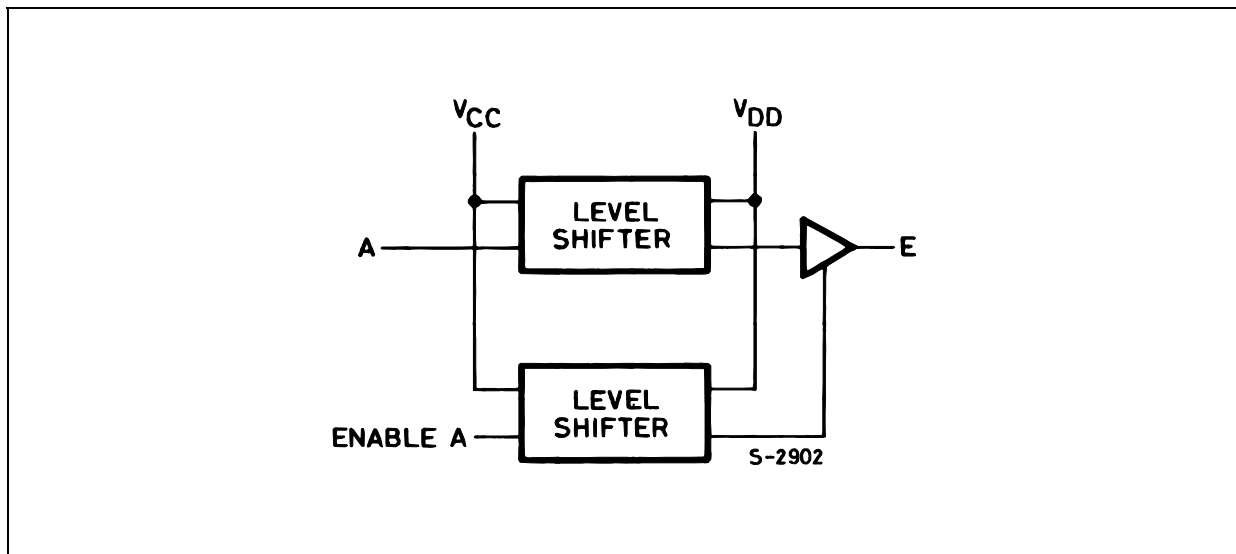
PIN No	SYMBOL	NAME AND FUNCTION
3, 6, 10, 14	A, B, C, D	Low Input Voltage
4, 5, 11, 13	E, F, G, H	High Input Voltage
2, 7, 9, 15	ENABLE A, B, C, D	Enable Input
12	NC	Not Connected
1	V <sub>CC</sub>	Low Supply Voltage
8	V <sub>SS</sub>	Negative Supply Voltage
16	V <sub>DD</sub>	Positive Supply Voltage

**TRUTH TABLE**

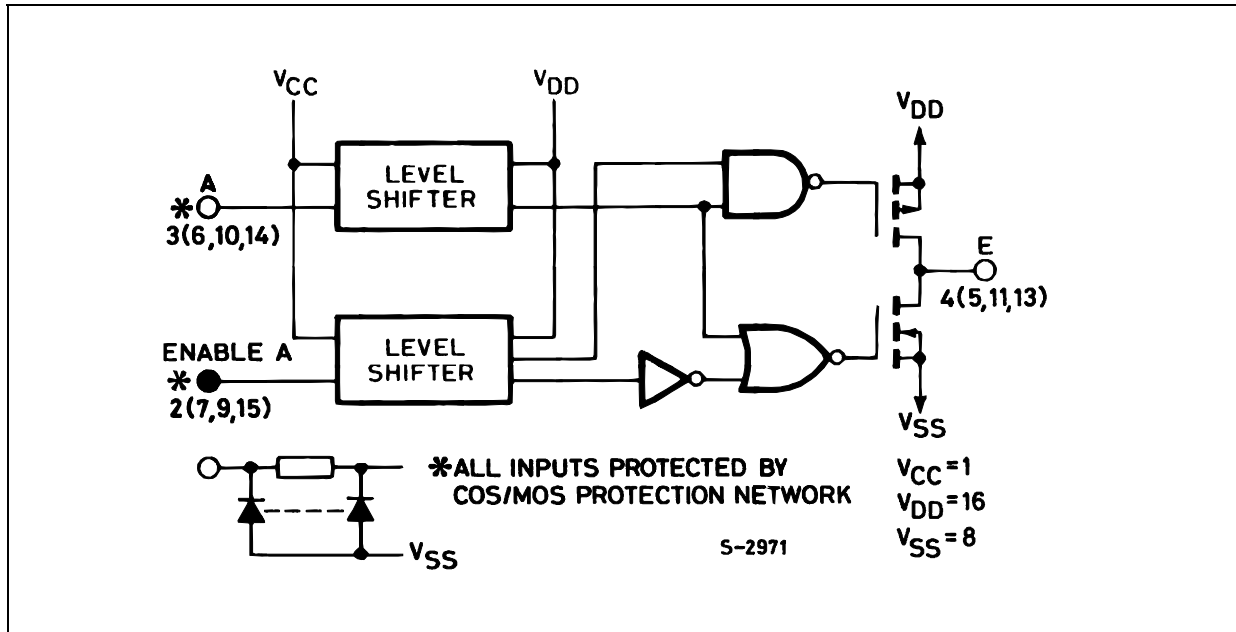
MODE	INPUTS		OUTPUT
	A, B, C, D	Enable A, B, C, D	E, F, G, H
Low to High Level Shift	L	H	L
	H	H	H
	X	L	Z

X : Don't Care  
Z : High Impedance

**FUNCTIONAL DIAGRAM**



LOGIC DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	-0.5 to +22	V
$V_I$	DC Input Voltage	-0.5 to +18	V
$I_I$	DC Input Current	$\pm 10$	mA
$P_D$	Power Dissipation per Package	200	mW
	Power Dissipation per Output Transistor	100	mW
$T_{op}$	Operating Temperature	-55 to +125	$^{\circ}C$
$T_{stg}$	Storage Temperature	-65 to +150	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.  
 All voltage values are referred to  $V_{SS}$  pin voltage.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
$V_{DD}$	Supply Voltage	3 to 20	V
$V_I$	Input Voltage	-0.5 to 15V	V
$T_{op}$	Operating Temperature	-55 to 125	$^{\circ}C$

DC SPECIFICATIONS

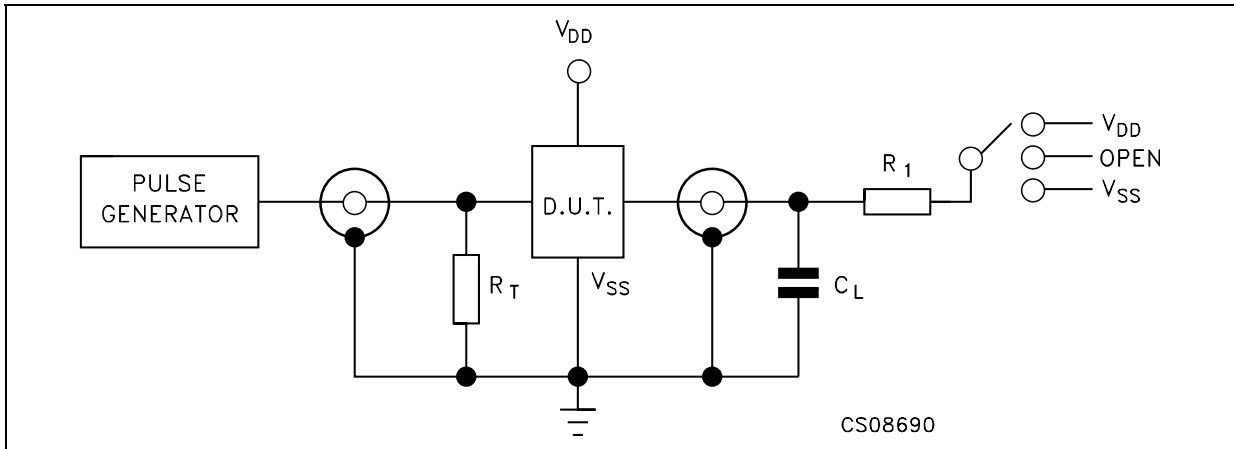
Symbol	Parameter	Test Condition				Value						Unit	
		V <sub>I</sub> (V)	V <sub>O</sub> (V)	I <sub>OL</sub>   ( $\mu$ A)	V <sub>DD</sub> (V)	T <sub>A</sub> = 25°C			-40 to 85°C		-55 to 125°C		
						Min.	Typ.	Max.	Min.	Max.	Min.		Max.
I <sub>L</sub>	Quiescent Current	0/5			5		0.02	1		30		30	$\mu$ A
		0/10			10		0.02	2		60		60	
		0/15			15		0.02	4		120		120	
		0/20			20		0.04	20		600		600	
V <sub>OH</sub>	High Level Output Voltage	0/5		<1	5	4.95			4.95		4.95		V
		0/10		<1	10	9.95			9.95		9.95		
		0/15		<1	15	14.95			14.95		14.95		
V <sub>OL</sub>	Low Level Output Voltage	5/0		<1	5		0.05			0.05		0.05	V
		10/0		<1	10		0.05			0.05		0.05	
		15/0		<1	15		0.05			0.05		0.05	
V <sub>IH</sub>	High Level Input Voltage		0.5/4.5	<1	5	3.5			3.5		3.5		V
			1/9	<1	10	7			7		7		
			1.5/13.5	<1	15	11			11		11		
V <sub>IL</sub>	Low Level Input Voltage		4.5/0.5	<1	5			1.5		1.5		1.5	V
			9/1	<1	10			3		3		3	
			13.5/1.5	<1	15			4		4		4	
I <sub>OH</sub>	Output Drive Current	0/5	2.5	<1	5	-1.53	-3.2		-1.36		-1.1		mA
		0/5	4.6	<1	5	-0.52	-1		-0.44		-0.36		
		0/10	9.5	<1	10	-1.3	-2.6		-1.1		-0.9		
		0/15	13.5	<1	15	-3.6	-6.8		-3.0		-2.4		
I <sub>OL</sub>	Output Sink Current	0/5	0.4	<1	5	0.52	1		0.44		0.36		mA
		0/10	0.5	<1	10	1.3	2.6		1.1		0.9		
		0/15	1.5	<1	15	3.6	6.8		3.0		2.4		
I <sub>I</sub>	Input Leakage Current	0/18	Any Input		18		$\pm 10^{-5}$	$\pm 0.1$		$\pm 1$		$\pm 1$	$\mu$ A
C <sub>I</sub>	Input Capacitance		Any Input				5	7.5					pF

The Noise Margin for both "1" and "0" level is: 1V min. with V<sub>DD</sub>=5V, 2V min. with V<sub>DD</sub>=10V, 2.5V min. with V<sub>DD</sub>=15V

**DYNAMIC ELECTRICAL CHARACTERISTICS** ( $T_{amb} = 25^{\circ}\text{C}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 200\text{K}\Omega$ ,  $t_r = t_f = 20\text{ ns}$ )

Symbol	Parameter	Test Condition			Value (*)			Unit
		V <sub>CC</sub> (V)	V <sub>DD</sub> (V)	SHITFING MODE	Min.	Typ.	Max.	
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Time : (Data input to output) High to Low Level	5	10	L - H		300	600	ns
		5	15			220	440	
		10	15			180	360	
		10	5	H - L		850	1600	
		15	5			850	1600	
		15	10			290	580	
	Low to High Level	5	10	L - H		130	260	ns
		5	15			120	240	
		10	15			70	140	
		10	5	H - L		230	460	
		15	5			230	460	
		15	10			80	160	
t <sub>PHZ</sub>	3-State Disable DelayTime Output High to High Impedance	5	10	L - H		60	120	ns
		5	15			50	100	
		10	15			35	70	
		10	5	H - L		120	240	
		15	5			120	240	
		15	10			40	80	
t <sub>PZH</sub>	High Impedance to Output High	5	10	L - H		320	640	ns
		5	15			230	460	
		10	15			180	360	
		10	5	H - L		800	1500	
		15	5			800	1500	
		15	10			280	560	
t <sub>PLZ</sub>	Output Low to High Impedance	5	10	L - H		370	740	ns
		5	15			300	600	
		10	15			250	500	
		10	5	H - L		850	1600	
		15	5			850	1600	
		15	10			350	700	
t <sub>PZL</sub>	High Impedance to Output Low	5	10	L - H		100	200	ns
		5	15			80	160	
		10	15			40	80	
		10	5	H - L		120	240	
		15	5			120	240	
		15	10			40	80	
t <sub>THL</sub> , t <sub>TLH</sub>	Transition Time	5	10	L - H		50	100	ns
		5	15			40	80	
		10	15			40	80	
		10	5	H - L		100	200	
		15	5			100	200	
		15	10			50	100	

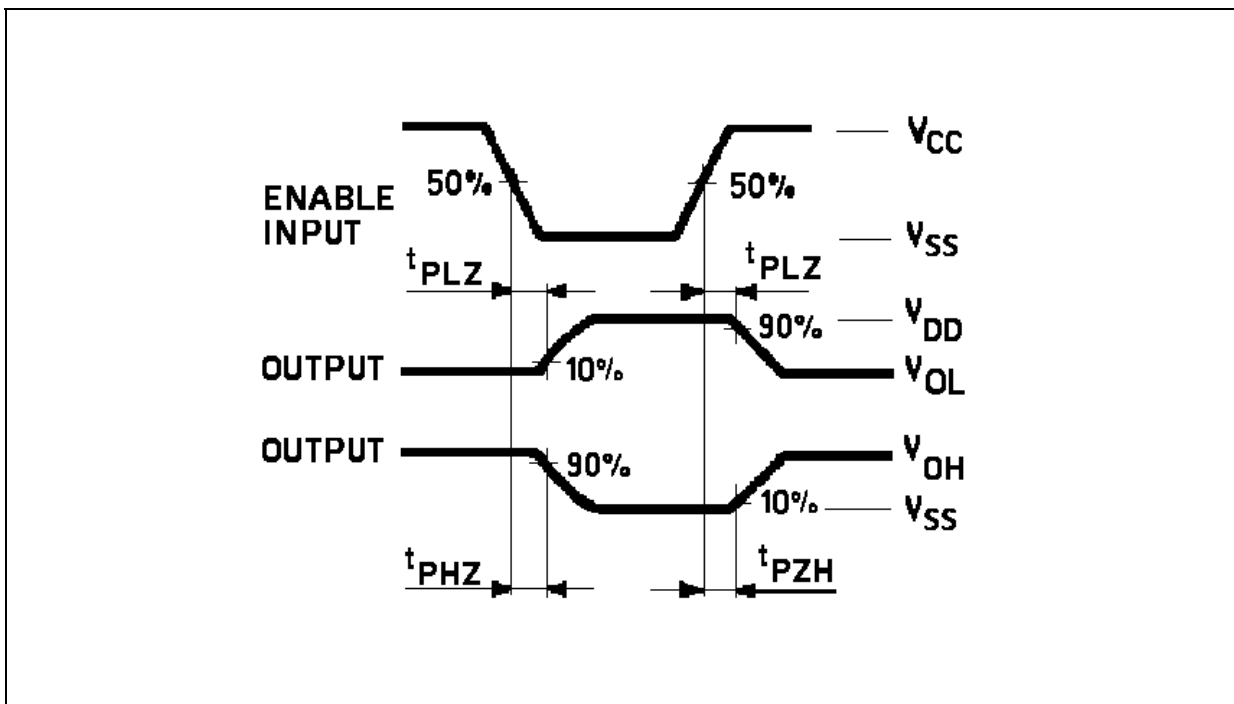
TEST CIRCUIT



TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	$V_{DD}$
$t_{PZH}$ , $t_{PHZ}$	$V_{SS}$

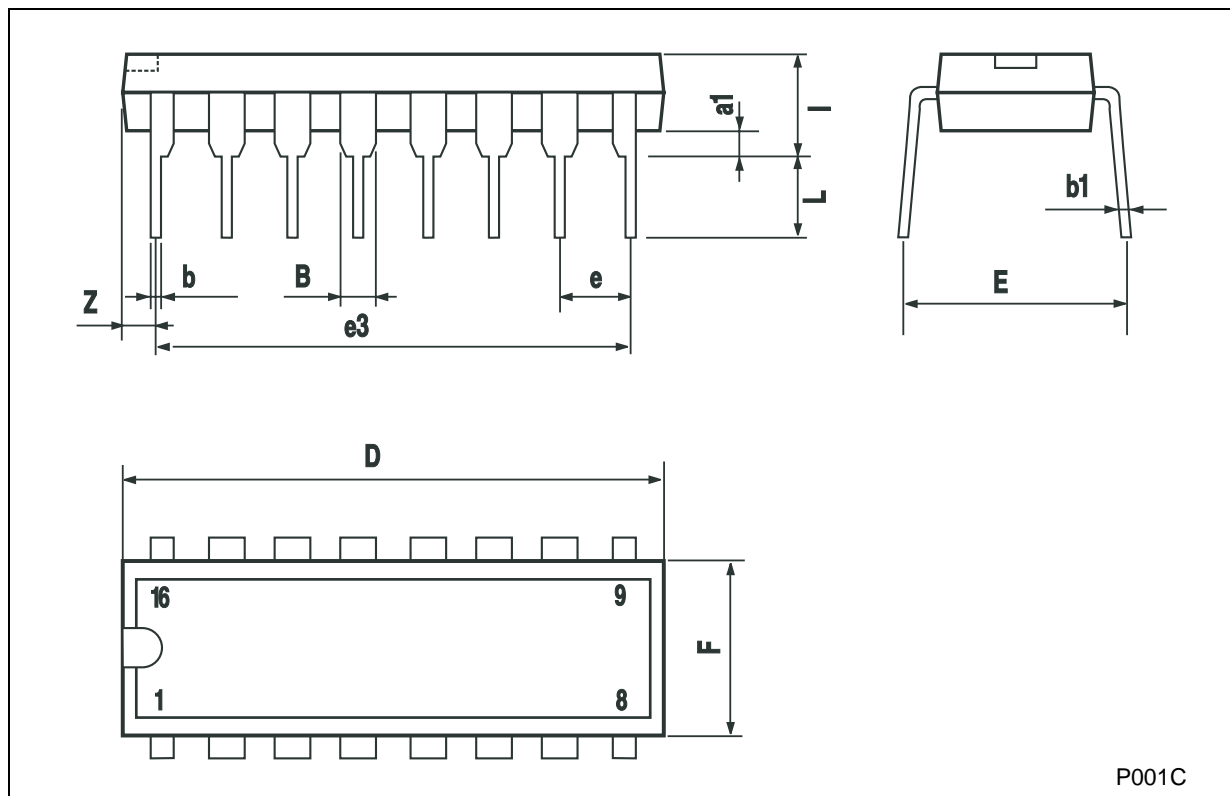
$C_L = 50\text{pF}$  or equivalent (includes jig and probe capacitance)  
 $R_L = 200\text{K}\Omega$   
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

WAVEFORM : PROPAGATION DELAY TIMES ( $f=1\text{MHz}$ ; 50% duty cycle)



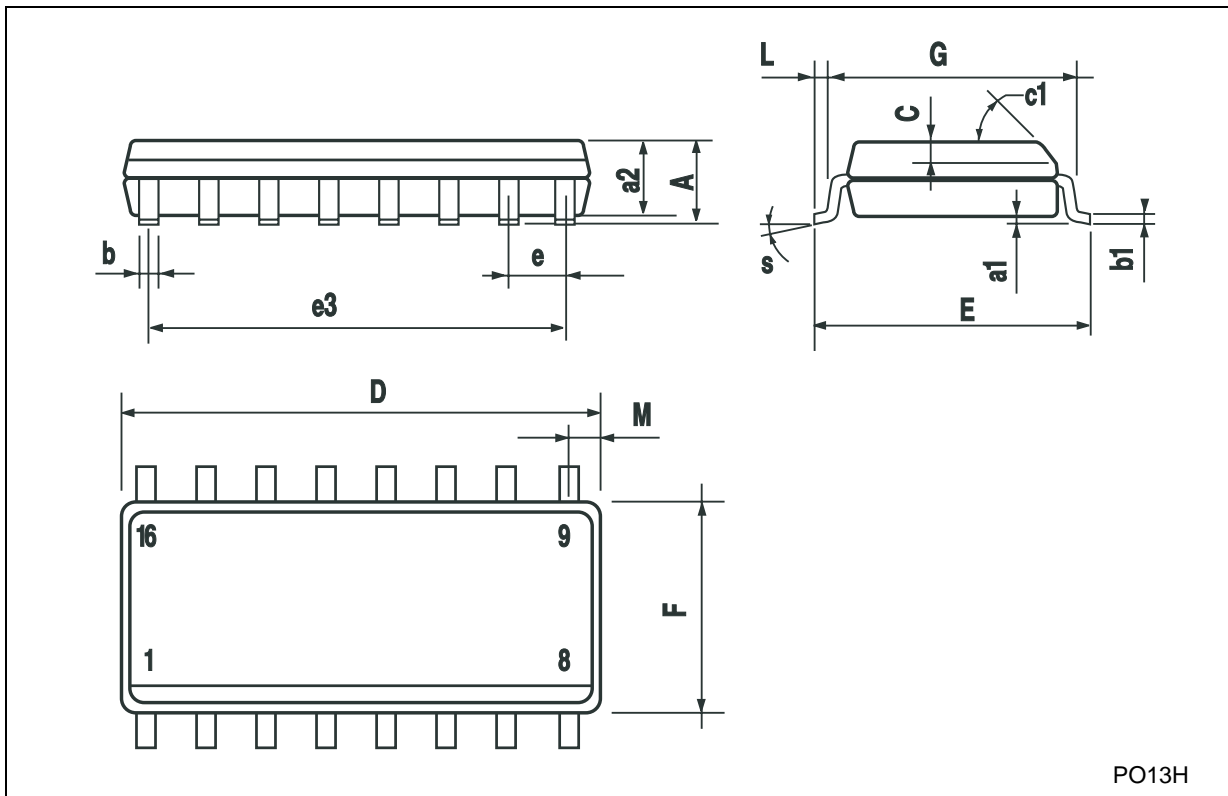
### Plastic DIP-16 (0.25) MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
a1	0.51			0.020		
B	0.77		1.65	0.030		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		17.78			0.700	
F			7.1			0.280
I			5.1			0.201
L		3.3			0.130	
Z			1.27			0.050



**SO-16 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.2	0.004		0.008
a2			1.65			0.064
b	0.35		0.46	0.013		0.018
b1	0.19		0.25	0.007		0.010
C		0.5			0.019	
c1	45° (typ.)					
D	9.8		10	0.385		0.393
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		8.89			0.350	
F	3.8		4.0	0.149		0.157
G	4.6		5.3	0.181		0.208
L	0.5		1.27	0.019		0.050
M			0.62			0.024
S	8			° (max.)		

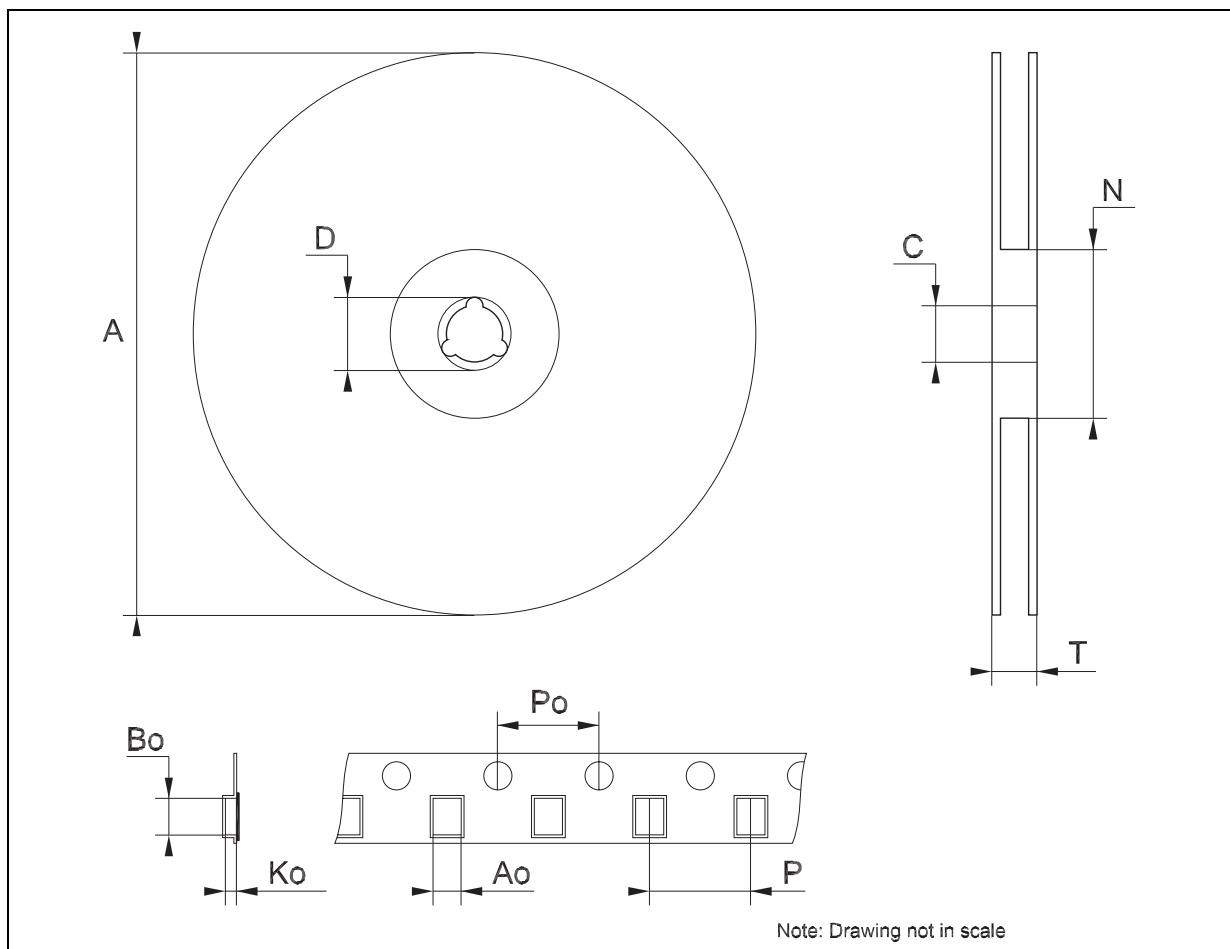


PO13H



**Tape & Reel SO-16 MECHANICAL DATA**

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			330			12.992
C	12.8		13.2	0.504		0.519
D	20.2			0.795		
N	60			2.362		
T			22.4			0.882
Ao	6.45		6.65	0.254		0.262
Bo	10.3		10.5	0.406		0.414
Ko	2.1		2.3	0.082		0.090
Po	3.9		4.1	0.153		0.161
P	7.9		8.1	0.311		0.319



Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2003 STMicroelectronics - Printed in Italy - All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco  
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>