## **SI4410DY**

N-channel TrenchMOS logic level FET

Rev. 03 — 4 December 2009

**Product data sheet** 

## 1. Product profile

#### **1.1 General description**

Logic level N-channel enhancement mode Field-Effect Transistor (FET) in a plastic package using TrenchMOS technology. This product is designed and qualified for use in computing, communications, consumer and industrial applications only.

#### 1.2 Features and benefits

- Low conduction losses due to low on-state resistance
- Suitable for high frequency applications due to fast switching characteristics

Notebook computers

Portable equipment

### **1.3 Applications**

- DC motor control
- DC-to-DC convertors
- Lithium-ion battery applications

#### 1.4 Quick reference data

#### Table 1. Quick reference

Table 1.	QUICK reference					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 150 °C	-	-	30	V
I <sub>D</sub>	drain current	T <sub>amb</sub> = 25 °C; pulsed; see <u>Figure 1</u> and <u>3</u>	-	-	10	А
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C; pulsed; see <u>Figure 2</u>	-	-	2.5	W
Dynamic	characteristics					
Q <sub>GD</sub>	gate-drain charge	V <sub>GS</sub> = 10 V; I <sub>D</sub> = 10 A; V <sub>DS</sub> = 15 V; T <sub>j</sub> = 25 °C; see <u>Figure 12</u>	-	7	-	nC
Static ch	aracteristics					
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A};$ $T_j = 25 \text{ °C};$ see <u>Figure 10</u> and <u>11</u>	-	15	20	mΩ
		$V_{GS}$ = 10 V; $I_D$ = 10 A; $T_j$ = 25 °C; see <u>Figure 10</u> and <u>11</u>	-	11	13.5	mΩ



## 2. Pinning information

Table 2.	Pinning	information				
Pin	Symbol	Description	Simplified outline	Graphic symbol		
1	S	source		-		
2	S	source				
3	S	source				
4	G	gate				
5	D	drain		mbb076 S		
6	D	drain	SOT96-1 (SO8)			
7	D	drain				
8	D	drain				

## 3. Ordering information

#### Table 3.Ordering information

Type number	Package		
	Name	Description	Version
SI4410DY	SO8	plastic small outline package; 8 leads; body width 3.9 mm	SOT96-1

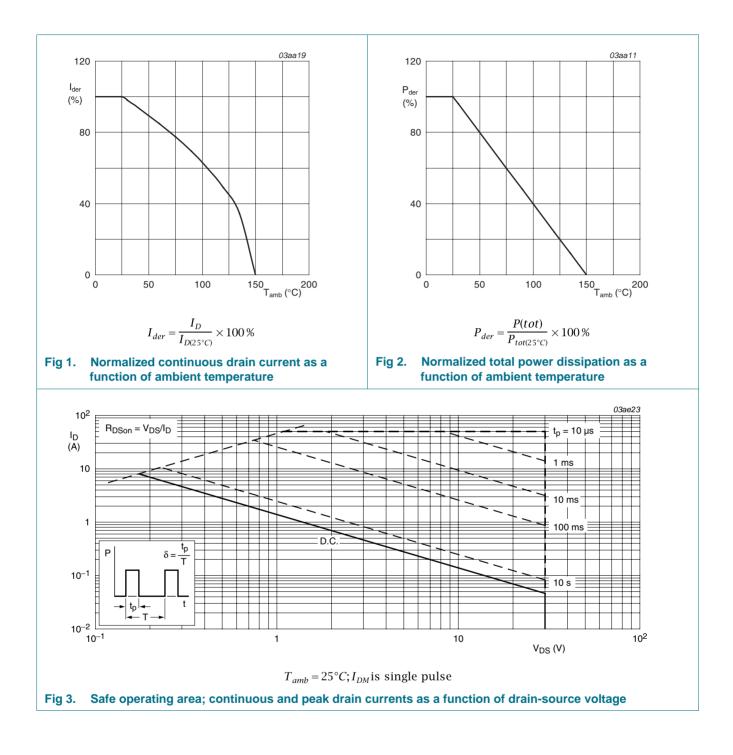
## 4. Limiting values

#### Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

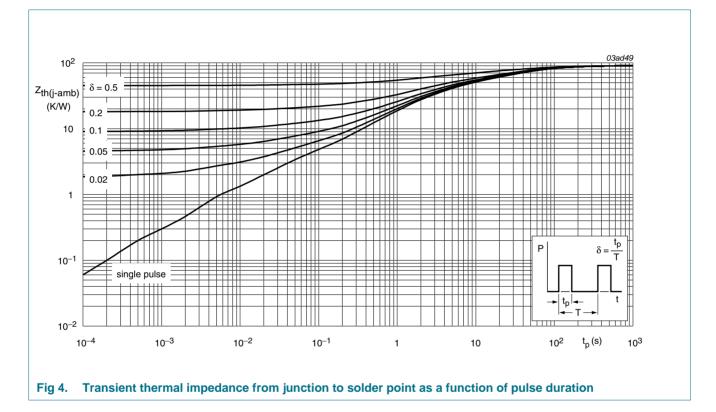
Symbol	Parameter	Conditions	Min	Мах	Unit
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> ≥ 25 °C; T <sub>j</sub> ≤ 150 °C	-	30	V
V <sub>GS</sub>	gate-source voltage		-20	20	V
I <sub>D</sub>	drain current	T <sub>amb</sub> = 70 °C; pulsed; see <u>Figure 1</u>	-	8	A
		$T_{amb} = 25 \text{ °C}; \text{ pulsed};$ see <u>Figure 1</u> and <u>3</u>	-	10	A
I <sub>DM</sub>	peak drain current	t <sub>p</sub> ≤ 10 μs; T <sub>amb</sub> = 25 °C; pulsed; see <u>Figure 3</u>	-	50	A
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 70 °C; pulsed; see <u>Figure 2</u>	-	1.6	W
		T <sub>amb</sub> = 25 °C; pulsed; see <u>Figure 2</u>	-	2.5	W
T <sub>stg</sub>	storage temperature		-55	150	°C
Tj	junction temperature		-55	150	°C
Source-dr	ain diode				
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C; pulsed	-	2.3	А

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## 5. Thermal characteristics

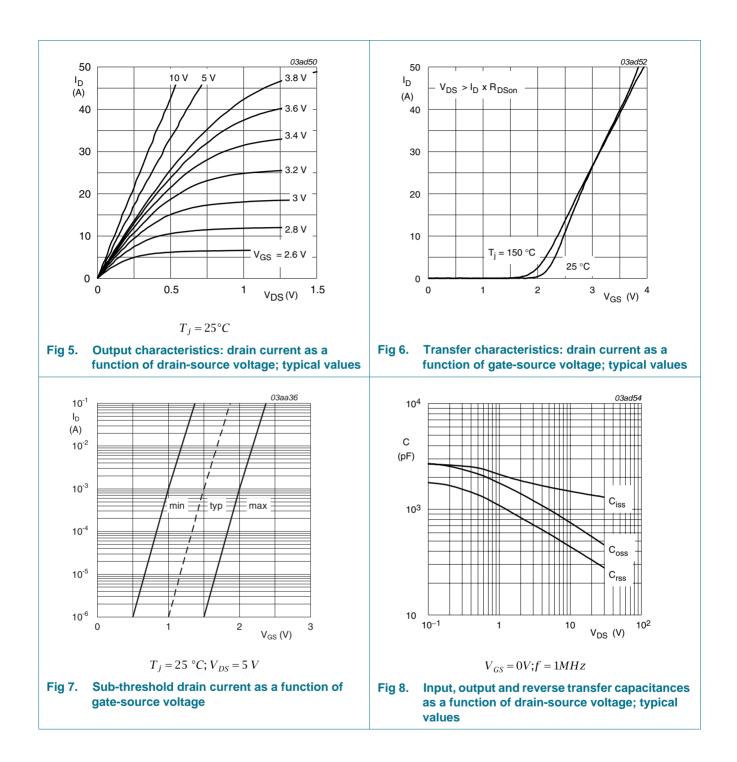
Table 5.	Thermal characteristics	5				
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
R <sub>th(j-sp)</sub>	thermal resistance from junction to solder point		-	-	-	K/W
R <sub>th(j-a)</sub>	thermal resistance from junction to ambient	mounted on a printed-circuit board; minimum footprint; tp ≤ 10 s; see <u>Figure 4</u>	-	-	50	K/W



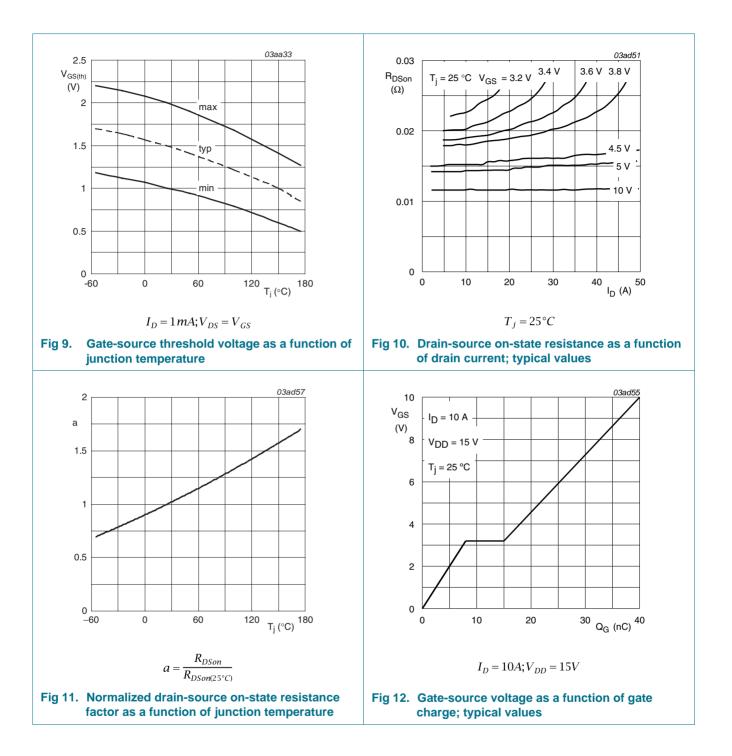
## 6. Characteristics

Table 6.	Characteristics					
Symbol	Parameter	Conditions	Min	Тур	Max	Unit
Static cha	aracteristics					
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 250 μA; V <sub>DS</sub> = V <sub>GS</sub> ; T <sub>j</sub> = 25 °C; see <u>Figure 9</u>	1	-	-	V
I <sub>DSS</sub>	drain leakage current	$V_{DS} = 30 \text{ V}; \text{ V}_{GS} = 0 \text{ V}; \text{ T}_{j} = 25 \text{ °C}$	-	-	1	μΑ
		$V_{DS} = 30 \text{ V}; V_{GS} = 0 \text{ V}; T_j = 55 \text{ °C}$	-	-	25	μA
I <sub>GSS</sub>	gate leakage current	$V_{GS} = 20 \text{ V}; V_{DS} = 0 \text{ V}; T_j = 25 \text{ °C}$	-	-	100	nA
		$V_{GS}$ = -20 V; $V_{DS}$ = 0 V; $T_j$ = 25 °C	-	-	100	nA
R <sub>DSon</sub>	drain-source on-state resistance	$V_{GS} = 4.5 \text{ V}; I_D = 5 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 10</u> and <u>11</u>	-	15	20	mΩ
		$V_{GS} = 10 \text{ V}; I_D = 10 \text{ A}; T_j = 25 \text{ °C};$ see <u>Figure 10</u> and <u>11</u>	-	11	13.5	mΩ
I <sub>DSon</sub>	on-state drain-source current	$V_{DS} \ge 5 \text{ V}; \text{ V}_{GS} = 10 \text{ V}$	20	-	-	A
Dynamic	characteristics					
Q <sub>G(tot)</sub>	total gate charge	I <sub>D</sub> = 10 A; V <sub>DS</sub> = 15 V; V <sub>GS</sub> = 5 V; T <sub>j</sub> = 25 °C; see <u>Figure 12</u>	-	21.5	34	nC
		$I_D = 10 \text{ A}; V_{DS} = 15 \text{ V}; V_{GS} = 10 \text{ V};$	-	40	60	nC
$Q_{GS}$	gate-source charge	$T_j = 25 \text{ °C}; \text{ see } \frac{\text{Figure } 12}{\text{Figure } 12}$	-	8	-	nC
$Q_{GD}$	gate-drain charge		-	7	-	nC
t <sub>d(on)</sub>	turn-on delay time	$V_{DS} = 25 \text{ V}; \text{ R}_{L} = 25 \Omega; \text{ V}_{GS} = 10 \text{ V};$	-	13.5	30	ns
t <sub>r</sub>	rise time	$R_{G(ext)} = 6 \Omega; T_j = 25 °C$	-	9	20	ns
t <sub>d(off)</sub>	turn-off delay time		-	70	100	ns
t <sub>f</sub>	fall time		-	30	80	ns
g <sub>fs</sub>	transfer conductance	V <sub>DS</sub> = 15 V; I <sub>D</sub> = 10 A; T <sub>j</sub> = 25 °C; see <u>Figure 13</u>	-	34	-	S
Source-d	rain diode					
V <sub>SD</sub>	source-drain voltage	I <sub>S</sub> = 2.3 A; V <sub>GS</sub> = 0 V; T <sub>j</sub> = 25 °C; see <u>Figure 14</u>	-	0.7	1.1	V
t <sub>rr</sub>	reverse recovery time	I <sub>S</sub> = 2.3 A; dI <sub>S</sub> /dt = -100 A/µs; V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; T <sub>i</sub> = 25 °C	-	50	80	ns

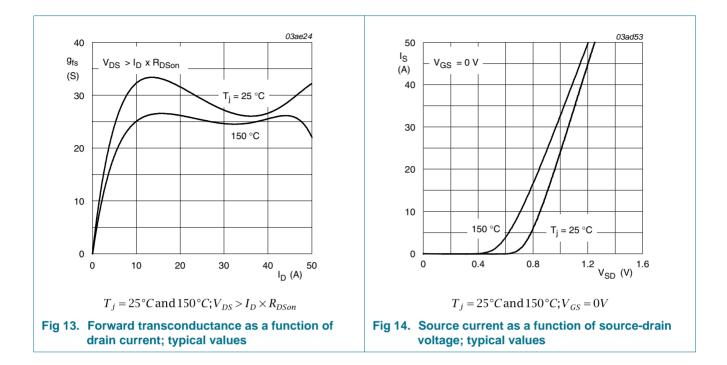
## SI4410DY N-channel TrenchMOS logic level FET



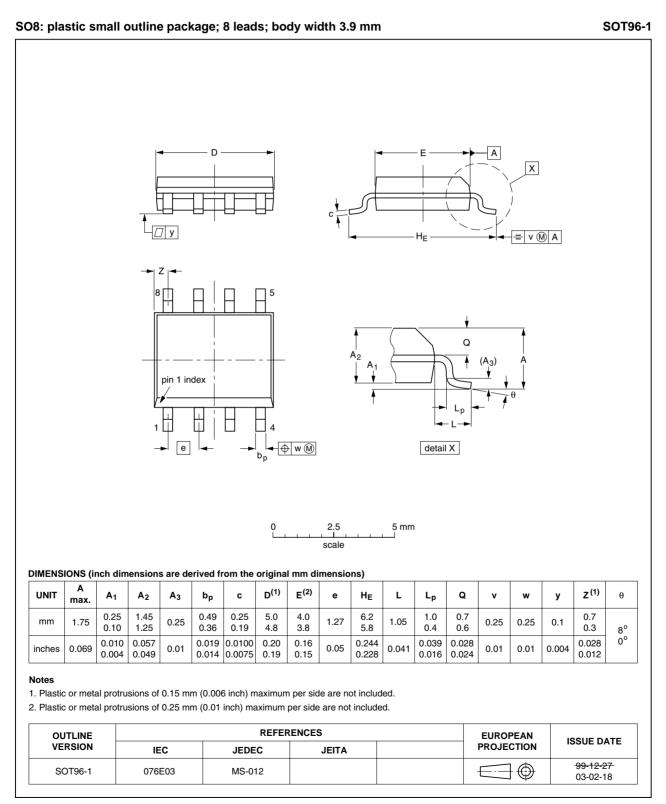
**SI4410DY** 



## SI4410DY N-channel TrenchMOS logic level FET



## 7. Package outline



#### Fig 15. Package outline SOT96-1 (SO8)

## 8. Revision history

Table 7. Revision	history			
Document ID	Release date	Data sheet status	Change notice	Supersedes
SI4410DY_3	20091204	Product data sheet	-	SI4410DY-02
Modifications:	guidelines	t of this data sheet has b of NXP Semiconductors		
	<ul> <li>Legal texts</li> </ul>	s have been adapted to the	ne new company name v	where appropriate.
SI4410DY-02	20010705	Product specification	-	SI4410DY-01
SI4410DY-01	20010220	Product specification	-	-

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#### 9.1 Data sheet status

Document status <sup>[1][2]</sup>	Product status <sup>[3]</sup>	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions"

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