-100mA / -50V Digital transistors (with built-in resistors) DTA114YEB

Applications

Inverter, Interface, Driver

Features

- 1) Built-in bias resistors enable the configuration of an inverter circuit without connecting external input resistors (see equivalent circuit).
- 2) The bias resistors consist of thin-film resistors with complete isolation to allow negative biasing of the input. They also have the advantage of almost completely eliminating parasitic effects.
- 3) Only the on/off conditions need to be set for operation, making the device design easy.

Structure

PNP silicon epitaxial planar transistor type (Resistor built-in)

Packaging specifications

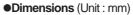
	Package	EMT3F
	Packaging type	Taping
	Code	TL
Part No.	Basic ordering unit (pieces)	3000
DTA114YEB		0

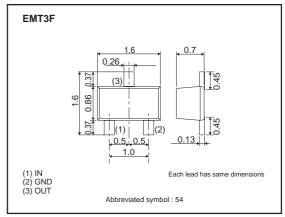
Absolute maximum ratings (Ta=25°C)

Parameter	Symbol	Limits	Unit				
Supply voltage	Vcc	-50	V				
Input voltage	VIN	-40 to +6	V				
Collector current	Ic(max) *1	-100	mA				
Output current	lo	-70	mA				
Power dissipation	PD *2	150	mW				
Junction temperature	Tj	150	°C				
Storage temperature	Tstg	-55 to +150	°C				

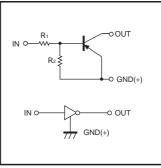
*1 Characteristics of built-in transistor

*2 Each terminal mounted on a recommended land





Equivalent circuit



R1=10kΩ, R2=47kΩ

DTA114YEB

Transistors

●Electrical characteristics (Ta=25°C)

Symbol	Min.	Тур.	Max.	Unit	Conditions
VI(off)	-	-	-300	mV	Vcc=–5V, Io=–100µA
VI(on)	-1.4	-	-	V	Vo=-0.3V, Io=-1mA
VO(on)	-	-100	-300	mV	lo/l=-5mA/-0.25mA
h	-	-	-880	μΑ	VI=-5V
IO(off)	-	-	-500	nA	Vcc=-50V, Vi=0V
Gı	68	-	-	-	Vo=–5V, Io=–5mA
f⊤ ∗	-	250	_	MHz	Vce=-10V, Ie=5mA, f=100MHz
R1	7	10	13	kΩ	_
R2/R1	3.7	4.7	5.7	-	-
	VI(off) VI(on) VO(on) II IO(off) GI fT * R1	Vi(off) - Vi(on) -1.4 Vo(on) - Ii - Io(off) - Gi 68 ft * - R1 7	$\begin{array}{c c c c c c c c c c c c c c c c c c c $	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	$\begin{array}{c ccccccccccccccccccccccccccccccccccc$

* Characteristics of built-in transistor



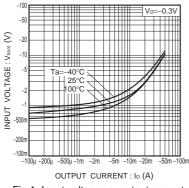
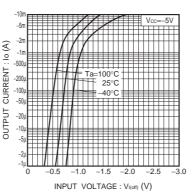
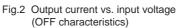
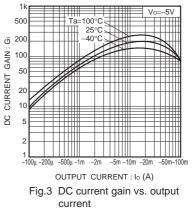
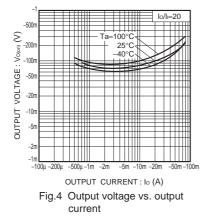


Fig.1 Input voltage vs. output current (ON characteristics)









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Appendix1-Rev2.0

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