

## 8-Mbit (512K x 16) Static RAM

### Features

- **Very high speed: 45 ns**
- **Wide voltage range: 4.5V–5.5V**
- **Ultra-low standby power**
  - Typical Standby current: 2  $\mu$ A
  - Maximum Standby current: 8  $\mu$ A (Industrial)
- **Ultra-low active power**
  - Typical active current: 1.8 mA @ f = 1 MHz
- **Ultra-low standby power**
- **Easy memory expansion with  $\overline{CE}_1$ ,  $\overline{CE}_2$  and  $\overline{OE}$  features**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in Pb-free 44-pin TSOP II and 48-ball VFBGA package**

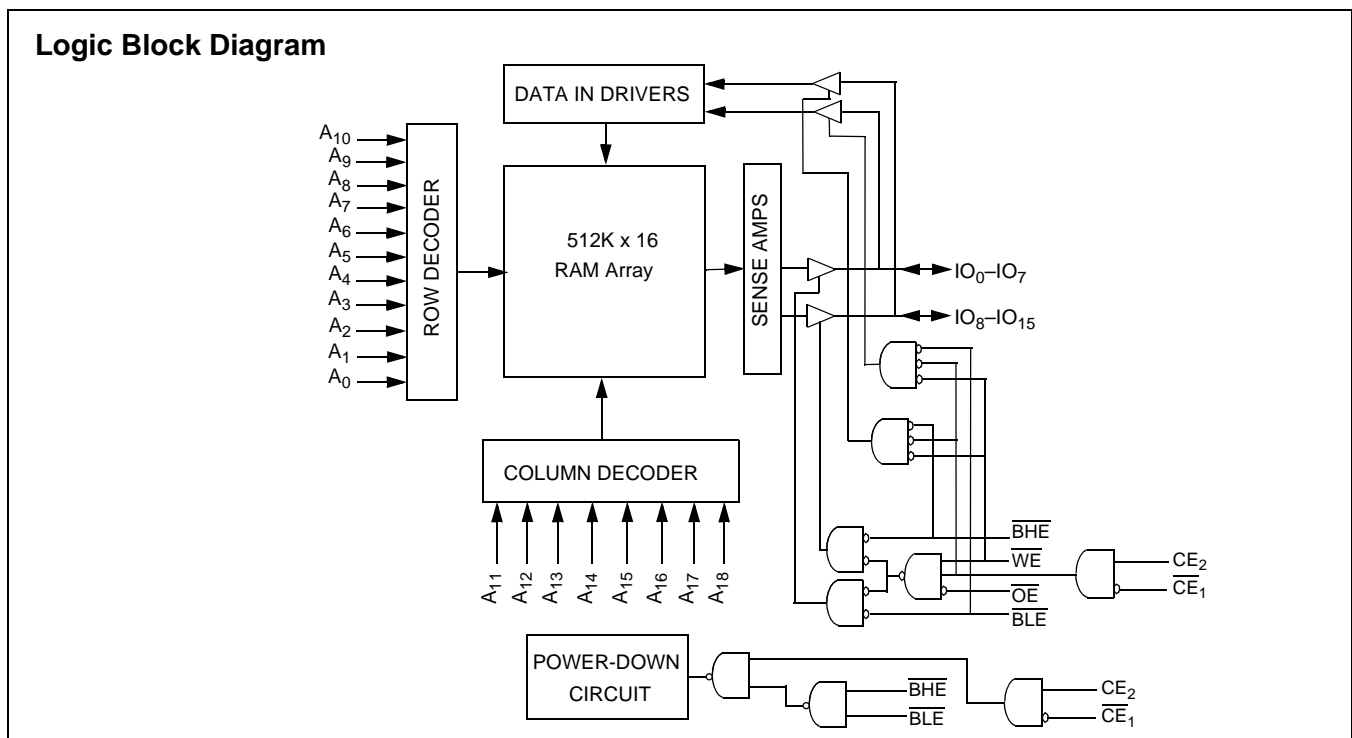
### Functional Description<sup>[1]</sup>

The CY62157E is a high-performance CMOS static RAM organized as 512K words by 16 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL<sup>®</sup>) in portable applications such as cellular telephones. The device

also has an automatic power-down feature that significantly reduces power consumption when addresses are not toggling. The device can also be put into standby mode when deselected ( $\overline{CE}_1$  HIGH or  $\overline{CE}_2$  LOW or both BHE and BLE are HIGH). The input/output pins (IO<sub>0</sub> through IO<sub>15</sub>) are placed in a high-impedance state when: deselected ( $\overline{CE}_1$  HIGH or  $\overline{CE}_2$  LOW), outputs are disabled ( $\overline{OE}$  HIGH), both Byte High Enable and Byte Low Enable are disabled (BHE, BLE HIGH), or during a write operation ( $\overline{CE}_1$  LOW,  $\overline{CE}_2$  HIGH and WE LOW).

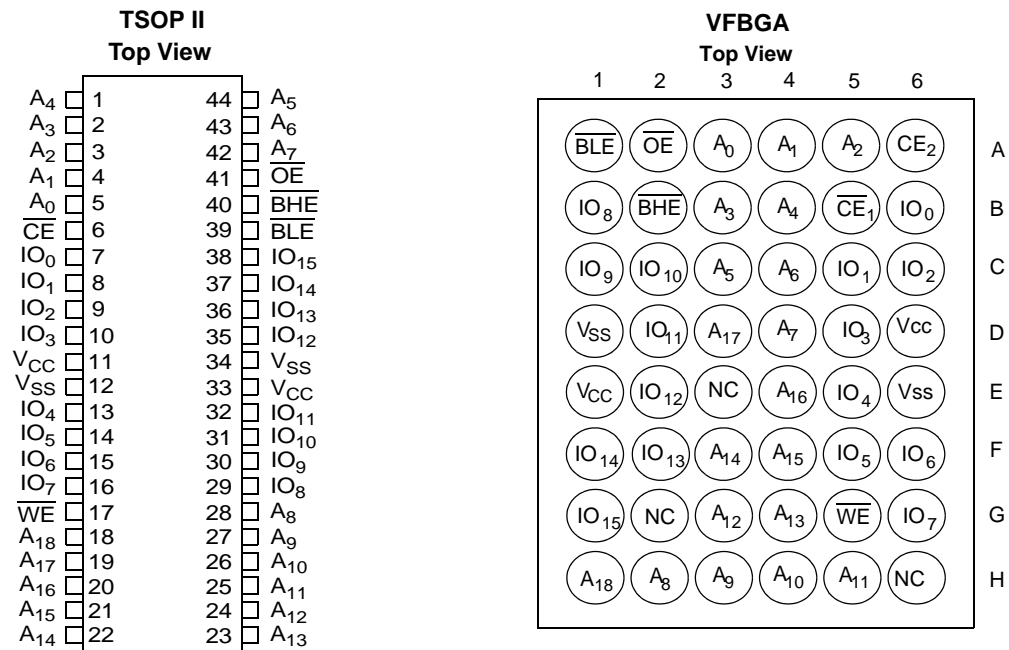
Writing to the device is accomplished by taking Chip Enable ( $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH) and Write Enable (WE) input LOW. If Byte Low Enable (BLE) is LOW, then data from IO pins (IO<sub>0</sub> through IO<sub>7</sub>), is written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>). If Byte High Enable (BHE) is LOW, then data from IO pins (IO<sub>8</sub> through IO<sub>15</sub>) is written into the location specified on the address pins (A<sub>0</sub> through A<sub>18</sub>).

Reading from the device is accomplished by taking Chip Enable ( $\overline{CE}_1$  LOW and  $\overline{CE}_2$  HIGH) and Output Enable ( $\overline{OE}$ ) LOW while forcing the Write Enable (WE) HIGH. If Byte Low Enable (BLE) is LOW, then data from the memory location specified by the address pins will appear on IO<sub>0</sub> to IO<sub>7</sub>. If Byte High Enable (BHE) is LOW, then data from memory will appear on IO<sub>8</sub> to IO<sub>15</sub>. See the truth table at the back of this data sheet for a complete description of read and write modes.



**Note:**

1. For best practice recommendations, please refer to the Cypress application note "System Design Guidelines" on <http://www.cypress.com>.

**Pin Configuration<sup>[2, 3]</sup>**

**Product Portfolio**

Product	Range	V <sub>CC</sub> Range (V)			Speed (ns)	Power Dissipation					
						Operating I <sub>CC</sub> , (mA)				Standby, I <sub>SB2</sub> (μA)	
		f = 1MHz		f = f <sub>max</sub>							
		Min	Typ <sup>[4]</sup>	Max		Typ <sup>[4]</sup>	Max	Typ <sup>[4]</sup>	Max	Typ <sup>[4]</sup>	Max
CY62157E-45	Ind'l	4.5	5.0	5.5	45	1.8	3	18	25	2	8
CY62157E-55 <sup>[5]</sup>	Auto	4.5	5.0	5.5	55	1.8	4	18	35	2	30

**Notes:**

2. NC pins are not connected on the die.
3. The 44-pin TSOP II package has only one chip enable ( $\overline{CE}$ ) pin.
4. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V<sub>CC</sub> = V<sub>CC(typ)</sub>, T<sub>A</sub> = 25°C.
5. Automotive product information is Preliminary.

**Maximum Ratings**

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... -65°C to + 150°C  
 Ambient Temperature with Power Applied ..... -55°C to + 125°C  
 Supply Voltage to Ground Potential ..... -0.5V to 6.0V  
 DC Voltage Applied to Outputs in High Z State<sup>[6, 7]</sup> ..... -0.5V to 6.0V

DC Input Voltage<sup>[6, 7]</sup> ..... -0.5V to 6.0V  
 Output Current into Outputs (LOW) ..... 20 mA  
 Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)  
 Latch-Up Current ..... > 200 mA

**Operating Range**

Device	Range	Ambient Temperature	V <sub>CC</sub> <sup>[8]</sup>
CY62157E	Industrial	-40°C to +85°C	4.5V to 5.5V
	Automotive	-40°C to +125°C	

**Electrical Characteristics (Over the Operating Range)**

Parameter	Description	Test Conditions	45 ns (Industrial)			55 ns (Automotive)			Unit
			Min	Typ <sup>[4]</sup>	Max	Min	Typ <sup>[4]</sup>	Max	
V <sub>OH</sub>	Output HIGH Voltage	I <sub>OH</sub> = -1 mA, V <sub>CC</sub> = 4.5V	2.4			2.4			V
V <sub>OL</sub>	Output LOW Voltage	I <sub>OL</sub> = 2.1 mA, V <sub>CC</sub> = 4.5V			0.4			0.4	V
V <sub>IH</sub>	Input HIGH Voltage	V <sub>CC</sub> = 4.5V to 5.5V	2.2		V <sub>CC</sub> + 0.5	2.2		V <sub>CC</sub> + 0.5	V
V <sub>IL</sub>	Input LOW Voltage	V <sub>CC</sub> = 4.5V to 5.5V	-0.5		0.8	-0.5		0.8	V
I <sub>IX</sub>	Input Leakage Current	GND ≤ V <sub>I</sub> ≤ V <sub>CC</sub>	-1		+1	-1		+1	μA
I <sub>OZ</sub>	Output Leakage Current	GND ≤ V <sub>O</sub> ≤ V <sub>CC</sub> , Output Disabled	-1		+1	-1		+1	μA
I <sub>CC</sub>	V <sub>CC</sub> Operating Supply Current	f = f <sub>max</sub> = 1/t <sub>RC</sub> , V <sub>CC</sub> = V <sub>CCmax</sub> , I <sub>OUT</sub> = 0 mA, CMOS levels		18	25		18	35	mA
		f = 1 MHz		1.8	3		1.8	4	
I <sub>SB1</sub>	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ , $CE_2 \leq 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ , $V_{IN} \leq 0.2V$ , f = f <sub>max</sub> (Address and Data Only), f = 0 (OE, BHE, BLE and WE), V <sub>CC</sub> = 3.60V		2	8		2	30	μA
I <sub>SB2</sub>	Automatic CE Power-Down Current — CMOS Inputs	$\overline{CE}_1 \geq V_{CC} - 0.2V$ or $CE_2 \leq 0.2V$ , $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$ , f = 0, V <sub>CC</sub> = 3.60V		2	8		2	30	μA

**Capacitance<sup>[9]</sup>**

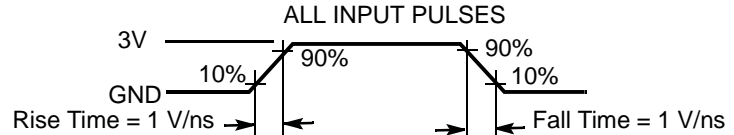
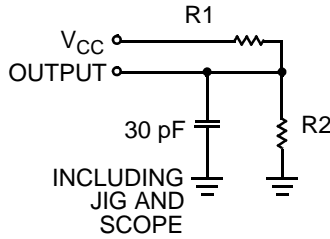
Parameter	Description	Test Conditions	Max	Unit
C <sub>IN</sub>	Input Capacitance	T <sub>A</sub> = 25°C, f = 1 MHz, V <sub>CC</sub> = V <sub>CC(typ)</sub>	10	pF
C <sub>OUT</sub>	Output Capacitance		10	pF

**Notes:**

6. V<sub>IL(min)</sub> = -2.0V for pulse durations less than 20 ns for I < 30 mA.
7. V<sub>IH(max)</sub> = V<sub>CC</sub> + 0.75V for pulse durations less than 20 ns.
8. Full device AC operation assumes a 100 μs ramp time from 0 to V<sub>CC(min)</sub> and 200 μs wait time after V<sub>CC</sub> stabilization.
9. Tested initially and after any design or process changes that may affect these parameters.

**Thermal Resistance<sup>[9]</sup>**

Parameter	Description	Test Conditions	TSOP II	VFBGA	Unit
$\Theta_{JA}$	Thermal Resistance (Junction to Ambient)	Still Air, soldered on a 3 x 4.5 inch, two-layer printed circuit board	77	72	°C/W
$\Theta_{JC}$	Thermal Resistance (Junction to Case)		13	8.86	°C/W

**AC Test Loads and Waveforms**


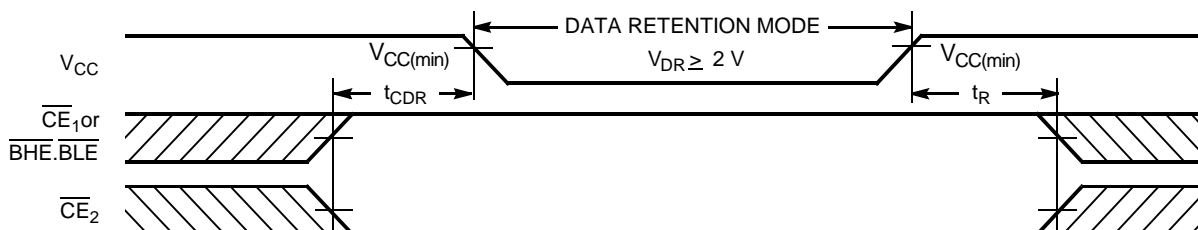
Equivalent to: THEVENIN EQUIVALENT



Parameters	Values	Unit
R1	1800	$\Omega$
R2	990	$\Omega$
$R_{TH}$	639	$\Omega$
$V_{TH}$	1.77	V

**Data Retention Characteristics (Over the Operating Range)**

Parameter	Description	Conditions	Min	Typ <sup>[4]</sup>	Max	Unit
$V_{DR}$	$V_{CC}$ for Data Retention		2			V
$I_{CCDR}$	Data Retention Current	$V_{CC}=2V, \overline{CE}_1 \geq V_{CC} - 0.2V,$ $CE_2 \leq 0.2V, V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	Industrial		8	$\mu A$
			Automotive		30	
$t_{CDR}^{[9]}$	Chip Deselect to Data Retention Time		0			ns
$t_R^{[10]}$	Operation Recovery Time		$t_{RC}$			ns

**Data Retention Waveform<sup>[11]</sup>**

**Notes:**

 10. Full device operation requires linear  $V_{CC}$  ramp from  $V_{DR}$  to  $V_{CC(min)} \geq 100 \mu s$  or stable at  $V_{CC(min)} \geq 100 \mu s$ .

 11.  $\overline{BHE.BLE}$  is the AND of both  $\overline{BHE}$  and  $\overline{BLE}$ . Chip can be deselected by either disabling the chip enable signals or by disabling both  $\overline{BHE}$  and  $\overline{BLE}$ .

**Switching Characteristics** Over the Operating Range <sup>[12]</sup>

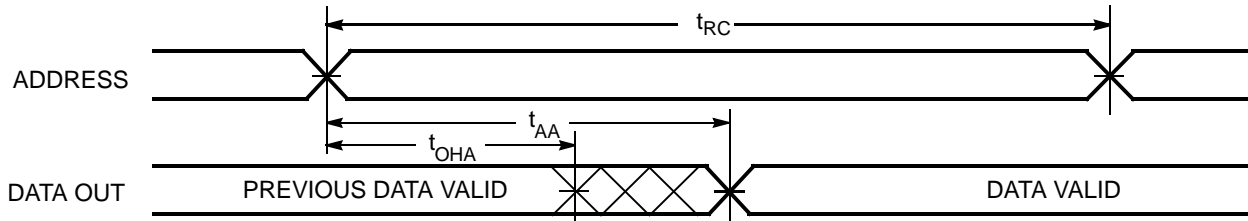
Parameter	Description	45 ns		55 ns		Unit
		Min	Max	Min	Max	
<b>Read Cycle</b>						
$t_{RC}$	Read Cycle Time	45		55		ns
$t_{AA}$	Address to Data Valid		45		55	ns
$t_{OHA}$	Data Hold from Address Change	10		10		ns
$t_{ACE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Data Valid		45		55	ns
$t_{DOE}$	$\overline{OE}$ LOW to Data Valid		22		25	ns
$t_{LZOE}$	$\overline{OE}$ LOW to LOW Z <sup>[13]</sup>	5		5		ns
$t_{HZOE}$	$\overline{OE}$ HIGH to High Z <sup>[13, 14]</sup>		18		20	ns
$t_{LZCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Low Z <sup>[13]</sup>	10		10		ns
$t_{HZCE}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to High Z <sup>[13, 14]</sup>		18		20	ns
$t_{PU}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Power-Up	0		0		ns
$t_{PD}$	$\overline{CE}_1$ HIGH and $CE_2$ LOW to Power-Down		45		55	ns
$t_{DBE}$	$\overline{BLE}/\overline{BHE}$ LOW to Data Valid		45		55	ns
$t_{LZBE}$	$\overline{BLE}/\overline{BHE}$ LOW to Low Z <sup>[13]</sup>	10		10		ns
$t_{HZBE}$	$\overline{BLE}/\overline{BHE}$ HIGH to HIGH Z <sup>[13, 14]</sup>		18		20	ns
<b>Write Cycle<sup>[15]</sup></b>						
$t_{WC}$	Write Cycle Time	45		55		ns
$t_{SCE}$	$\overline{CE}_1$ LOW and $CE_2$ HIGH to Write End	35		40		ns
$t_{AW}$	Address Set-Up to Write End	35		40		ns
$t_{HA}$	Address Hold from Write End	0		0		ns
$t_{SA}$	Address Set-Up to Write Start	0		0		ns
$t_{PWE}$	$\overline{WE}$ Pulse Width	35		40		ns
$t_{BW}$	$\overline{BLE}/\overline{BHE}$ LOW to Write End	35		40		ns
$t_{SD}$	Data Set-Up to Write End	25		25		ns
$t_{HD}$	Data Hold from Write End	0		0		ns
$t_{HZWE}$	$\overline{WE}$ LOW to High-Z <sup>[13, 14]</sup>		18		20	ns
$t_{LZWE}$	$\overline{WE}$ HIGH to Low-Z <sup>[13]</sup>	10		10		ns

**Notes:**

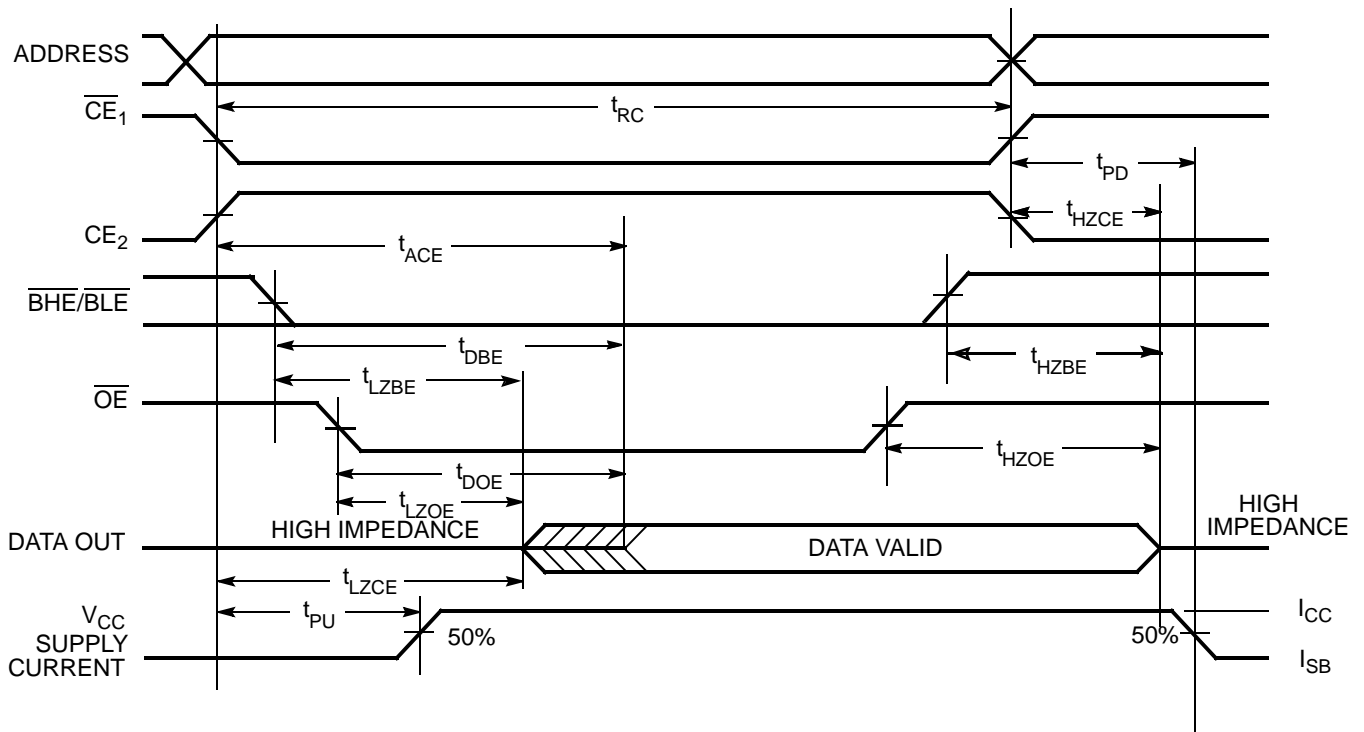
12. Test conditions for all parameters other than Tri-state parameters assume signal transition time of 3 ns or less, timing reference levels of  $V_{CC(typ)}/2$ , input pulse levels of 0 to  $V_{CC(typ)}$ , and output loading of the specified  $I_{OL}/I_{OH}$  as shown in the "AC Test Loads and Waveforms" section.
13. At any given temperature and voltage condition,  $t_{HZCE}$  is less than  $t_{LZCE}$ ,  $t_{HZBE}$  is less than  $t_{LZBE}$ ,  $t_{HZOE}$  is less than  $t_{LZOE}$ , and  $t_{HZWE}$  is less than  $t_{LZWE}$  for any given device.
14.  $t_{HZOE}$ ,  $t_{HZCE}$ ,  $t_{HZBE}$ , and  $t_{HZWE}$  transitions are measured when the outputs enter a high-impedance state.
15. The internal Write time of the memory is defined by the overlap of  $\overline{WE}$ ,  $CE_1 = V_{IL}$ ,  $BHE$  and/or  $BLE = V_{IL}$ , and  $CE_2 = V_{IH}$ . All signals must be ACTIVE to initiate a write and any of these signals can terminate a write by going INACTIVE. The data input set-up and hold timing should be referenced to the edge of the signal that terminates the Write.

### Switching Waveforms

#### Read Cycle 1 (Address Transition Controlled)<sup>[16, 17]</sup>



#### Read Cycle 2 ( $\overline{\text{OE}}$ Controlled)<sup>[17, 18]</sup>

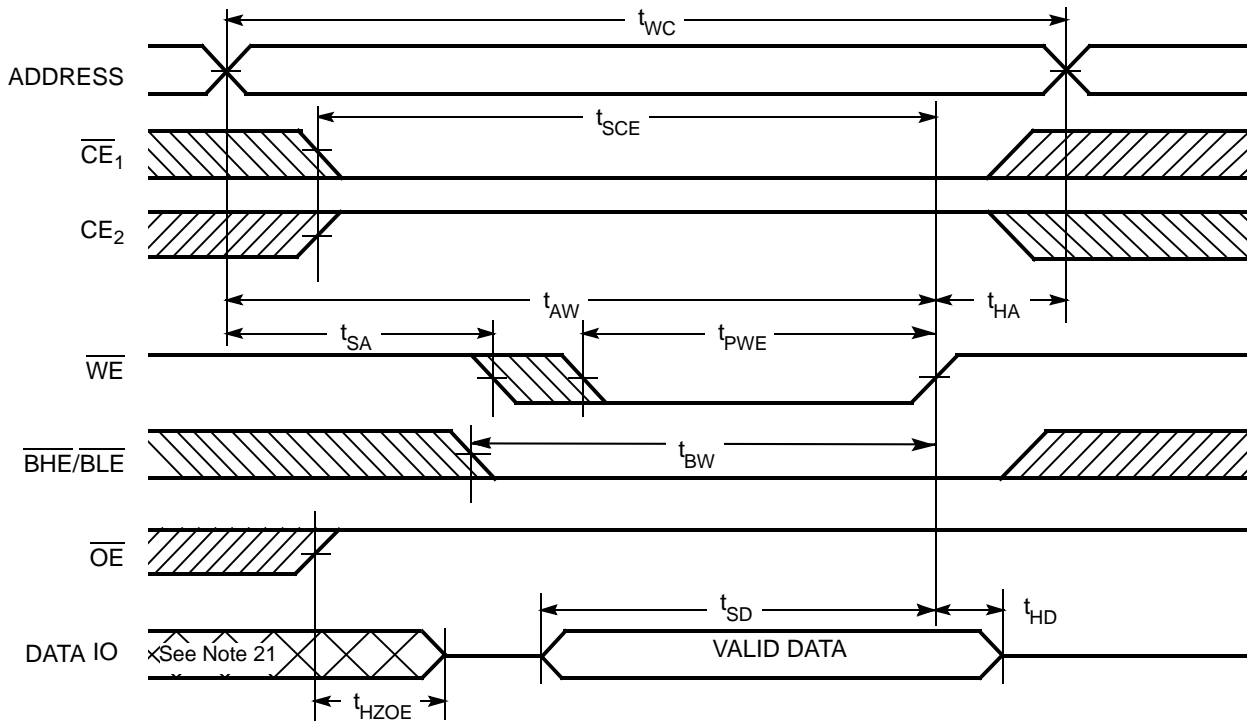


**Notes:**

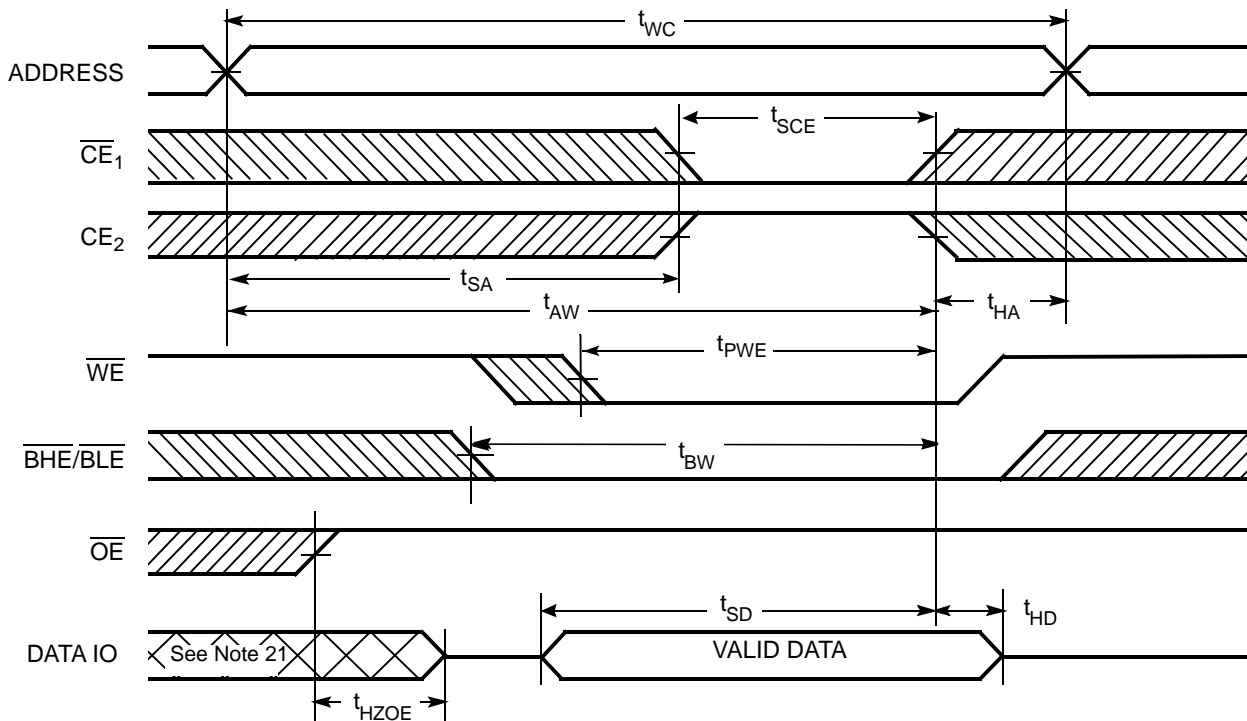
- 16. The device is continuously selected.  $\overline{\text{OE}}$ ,  $\overline{\text{CE}}_1 = V_{\text{IL}}$ ,  $\overline{\text{BHE}}$  and/or  $\overline{\text{BLE}} = V_{\text{IL}}$ , and  $\text{CE}_2 = V_{\text{IH}}$ .
- 17. WE is HIGH for read cycle.
- 18. Address valid prior to or coincident with  $\overline{\text{CE}}_1$ ,  $\overline{\text{BHE}}$ ,  $\overline{\text{BLE}}$  transition LOW and  $\text{CE}_2$  transition HIGH.

**Switching Waveforms (continued)**

**Write Cycle 1 ( $\overline{\text{WE}}$  Controlled)<sup>[15, 19, 20, 21]</sup>**



**Write Cycle 2 ( $\overline{\text{CE}}_1$  or  $\text{CE}_2$  Controlled)<sup>[15, 19, 20, 21]</sup>**

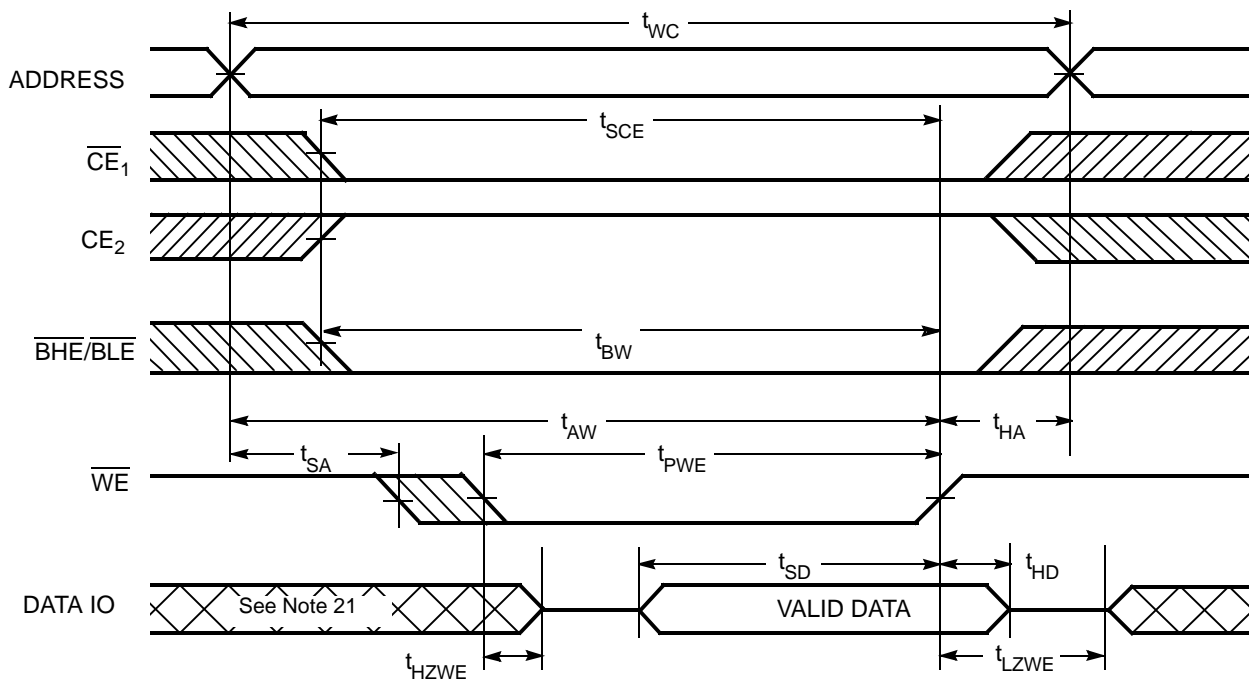


**Notes:**

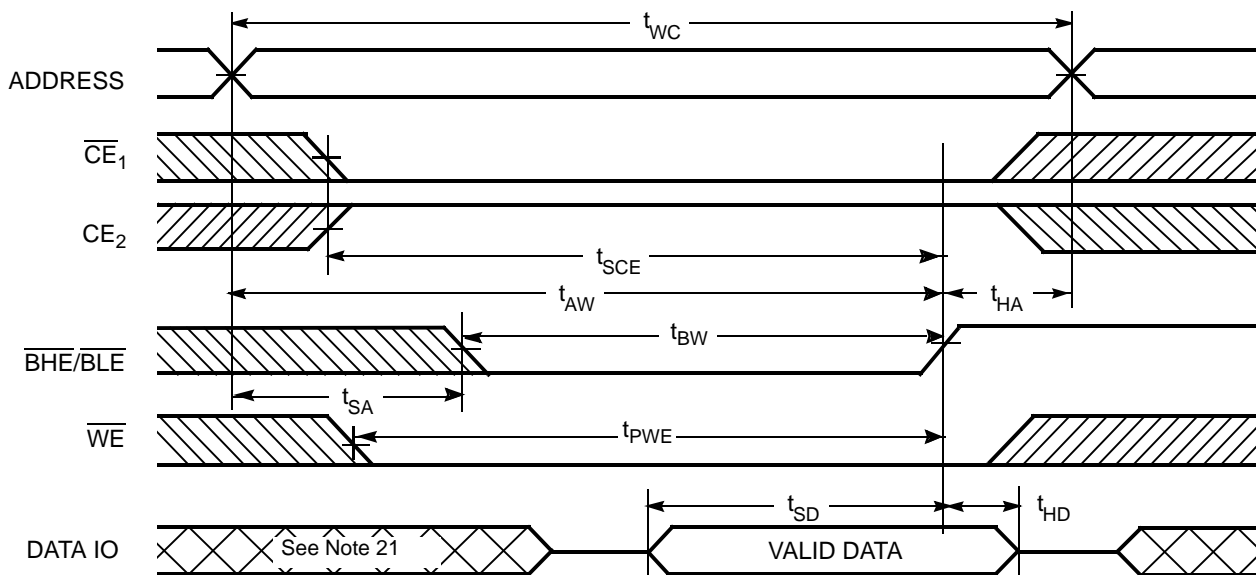
19. Data IO is high impedance if  $\overline{\text{OE}} = V_{\text{IH}}$ .
20. If  $\overline{\text{CE}}_1$  goes HIGH and  $\text{CE}_2$  goes LOW simultaneously with  $\overline{\text{WE}} = V_{\text{IH}}$ , the output remains in a high-impedance state.
21. During this period, the IOs are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle 3 ( $\overline{\text{WE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[20, 21]</sup>



Write Cycle 4 ( $\overline{\text{BHE/BLE}}$  Controlled,  $\overline{\text{OE}}$  LOW)<sup>[20, 21]</sup>





**Truth Table**

$\overline{CE}_1$	$CE_2$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs	Mode	Power
H	X	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
X	L	X	X	X	X	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
X	X	X	X	H	H	High Z	Deselect/Power-Down	Standby ( $I_{SB}$ )
L	H	H	L	L	L	Data Out ( $IO_0$ – $IO_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	H	L	Data Out ( $IO_0$ – $IO_7$ ); High Z ( $IO_8$ – $IO_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	L	L	H	High Z ( $IO_0$ – $IO_7$ ); Data Out ( $IO_8$ – $IO_{15}$ )	Read	Active ( $I_{CC}$ )
L	H	H	H	L	H	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	H	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	H	H	L	L	High Z	Output Disabled	Active ( $I_{CC}$ )
L	H	L	X	L	L	Data In ( $IO_0$ – $IO_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	H	L	Data In ( $IO_0$ – $IO_7$ ); High Z ( $IO_8$ – $IO_{15}$ )	Write	Active ( $I_{CC}$ )
L	H	L	X	L	H	High Z ( $IO_0$ – $IO_7$ ); Data In ( $IO_8$ – $IO_{15}$ )	Write	Active ( $I_{CC}$ )

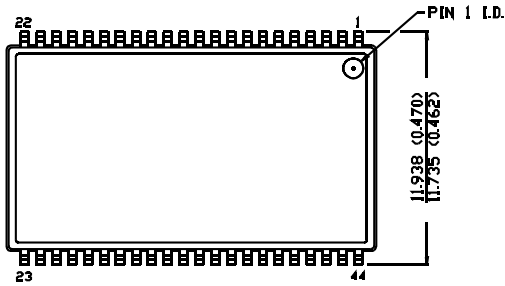
**Ordering Information**

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY62157ELL-45ZSXI	51-85087	44-pin Thin Small Outline Package Type II (Pb-free)	Industrial
55	CY62157ELL-55ZSXE	51-85087	44-pin Thin Small Outline Package Type II (Pb-free)	Automotive
	CY62157ELL-55BVXE	51-85150	48-ball Very Fine Pitch Ball Grid Array (Pb-free)	

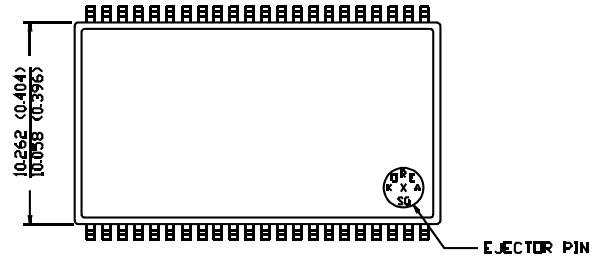
Package Diagrams

44-pin TSOP II (51-85087)

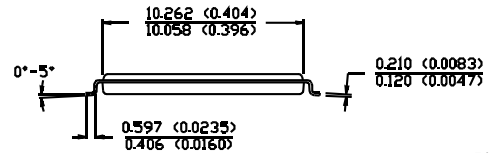
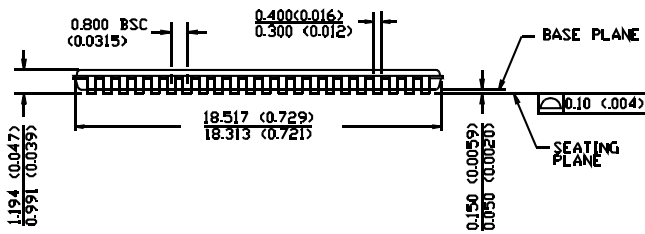
DIMENSION IN MM (INCH)  
MAX  
MIN



TOP VIEW



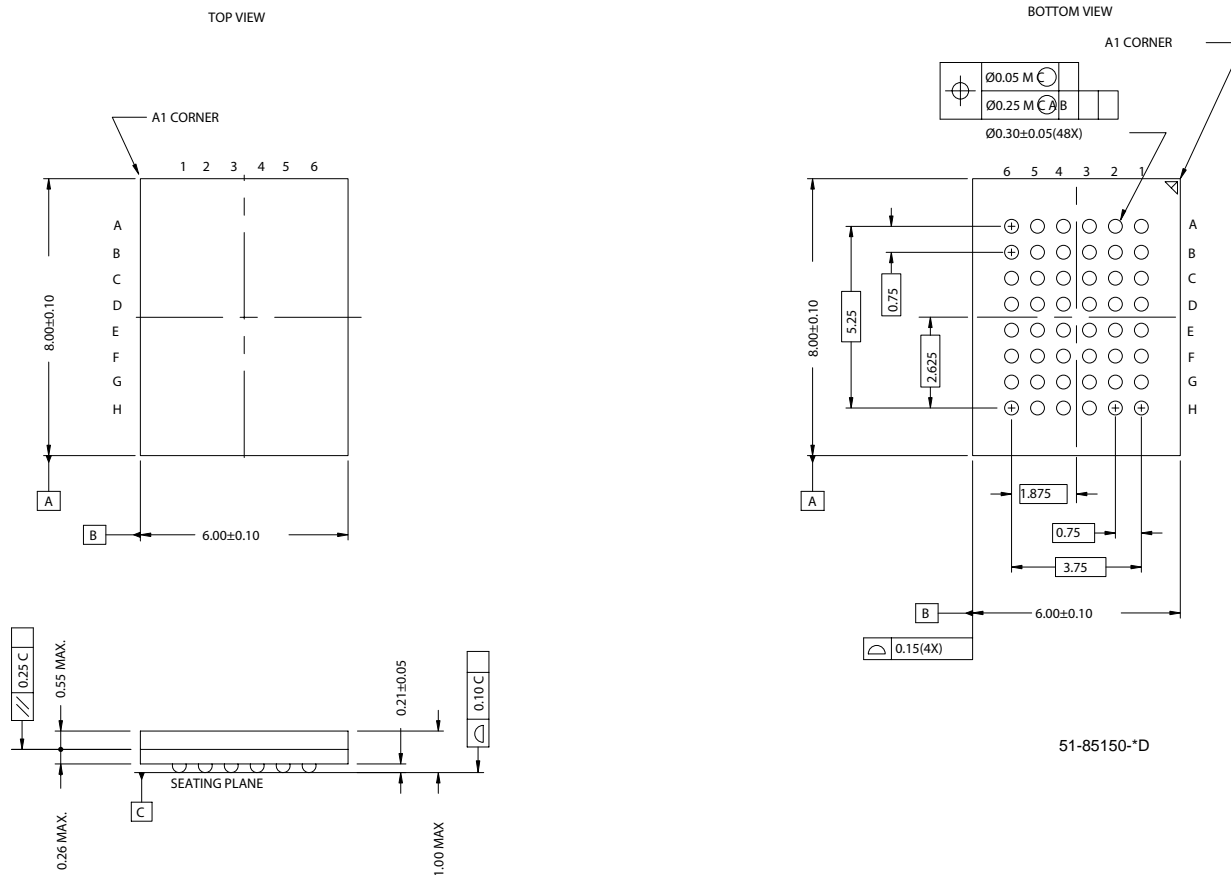
BOTTOM VIEW



51-85087-A

Package Diagrams (continued)

48-ball VFBGA (6 x 8 x 1 mm) (51-85150)



51-85150-D

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**Document History Page**

Document Title: CY62157E MoBL®, 8-Mbit (512K x 16) Static RAM Document Number: 38-05695				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	291273	See ECN	PCI	New data sheet
*A	457689	See ECN	NXR	Added Automotive Product Removed Industrial Product Removed 35 ns and 45 ns speed bins Removed "L" bin Updated AC Test Loads table Corrected $t_R$ in Data Retention Characteristics from 100 $\mu$ s to $t_{RC}$ ns Updated the Ordering Information and replaced the Package Name column with Package Diagram
*B	467033	See ECN	NXR	Added Industrial Product (Final Information) Removed 48 ball VFPGA package and its relevant information Changed the $I_{CC(typ)}$ value of Automotive from 2 mA to 1.8 mA for $f = 1$ MHz Changed the $I_{SB2(typ)}$ value of Automotive from 5 $\mu$ A to 1.8 $\mu$ A Modified footnote #4 to include current limit Updated the Ordering Information table
*C	569114	See ECN	VKN	Added 48 ball VFPGA package Updated Logic Block Diagram Added footnote #3 Updated the Ordering Information table