CY62138V MoBL™

2-Mbit (256K x 8) Static RAM

Features

- **High Speed:**
  — 70 ns
- **Low voltage range:**
  — 2.7V – 3.6V
- **Ultra-low active power**
- **Low standby power**
- **Easy memory expansion with $\overline{CS_1}$/CS_2 and $\overline{OE}$ features**
- **TTL-compatible inputs and outputs**
- **Automatic power-down when deselected**
- **CMOS for optimum speed/power**
- **Available in non Pb-free 36-ball FBGA package**

Functional Description

The CY62138V is a high-performance CMOS static RAM organized as 256K words by 8 bits. This device features advanced circuit design to provide ultra-low active current. This is ideal for providing More Battery Life™ (MoBL®) in portable applications such as cellular telephones. The device also has an automatic power-down feature that reduces power consumption by 99% when addresses are not toggling. The device can be put into standby mode when deselected ($\overline{CS_1}$ HIGH or CS_2 LOW).

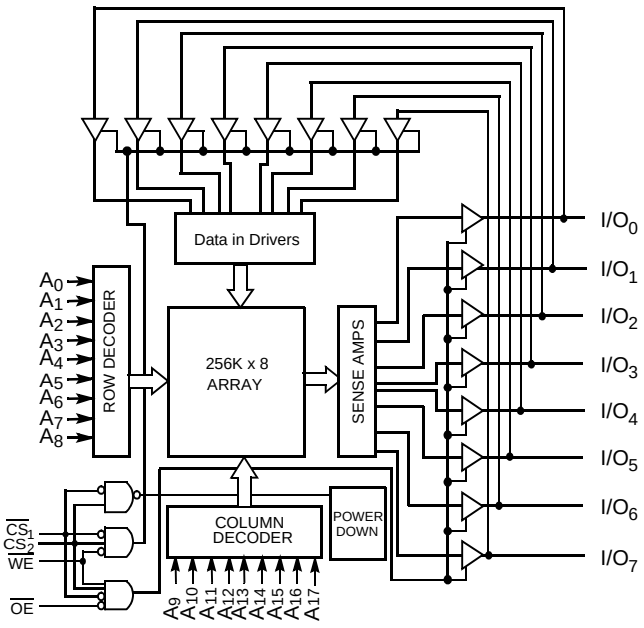
Writing to the device is accomplished by taking Chip Enable One ($\overline{CS_1}$) and Write Enable ($\overline{WE}$) inputs LOW and Chip Enable Two (CS_2) HIGH. Data on the eight I/O pins (I/O_0 through I/O_7) is then written into the location specified on the address pins (A_0 through A_{17}).

Reading from the device is accomplished by taking Chip Enable One ($\overline{CS_1}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) and Chip Enable Two (CS_2) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The eight input/output pins (I/O_0 through I/O_7) are placed in a high-impedance state when the device is deselected ($\overline{CS_1}$ HIGH or CS_2 LOW), the outputs are disabled ($\overline{OE}$ HIGH), or during a write operation ($\overline{CS_1}$ LOW, CS_2 HIGH, and $\overline{WE}$ LOW).

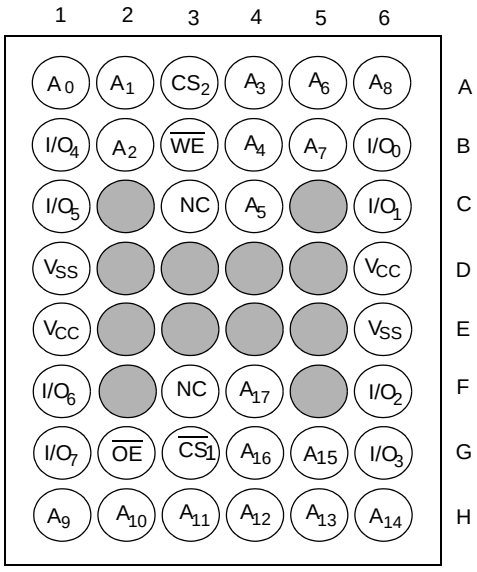
The CY62138V is available in a 36-ball FBGA package.

Logic Block Diagram



Pin Configuration

36-ball FBGA
TOP View



Product Portfolio

Product	V_{CC} Range (V)			Speed (ns)	Power Dissipation (Industrial)			
					Operating, I_{CC} (mA)		Standby, I_{SB2} (µA)	
	$V_{CC(min)}$	$V_{CC(typ)}$[1]	$V_{CC(max)}$		Typ.[1]	Maximum	Typ.[1]	Maximum
CY62138V	2.7	3.0	3.6	70	7	15	1	15

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... –65°C to +150°C

Ambient Temperature with Power Applied ..... –55°C to +125°C

Supply Voltage to Ground Potential ..... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[2] ..... –0.5V to V_{CC} + 0.5V

DC Input Voltage[2] ..... –0.5V to V_{CC} + 0.5V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current ..... > 200 mA

Operating Range

Device	Range	Ambient Temperature	V_{CC}
CY62138V	Industrial	–40°C to +85°C	2.7V to 3.6V

Electrical Characteristics Over the Operating Range

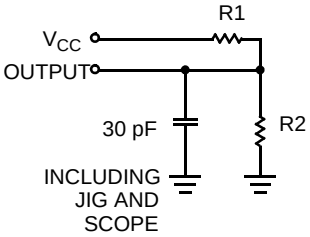
Parameter	Description	Test Conditions		CY62138V			Unit
				Min.	Typ.[1]	Max.	
V_{OH}	Output HIGH Voltage	I_{OH} = –1.0 mA	V_{CC} = 2.7V	2.4			V
V_{OL}	Output LOW Voltage	I_{OL} = 2.1 mA	V_{CC} = 2.7V			0.4	V
V_{IH}	Input HIGH Voltage		V_{CC} = 3.6V	2.2		V_{CC} + 0.5V	V
V_{IL}	Input LOW Voltage		V_{CC} = 2.7V	–0.5		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_I ≤ V_{CC}		–1	±1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		–1	+1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	I_{OUT} = 0 mA, f = f_{Max} = $1/t_{RC}$, CMOS Levels	V_{CC} = 3.6V		7	15	mA
		I_{OUT} = 0 mA, f = 1 MHz, CMOS Levels			1	2	mA
I_{SB1}	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, f = f_{Max}				100	µA
I_{SB2}	Automatic CE Power-down Current—CMOS Inputs	$\overline{CE}$ ≥ V_{CC}–0.3V V_{IN} ≥ V_{CC}–0.3V or V_{IN} ≤ 0.3V, f = 0	V_{CC} = 3.6V		1	15	µA

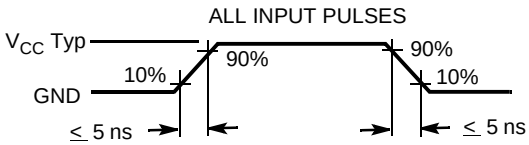
Capacitance[3]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = $V_{CC(typ)}$	6	pF
C_{OUT}	Output Capacitance		8	pF

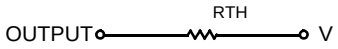
Notes:
1. Typical values are included for reference only and are not guaranteed or tested. Typical values are measured at V_{CC} = V_{CC} Typ, T_A = 25°C.
2. V_{IL}(min) = –2.0V for pulse durations less than 20 ns.
3. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms





Equivalent to: THEVENIN EQUIVALENT

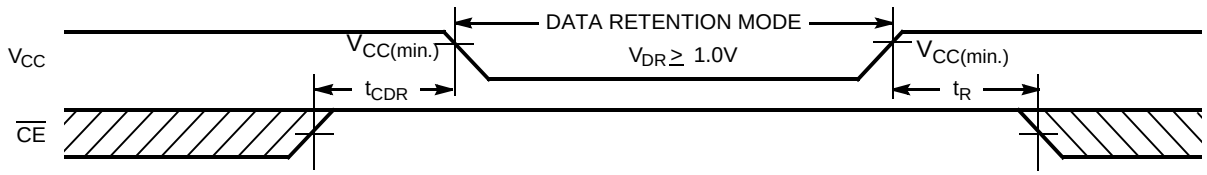


Parameters	3.0V	Unit
R1	1105	Ohms
R2	1550	Ohms
R_{TH}	645	Ohms
V_{TH}	1.75	Volts

Data Retention Characteristics (Over the Operating Range)

Parameter	Description	Conditions[4]	Min.	Typ.[1]	Max.	Unit
V_{DR}	V_{CC} for Data Retention		1.0		3.6	V
I_{CCDR}	Data Retention Current	V_{CC} = 1.0V, CE ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V or V_{IN} ≤ 0.3V, No input may exceed V_{CC}+0.3V		0.1	5	µA
t_{CDR}[3]	Chip Deselect to Data Retention Time		0			ns
t_R	Operation Recovery Time		100			µs

Data Retention Waveform[5]



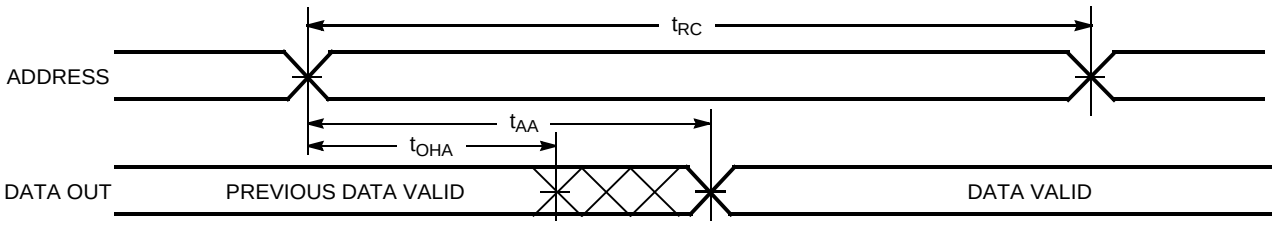
Notes:
4. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to $V_{CC(typ.)}$, and output loading of the specified I_{OL}/I_{OH} and 30 pF load capacitance.
5. $\overline{CE}$ is the combination of both $\overline{CS_1}$ and CS_2.

Switching Characteristics Over the Operating Range[4]

Parameter	Description	70 ns		Unit
		Min.	Max.	
Read Cycle				
t_{RC}	Read Cycle Time	70		ns
t_{AA}	Address to Data Valid		70	ns
t_{OHA}	Data Hold from Address Change	10		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		70	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		35	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[6]	5		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[6, 7]		25	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[6]	10		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[6, 7]		25	ns
t_{PU}	$\overline{CE}$ LOW to Power-up	0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-down		70	ns
Write Cycle[8, 9]				
t_{WC}	Write Cycle Time	70		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	60		ns
t_{AW}	Address Set-up to Write End	60		ns
t_{HA}	Address Hold from Write End	0		ns
t_{SA}	Address Set-up to Write Start	0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	50		ns
t_{SD}	Data Set-up to Write End	30		ns
t_{HD}	Data Hold from Write End	0		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[6, 7]		25	ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[6]	10		ns

Switching Waveforms

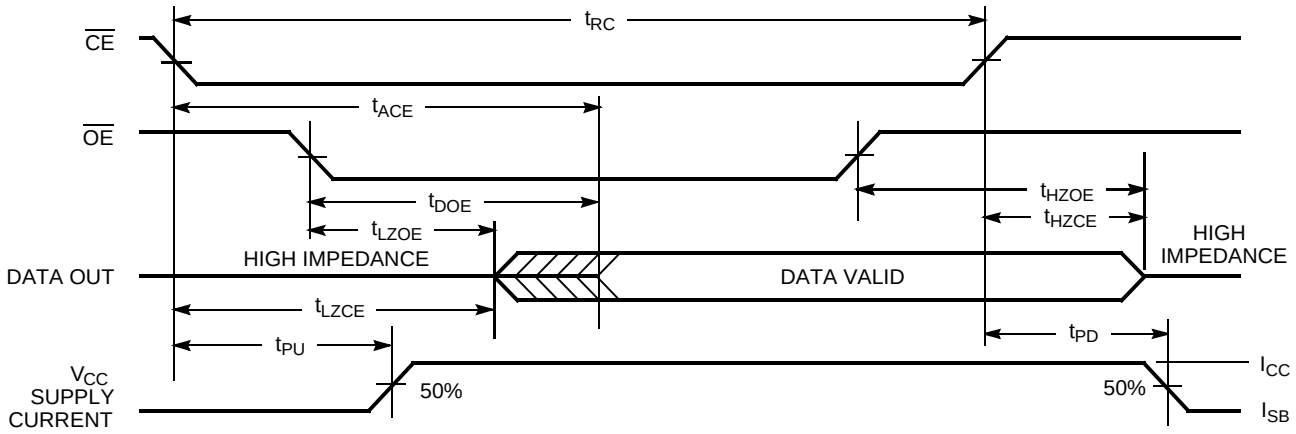
Read Cycle No. 1 (Address Transition Controlled)[10, 11]



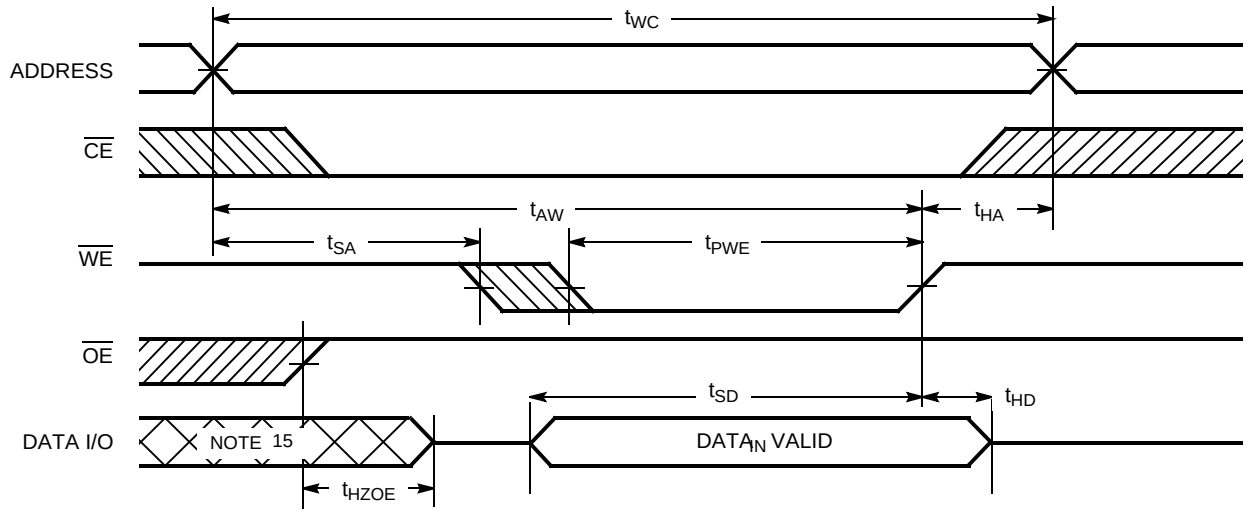
Notes:
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
7. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with C_L = 5 pF as in (b) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. The minimum write cycle time for write cycle #3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.
10. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
11. $\overline{WE}$ is HIGH for read cycle.

Switching Waveforms (continued)

Read Cycle No. 2 (OE Controlled)[5, 11, 12]



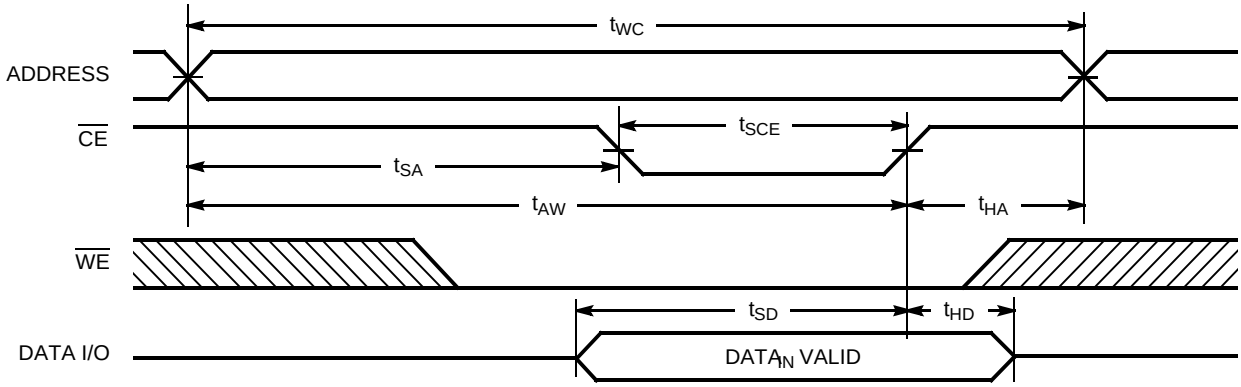
Write Cycle No. 1 (WE Controlled)[5, 8, 13, 14]



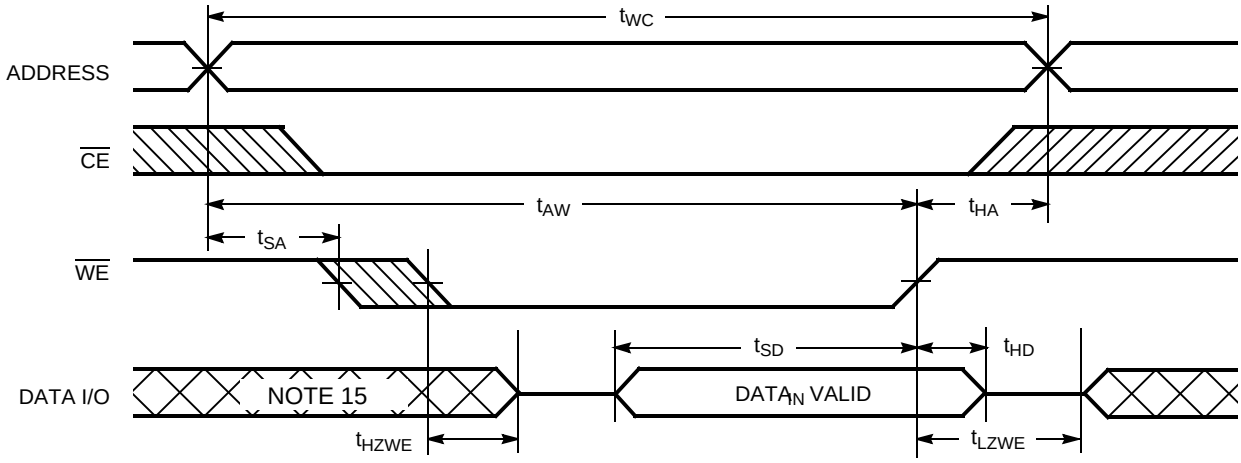
Notes:
12. Address valid prior to or coincident with CE transition LOW.
13. Data I/O is high impedance if OE = VIH.
14. If CE goes HIGH simultaneously with WE HIGH, the output remains in a high-impedance state.
15. During this period, the I/Os are in output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 2 ($\overline{CE}$ Controlled)[5, 8, 13, 14]

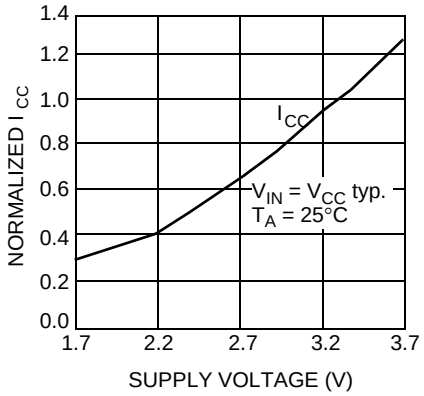


Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[5, 9, 14]

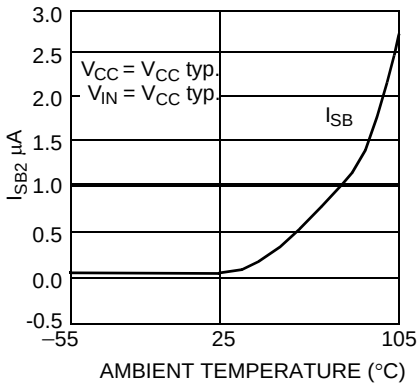


Typical DC and AC Characteristics

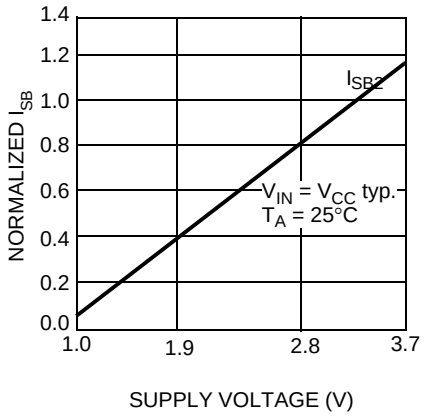
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



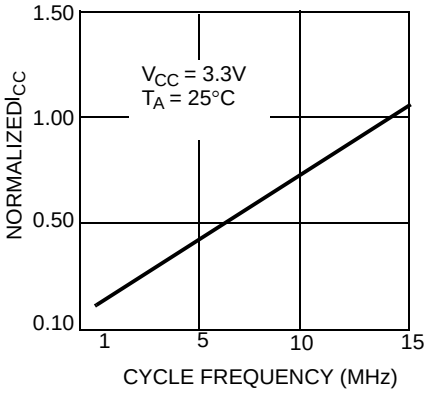
STANDBY CURRENT vs. AMBIENT TEMPERATURE



NORMALIZED STANDBY CURRENT vs. SUPPLY VOLTAGE



NORMALIZED I_{CC} vs. CYCLE TIME



Truth Table

$\overline{CS_1}$	CS_2	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs	Mode	Power
H	X	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
X	L	X	X	High-Z	Deselect/Power-down	Standby (I_{SB})
L	H	H	L	Data Out	Read	Active (I_{CC})
L	H	L	X	Data In	Write	Active (I_{CC})
L	H	H	H	High-Z	Deselect, Output Disabled	Active (I_{CC})

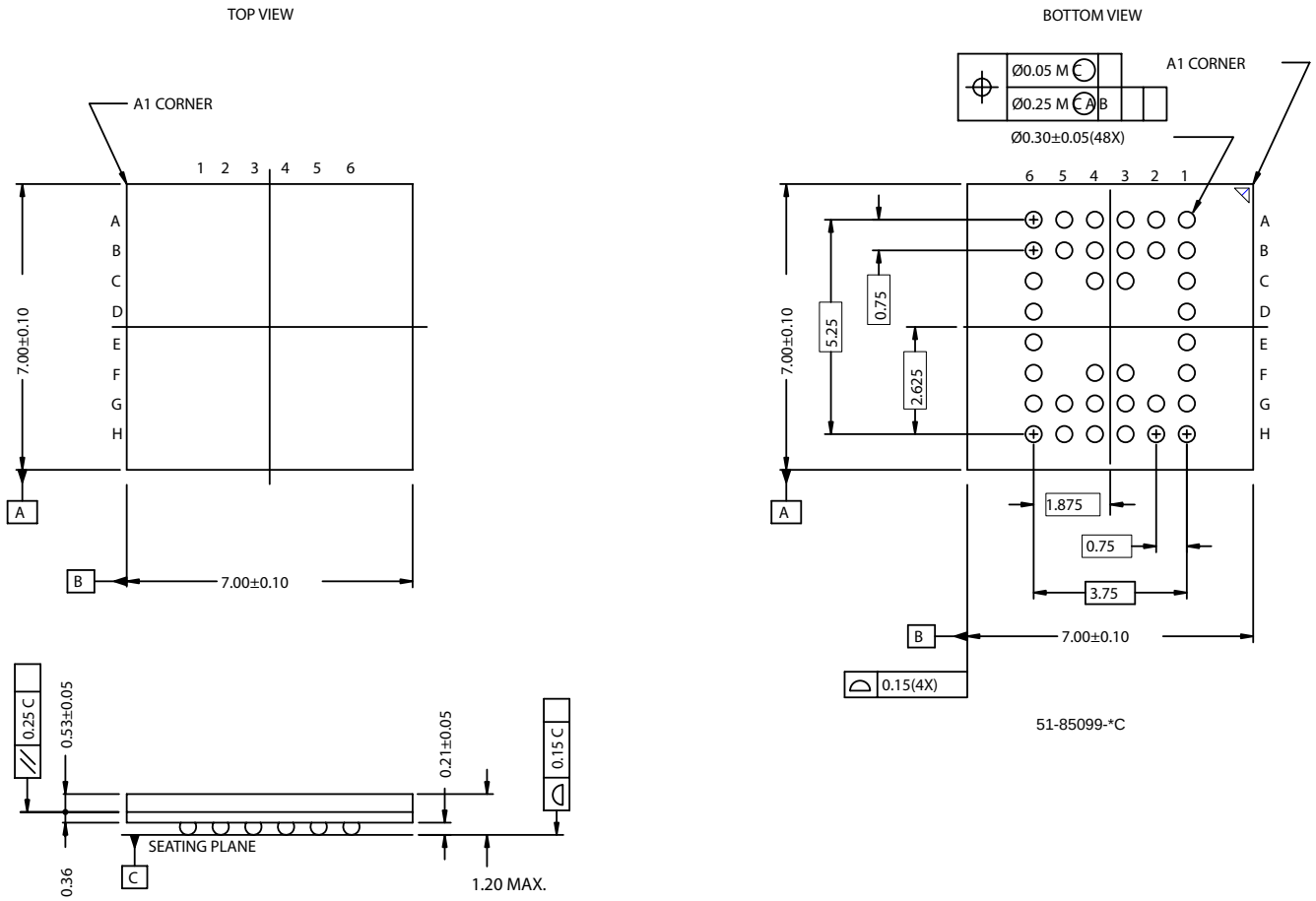
Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
70	CY62138VLL-70BAI	51-85099	36-ball Fine Pitch Ball Grid Array (7 x 7 x 1.2 mm)	Industrial

Please contact your local Cypress sales representative for availability of these parts

Package Diagram

36-ball FBGA (7 x 7 x 1.2 mm) (51-85099)



More Battery Life is a trademark, and MoBL is a registered trademark, of Cypress Semiconductor. All products and company names mentioned in this document may be the trademarks of their respective holders.

Document History Page

Document Title: CY62138V MoBL™ 2-Mbit (256K x 8) Static RAM Document Number: 38-05088				
REV.	**ECN NO.**	**Issue Date**	**Orig. of Change**	**Description of Change**
**	107348	06/12/01	SZV	Change from Spec #: 38-00729 to 38-05088
*A	114936	05/28/02	CBD	Replaced wrong package diagram with correct diagram (36-ball FBGA [see p. 8])
*B	486789	SEE ECN	VKN	Changed address of Cypress Semiconductor Corporation on Page# 1 from “3901 North First Street” to “198 Champion Court”. Updated Ordering Information table