

Features

- Industry-standard Architecture
 - Low-cost, Easy-to-use Software Tools
- High-speed, Electrically Erasable Programmable Logic Devices
 - 5 ns Maximum Pin-to-pin Delay
- Latch Feature Holds Inputs to Previous Logic States
- Pin-controlled Standby Power (10 μ A Typical)
- Advanced Flash Technology
 - Reprogrammable
 - 100% Tested
- High-reliability CMOS Process
 - 20-year Data Retention
 - 100 Erase/Write Cycles
 - 2,000V ESD Protection
 - 200 mA Latch-up Immunity
- Dual Inline and Surface Mount Packages in Standard Pinouts
- PCI-compliant
- Green Package Options (Pb/Halide-free/RoHS Compliant) Available
- Full Military, Commercial and Industrial Temperature Ranges
- Backward-Compatible with ATF22V10B(Q) and AT22V10(L)

1. Description

The ATF22V10C is a high-performance CMOS (electrically erasable) programmable logic device (PLD) that utilizes Atmel's proven electrically erasable Flash memory technology. Speeds down to 5 ns and power dissipation as low as 100 μ A are offered. All speed ranges are specified over the full 5V \pm 10% range for military and industrial temperature ranges, and 5V \pm 5% for commercial temperature ranges.

Several low-power options allow selection of the best solution for various types of power-limited applications. Each of these options significantly reduces total system power and enhances system reliability.

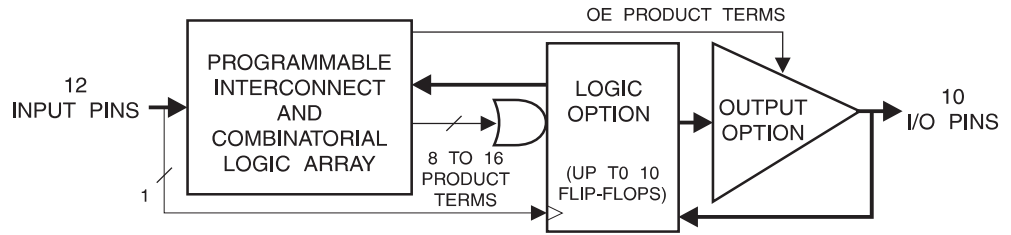


**High-
performance
EE PLD**

**ATF22V10C
ATF22V10CQ**

**See separate datasheet
for the ATF22V10CQZ.**

Figure 1-1. Logic Diagram



2. Pin Configurations

Table 2-1. Pin Configurations (All Pinouts Top View)

| Pin Name | Function |
|----------|------------------------|
| CLK | Clock |
| IN | Logic Inputs |
| I/O | Bi-directional Buffers |
| GND | Ground |
| VCC | +5V Supply |
| PD | Power-down |

Figure 2-1. TSSOP

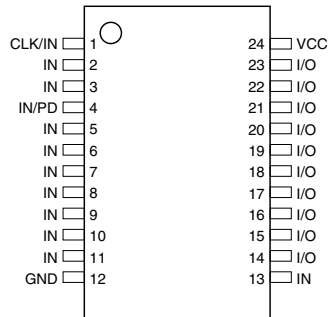


Figure 2-2. DIP/SOIC

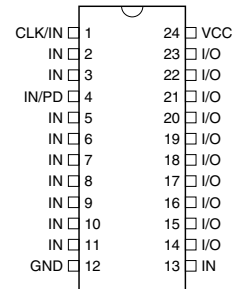
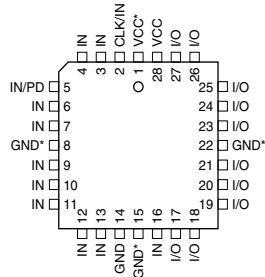


Figure 2-3. PLCC/LCC



Note: For all PLCCs (except "-5"), pins 1, 8, 15 and 22 can be left unconnected. However, if they are connected, superior performance will be achieved.

3. Absolute Maximum Ratings*

| | |
|---|--------------------------------|
| Temperature under Bias | -55°C to +125°C |
| Storage Temperature | -65°C to +150°C |
| Voltage on Any Pin with Respect to Ground | -2.0V to +7.0V ⁽¹⁾ |
| Voltage on Input Pins with Respect to Ground during Programming | -2.0V to +14.0V ⁽¹⁾ |
| Programming Voltage with Respect to Ground | -2.0V to +14.0V ⁽¹⁾ |

*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is $V_{CC} + 0.75V$ DC, which may overshoot to 7.0V for pulses of less than 20 ns.

4. DC and AC Operating Conditions

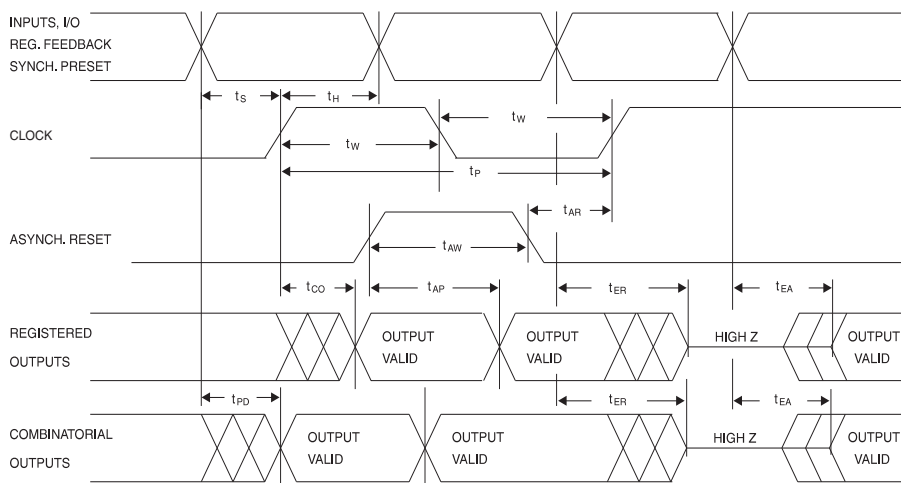
| | Commercial | Industrial | Military |
|---------------------------------|------------|--------------|----------------------|
| Operating Temperature (Ambient) | 0°C - 70°C | -40°C - 85°C | -55°C - 125°C (case) |
| V_{CC} Power Supply | 5V ± 5% | 5V ± 10% | 5V ± 10% |

4.1 DC Characteristics

| Symbol | Parameter | Condition | Min | Typ | Max | Units | |
|----------------|-----------------------------------|--|----------------------------|------------|---------------|---------------|----|
| I_{IL} | Input or I/O Low Leakage Current | $0 \leq V_{IN} \leq V_{IL} \text{ (Max)}$ | | | -10.0 | μA | |
| I_{IH} | Input or I/O High Leakage Current | $3.5 \leq V_{IN} \leq V_{CC}$ | | | 10.0 | μA | |
| I_{CC} | Power Supply Current, Standby | $V_{CC} = \text{Max},$ $V_{IN} = \text{Max},$ Outputs Open | C-5, 7, 10 | Com. | 85.0 | 130.0 | mA |
| | | | C-10 | Ind., Mil. | 90.0 | 140.0 | mA |
| | | | C-15 | Com. | 65.0 | 90.0 | mA |
| | | | C-15 | Ind., Mil. | 65.0 | 115.0 | mA |
| | | | CQ-15 | Com. | 35.0 | 55.0 | mA |
| | | | CQ-15 | Ind. | 35.0 | 70.0 | mA |
| I_{CC2} | Clocked Power Supply Current | $V_{CC} = \text{Max},$ Outputs Open, $f = 15 \text{ MHz}$ | C-5, 7, 10 | Com. | | 150.0 | mA |
| | | | C-10 | Ind., Mil. | | 160.0 | mA |
| | | | C-15 | Com. | 70.0 | 90.0 | mA |
| | | | C-15 | Ind., Mil. | 70.0 | 90.0 | mA |
| | | | CQ-15 | Com. | 40.0 | 60.0 | mA |
| | | | CQ-15 | Ind. | 40.0 | 80.0 | mA |
| I_{PD} | Power Supply Current, PD Mode | $V_{CC} = \text{Max}$ | Com. | 10.0 | 100.0 | μA | |
| | | $V_{IN} = 0, \text{ Max}$ | Ind. | 10.0 | 100.0 | μA | |
| $I_{OS}^{(1)}$ | Output Short Circuit Current | $V_{OUT} = 0.5\text{V}$ | | | -130.0 | mA | |
| V_{IL} | Input Low Voltage | | -0.5 | | 0.8 | V | |
| V_{IH} | Input High Voltage | | 2.0 | | $V_{CC}+0.75$ | V | |
| V_{OL} | Output Low Voltage | $V_{IN} = V_{IH} \text{ or } V_{IL},$ $V_{CC} = \text{Min}$ | $I_{OL} = 16 \text{ mA}$ | Com., Ind. | | 0.5 | V |
| | | | $I_{OL} = 12 \text{ mA}$ | Mil. | | 0.5 | V |
| V_{OH} | Output High Voltage | $V_{IN} = V_{IH} \text{ or } V_{IL},$ $V_{CC} = \text{Min}$ | $I_{OH} = -4.0 \text{ mA}$ | | 2.4 | | V |

Note: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

4.2 AC Waveforms ⁽¹⁾



Note: 1. Timing measurement reference is 1.5V. Input AC driving levels are 0.0V and 3.0V, unless otherwise specified.

4.3 AC Characteristics ⁽¹⁾

| Symbol | Parameter | -5 | | -7 | | -10 | | -15 | | Units |
|-----------|--|-------|-----|----------------------|--------------------|-------|------|------|------|-------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{PD} | Input or Feedback to Combinatorial Output | 1.0 | 5.0 | 3.0 | 7.5 | 3.0 | 10.0 | 3.0 | 15.0 | ns |
| t_{CO} | Clock to Output | 1.0 | 4.0 | 2.0 | 4.5 ⁽²⁾ | 2.0 | 6.5 | 2.0 | 8.0 | ns |
| t_{CF} | Clock to Feedback | | 2.5 | | 2.5 | | 2.5 | | 2.5 | ns |
| t_S | Input or Feedback Setup Time | 3.0 | | 3.5 | | 4.5 | | 10.0 | | ns |
| t_H | Hold Time | 0 | | 0 | | 0 | | 0 | | ns |
| f_{MAX} | External Feedback $1/(t_S + t_{CO})$ | 142.0 | | 125.0 ⁽³⁾ | | 90.0 | | 55.5 | | MHz |
| | Internal Feedback $1/(t_S + t_{CF})$ | 166.0 | | 142.0 | | 117.0 | | 80.0 | | MHz |
| | No Feedback $1/(t_{WH} + t_{WL})$ | 166.0 | | 166.0 | | 125.0 | | 83.3 | | MHz |
| t_W | Clock Width (t_{WL} and t_{WH}) | 3.0 | | 3.0 | | 3.0 | | 6.0 | | ns |
| t_{EA} | Input or I/O to Output Enable | 2.0 | 6.0 | 3.0 | 7.5 | 3.0 | 10.0 | 3.0 | 15.0 | ns |
| t_{ER} | Input or I/O to Output Disable | 2.0 | 5.0 | 3.0 | 7.5 | 3.0 | 9.0 | 3.0 | 15.0 | ns |
| t_{AP} | Input or I/O to Asynchronous Reset of Register | 3.0 | 7.0 | 3.0 | 10.0 | 3.0 | 12.0 | 3.0 | 20.0 | ns |
| t_{AW} | Asynchronous Reset Width | 5.5 | | 7.0 | | 8.0 | | | 15.0 | ns |
| t_{AR} | Asynchronous Reset Recovery Time | 4.0 | | 5.0 | | 6.0 | | | 10.0 | ns |
| t_{SP} | Setup Time, Synchronous Preset | 4.0 | | 4.5 | | 6.0 | | | 10.0 | ns |
| t_{SPR} | Synchronous Preset to Clock Recovery Time | 4.0 | | 5.0 | | 8.0 | | | 10.0 | ns |

Notes: 1. See ordering information for valid part numbers.
 2. 5.5 ns for DIP package devices.
 3. 111 MHz for DIP package devices.

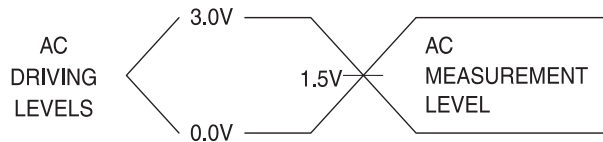
4.4 Power-down AC Characteristics⁽¹⁾⁽²⁾⁽³⁾

| Symbol | Parameter | -5 | | -7 | | -10 | | -15 | | Units |
|------------|--|-----|------|-----|------|------|------|------|------|-------|
| | | Min | Max | Min | Max | Min | Max | Min | Max | |
| t_{IVDH} | Valid Input before PD High | 5.0 | | 7.5 | | 10.0 | | 15.0 | | ns |
| t_{GVDH} | Valid \overline{OE} before PD High | 0 | | 0 | | 0 | | 0 | | ns |
| t_{CVDH} | Valid Clock before PD High | 0 | | 0 | | 0 | | | | ns |
| t_{DHIX} | Input Don't Care after PD High | | 5.0 | | 7.0 | | 10.0 | | 15.0 | ns |
| t_{DHGX} | \overline{OE} Don't Care after PD High | | 5.0 | | 7.0 | | 10.0 | | 15.0 | ns |
| t_{DHCX} | Clock Don't Care after PD High | | 5.0 | | 7.0 | | 10.0 | | 15.0 | ns |
| t_{DLIV} | PD Low to Valid Input | | 5.0 | | 7.5 | | 10.0 | | 15.0 | ns |
| t_{DLGV} | PD Low to Valid \overline{OE} | | 15.0 | | 20.0 | | 25.0 | | 30.0 | ns |
| t_{DLCV} | PD Low to Valid Clock | | 15.0 | | 20.0 | | 25.0 | | 30.0 | ns |
| t_{DLOV} | PD Low to Valid Output | | 20.0 | | 25.0 | | 30.0 | | 35.0 | ns |

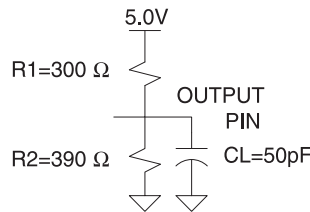
- Notes:
1. Output data is latched and held.
 2. High-Z outputs remain high-Z.
 3. Clock and input transitions are ignored.

4.5 Input Test Waveforms

4.5.1 Input Test Waveforms and Measurement Levels



4.5.2 Commercial Output Test Loads



4.6 Pin Capacitance

Table 4-1. Pin Capacitance ($f = 1 \text{ MHz}$, $T = 25^\circ\text{C}$ ⁽¹⁾)

| | Typ | Max | Units | Conditions |
|-----------|-----|-----|-------|----------------|
| C_{IN} | 5 | 8 | pF | $V_{IN} = 0V$ |
| C_{OUT} | 6 | 8 | pF | $V_{OUT} = 0V$ |

- Note:
1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

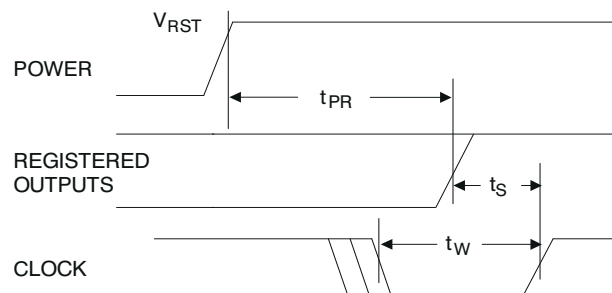
4.7 Power-up Reset

The registers in the ATF22V10Cs are designed to reset during power-up. At a point delayed slightly from V_{CC} crossing V_{RST} , all registers will be reset to the low state. The output state will depend on the polarity of the output buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V_{CC} actually rises in the system, the following conditions are required:

1. The V_{CC} rise must be monotonic, and starts below 0.7V,
2. After reset occurs, all input and feedback setup times must be met before driving the clock pin high, and
3. The clock must remain stable during t_{PR} .

Figure 4-1. Power-up Reset Timing



4.8 Preload of Registered Outputs

The ATF22V10C's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

5. Electronic Signature Word

There are 64 bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

6. Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF22V10C fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible.

The security fuse should be programmed last, as its effect is immediate.

7. Programming/Erasing

Programming/erasing is performed using standard PLD programmers. See “CMOS PLD Programming Hardware & Software Support” for information on software/programming.

Table 7-1. Programming/Erasing

| Parameter | Description | Typ | Max | Units |
|-----------|------------------------|-----|-------|-------|
| t_{PR} | Power-up Reset Time | 600 | 1,000 | ns |
| V_{RST} | Power-up Reset Voltage | 3.8 | 4.5 | V |

8. Input and I/O Pin-keeper Circuits

The ATF22V10C contains internal input and I/O pin-keeper circuits. These circuits allow each ATF22V10C pin to hold its previous value even when it is not being driven by an external source or by the device’s output buffer. This helps to ensure that all logic array inputs are at known valid logic levels. This reduces system power by preventing pins from floating to indeterminate levels. By using pin-keeper circuits rather than pull-up resistors, there is no DC current required to hold the pins in either logic state (high or low).

These pin-keeper circuits are implemented as weak feedback inverters, as shown in the Input Diagram below. These keeper circuits can easily be overdriven by standard TTL- or CMOS-compatible drivers. The typical overdrive current required is 40 μ A.

Figure 8-1. Input Diagram

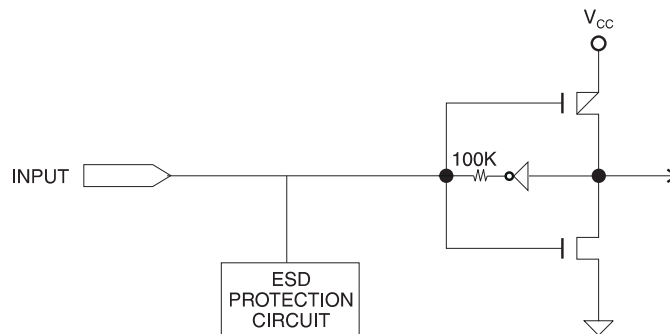
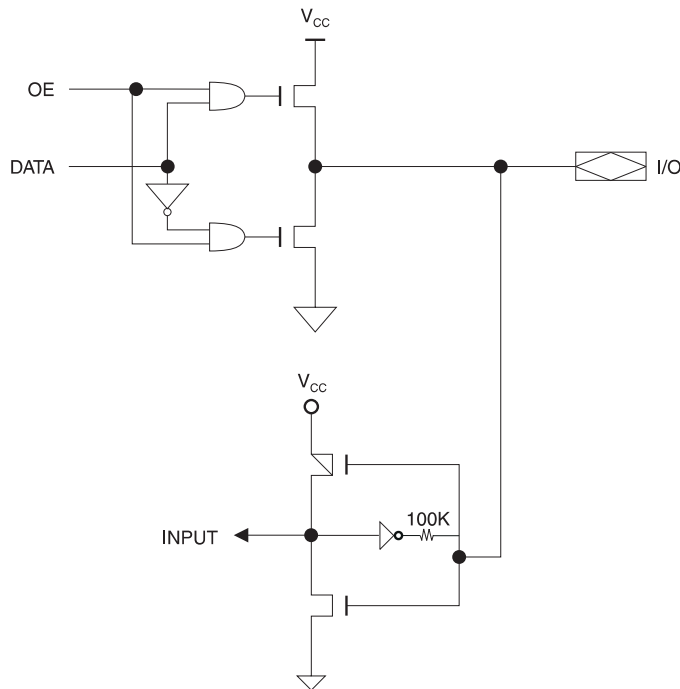


Figure 8-2. I/O Diagram



9. Power-down Mode

The ATF22V10C includes an optional pin-controlled power-down feature. When this mode is enabled, the PD pin acts as the power-down pin (Pin 4 on the DIP/SOIC packages and Pin 5 on the PLCC package). When the PD pin is high, the device supply current is reduced to less than 100 mA. During power-down, all output data and internal logic states are latched and held. Therefore, all registered and combinatorial output data remain valid. Any outputs that were in an undetermined state at the onset of power-down will remain at the same state. During power-down, all input signals except the power-down pin are blocked. Input and I/O hold latches remain active to ensure that pins do not float to indeterminate levels, further reducing system power. The power-down pin feature is enabled in the logic design file. Designs using the power-down pin may not use the PD pin logic array input. However, all other PD pin macrocell resources may still be used, including the buried feedback and foldback product term array inputs.

PD pin configuration is controlled by the design file, and appears as a separate fuse bit in the JEDEC file. When the power-down feature is not specified in the design file, the IN/PD pin will be configured as a regular logic input.

Note: Some programmers list the 22V10 JEDEC compatible 22V10C (no PD used) separately from the non-22V10 JEDEC compatible 22V10CEX (with PD used).

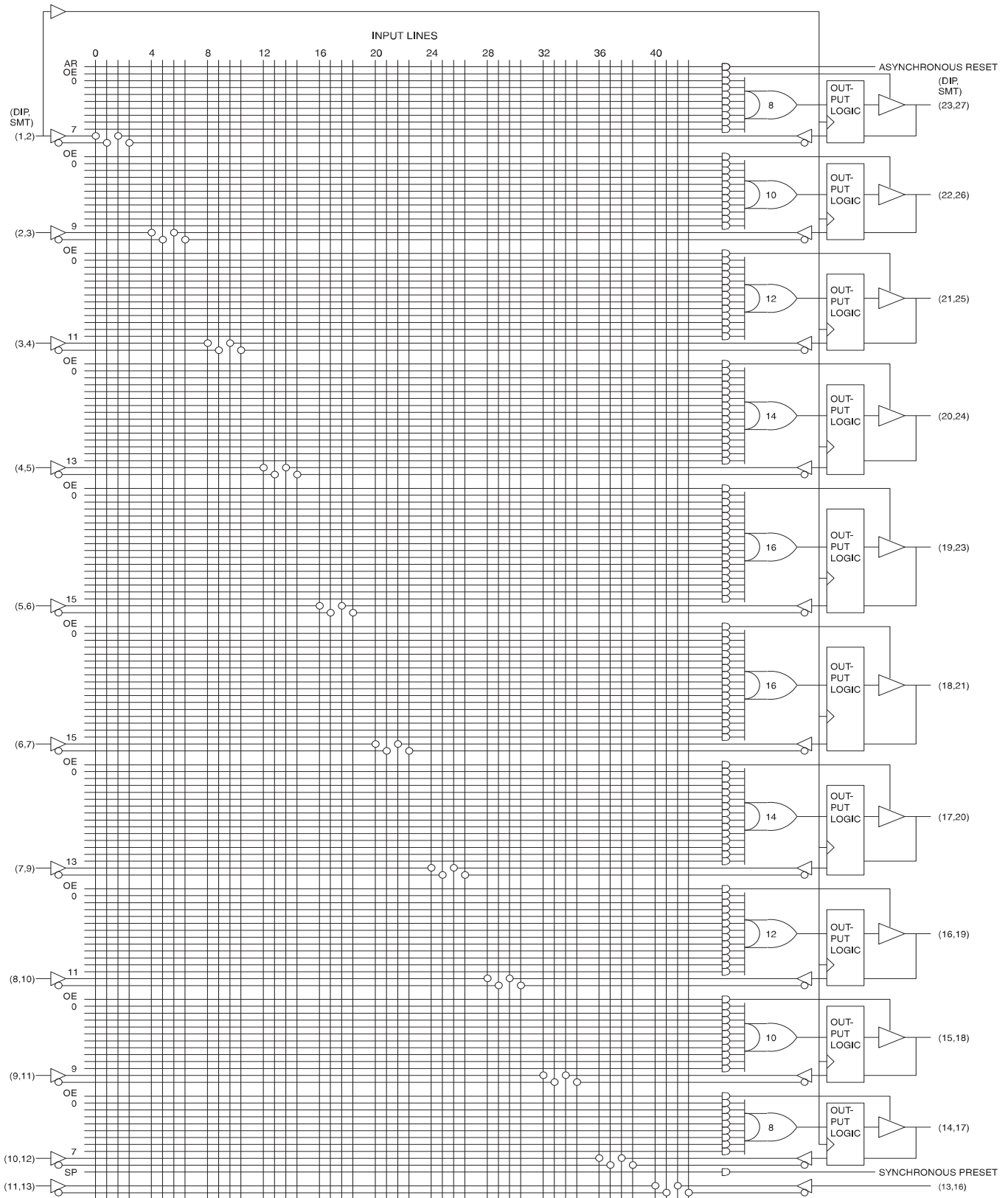
10. Compiler Mode Selection

Table 10-1. Compiler Mode Selection

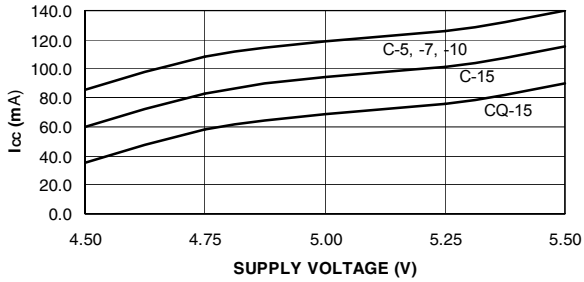
| | PAL Mode (5828 Fuses) | GAL Mode (5892 Fuses) | Power-down Mode⁽¹⁾ (5893 Fuses) |
|----------|-------------------------------------|--|---|
| Synario | ATF22V10C (DIP) ATF22V10C (PLCC) | ATTF22V10C DIP (UES) ATF22C10C PLCC (UES) | ATF22V10C DIP (PWD) ATF22V10C PLCC (PWD) |
| WINCUPPL | P22V10 P22V10LCC | G22V10 G22V10LCC | G22V10CP G22V10CPLCC |

Note: 1. These device types will create a JEDEC file which when programmed in ATF22V10C devices will enable the power-down mode feature. All other device types have the feature disabled.

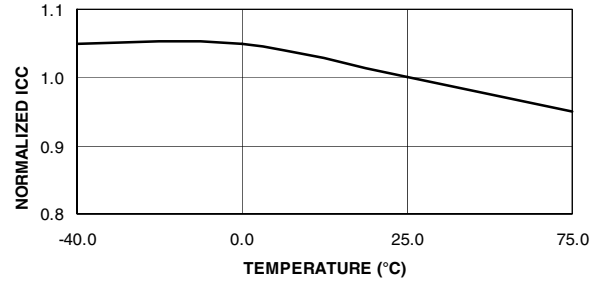
11. Functional Logic Diagram



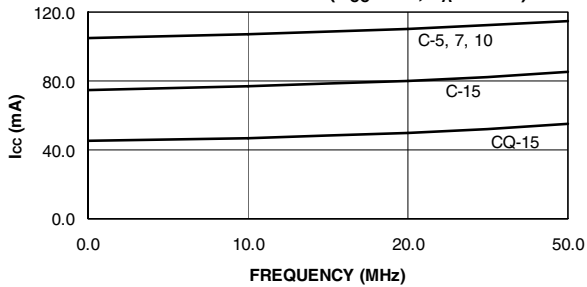
ATF22V10C/CQ SUPPLY CURRENT VS. SUPPLY VOLTAGE ($T_A = 25^\circ\text{C}$)



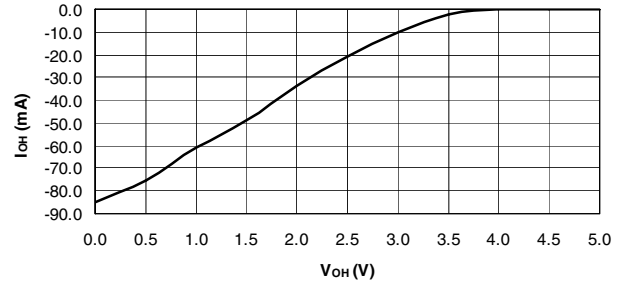
ATF22V10C/CQ NORMALIZED I_{CC} VS. TEMPERATURE



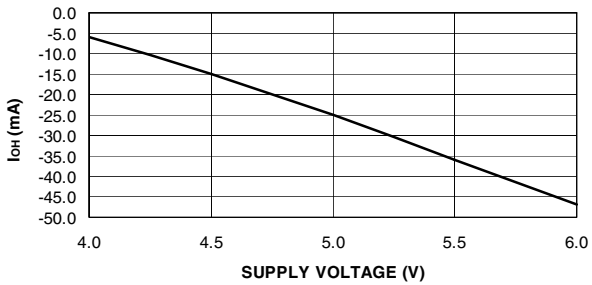
ATF22V10C/CQ SUPPLY CURRENT VS. INPUT FREQUENCY ($V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$)



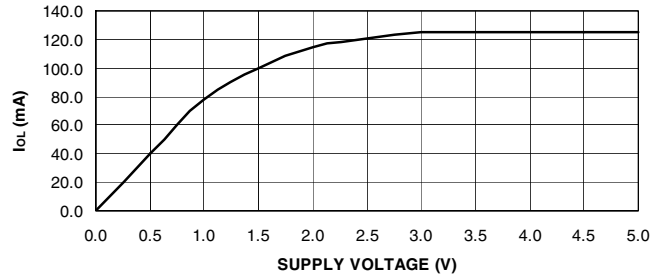
ATF22V10C/CQ OUTPUT SOURCE CURRENT VS. OUTPUT VOLTAGE ($V_{CC} = 5\text{V}$, $T_A = 25^\circ\text{C}$)



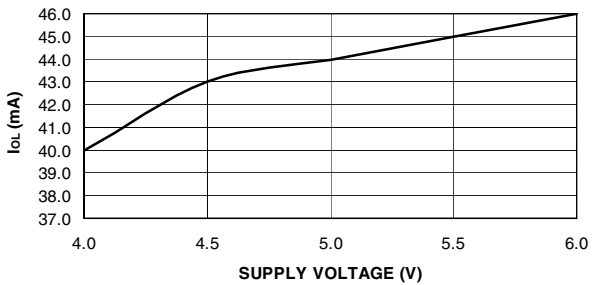
ATF22V10C/CQ OUTPUT SOURCE CURRENT VS. SUPPLY VOLTAGE ($V_{OH} = 2.4\text{V}$)



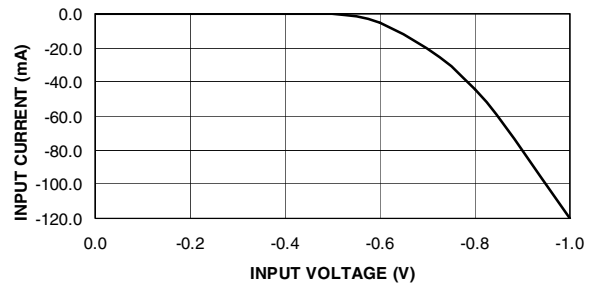
ATF22V10C/CQ OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE ($V_{OL} = 0.5\text{V}$)



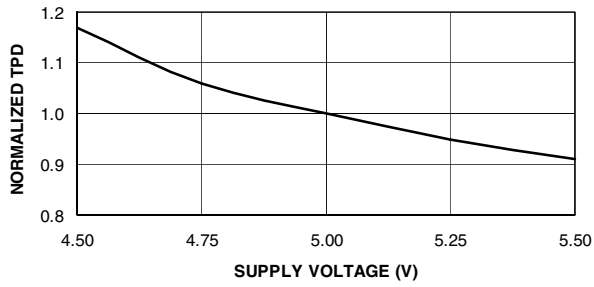
ATF22V10C/CQ OUTPUT SINK CURRENT VS. SUPPLY VOLTAGE ($V_{OL} = 0.5\text{V}$)



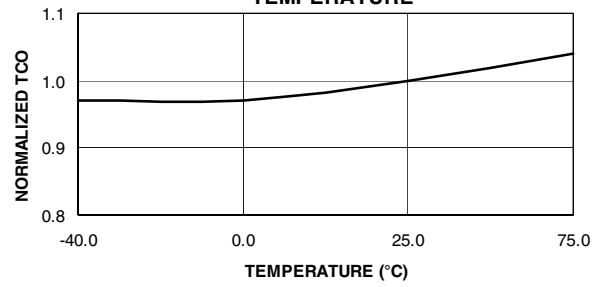
ATF22V10C/CQ INPUT CLAMP CURRENT VS. INPUT VOLTAGE ($V_{CC} = 5\text{V}$, $T_A = 35^\circ\text{C}$)



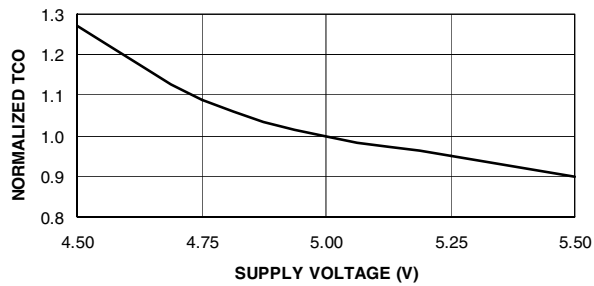
ATF22V10C/CQ NORMALIZED T_{PD} VS. V_{CC}



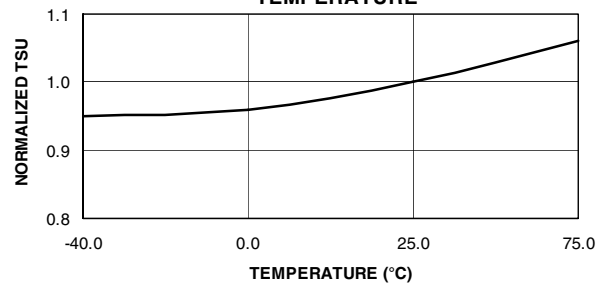
ATF22V10C/CQ NORMALIZED T_{CO} VS. TEMPERATURE



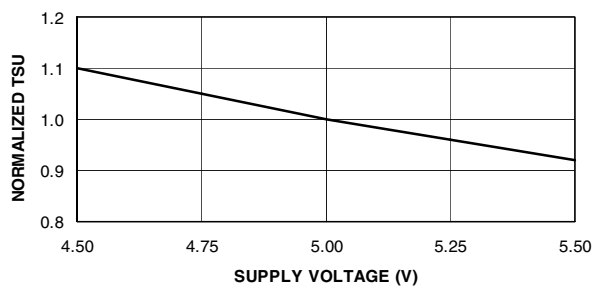
ATF22V10C/CQ NORMALIZED T_{CO} VS. V_{CC}



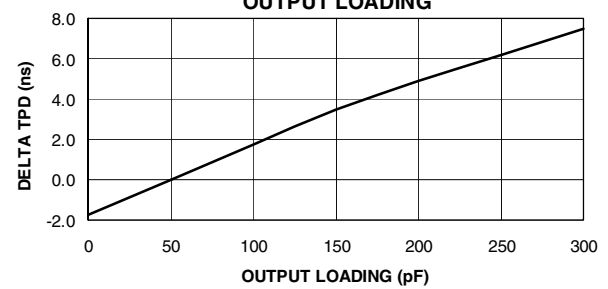
ATF22V10C/CQ NORMALIZED T_{SU} VS. TEMPERATURE



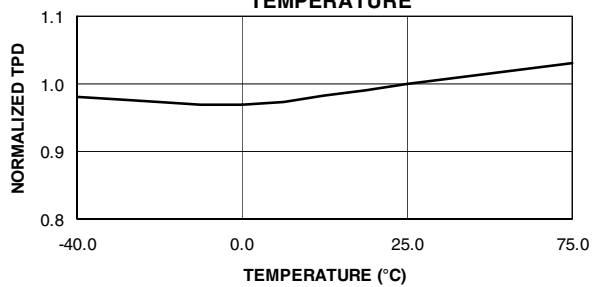
ATF22V10C/CQ NORMALIZED T_{SU} VS. V_{CC}



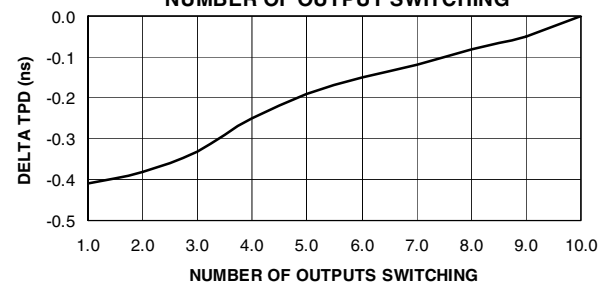
ATF22V10C/CQ DELTA T_{PD} VS. OUTPUT LOADING



ATF22V10C/CQ NORMALIZED T_{PD} VS. TEMPERATURE

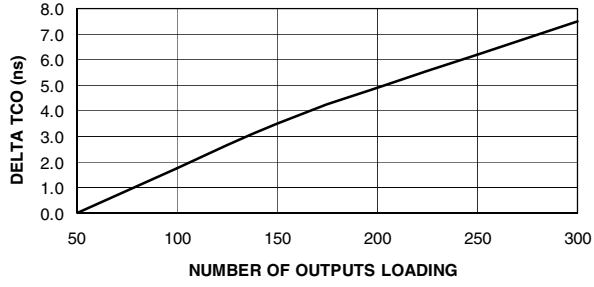


ATF22V10C/CQ DELTA T_{PD} VS. NUMBER OF OUTPUT SWITCHING

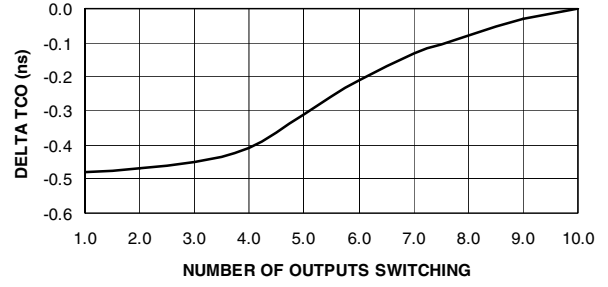




**ATF22V10C/CQ DELTA T_{CO} VS.
OUTPUT LOADING**



**ATF22V10C/CQ DELTA T_{CO} VS.
NUMBER OF SWITCHING**



12. Ordering Information

12.1 ATF22V10C(Q) Green Package Options (Pb/Halide-free/RoHS Compliant)

| t _{PD} (ns) | t _S (ns) | t _{CO} (ns) | Ordering Code | Package | Operation Range |
|----------------------|---------------------|----------------------|--|---------------------------|-------------------------------|
| 5 | 3 | 4 | ATF22V10C-5JX | 28J | Commercial (0°C to 70°C) |
| 7.5 | 3.5 | 4.5 | ATF22V10C-7PX ATF22V10C-7SX | 24P3 24S | Commercial (0°C to 70°C) |
| 7.5 | 3.5 | 4.5 | ATF22V10C-7JU | 28J | Industrial (-40°C to 85°C) |
| 10 | 4.5 | 6.5 | ATF22V10C-10JU ATF22V10C-10PU ATF22V10C-10SU ATF22V10C-10XU | 28J 24P3 24S 24X | Industrial (-40°C to 85°C) |
| 15 | 10 | 8 | ATF22V10C-15JU ATF22V10C-15PU | 28J 24P3 | Industrial (-40°C to 85°C) |
| | | | ATF22V10CQ-15JU | 28J | Industrial (-40°C to 85°C) |

12.2 Using “C” Product for Industrial

To use commercial product for industrial temperature ranges, down-grade one speed grade from the industrial-grade to the commercial-grade device (e.g. 7 ns PX = 10 ns PU) and de-rate power by 30%.

12.3 Military Package Options (Lead-based)

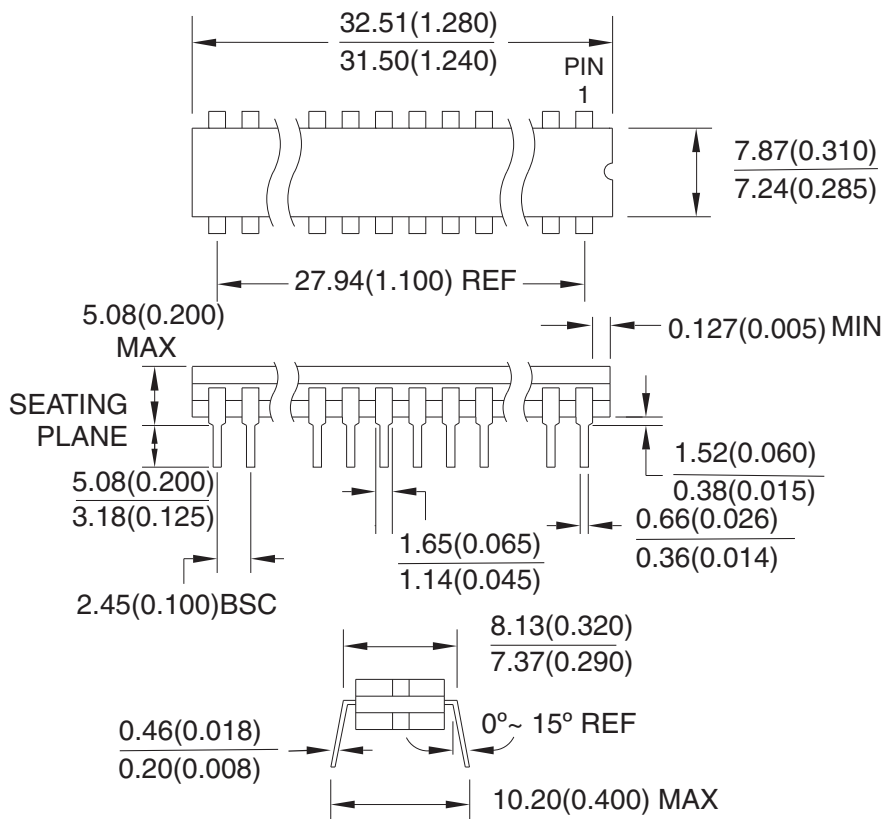
| t _{PD} (ns) | t _S (ns) | t _{CO} (ns) | Ordering Code | Package | Operation Range |
|----------------------|---------------------|----------------------|--------------------|---------|--|
| 10 | 4.5 | 6.5 | ATF22V10C-10GM/883 | 24D3 | Military (-55°C to 125°C) Class B, Fully Compliant |
| | | | ATF22V10C-10NM/883 | 28L | |
| | | | 5962-8984116LA | 24D3 | |
| | | | 5962-89841163A | 28L | |
| 15 | 10 | 8 | ATF22V10C-15GM/883 | 24D3 | Military (-55°C to 125°C) Class B, Fully Compliant |
| | | | ATF22V10C-15NM/883 | 28L | |
| | | | 5962-8984115LA | 24D3 | |
| | | | 5962-89841153A | 28L | |

| Package Type | |
|--------------|---|
| 24D3 | 24-lead, 0.300" Wide, Non-windowed Ceramic Dual Inline Package (CERDIP) |
| 24P3 | 24-pin, 0.300" Wide, Plastic Dual Inline Package (PDIP) |
| 24S | 24-lead, 0.300" Wide, Plastic Gull Wing Small Outline (SOIC) |
| 24X | 24-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP) |
| 28J | 28-lead, Plastic J-leaded Chip Carrier (PLCC) |
| 28L | 28-lead, Ceramic Leadless Chip Carrier (LCC) |

13. Packaging Information

13.1 24D3 – CERDIP

Dimensions in Millimeters and (Inches).
 Controlling dimension: Inches.
 MIL-STD 1835 D-9 Config A (Glass Sealed)



10/21/03



2325 Orchard Parkway
 San Jose, CA 95131

TITLE

24D3, 24-lead, 0.300" Wide. Non-windowed, Ceramic
 Dual Inline Package (Cerdip)

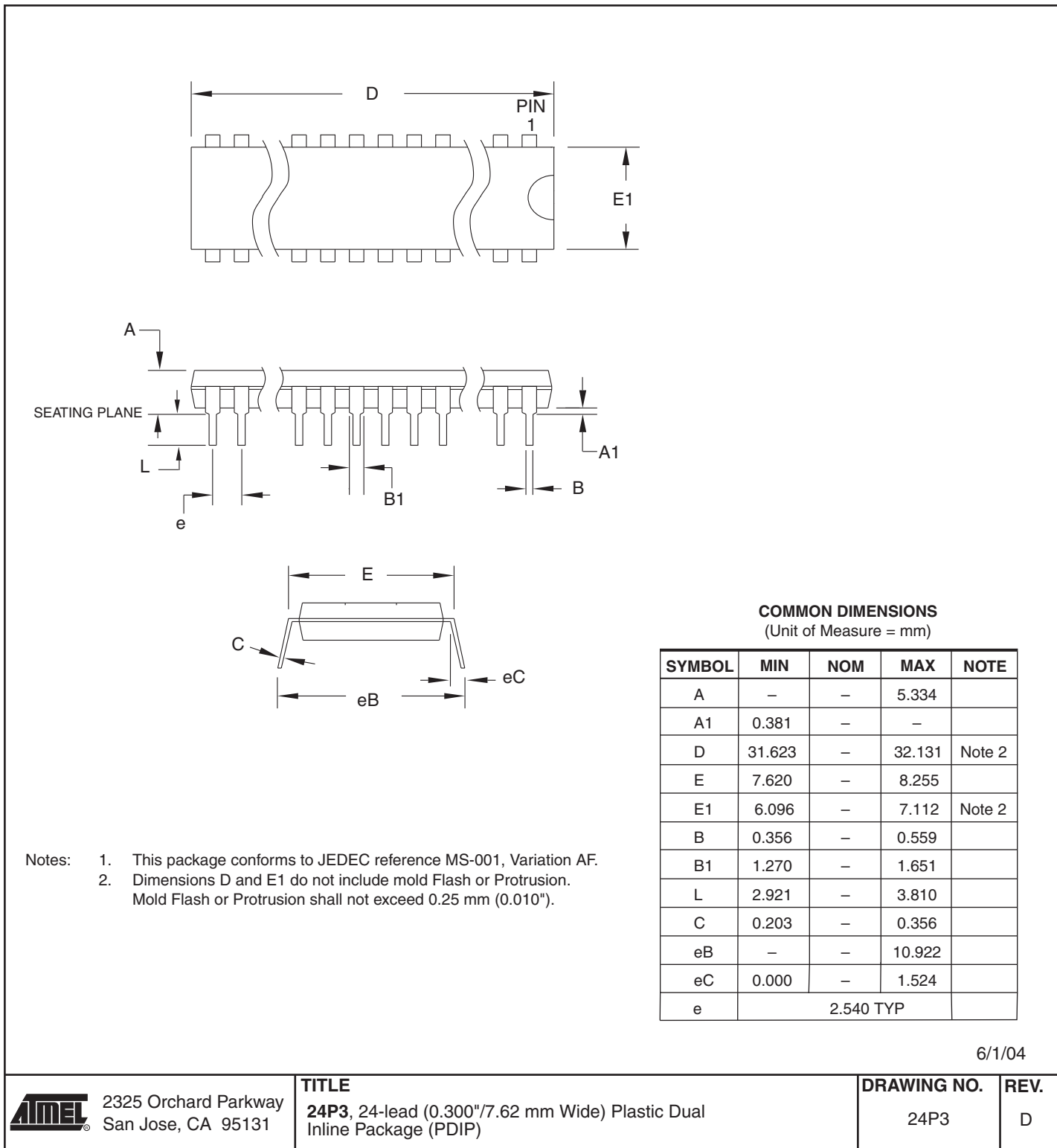
DRAWING NO.

24D3

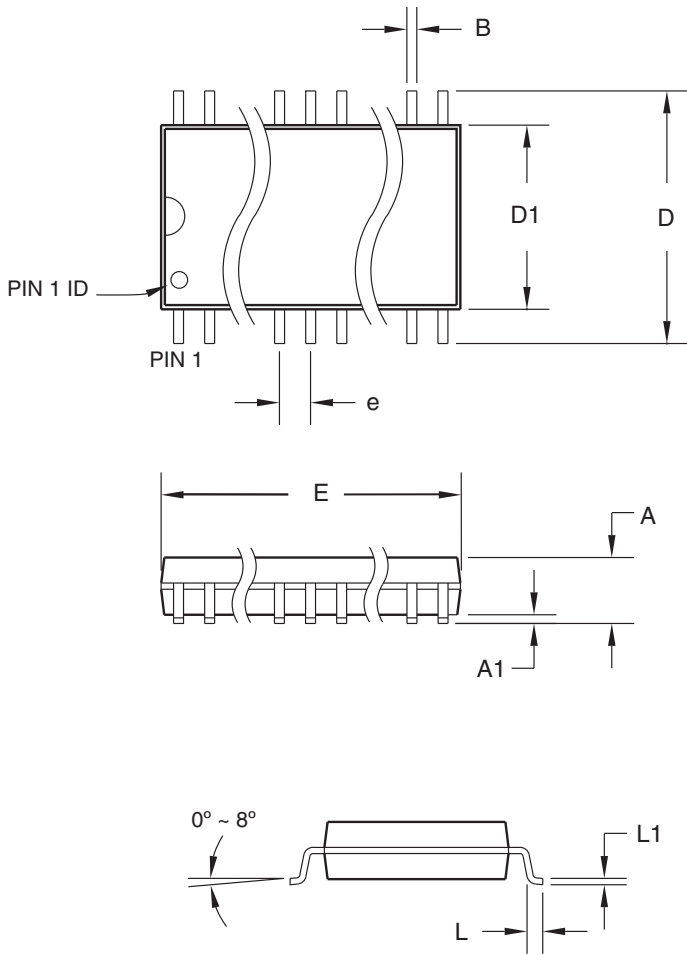
REV.

B

13.2 24P3 – PDIP



13.3 24S – SOIC



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|----------|-----|-------|------|
| A | – | – | 2.65 | |
| A1 | 0.10 | – | 0.30 | |
| D | 10.00 | – | 10.65 | |
| D1 | 7.40 | – | 7.60 | |
| E | 15.20 | – | 15.60 | |
| B | 0.33 | – | 0.51 | |
| L | 0.40 | – | 1.27 | |
| L1 | 0.23 | – | 0.32 | |
| e | 1.27 BSC | | | |

06/17/2002



2325 Orchard Parkway
San Jose, CA 95131

TITLE

24S, 24-lead (0.300" body) Plastic Gull Wing Small Outline (SOIC)

DRAWING NO.

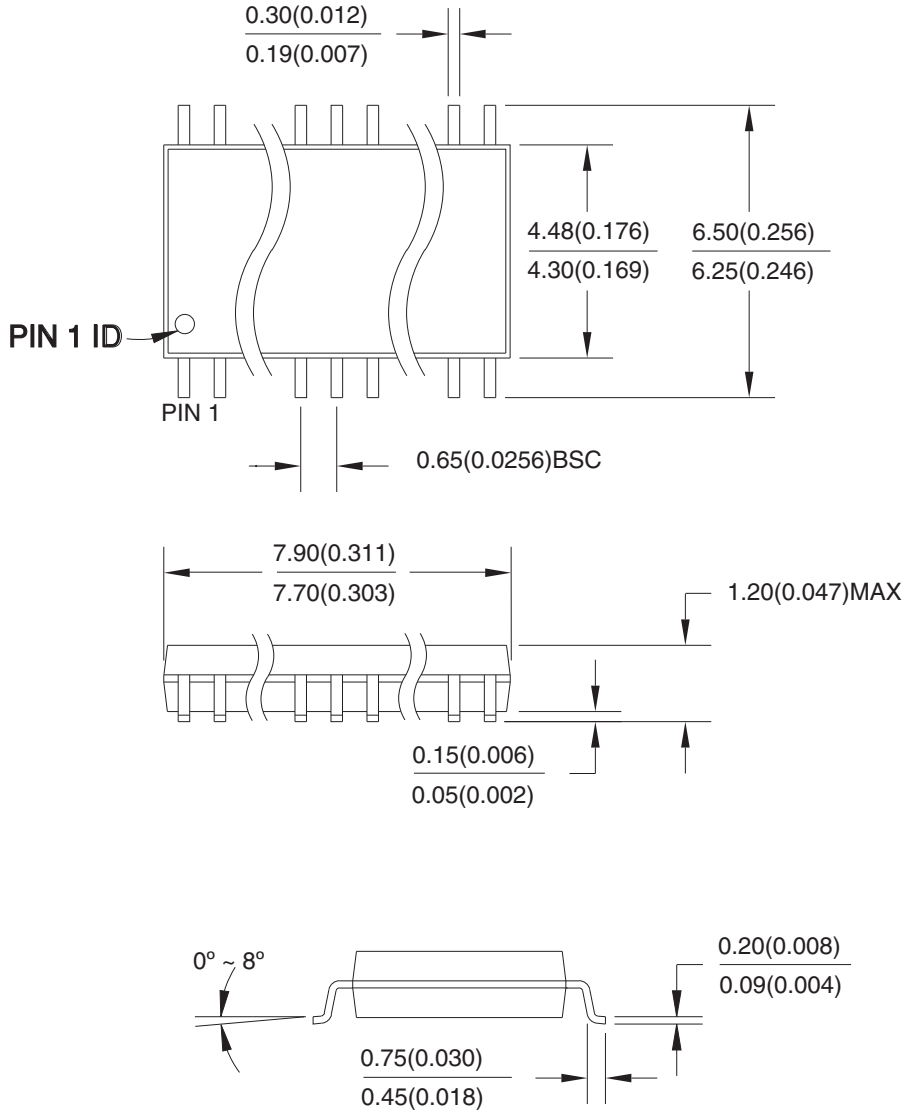
24S

REV.

B

13.4 24X – TSSOP

Dimensions in Millimeter and (Inches)*
 JEDEC STANDARD MO-153 AD
 Controlling dimension: millimeters



04/11/2001



2325 Orchard Parkway
 San Jose, CA 95131

TITLE

24X, 24-lead (4.4 mm body width) Plastic Thin Shrink Small Outline Package (TSSOP)

DRAWING NO.

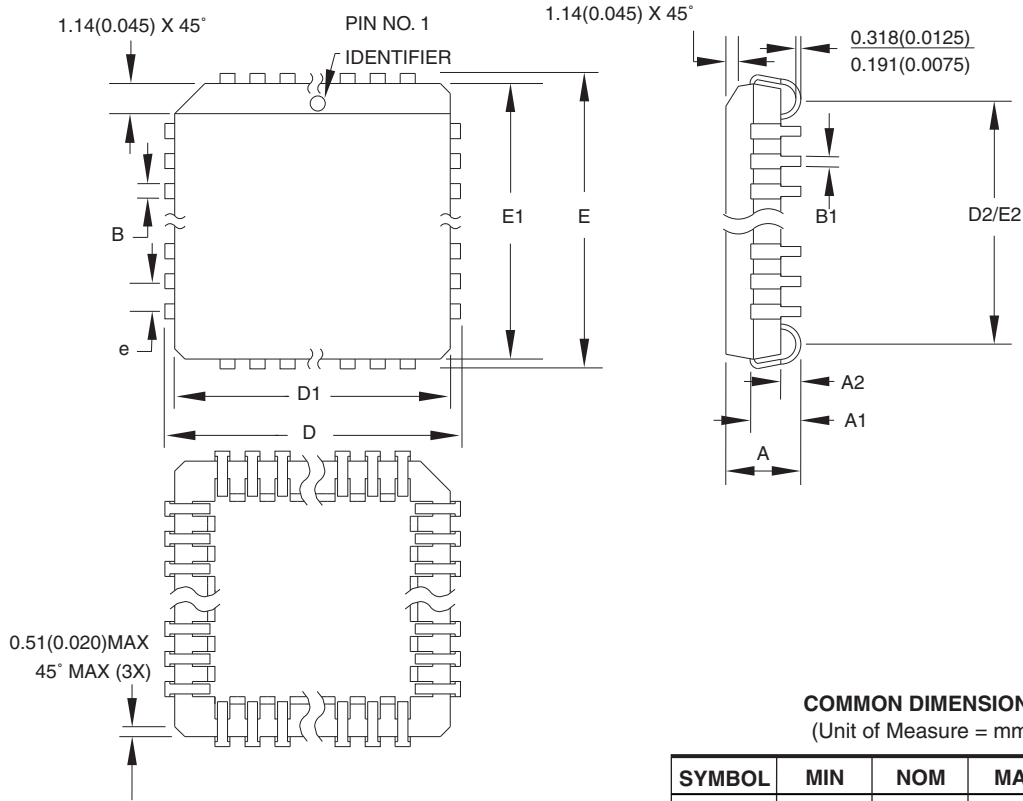
24X

REV.

A



13.5 28J – PLCC



COMMON DIMENSIONS
(Unit of Measure = mm)

| SYMBOL | MIN | NOM | MAX | NOTE |
|--------|-----------|-----|--------|--------|
| A | 4.191 | – | 4.572 | |
| A1 | 2.286 | – | 3.048 | |
| A2 | 0.508 | – | – | |
| D | 12.319 | – | 12.573 | |
| D1 | 11.430 | – | 11.582 | Note 2 |
| E | 12.319 | – | 12.573 | |
| E1 | 11.430 | – | 11.582 | Note 2 |
| D2/E2 | 9.906 | – | 10.922 | |
| B | 0.660 | – | 0.813 | |
| B1 | 0.330 | – | 0.533 | |
| e | 1.270 TYP | | | |

- Notes:
1. This package conforms to JEDEC reference MS-018, Variation AB.
 2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is .010" (0.254 mm) per side. Dimension D1 and E1 include mold mismatch and are measured at the extreme material condition at the upper or lower parting line.
 3. Lead coplanarity is 0.004" (0.102 mm) maximum.

10/04/01



2325 Orchard Parkway
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TITLE

28J, 28-lead, Plastic J-leaded Chip Carrier (PLCC)

DRAWING NO.

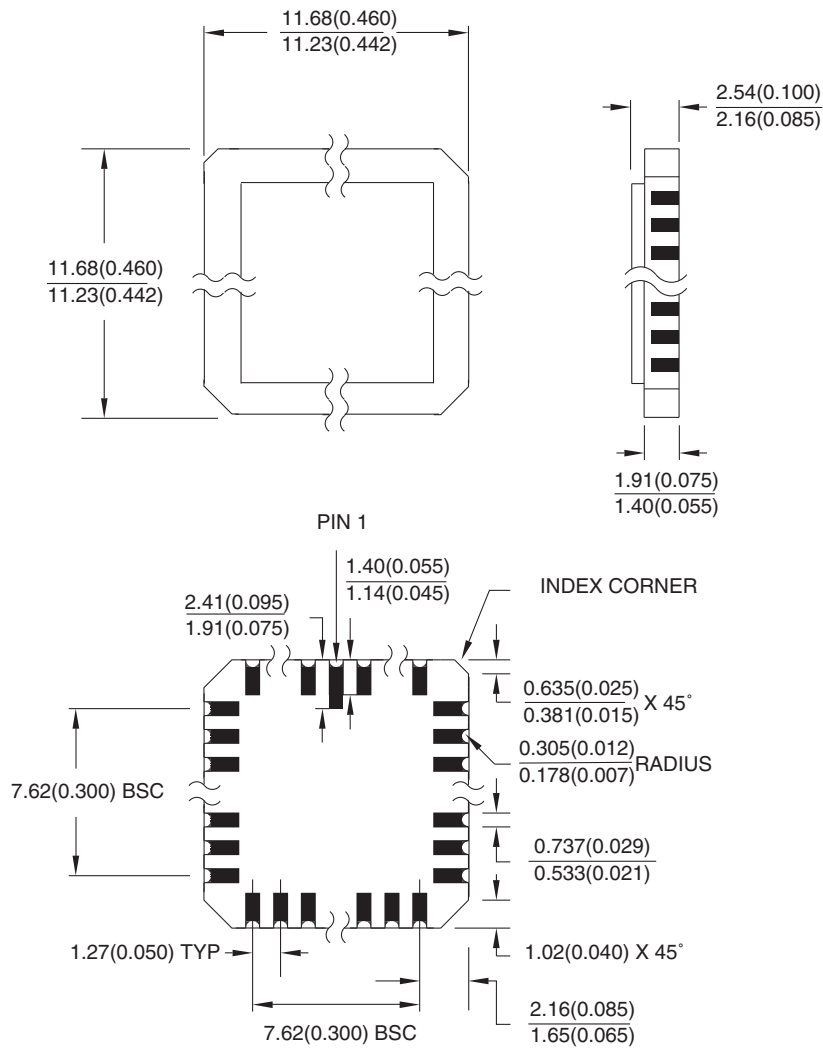
28J

REV.

B

13.6 28L – LCC

Dimensions in Millimeters and (Inches).
 Controlling dimension: Inches.
 MIL-STD 1835 C-4



10/21/03



2325 Orchard Parkway
 San Jose, CA 95131

TITLE

28L, 28-pad, Non-windowed, Ceramic Lid, Leadless Chip Carrier (LCC)

DRAWING NO.

28L

REV.

B





14. Revision History

| Revision Level – Revision Date | History |
|--------------------------------|---|
| R – June 2006 | Updated Green package options. |
| S – August 2008 | Added new green part. |
| T – May 2009 | Added military-grade packages and removed leaded parts. |





Headquarters

Atmel Corporation
2325 Orchard Parkway
San Jose, CA 95131
USA
Tel: 1(408) 441-0311
Fax: 1(408) 487-2600

International

Atmel Asia
Unit 1-5 & 16, 19/F
BEA Tower, Millennium City 5
418 Kwun Tong Road
Kwun Tong, Kowloon
Hong Kong
Tel: (852) 2245-6100
Fax: (852) 2722-1369

Atmel Europe
Le Krebs
8, Rue Jean-Pierre Timbaud
BP 309
78054 Saint-Quentin-en-
Yvelines Cedex
France
Tel: (33) 1-30-60-70-00
Fax: (33) 1-30-60-71-11

Atmel Japan
9F, Tonetsu Shinkawa Bldg.
1-24-8 Shinkawa
Chuo-ku, Tokyo 104-0033
Japan
Tel: (81) 3-3523-3551
Fax: (81) 3-3523-7581

Product Contact

Web Site
www.atmel.com

Technical Support
PLD@atmel.com

Sales Contact
www.atmel.com/contacts

Literature Requests
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