Document order number: MM908E626
Rev. 5.0, 7/2009

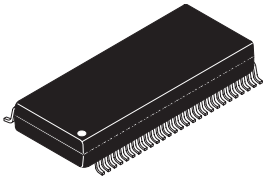
Integrated Stepper Motor Driver with Embedded MCU and LIN Serial Communication

908E626

STEPPER MOTOR DRIVER WITH EMBEDDED MCU AND LIN

The 908E626 is an integrated single-package solution that includes a high performance HC08 microcontroller with a *SMARTMOS*™ analog control IC. The HC08 includes flash memory, a timer, enhanced serial communications interface (ESCI), an analog-to-digital converter (ADC), serial peripheral interface (SPI) (only internal), and an internal clock generator (ICG) module. The analog control die provides fully protected H-bridge outputs, voltage regulator, autonomous watchdog, and local interconnect network (LIN) physical layer.

The single-package solution, together with LIN, provides optimal application performance adjustments and space-saving PCB design. It is well suited for the control of automotive stepper applications like climate control and light-levelling.



DWB SUFFIX
EK SUFFIX (PB-FREE)
98ARL10519D
54-PIN SOICWB-EP

Features

- High performance M68HC08EY16 core
- 16 K bytes of on-chip flash memory
- 512 bytes of RAM
- Internal clock generation module
- Two 16-bit, 2-channel timers
- 10-Bit Analog-to-Digital converter
- Four low $R_{DS(ON)}$ half-bridge outputs
- 13 microcontroller I/Os
- Pb-free packaging designated by suffix code EK

ORDERING INFORMATION		
Device	**Temperature Range (T_A)**	**Package**
MM908E626AVEK	-40°C to 115°C	54 SOICW EP
MM908E626AVDWB		

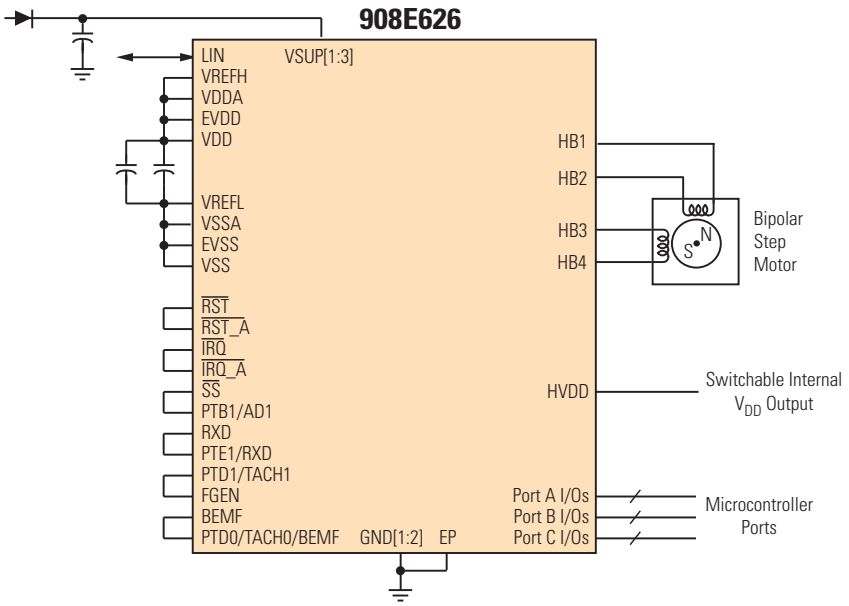


Figure 1. 908E626 Simplified Application Diagram

* This document contains certain information on a new product.
Specifications and information herein are subject to change without notice.

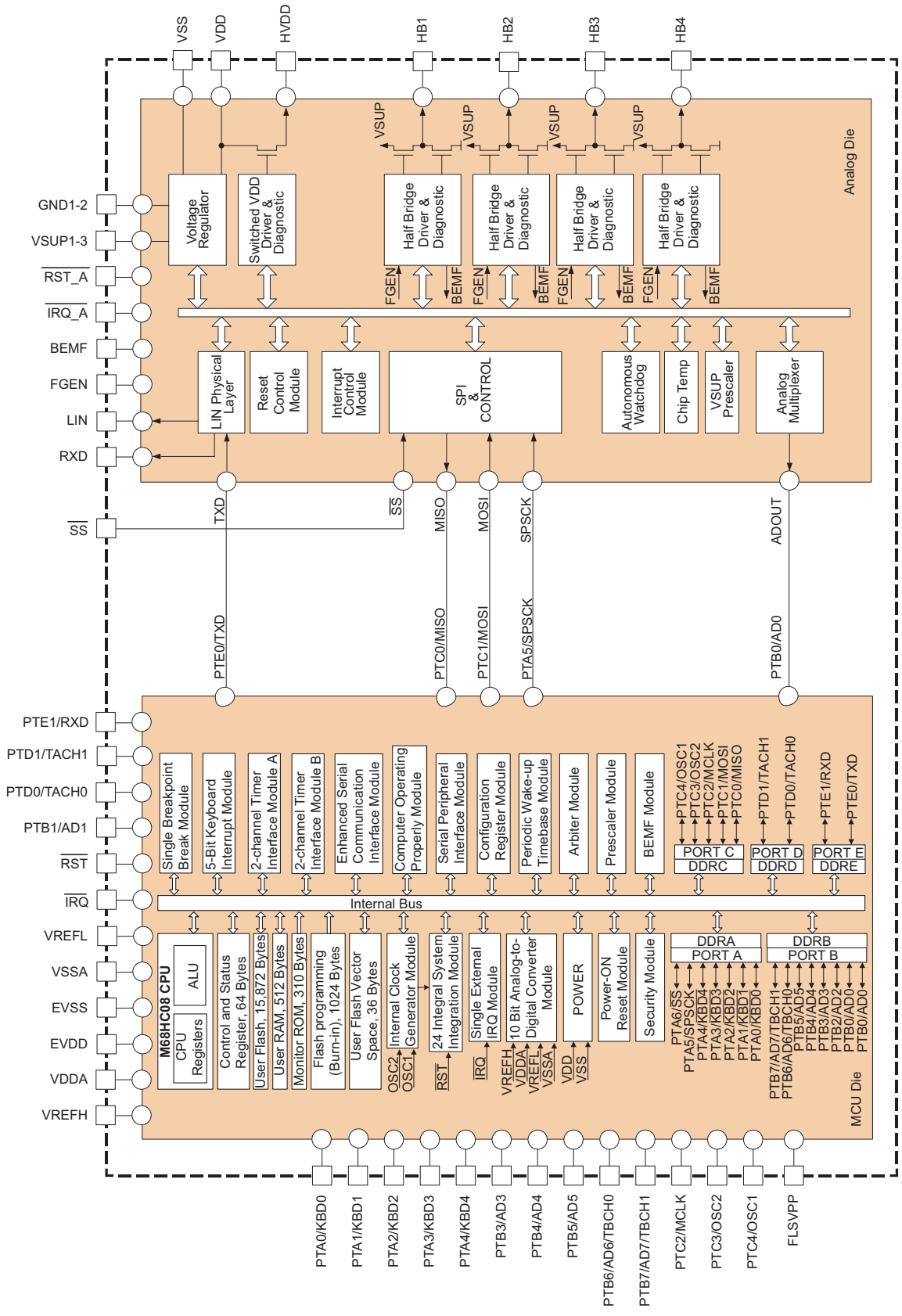


Figure 2. Figure 1. 908E626 Simplified Internal Block Diagram

PIN CONNECTIONS

Transparent Top View of Package

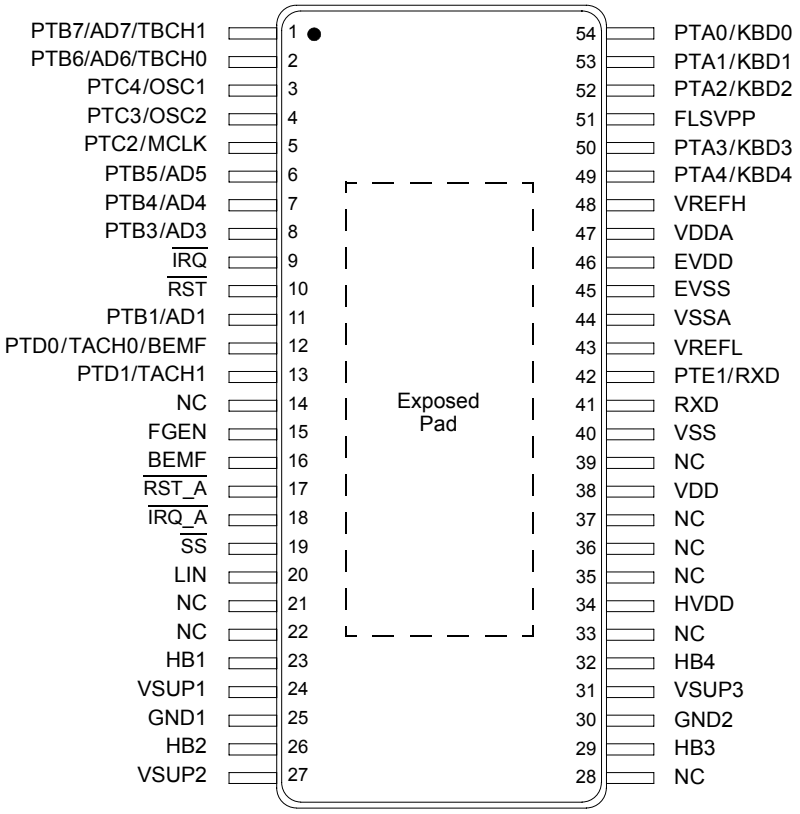


Figure 3. 908E626 Pin Connections

Table 1. 908E626 PIN DEFINITIONS

A functional description of each pin can be found in the Functional Pin Description section beginning on page 14.

Die	Pin	Pin Name	Formal Name	Definition
MCU	1 2 6 7 8 11	PTB7/AD7/TBCH1 PTB6/AD6/TBCH0 PTB5/AD5 PTB4/AD4 PTB3/AD3 PTB1/AD1	Port B I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	3 4 5	PTC4/OSC1 PTC3/OSC2 PTC2/MCLK	Port C I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	9	IRQ	External Interrupt Input	This pin is an asynchronous external interrupt input pin.
MCU	10	RST	External Reset	This pin is bidirectional, allowing a reset of the entire system. It is driven low when any internal reset source is asserted.
MCU	12 13	PTD0/TACH0/BEMF PTD1/TACH1	Port D I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.

Table 1. 908E626 PIN DEFINITIONS

A functional description of each pin can be found in the Functional Pin Description section beginning on page 14.

Die	Pin	Pin Name	Formal Name	Definition
–	14, 21, 22, 28, 33, 35, 36, 37, 39	NC	No Connect	Not connected.
MCU	42	PTE1/RXD	Port E I/O	This pin is a special function, bidirectional I/O port pin that can is shared with other functional modules in the MCU.
MCU	43 48	VREFL VREFH	ADC References	These pins are the reference voltage pins for the analog-to-digital converter (ADC).
MCU	44 47	VSSA VDDA	ADC Supply Pins	These pins are the power supply pins for the analog-to-digital converter.
MCU	45 46	EVSS EVDD	MCU Power Supply Pins	These pins are the ground and power supply pins, respectively. The MCU operates from a single power supply.
MCU	49 50 52 53 54	PTA4/KBD4 PTA3/KBD3 PTA2/KBD2 PTA1/KBD1 PTA0/KBD0	Port A I/Os	These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU.
MCU	51	FLSVPP	Test Pin	For test purposes only. Do not connect in the application.
Analog	15	FGEN	Current Limitation Frequency Input	This is the input pin for the half-bridge current limitation PWM frequency.
Analog	16	BEMF	Back Electromagnetic Force Output	This pin gives the user information about back electromagnetic force (BEMF).
Analog	17	$\overline{\text{RST\_A}}$	Internal Reset	This pin is the bidirectional reset pin of the analog die.
Analog	18	$\overline{\text{IRQ\_A}}$	Internal Interrupt Output	This pin is the interrupt output pin of the analog die indicating errors or wake-up events.
Analog	19	$\overline{\text{SS}}$	Slave Select	This pin is the SPI slave select pin for the analog chip.
Analog	20	LIN	LIN Bus	This pin represents the single-wire bus transmitter and receiver.
Analog	23 26 29 32	HB1 HB2 HB3 HB4	Half-bridge Outputs	This device includes power MOSFETs configured as four half-bridge driver outputs. These outputs may be configured for step motor drivers, DC motor drivers, or as high side and low side switches.
Analog	24 27 31	VSUP1 VSUP2 VSUP3	Power Supply Pins	These pins are device power supply pins.
Analog	25 30	GND1 GND2	Power Ground Pins	These pins are device power ground connections.
Analog	34	HVDD	Switchable V_{DD} Output	This pin is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0V supply; e.g., 3 pin Hall-effect sensors.
Analog	38	VDD	Voltage Regulator Output	The +5.0V voltage regulator output pin is intended to supply the embedded microcontroller.
Analog	40	VSS	Voltage Regulator Ground	Ground pin for the connection of all non-power ground connections (microcontroller and sensors).
Analog	41	RXD	LIN Transceiver Output	This pin is the output of LIN transceiver.
–	EP	Exposed Pad	Exposed Pad	The exposed pad pin on the bottom side of the package conducts heat from the chip to the PCB board.

ELECTRICAL CHARACTERISTICS

MAXIMUM RATINGS

Table 2. MAXIMUM RATINGS

All voltages are with respect to ground unless otherwise noted. Exceeding limits on any pin may cause permanent damage to the device.

Rating	Symbol	Value	Unit
Supply Voltage Analog Chip Supply Voltage under Normal Operation (Steady-state) Analog Chip Supply Voltage under Transient Conditions (1) Microcontroller Chip Supply Voltage	 $V_{SUP(SS)}$ $V_{SUP(PK)}$ V_{DD}	 -0.3 to 28 -0.3 to 40 -0.3 to 6.0	V
Input Pin Voltage Analog Chip Microcontroller Chip	 $V_{IN(ANALOG)}$ $V_{IN(MCU)}$	 -0.3 to 5.5 V_{SS}-0.3 to V_{DD}+0.3	V
Maximum Microcontroller Current per Pin All Pins Except VDD, VSS, PTA0:PTA6, PTC0:PTC1 Pins PTA0:PTA6, PTC0:PTC1	 $I_{PIN(1)}$ $I_{PIN(2)}$	 ±15 ±25	mA
Maximum Microcontroller V_{SS} Output Current	I_{MVSS}	100	mA
Maximum Microcontroller V_{DD} Input Current	I_{MVDD}	100	mA
LIN Supply Voltage Normal Operation (Steady-state) Transient Conditions (1)	 $V_{BUS(SS)}$ $V_{BUS(DYNAMIC)}$	 -18 to 28 40	V
ESD Voltage Human Body Model (2) Machine Model (3) Charge Device Model (4)	 V_{ESD1} V_{ESD2} V_{ESD3}	 ±3000 ±150 ±500	V
THERMAL RATINGS			
Storage Temperature	T_{STG}	-40 to 150	°C
Operating Case Temperature (5)	T_C	-40 to 115	°C
Operating Junction Temperature(6)	T_J	-40 to 135	°C
Peak Package Reflow Temperature During Solder Mounting (7)	T_{SOLDER}	245	°C

Notes

1. Transient capability for pulses with a time of t < 0.5 sec.
2. ESD1 testing is performed in accordance with the Human Body Model (C_{ZAP} = 100pF, R_{ZAP} = 1500Ω).
3. ESD2 testing is performed in accordance with the Machine Model (C_{ZAP} = 200pF, R_{ZAP} = 0Ω).
4. ESD3 testing is performed in accordance with Charge Device Model, robotic (C_{ZAP} = 4.0pF).
5. The limiting factor is junction temperature, taking into account the power dissipation, thermal resistance, and heat sinking.
6. The temperature of analog and MCU die is strongly linked via the package, but can differ in dynamic load conditions, usually because of higher power dissipation on the analog die. The analog die temperature must not exceed 150°C under these conditions
7. Pin soldering temperature is for 10 seconds maximum duration. Not designed for immersion soldering. Exceeding these limits may cause malfunction or permanent damage to the device.

STATIC ELECTRICAL CHARACTERISTICS

Table 3. STATIC ELECTRICAL CHARACTERISTICS

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0V ≤ V_{SUP} ≤ 16V, -40°C ≤ T_J ≤ 135°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SUPPLY VOLTAGE					
Nominal Operating Voltage	V_{SUP}	8.0	–	18	V
SUPPLY CURRENT					
NORMAL Mode V_{SUP} = 12V, Power Die ON (PSON=1), MCU Operating Using Internal Oscillator at 32MHz (8.0 MHz Bus Frequency), SPI, ESCI, ADC Enabled	I_{RUN}	–	20	–	mA
STOP Mode [8] V_{SUP} = 12V, Cyclic Wake-up Disabled	I_{STOP}	–	–	75	µA
DIGITAL INTERFACE RATINGS (ANALOG DIE)					
Output Pins $\overline{RST\_A}$, $\overline{IRQ\_A}$					V
Low State Output Voltage (I_{OUT} = -1.5mA)	V_{OL}	–	–	0.4	
High State Output Voltage (I_{OUT} = 1.0µA)	V_{OH}	3.85	–	–	
Output Pins BEMF, RXD					V
Low State Output Voltage (I_{OUT} = -1.5mA)	V_{OL}	–	–	0.4	
High State Output Voltage (I_{OUT} = 1.5mA)	V_{OH}	3.85	–	–	
Output Pin RXD–Capacitance [9]	C_{IN}	–	4.0	–	pF
Input Pins $\overline{RST\_A}$, FGEN, $\overline{SS}$					V
Input Logic Low Voltage	V_{IL}	–	–	1.5	
Input Logic High Voltage	V_{IH}	3.5	–	–	
Input Pins $\overline{RST\_A}$, FGEN, $\overline{SS}$–Capacitance [9]	C_{IN}	–	4.0	–	pF
Pins $\overline{RST\_A}$, $\overline{IRQ\_A}$–Pull-up Resistor	$R_{PULLUP1}$	–	10	–	kΩ
Pin $\overline{SS}$–Pull-up Resistor	$R_{PULLUP2}$	–	60	–	kΩ
Pins FGEN, MOSI, SPSCK–Pull-down Resistor	$R_{PULLDOWN}$	–	60	–	kΩ
Pin TXD–Pull-up Current Source	I_{PULLUP}	–	35	–	µA

Notes

8. STOP mode current will increase if V_{SUP} exceeds 15V.
9. This parameter is guaranteed by process monitoring but is not production tested.

Table 3. STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0V ≤ V_{SUP} ≤ 16V, -40°C ≤ T_J ≤ 135°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SYSTEM RESETS AND INTERRUPTS					
High Voltage Reset					V
Threshold	V_{HVRON}	27	30	33	
Hysteresis	V_{HVRH}	–	1.5	–	
Low Voltage Reset					
Threshold	V_{LVRON}	3.6	4.0	4.7	V
Hysteresis	V_{LVRH}	–	100	–	mV
High Voltage Interrupt					V
Threshold	V_{HVION}	17.5	21	23	
Hysteresis	V_{HVIH}	–	1.0	–	
Low Voltage Interrupt					V
Threshold	V_{LVION}	6.5	–	8.0	
Hysteresis	V_{LVIH}	–	0.4	–	
High Temperature Reset (11)					°C
Threshold	T_{RON}	–	170	–	
Hysteresis	T_{RH}	5.0	–	–	
High Temperature Interrupt (12)					°C
Threshold	T_{ION}	–	160	–	
Hysteresis	T_{IH}	5.0	–	–	
VOLTAGE REGULATOR					
Normal Mode Output Voltage I_{OUT} = 60mA, 6.0V < V_{SUP} < 18V	V_{DDRUN}	4.75	5.0	5.25	V
Load Regulation I_{OUT} = 80mA, V_{SUP} = 9.0V	V_{LR}	–	–	100	mV
STOP Mode Output Voltage (Maximum Output Current 100µA)(10)	V_{DDSTOP}	4.45	4.7	5.0	V

Notes
10. Tested to be VLVRON < VDDSTOP
11. This parameter is guaranteed by process monitoring but is not production tested.
12. High Temperature Interrupt (HTI) threshold is linked to High Temperature Reset (HTR) threshold (HTR = HTI + 10°C).

Table 3. STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0V ≤ V_{SUP} ≤ 16V, -40°C ≤ T_J ≤ 135°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
Output Low Level TXD LOW, 500Ω Pull-up to V_{SUP}	$V_{LIN-LOW}$	–	–	1.4	V
Output High Level TXD HIGH, I_{OUT} = 1.0µA	$V_{LIN-HIGH}$	V_{SUP}-1.0	–	–	V
Pullup Resistor to V_{SUP}	R_{SLAVE}	20	30	60	kΩ
Leakage Current to GND Recessive State (-0.5V < V_{LIN} < V_{SUP})	$I_{BUS\_PAS\_REC}$	0.0	–	20	µA
Leakage Current to GND (V_{SUP} Disconnected) Including Internal Pullup Resistor, V_{LIN} @ -18V Including Internal Pullup Resistor, V_{LIN} @ +18V	 $I_{BUS\_NO\_GND}$ I_{BUS}	 – –	 -600 25	 – –	µA
LIN Receiver Recessive Dominant Threshold Input Hysteresis	 V_{IH} V_{IL} V_{ITH} V_{IHY}	 0.6V_{LIN} 0 – 0.01V_{SUP}	 – – V_{SUP}/2 –	 V_{SUP} 0.4V_{LIN} – 0.1V_{SUP}	V
LIN Wake-up Threshold	V_{WTH}	–	V_{SUP}/2	–	V
HALF-bridge OUTPUTS (HB1:HB4)					
Switch ON Resistance @ T_J = 25°C with I_{LOAD} = 1.0A High Side Low Side	 $R_{DS(ON)HB\_HS}$ $R_{DS(ON)HB\_LS}$	 – –	 425 400	 500 500	mΩ
High Side Over-current Shutdown	I_{HBHSOC}	3.0	–	7.5	A
Low Side Over-current Shutdown	I_{HBLSOC}	2.5	–	7.5	A
Low Side Current Limitation @ T_J = 25°C Current Limit 1 (CLS2 = 0, CLS1 = 1, CLS0 = 1) Current Limit 2 (CLS2 = 1, CLS1 = 0, CLS0 = 0) Current Limit 3 (CLS2 = 1, CLS1 = 0, CLS0 = 1) Current Limit 4 (CLS2 = 1, CLS1 = 1, CLS0 = 0) Current Limit 5 (CLS2 = 1, CLS1 = 1, CLS0 = 1)	 I_{CL1} I_{CL2} I_{CL3} I_{CL4} I_{CL5}	 – 210 300 450 600	 55 260 370 550 740	 – 315 440 650 880	mA
Half-bridge Output HIGH Threshold for BEMF Detection	V_{BEMFH}	–	-30	0.0	V
Half-bridge Output LOW Threshold for BEMF Detection	V_{BEMFL}	–	-60	-5.0	mV
Hysteresis for BEMF Detection	V_{BEMFHY}	–	30	–	mV
Low Side Current-to-Voltage Ratio (V_{ADOUT} [V]/I_{HB} [A]) CSA = 1 CSA = 0	 $RATIO_H$ $RATIO_L$	 7.0 1.0	 12.0 2.0	 14.0 3.0	V/A

Table 3. STATIC ELECTRICAL CHARACTERISTICS (continued)

All characteristics are for the analog chip only. Refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0V ≤ V_{SUP} ≤ 16V, -40°C ≤ T_J ≤ 135°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
SWITCHABLE V_{DD} OUTPUT (HVDD)					
Over-current Shutdown Threshold	$I_{HVDDOCT}$	24	30	40	mA
V_{SUP} DOWN-SCALER					
Voltage Ratio ($RATIO_{VSUP}$ = V_{SUP} /V_{ADOUT})	$RATIO_{VSUP}$	4.8	5.1	5.35	–
INTERNAL DIE TEMPERATURE SENSOR					
Voltage/Temperature Slope	S_{TTOV}	–	19	–	mV/°C
Output Voltage @ 25°C	V_{T25}	1.7	2.1	2.5	V

DYNAMIC ELECTRICAL CHARACTERISTICS

Table 4. DYNAMIC ELECTRICAL CHARACTERISTICS

All characteristics are for the analog chip only. Please refer to the 68HC908EY16 datasheet for characteristics of the microcontroller chip. Characteristics noted under conditions 9.0V ≤ V_{SUP} ≤ 16V, -40°C ≤ T_J ≤ 135°C, unless otherwise noted. Typical values noted reflect the approximate parameter mean at T_A = 25°C under nominal conditions, unless otherwise noted.

Characteristic	Symbol	Min	Typ	Max	Unit
LIN PHYSICAL LAYER					
Propagation Delay (13), (14)					µs
TXD LOW to LIN LOW	$t_{TXD-LIN-LOW}$	–	–	6.0	
TXD HIGH to LIN HIGH	$t_{TXD-LIN-HIGH}$	–	–	6.0	
LIN LOW to RXD LOW	$t_{LIN-RXD-LOW}$	–	4.0	8.0	
LIN HIGH to RXD HIGH	$t_{LIN-RXD-HIGH}$	–	4.0	8.0	
TXD Symmetry	$t_{TXD-SYM}$	-2.0	–	2.0	
RXD Symmetry	$t_{RXD-SYM}$	-2.0	–	2.0	
Output Falling Edge Slew Rate (13), (15) 80% to 20%	SR_F	-1.0	-2.0	-3.0	V/µs
Output Rising Edge Slew Rate (13), (15) 20% to 80%, R_{BUS} > 1.0kΩ, C_{BUS} < 10nF	SR_R	1.0	2.0	3.0	V/µs
LIN Rise/Fall Slew Rate Symmetry (13), (15)	SR_S	-2.0	–	2.0	µs
AUTONOMOUS WATCHDOG (AWD)					
AWD Oscillator Period	t_{OSC}	–	40	–	µs
AWD Period Low = 512 t_{OSC}	t_{AWDPH}	16	22	28	ms
AWD Period High = 256 t_{OSC}	t_{AWDPL}	8.0	11	14	ms
AWD Cyclic Wake-up On Time	$t_{AWDHPON}$	–	90	–	µs

Notes
13. All LIN characteristics are for initial LIN slew rate selection (20 kbaud) (SRS0:SRS1= 00).
14. See Figure 4, page 11.
15. See Figure 5, page 12.

MICROCONTROLLER PARAMETRICS

Table 5. MICROCONTROLLER

For a detailed microcontroller description, refer to the MC68HC908EY16 datasheet.

Module	Description
Core	High Performance HC08 Core with a Maximum Internal Bus Frequency of 8.0MHz
Timer	Two 16-Bit Timers with Two Channels (TIM A and TIM B)
Flash	16K Bytes
RAM	512 Bytes
ADC	10 Bit Analog-to-Digital Converter
SPI	SPI Module

Table 5. MICROCONTROLLER

For a detailed microcontroller description, refer to the MC68HC908EY16 datasheet.

Module	Description
ESCI	Standard Serial Communication Interface (SCI) Module Bit-Time Measurement Arbitration Prescaler with Fine Baud-Rate Adjustment
ICG	Internal Clock Generation Module
BEMF Counter	Special Counter for *SMARTMOS* BEMF Output

TIMING DIAGRAMS

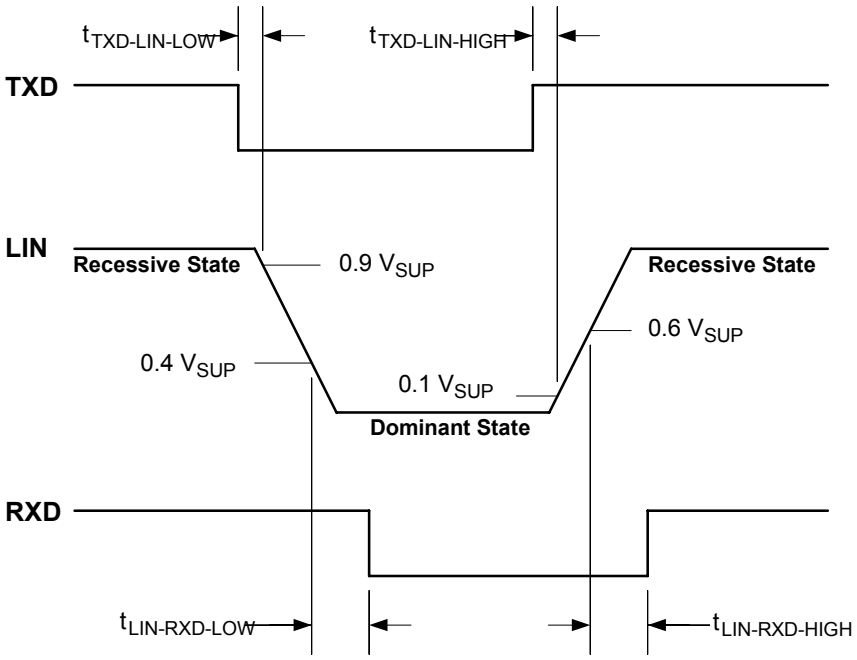


Figure 4. LIN Timing Description

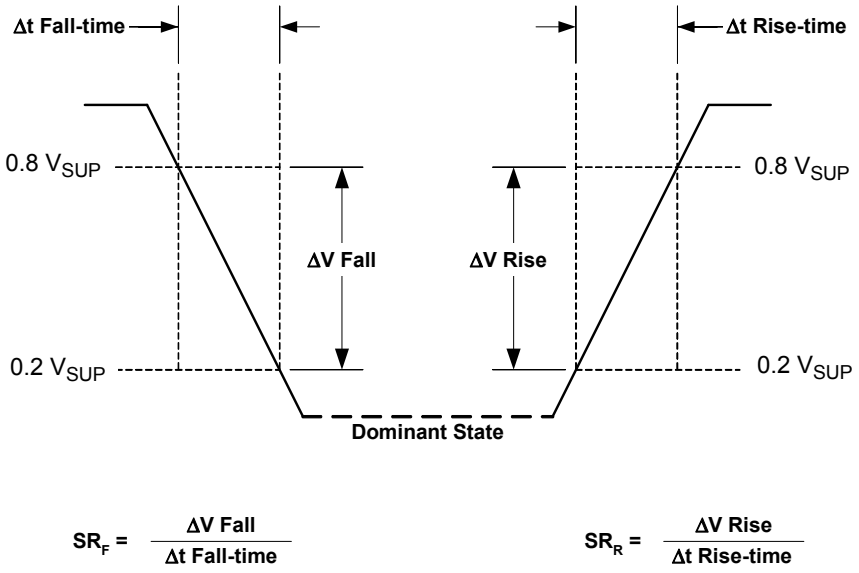


Figure 5. LIN Slew Rate Description

FUNCTIONAL DIAGRAMS

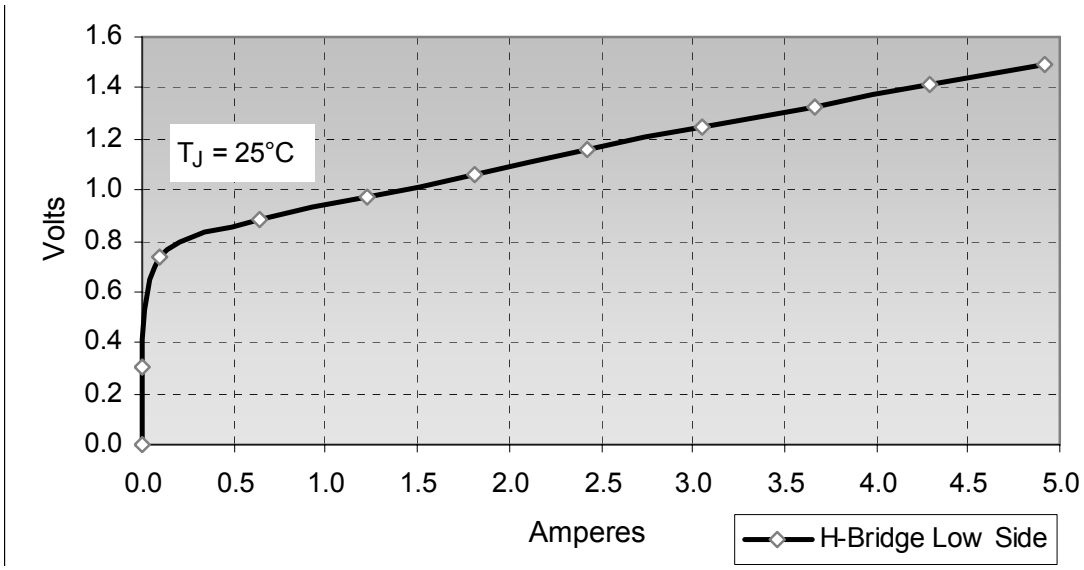


Figure 6. Free Wheel Diode Forward Voltage

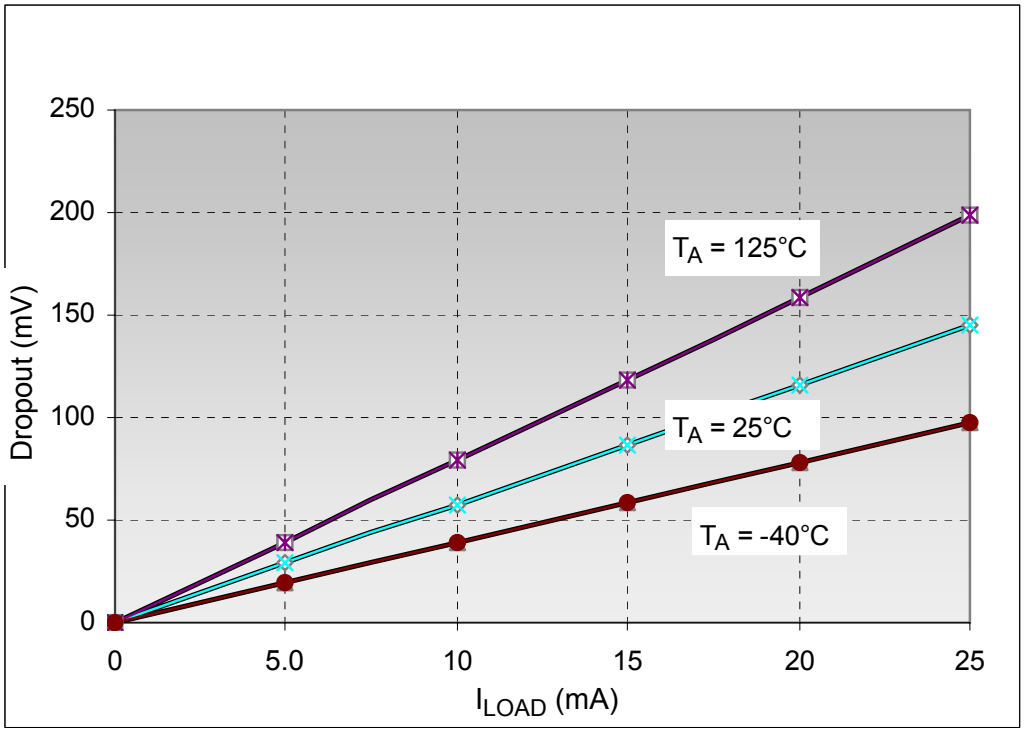


Figure 7. Dropout Voltage on HVDD

FUNCTIONAL DESCRIPTION

INTRODUCTION

The 908E626 device was designed and developed as a highly integrated and cost-effective solution for automotive and industrial applications. For automotive body electronics, the 908E626 is well suited to perform stepper motor control, e.g. for climate or light-levelling control via a 3-wire LIN bus.

This device combines an standard HC08 MCU core (68HC908EY16) with flash memory together with a *SMARTMOS* IC chip. The *SMARTMOS* IC chip combines power and control in one chip. Power switches are provided on the *SMARTMOS* IC configured as four half-bridge outputs. Other ports are also provided including a selectable HVDD pin. An internal voltage regulator is provided on the *SMARTMOS* IC chip, which provides power to the MCU chip.

Also included in this device is a LIN physical layer, which communicates using a single wire. This enables the device to be compatible with 3-wire bus systems, where one wire is used for communication, one for battery, and the third for ground.

FUNCTIONAL PIN DESCRIPTION

See Figures 1, for a graphic representation of the various pins referred to in the following paragraphs. Also, see the pin diagram on Figures 3 for a depiction of the pin locations on the package.

PORT A I/O PINS (PTA0:4)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. PTA0:PTA4 are shared with the keyboard interrupt pins, KBD0:KBD4.

The PTA5/SPSCK pin is not accessible in this device and is internally connected to the SPI clock pin of the analog die. The PTA6/$\overline{SS}$ pin is likewise not accessible.

For details refer to the 68HC908EY16 datasheet.

PORT B I/O PINS (PTB1, PTB3:7)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. All pins are shared with the ADC module. The PTB6:PTB7 pins are also shared with the Timer B module.

PTB0/AD0 is internally connected to the ADOUT pin of the analog die, allowing diagnostic measurements to be calculated; e.g., current recopy, V_{SUP}, etc. The PTB2/AD2 pin is not accessible in this device.

For details refer to the 68HC908EY16 datasheet.

PORT C I/O PINS (PTC2:4)

These pins are special function, bidirectional I/O port pins that are shared with other functional modules in the MCU. For example, PTC2:PTC4 are shared with the ICG module.

PTC0/MISO and PTC1/MOSI are not accessible in this device and are internally connected to the MISO and MOSI SPI pins of the analog die.

For details refer to the 68HC908EY16 datasheet.

PORT D I/O PINS (PTD0:1)

PTD1/TACH1 and PTD0/TACH0/BEMF are special function, bidirectional I/O port pins that can also be programmed to be timer pins.

In step motor applications the PTD0 pin should be connected to the BEMF output of the analog die in order to evaluate the BEMF signal with a special BEMF module of the MCU.

PTD1 pin is recommended for use as an output pin for generating the FGEN signal (PWM signal) if required by the application.

PORT E I/O PIN (PTE1)

PTE1/RXD and PTE0/TXD are special function, bidirectional I/O port pins that can also be programmed to be enhanced serial communication.

PTE0/TXD is internally connected to the TXD pin of the analog die. The connection for the receiver must be done externally.

EXTERNAL INTERRUPT PIN ($\overline{IRQ}$)

The $\overline{IRQ}$ pin is an asynchronous external interrupt pin. This pin contains an internal pull-up resistor that is always activated, even when the $\overline{IRQ}$ pin is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

EXTERNAL RESET PIN ($\overline{RST}$)

A logic [0] on the $\overline{RST}$ pin forces the MCU to a known startup state. $\overline{RST}$ is bidirectional, allowing a reset of the entire system. It is driven LOW when any internal reset source is asserted.

This pin contains an internal pull-up resistor that is always activated, even when the reset pin is pulled LOW.

For details refer to the 68HC908EY16 datasheet.

CURRENT LIMITATION FREQUENCY INPUT PIN (FGEN)

Input pin for the half-bridge current limitation PWM frequency. This input is not a real PWM input pin; it should just supply the period of the PWM. The duty cycle will be generated automatically.

Important The recommended FGEN frequency should be in the range of 0.1kHz to 20kHz.

BACK ELECTROMAGNETIC FORCE OUTPUT PIN (BEMF)

This pin gives the user information about back electromagnetic force (BEMF). This feature allows stall detection and coil failures in step motor applications. In order to evaluate this signal the pin must be directly connected to pin PTD0/TACH0/BEMF.

RESET PIN ($\overline{\text{RST\_A}}$)

$\overline{\text{RST\_A}}$ is the bidirectional reset pin of the analog die. It is an open drain with pull-up resistor and must be connected to the $\overline{\text{RST}}$ pin of the MCU.

INTERRUPT PIN ($\overline{\text{IRQ\_A}}$)

$\overline{\text{IRQ\_A}}$ is the interrupt output pin of the analog die indicating errors or wake-up events. It is an open drain with pull-up resistor and must be connected to the $\overline{\text{IRQ}}$ pin of the MCU.

SLAVE SELECT PIN ($\overline{\text{SS}}$)

This pin is the SPI Slave Select pin for the analog chip. All other SPI connections are done internally. $\overline{\text{SS}}$ must be connected to PTB1 or any other logic I/O of the microcontroller.

LIN BUS PIN (LIN)

The LIN pin represents the single-wire bus transmitter and receiver. It is suited for automotive bus systems and is based on the LIN bus specification.

HALF-BRIDGE OUTPUT PINS (HB1:HB4)

The 908E626 device includes power MOSFETs configured as four half-bridge driver outputs. The HB1:HB4 outputs may be configured for step motor drivers, DC motor drivers, or as high side and low side switches.

The HB1:HB4 outputs are short-circuit and over-temperature protected, and they feature current recopy, current limitation, and BEMF generation. Current limitation and recopy are done on the low side MOSFETs.

POWER SUPPLY PINS (VSUP1:VSUP3)

VSUP1:VSUP3 are device power supply pins. The nominal input voltage is designed for operation from 12V systems. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs, multiple VSUP pins are provided.

All VSUP pins must be connected to get full chip functionality.

POWER GROUND PINS (GND1 AND GND2)

GND1 and GND2 are device power ground connections. Owing to the low ON-resistance and current requirements of the half-bridge driver outputs multiple pins are provided.

GND1 and GND2 pins must be connected to get full chip functionality.

SWITCHABLE V_{DD} OUTPUT PIN (HVDD)

The HVDD pin is a switchable V_{DD} output for driving resistive loads requiring a regulated 5.0V supply; The output is short-circuit protected.

+5.0V VOLTAGE REGULATOR OUTPUT PIN (VDD)

The VDD pin is needed to place an external capacitor to stabilize the regulated output voltage. The VDD pin is intended to supply the embedded microcontroller.

Important The VDD pin should not be used to supply other loads; use the HVDD pin for this purpose. The VDD, EVDD, VDDA, and VREFH pins must be connected together.

VOLTAGE REGULATOR GROUND PIN (VSS)

The VSS pin is the ground pin for the connection of all non-power ground connections (microcontroller and sensors).

Important VSS, EVSS, VSSA, and VREFL pins must be connected together.

LIN TRANSCEIVER OUTPUT PIN (RXD)

This pin is the output of LIN transceiver. The pin must be connected to the microcontroller's Enhanced Serial Communications Interface (ESCI) module (RXD pin).

ADC REFERENCE PINS (VREFL AND VREFH)

VREFL and VREFH are the reference voltage pins for the ADC. It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

Important VREFH is the high reference supply for the ADC and should be tied to the same potential as VDDA via separate traces. VREFL is the low reference supply for the ADC and should be tied to the same potential as VSS via separate traces.

For details refer to the 68HC908EY16 datasheet.

ADC SUPPLY PINS (VDDA AND VSSA)

VDDA and VSSA are the power supply pins for the analog-to-digital converter (ADC). It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

Important VDDA is the supply for the ADC and should be tied to the same potential as EVDD via separate traces.

VSSA is the ground pin for the ADC and should be tied to the same potential as EVSS via separate traces.

For details refer to the 68HC908EY16 datasheet.

MCU POWER SUPPLY PINS (EVDD AND EVSS)

EVDD and EVSS are the power supply and ground pins. The MCU operates from a single power supply.

Fast signal transitions on MCU pins place high, short-duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU.

For details refer to the 68HC908EY16 datasheet.

TEST PIN (FLSVPP)

This pin is for test purposes only. This pin should be either left open (not connected) or connected to GND.

EXPOSED PAD PIN

The exposed pad pin on the bottom side of the package conducts heat from the chip to the PCB board. For thermal performance the pad must be soldered to the PCB board. It is recommended that the pad be connected to the ground potential.

FUNCTIONAL DEVICE OPERATION

OPERATIONAL MODES

INTERRUPTS

The 908E626 has six different interrupt sources as described in the following paragraphs. The interrupts can be disabled or enabled via the SPI. After reset all interrupts are automatically disabled.

LOW VOLTAGE INTERRUPT

The Low Voltage Interrupt (LVI) is related to the external supply voltage, V_{SUP}. If this voltage falls below the LVI threshold, it will set the LVI flag. If the low voltage interrupt is enabled, an interrupt will be initiated.

With LVI the H-bridges (high side MOSFET only) are switched off. All other modules are not influenced by this interrupt.

During STOP mode the LVI circuitry is disabled.

HIGH VOLTAGE INTERRUPT

The High voltage Interrupt (HVI) is related to the external supply voltage, V_{SUP}. If this voltage rises above the HVI threshold, it will set the HVI flag. If the High voltage Interrupt is enabled, an interrupt will be initiated.

With HVI the H-bridges (high side MOSFET only) are switched off. All other modules are not influenced by this interrupt.

During STOP mode the HVI circuitry is disabled.

HIGH TEMPERATURE INTERRUPT

The High Temperature Interrupt (HTI) is generated by the on-chip temperature sensors. If the chip temperature is above the HTI threshold, the HTI flag will be set. If the High Temperature Interrupt is enabled, an interrupt will be initiated.

During STOP mode the HTI circuitry is disabled.

AUTONOMOUS WATCHDOG INTERRUPT (AWD)

Refer to Autonomous Watchdog (AWD) on page 31.

LIN INTERRUPT

If the LINIE bit is set, a falling edge on the LIN pin will generate an interrupt. During STOP mode this interrupt will initiate a system wake-up.

OVER-CURRENT INTERRUPT

If an over-current condition on a half-bridge or the HVDD output is detected and the OCIE bit is set and an interrupt generated.

SYSTEM WAKE-UP

System wake-up can be initiated by any of four events:

- A falling edge on the LIN pin
- A wake-up signal from the AWD
- An LVR condition

If one of these wake-up events occurs and the interrupt mask bit for this event is set, the interrupt will wake-up the microcontroller as well as the main voltage regulator (MREG) Figures 8.

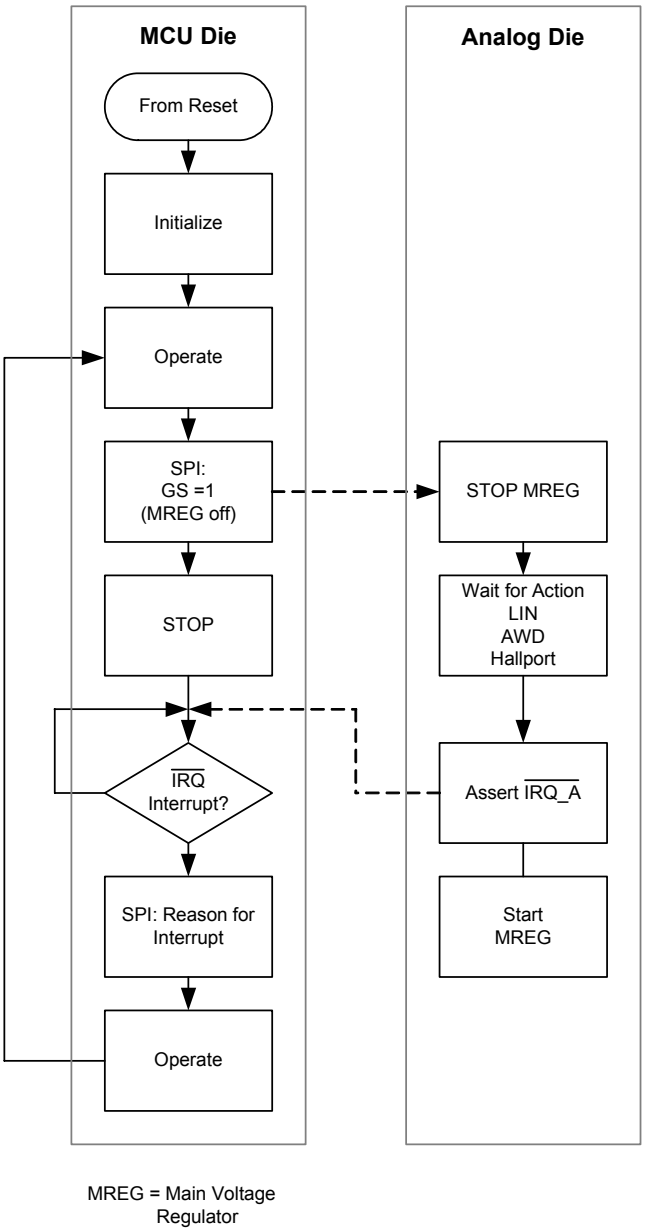


Figure 8. STOP Mode/Wake-up Procedure

INTERRUPT FLAG REGISTER (IFR)

Register Name and Address: IFR - $05

	6	5	4	3	2	1	Bit0
Read	0	0	LINF	HTF	LVF	HVF	OCF	0
	0	0	0	0	0	0	0	0

LINF—LIN FLAG BIT

This read/write flag is set on the falling edge at the LIN data line. Clear LINF by writing a logic [1] to LINF. Reset clears the LINF bit. Writing a logic [0] to LINF has no effect.

- 1 = Falling edge on LIN data line has occurred.
- 0 = Falling edge on LIN data line has not occurred since last clear.

HTF—HIGH TEMPERATURE FLAG BIT

This read/write flag is set on a high temperature condition. Clear HTF by writing a logic [1] to HTF. If a high temperature condition is still present while writing a logic [1] to HTF, the

writing has no effect. Therefore, a high temperature interrupt cannot be lost due to inadvertent clearing of HTF. Reset clears the HTF bit. Writing a logic [0] to HTF has no effect.

- 1 = High temperature condition has occurred.
- 0 = High temperature condition has not occurred.

LVF—LOW VOLTAGE FLAG BIT

This read/write flag is set on a low voltage condition. Clear LVF by writing a logic [1] to LVF. If a low voltage condition is still present while writing a logic [1] to LVF, the writing has no effect. Therefore, a low voltage interrupt cannot be lost due to inadvertent clearing of LVF. Reset clears the LVF bit. Writing a logic [0] to LVF has no effect.

- 1 = Low voltage condition has occurred.
- 0 = Low voltage condition has not occurred.

HVF—HIGH VOLTAGE FLAG BIT

This read/write flag is set on a high voltage condition. Clear HVF by writing a logic [1] to HVF. If high voltage condition is still present while writing a logic [1] to HVF, the writing has no effect. Therefore, a high voltage interrupt cannot be lost due to inadvertent clearing of HVF. Reset clears the HVF bit. Writing a logic [0] to HVF has no effect.

- 1 = High voltage condition has occurred.
- 0 = High voltage condition has not occurred.

OCF—OVER-CURRENT FLAG BIT

This read-only flag is set on an overcurrent condition. Reset clears the OCF bit. To clear this flag, write a logic [1] to the appropriate overcurrent flag in the SYSSTAT Register. See Figure 9, which shows the two signals triggering the OCF.

- 1 = High current condition has occurred.
- 0 = High current condition has not occurred.

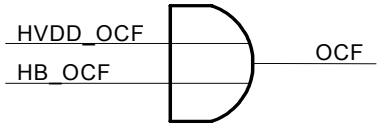


Figure 9. Principal Implementation for OCF

INTERRUPT MASK REGISTER (IMR)

Register Name and Address: IMR - $04

	6	5	4	3	2	1	Bit0
Read	0	0	LINIE	HTIE	LVIE	HVIE	OCIE	0
	0	0	0	0	0	0	0	0

LINIE—LIN LINE INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the LIN flag, LINF. Reset clears the LINIE bit.

- 1 = Interrupt requests from LINF flag enabled.
- 0 = Interrupt requests from LINF flag disabled.

HTIE—HIGH TEMPERATURE INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the high temperature flag, HTF. Reset clears the HTIE bit.

- 1 = Interrupt requests from HTF flag enabled.
- 0 = Interrupt requests from HTF flag disabled.

LVIE—LOW VOLTAGE INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the low voltage flag, LVF. Reset clears the LVIE bit.

- 1 = Interrupt requests from LVF flag enabled.
- 0 = Interrupt requests from LVF flag disabled.

HVIE—HIGH VOLTAGE INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the high voltage flag, HVF. Reset clears the HVIE bit.

- 1 = Interrupt requests from HVF flag enabled.
- 0 = Interrupt requests from HVF flag disabled.

OCIE—OVER-CURRENT INTERRUPT ENABLE BIT

This read/write bit enables CPU interrupts by the overcurrent flag, OCF. Reset clears the OCIE bit.

- 1 = Interrupt requests from OCF flag enabled.
- 0 = Interrupt requests from OCF flag disabled.

RESET

The 908E626 chip has four internal reset sources and one external reset source, as explained in the paragraphs below. Figure 10 depicts the internal reset sources.

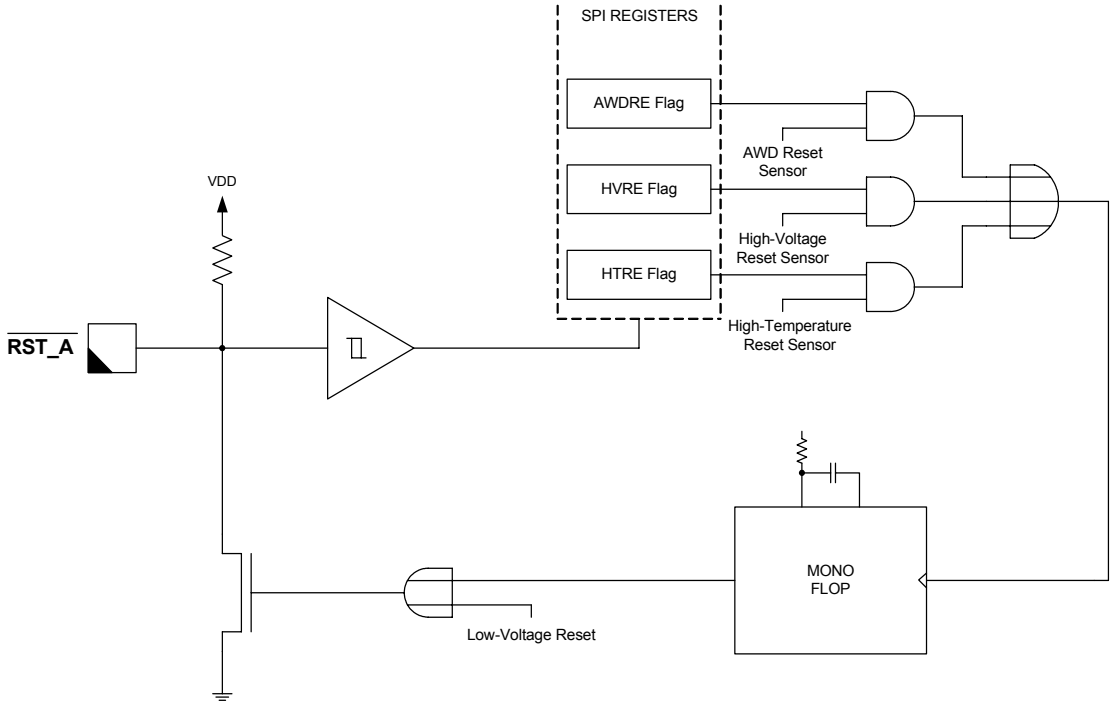


Figure 10. Internal Reset Routing

RESET INTERNAL SOURCES

Autonomous Watchdog

AWD modules generates a reset because of a timeout (watchdog function).

High Temperature Reset

To prevent damage to the device, a reset will be initiated if the temperature rises above a certain value. The reset is maskable with bit HTRE in the Reset Mask Register. After a reset the high temperature reset is disabled.

Low Voltage Reset

The LVR is related to the internal V_{DD}. In case the voltage falls below a certain threshold, it will pull down the $\overline{\text{RST\_A}}$ pin.

High Voltage Reset

The HVR is related to the external V_{SUP} voltage. In case the voltage is above a certain threshold, it will pull down the $\overline{\text{RST\_A}}$ pin. The reset is maskable with bit HVRE in the Reset Mask Register. After a reset the high voltage reset is disabled.

RESET EXTERNAL SOURCE

External Reset Pin

The microcontroller has the capability of resetting the *SMARTMOS* device by pulling down the $\overline{\text{RST}}$ pin.

Reset Mask Register (RMR)

Register Name and Address: RMR - $06

	6	5	4	3	2	1	Bit0
Read	TTEST	0	0	0	0	0	HVRE	HTRE
	0	0	0	0	0	0	0	0

TTEST—High Temperature Reset Test

This read/write bit is for test purposes only. It decreases the overtemperature shutdown limit for final test. Reset clears the HTRE bit.

- 1 = Low temperature threshold enabled.
- 0 = Low temperature threshold disabled.

HVRE—High Voltage Reset Enable Bit

This read/write bit enables resets on high voltage conditions. Reset clears the HVRE bit.

- 1 = High voltage reset enabled.
- 0 = High voltage reset disabled.

HTRE—High Temperature Reset Enable Bit

This read/write bit enables resets on high temperature conditions. Reset clears the HTRE bit.

- 1 = High temperature reset enabled.
- 0 = High temperature reset disabled.

SERIAL PERIPHERAL INTERFACE

The serial peripheral interface (SPI) creates the communication link between the microcontroller and the 908E626.

The interface consists of four pins (see Figure 11):

- $\overline{\text{SS}}$—Slave Select
- MOSI—Master-Out Slave-In
- MISO—Master-In Slave-Out
- SPSCK—Serial Clock (maximum frequency 4.0 MHz)

A complete data transfer via the SPI consists of 2 bytes. The master sends address and data, slave system status, and data of the selected address.

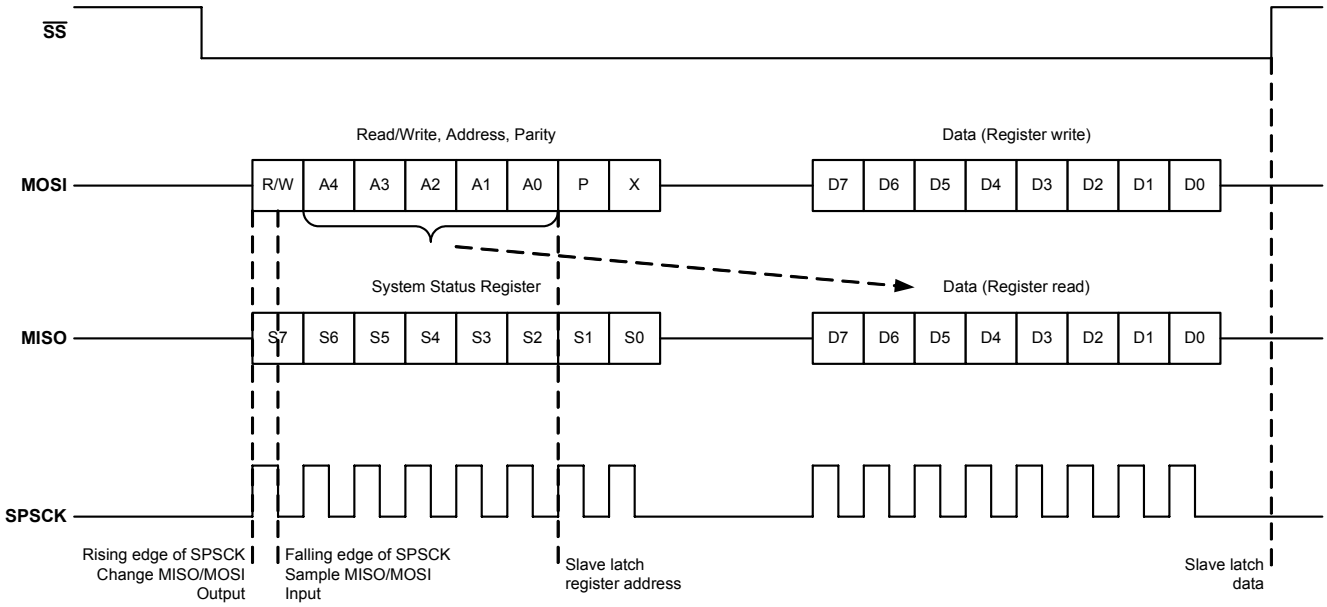


Figure 11. SPI Protocol

During the inactive phase of $\overline{\text{SS}}$, the new data transfer is prepared. The falling edge on the $\overline{\text{SS}}$ line indicates the start of a new data transfer and puts MISO in the low-impedance mode. The first valid data are moved to MISO with the rising edge of SPSCK.

The MISO output changes data on a rising edge of SPSCK. The MOSI input is sampled on a falling edge of SPSCK. The data transfer is only valid if exactly 16 sample clock edges are present in the active phase of $\overline{\text{SS}}$.

After a write operation, the transmitted data is latched into the register by the rising edge of $\overline{SS}$. Register read data is internally latched into the SPI at the time when the parity bit is transferred. $\overline{SS}$ HIGH forces MISO to high impedance.

MASTER ADDRESS BYTE

A4:A0

Contains the address of the desired register.

R/$\overline{W}$

Contains information about a read or a write operation.

- If R/$\overline{W}$ = 1, the second byte of master contains no valid information, slave just transmits back register data.
- If R/$\overline{W}$ = 0, the master sends data to be written in the second byte, slave sends concurrently contents of selected register prior to write operation, write data is latched in the *SMARTMOS* register on rising edge of $\overline{SS}$.

Parity P

The parity bit is equal to “0” if the number of 1 bits is an even number contained within R/$\overline{W}$, A4:A0. If the number of 1 bits is odd, P equals “1”. For example, if R/$\overline{W}$ = 1, A4:A0 = 00001, then P equals “0.”

The parity bit is only evaluated during a write operation.

Bit X

Not used.

Master Data Byte

Contains data to be written or no valid data during a read operation.

Table 6. List of Registers

Addr	Register Name	R/W	Bit							
			7	6	5	4	3	2	1	0
$01	H-bridge Output (HBOUT)	R	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB1_H	HB1_L
		W								
$02	H-bridge Control (HBCTL)	R	OFC_EN	CSA	0	0	0	CLS2	CLS1	CLS0
		W								
$03	System Control (SYSCTL)	R	PSON	SRS1	SRS0	0	0	0	0	0
		W								GS
$04	Interrupt Mask (IMR)	R	0	0	LINIE	HTIE	LVIE	HVIE	OCIE	0
		W								
$05	Interrupt Flag (IFR)	R	0	0	LINF	HTF	LVF	HVF	OCF	0
		W								
$06	Reset Mask (RMR)	R	TTEST	0	0	0	0	0	HVRE	HTRE
		W								
$07	Analog Multiplexer Configuration (ADMUX)	R	0	0	0	0	SS3	SS2	SS1	SS0
		W								
$08	Reserved	R	0	0	0	0	0	0	0	0
		W								
$09	Reserved	R	0	0	0	0	0	0	0	0
		W								
$0a	AWD Control (AWDCTL)	R	0	0	0	AWDRE	AWDIE	0	AWDF	AWDR
		W			AWDRST					
$0b	Power Output (POUT)	R	0	0	0	0	0	0	HVDDON	0
		W								
$0c	System Status (SYSSTAT)	R	0	LINCL	HVDD_OCF	0	LVF	HVF	HB_OCF	HTF
		W								

Slave Status Byte

Contains the contents of the System Status Register ($0c) independent of whether it is a write or read operation or which register was selected.

Slave Data Byte

Contains the contents of selected register. During a write operation it includes the register content prior to a write operation.

SPI Register Overview

Table 6 summarizes the SPI Register addresses and the bit names of each register.

ANALOG DIE I/OS

LIN Physical Layer

The LIN bus pin provides a physical layer for single-wire communication in automotive applications. The LIN physical layer is designed to meet the LIN physical layer specification.

The LIN driver is a low side MOSFET with internal current limitation and thermal shutdown. An internal pull-up resistor with a serial diode structure is integrated, so no external pullup components are required for the application in a slave node. The fall time from dominant to recessive and the rise time from recessive to dominant is controlled. The symmetry between both slew rate controls is guaranteed.

The LIN pin offers high susceptibility immunity level from external disturbance, guaranteeing communication during external disturbance.

The LIN transmitter circuitry is enabled by setting the PSON bit in the System Control Register (SYSCTL). If the transmitter works in the current limitation region, the LINCL bit in the System Status Register (SYSSTAT) is set. Due to excessive power dissipation in the transmitter, software is advised to monitor this bit and turn the transmitter off immediately.

TXD Pin

The TXD pin is the MCU interface to control the state of the LIN transmitter (see Figure , page 2). When TXD is LOW, LIN output is low (dominant state). When TXD is HIGH, the LIN output MOSFET is turned off. The TXD pin has an internal pullup current source in order to set the LIN bus in recessive state in the event, for instance, the microcontroller could not control it during system power-up or power-down.

RXD Pin

The RXD transceiver pin is the MCU interface, which reports the state of the LIN bus voltage. LIN HIGH (recessive state) is reported by a high level on RXD, LIN LOW (dominant state) by a low level on RXD.

STOP Mode/Wake-up Feature

During STOP mode operation the transmitter of the physical layer is disabled. The receiver pin is still active and able to detect wake-up events on the LIN bus line.If LIN interrupt is enabled (LINIE bit in the Interrupt Mask Register is set), a falling edge on the LIN line causes an interrupt. This interrupt switches on the main voltage regulator and generates a system wake-up.

Analog Multiplexer/ADOUT Pin

The ADOUT pin is the analog output interface to the ADC of the MCU (see Figure , page 2). An analog multiplexer is used to read six internal diagnostic analog voltages.

Current Recopy

The analog multiplexer is connected to the four low side current sense circuits of the half-bridges. These sense circuits offer a voltage proportional to the current through the low side MOSFET. High or low resolution is selectable: 5.0V/2.5A or 5.0V/500mA, respectively. (Refer to Half-Bridge Current Recopy on page 28.)

Temperature Sensor

The 908E626 includes an on-chip temperature sensor. This sensor offers a voltage that is proportional to the actual chip junction temperature.

V_{SUP} Prescaler

The V_{SUP} prescaler permits the reading or measurement of the external supply voltage. The output of this voltage is $V_{SUP}/RATIO_{VSUP}$.

The different internal diagnostic analog voltages can be selected with the ADMUX Register.

Analog Multiplexer Configuration Register (ADMUX)

Register Name and Address: ADMUX - $07

	6	5	4	3	2	1	Bit0
Read	0	0	0	0	SS3	SS2	SS1	SS0
	0	0	0	0	0	0	0	0

SS3, SS2, SS1, and SS0—A/D Input Select Bits

These read/write bits select the input to the ADC in the microcontroller according to Table 7, page 24. Reset clears SS3, SS2, SS1, and SS0 bits.

Table 7. Analog Multiplexer Configuration Register

SS3	SS2	SS1	SS0	Channel
0	0	0	0	Current Recopy HB1
0	0	0	1	Current Recopy HB2
0	0	1	0	Current Recopy HB3
0	0	1	1	Current Recopy HB4
0	1	0	0	V_{SUP} Prescaler
0	1	0	1	Temperature Sensor
0	1	1	0	Not Used
0	1	1	1	
1	0	0	0	
1	0	0	1	
1	0	1	0	
1	0	1	1	
1	1	0	0	
1	1	0	1	
1	1	1	0	
1	1	1	1	

Power Output Register (POUT)

Register Name and Address: P_{OUT} - $0b

	6	5	4	3	2	1	Bit0
Read	0	0	0 (16)	0 (16)	0 (16)	0 (16)	HVDDON	0 (16)
	0	0	0	0	0	0	0	0

Notes

HVDDON—HVDD On Bit

This read/write bit enables HVDD output. Reset clears the HVDDON bit.

- 1 = HVDD enabled.
- 0 = HVDD disabled.

HALF-BRIDGES

Outputs HB1:HB4 provide four low resistive half-bridge output stages. The half-bridges can be used in H-bridge, high side, or low side configurations.

Reset clears all bits in the H-bridge Output Register (HBOUT) owing to the fact that all half-bridge outputs are switched off.

HB1:HB4 output features:

- Short circuit (over-current) protection on high side and low side MOSFETs.
- Current recopy feature (low side MOSFET).
- Over-temperature protection.
- Over-voltage and under-voltage protection.
- Current limitation feature (low side MOSFET).

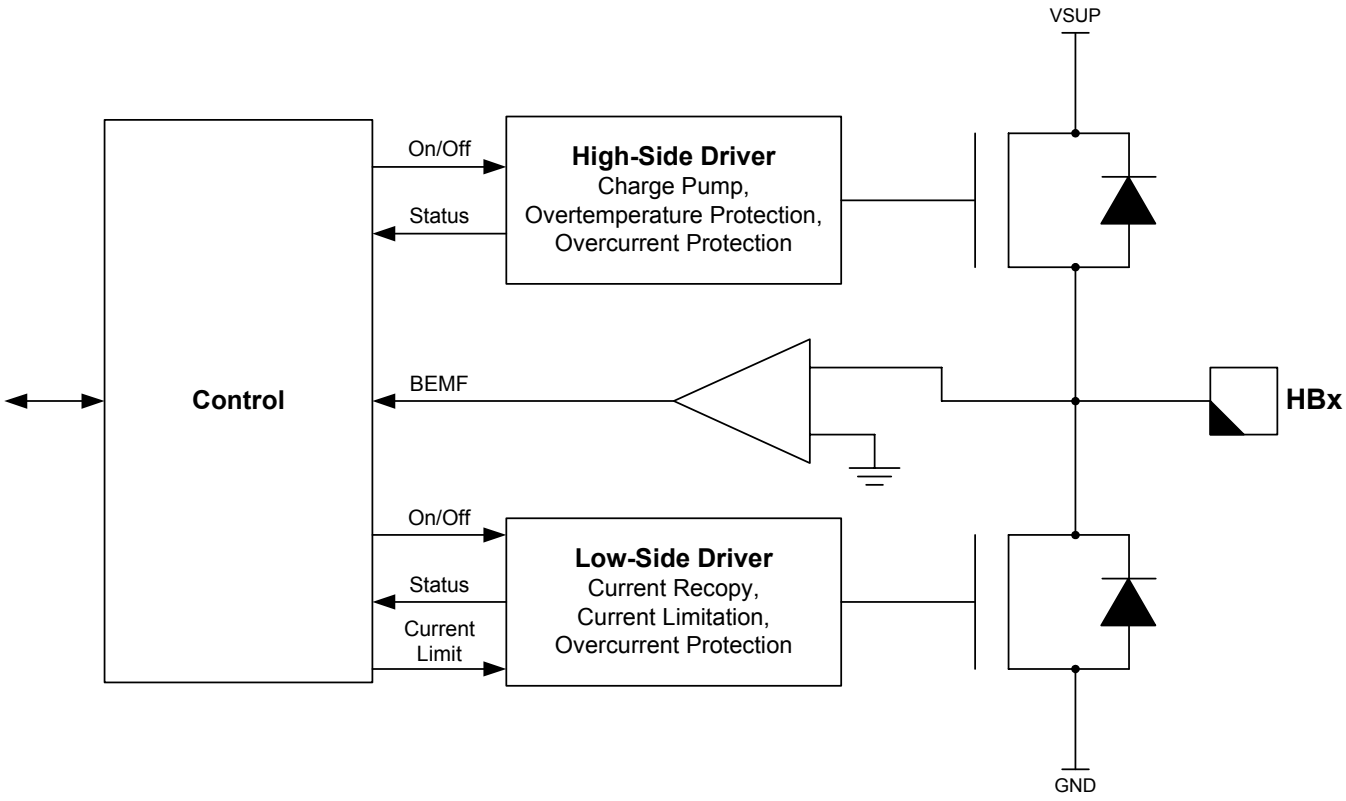


Figure 12. Half-bridge Push-Pull Output Driver

Half-Bridge Control

Each output MOSFET can be controlled individually. The general enable of the circuitry is done by setting PSON in the System Control Register (SYSCTL). HBx_L and HBx_H form one half-bridge. It is not possible to switch on both MOSFETs in one half-bridge at the same time. If both bits are set, the high side MOSFET has a higher priority.

To avoid both MOSFETs (high side and low side) of one half-bridge being on at the same time, a break-before-make circuit exists. Switching the high side MOSFET on is inhibited as long as the potential between gate and V_{SS} is not below a certain threshold. Switching the low side MOSFET on is blocked as long as the potential between gate and source of the high side MOSFET did not fall below a certain threshold.

Half-bridge Output Register (HBOUT)

Register Name and Address: HBOUT - $01

	6	5	4	3	2	1	Bit0
Read	HB4_H	HB4_L	HB3_H	HB3_L	HB2_H	HB2_L	HB1_H	HB1_L
Reset	0	0	0	0	0	0	0	0

HBx_L—Low Side On/Off Bits

These read/write bits turn on the low side MOSFETs. Reset clears the HBx_L bits.

- 1 = Low side MOSFET turned on for half-bridge output x.
- 0 = Low side MOSFET turned off for half-bridge output x.

HBx_H—High Side On/Off Bits

These read/write bits turn on the high side MOSFETs. Reset clears the HBx_H bits.

- 1 = High side MOSFET turned on for half-bridge output x.
- 0 = High side MOSFET turned on for half-bridge output x.

HALF-BRIDGE CURRENT LIMITATION

Each low side MOSFET offers a current limit or constant current feature. This features is realized by a pulse width modulation on the low side MOSFET. The pulse width modulation on the outputs is controlled by the FGEN input and the load characteristics. The FGEN input provides the PWM frequency, whereas the duty cycle is controlled by the load characteristics.

The recommended frequency range for the FGEN and the PWM is 0.1kHz to 20kHz.

Functionality

Each low side MOSFET switches off if a current above the selected current limit was detected. The 908E626 offers five different current limits (refer to Table 8, page 30, for current limit values). The low side MOSFET switches on again if a rising edge on the FGEN input was detected (Figure 13).

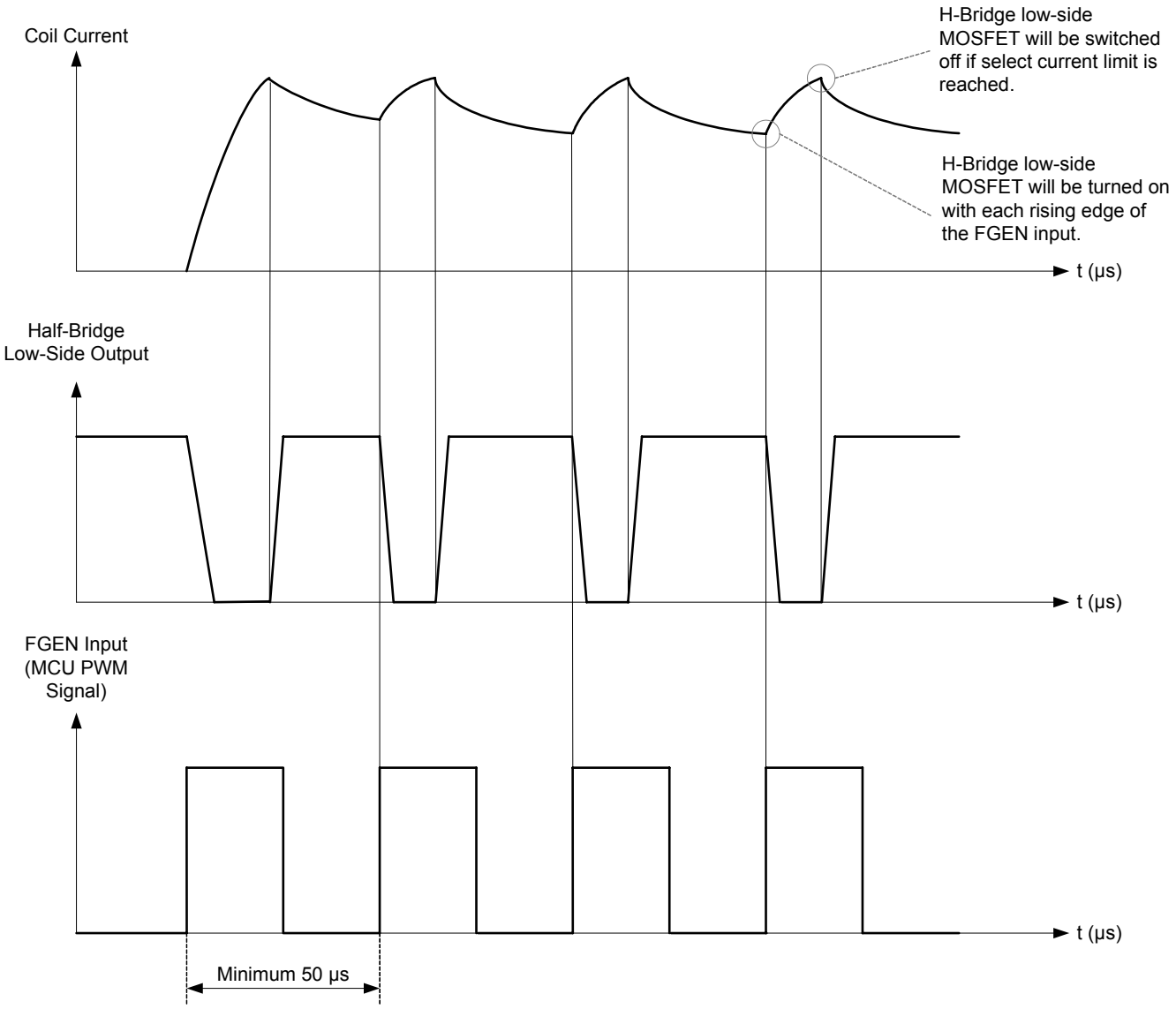


Figure 13. Half-bridge Current Limitation

Offset Chopping

If bit OFC_EN in the H-bridge Control Register (HBCTL) is set, HB1 and HB2 will continue to switch on the low side MOSFETs with the rising edge of the FGEN signal and HB3 and HB4 will switch on the low side MOSFETs with the falling edge on the FGEN input. In step motor applications, this feature allows the reduction of EMI due to a reduction of the di/dt (Figure 14).

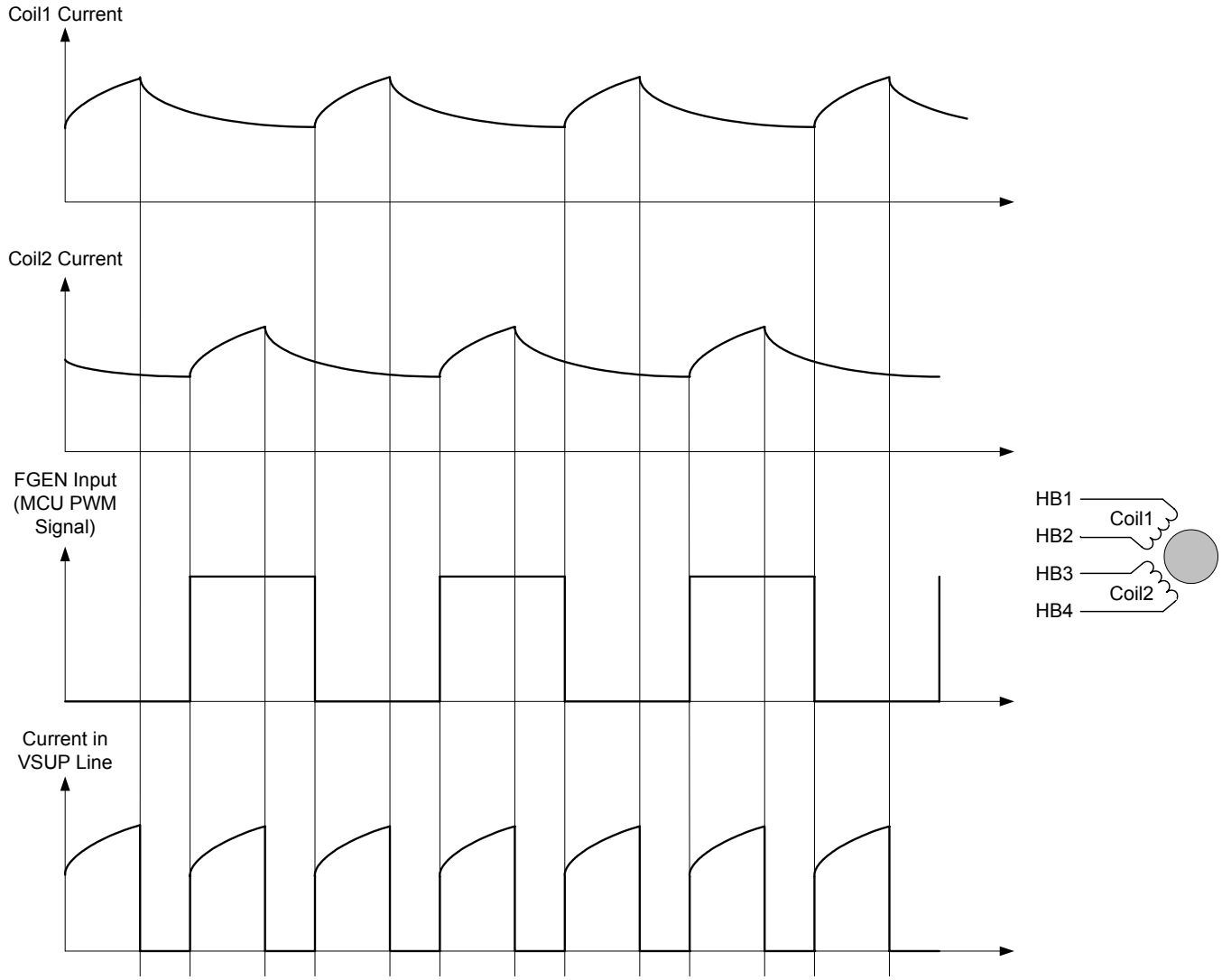


Figure 14. Offset Chopping for Step Motor Control

HALF-BRIDGE CURRENT RECOPY

Each low side MOSFET has an additional sense output to allow a current recopy feature. This sense source is internally connected to a shunt resistor. The drop voltage is amplified and switched to the analog multiplexer.

The factor for the current sense amplification can be selected via bit CSA in the System Control Register.

- CSA = 1: Low resolution selected (500 mA measurement range).
- CSA = 0: High resolution selected (2.5 A measurement range).

HALF-BRIDGE BEMF GENERATION

The BEMF output is set to “1” if a recirculation current is detected in any half-bridge. This recirculation current flows via the two freewheeling diodes of the power MOSFETs. The BEMF circuitry detects that and generates a HIGH on the BEMF output as long as a recirculation current is detected. This signal provides a flexible and reliable detection of stall in step motor applications. For this the BEMF circuitry takes advantage of the instability of the electrical and mechanical behavior of a step motor when blocked. In addition the signal can be used for open load detection (absence of this signal) (see Figure 15, page 29).

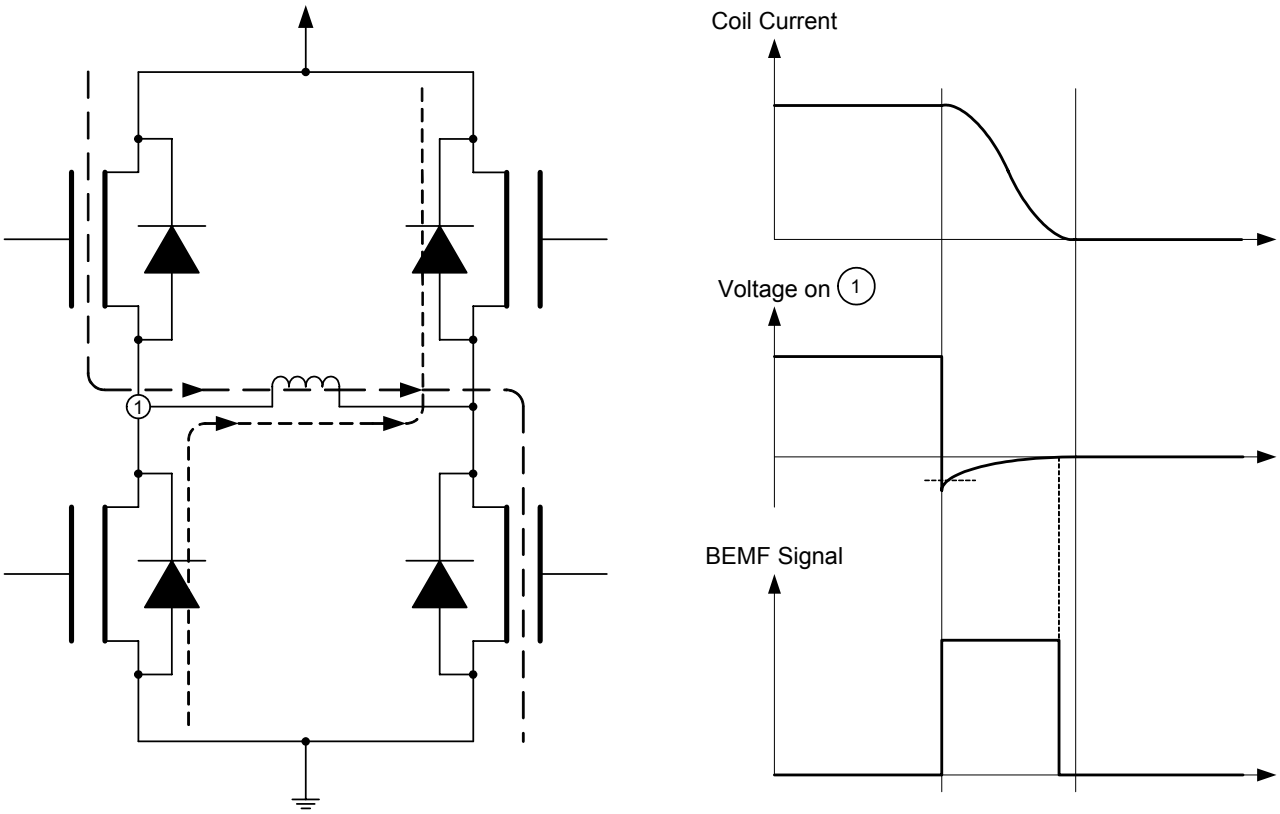


Figure 15. BEMF Signal Generation

HALF-BRIDGE OVERTEMPERATURE PROTECTION

The half-bridge outputs provide an over-temperature pre-warning with the HTF in the Interrupt Flag Register (IFR). In order to protect the outputs against over-temperature, the High Temperature Reset must be enabled. If this value is reached, the part generates a reset and disables all power outputs.

HALF-BRIDGE OVER-CURRENT PROTECTION

The half-bridges are protected against short to GND, short to VSUP, and load shorts.

In the event an over-current on the high side is detected, the high side MOSFETs on all HB high side MOSFETs are switched off automatically. In the event an over-current on the low side is detected, all HB low side MOSFETs are switched off automatically. In both cases, the over-current status flag HB_OCF in the System Status Register (SYSSTAT) is set.

The over-current status flag is cleared (and the outputs re-enabled) by writing a logic [1] to the HB_OCF flag in the System Status Register or by reset.

HALF-BRIDGE OVER-VOLTAGE/UNDER-VOLTAGE

The half-bridge outputs are protected against under-voltage and over-voltage conditions. This protection is done by the low and high voltage interrupt circuitry. If one of these flags (LVF, HVF) is set, the outputs are automatically disabled.

The over-voltage/under-voltage status flags are cleared (and the outputs re-enabled) by writing a logic [1] to the LVF/HVF flags in the Interrupt Flag Register or by reset. Clearing this flag is useless as long as a high or low voltage condition is present.

Half-bridge Control Register (HBCTL)

Register Name and Address: HBCTL - $02

	6	5	4	3	2	1	Bit0
Read	OFC_EN	CSA	0	0	0	CLS2	CLS1	CLS0
	0	0	0	0	0	0	0	0

OFC_EN—H-bridge Offset Chopping Enable Bit

This read/write bit enables offset chopping. Reset clears the OFC_EN bit.

- 1 = Offset chopping enabled.
- 0 = Offset chopping disabled.

CSA—H-bridges Current Sense Amplification Select Bit

This read/write bit selects the current sense amplification of the H-bridges. Reset clears the CSA bit.

- 1 = Current sense amplification set for measuring 0.5 A.
- 0 = Current sense amplification set for measuring 2.5 A.

CLS2:CLS0—H-bridge Current Limitation Selection Bits

These read/write bits select the current limitation value according to Table 8. Reset clears the CLS2:CLS0 bits.

Table 8. H-bridge Current Limitation Value Selection

CLS2	CLS1	CLS0	Current Limit
0	0	0	No Limit
0	0	1	
0	1	0	
0	1	1	55mA (typ)
1	0	0	260mA (typ)
1	0	1	370mA (typ)
1	1	0	550mA (typ)
1	1	1	740mA (typ)

Bits

Switchable VDD Outputs

The HVDD pin is a switchable VDD output pin. It can be used for driving external circuitry that requires a V_{DD} voltage. The output is enabled with bit PSON in the System Control Register and can be switched on/off with bit HVDDON in the Power Output Register. Low or high voltage conditions (LVI/HVI) have no influence on this circuitry.

HVDD Over-temperature Protection

Over-temperature protection is enabled if the high temperature reset is enabled.

HVDD Over-current Protection

The HVDD output is protected against over-current. In the event the over-current limit is or was reached, the output automatically switches off and the HVDD over-current flag in the System Status Register is set.

System Control Register (SYSCTL)

Register Name and Address: SYSCTL - $03

	Bit7	6	5	4	3	2	1	Bit0
Read	PSON	SRS1	SRS0	0	0	0	0	0
Write								GS
Reset	0	0	0	0	0	0	0	0

PSON—Power Stages On Bit

This read/write bit enables the power stages (half-bridges, LIN transmitter and HVDD output). Reset clears the PSON bit.

- 1 = Power stages enabled.
- 0 = Power stages disabled.

SRS0:SRS1—LIN Slew Rate Selection Bits

These read/write bits enable the user to select the appropriate LIN slew rate for different baud rate configurations as shown in Table 9.

The high speed slew rates are used, for example, for programming via the LIN and are not intended for use in the application.

Table 9. LIN Slew Rate Selection Bits

SRS1	SRS0	LIN Slew Rate
0	0	Initial Slew Rate (20 kBaud)
0	1	Slow Slew Rate (10 kBaud)
1	0	High Speed II (8x)
1	1	High Speed I (4x)

Go to STOP Mode Bit (GS)

This write-only bit instructs the 908E626 to power down and go into STOP mode. Reset or CPU interrupt requests clear the GS bit.

- 1 = Power down and go into STOP mode
- 0 = Not in STOP mode

System Status Register (SYSSTAT)

Register Name and Address: SYSSTAT - $0c

	6	5	4	3	2	1	Bit0
Read	LINCL	HVDD_OCF	0	LVF	HVF	HB_OCF	HTF
	0	0	0	0	0	0	0

LINCL — LIN Current Limitation Bit

This read-only bit is set if the LIN transmitter operates in current limitation region. Due to excessive power dissipation

in the transmitter, software is advised to turn the transmitter off immediately.

- 1 = Transmitter operating in current limitation region.
- 0 = Transmitter not operating in current limitation region.

HVDD_OCF—HVDD Output Over-current Flag Bit

This read/write flag is set on an over-current condition at the HVDD pin. Clear HVDD_OCF and enable the output by writing a logic [1] to the HVDD_OCF Flag. Reset clears the HVDD_OCF bit. Writing a logic [0] to HVDD_OCF has no effect.

- 1 = Over-current condition on HVDD has occurred.
- 0 = No over-current condition on HVDD has occurred.

LVF—Low Voltage Bit

This read only bit is a copy of the LVF bit in the Interrupt Flag Register.

- 1 = Low voltage condition has occurred.
- 0 = No low voltage condition has occurred.

HVF—High Voltage Sensor Bit

This read-only bit is a copy of the HVF bit in the Interrupt Flag Register.

- 1 = High voltage condition has occurred.
- 0 = No high voltage condition has occurred.

HB_OCF—H-bridge Over-current Flag Bit

This read / write flag is set on an over-current condition at the H-bridges. Clear HB_OCF and enable the H-bridge driver by writing a logic [1] to HB_OCF. Reset clears the HB_OCF bit. Writing a logic [0] to HB_OCF has no effect.

- 1 = Over-current condition on H-bridges has occurred.
- 0 = No over-current condition on H-bridges has occurred.

HTF—Over-temperature Status Bit

This read-only bit is a copy of the HTF bit in the Interrupt Flag Register.

- 1 = Over-temperature condition has occurred.
- 0 = No over-temperature condition has occurred.

AUTONOMOUS WATCHDOG (AWD)

The Autonomous Watchdog module consists of three functions:

- Watchdog function for the CPU in RUN mode
- Periodic interrupt function in STOP mode

The Autonomous Watchdog module allows to protect the CPU against code runaways.

The AWD is enabled if AWDIE, AWDRE in the AWDCTL Register is set. If this bit is cleared, the AWD oscillator is disabled and the watchdog switched off.

Watchdog

The watchdog function is only available in RUN mode. On setting the AWDRE bit, watchdog functionality in RUN mode is activated. Once this function is enabled, it is not possible to disable it via software.

If the timer reaches end value and AWDRE is set, a system reset is initiated. Operations of the watchdog function cease in STOP mode. Normal operation will be continued when the system is back to RUN mode.

To prevent a watchdog reset, the watchdog timeout counter must be reset before it reaches the end value. This is done by a write to the AWDRST bit in the AWDCTL Register.

PERIODIC INTERRUPT

Periodic interrupt is only available in STOP mode. It is enabled by setting the AWDIE bit in the AWDCTL Register. If AWDIE is set, the AWD wakes up the system after a fixed period of time. This time period can be selected with bit AWDR in the AWDCTL Register.

Autonomous Watchdog Control Register (AWDCTL)

Register Name and Address: AWDCTL - $0a

	6	5	4	3	2	1	Bit0
Read	0	0	0	AWDRE	AWDIE	0[17]	0	AWDR
			AWDRST					
	0	0	0	0	0	0	0	0

Notes

AWDRST—Autonomous Watchdog Reset Bit

This write-only bit resets the Autonomous Watchdog timeout period. AWDRST always reads 0. Reset clears AWDRST bit.

- 1 = Reset AWD and restart timeout period.
- 0 = No effect.

AWDRE—Autonomous Watchdog Reset Enable Bit

This read/write bit enables resets on AWD time-outs. A reset on the $\overline{\text{RST\_A}}$ is asserted when the Autonomous Watchdog has reached the timeout and the Autonomous Watchdog is enabled. AWDRE is one-time setable (write once) after each reset. Reset clears the AWDRE bit.

- 1 = Autonomous watchdog enabled.
- 0 = Autonomous watchdog disabled.

Autonomous Watchdog Interrupt Enable Bit (AWDIE)

This read/write bit enables CPU interrupts by the Autonomous Watchdog timeout flag, AWFD. IRQ_A is only asserted when the device is in STOP mode. Reset clears the AWDIE bit.

- 1 = CPU interrupt requests from AWDF enabled
- 0 = CPU interrupt requests from AWDF disabled

AWDR—Autonomous Watchdog Rate Bit

This read/write bit selects the clock rate of the Autonomous Watchdog. Reset clears the AWDR bit.

- 1 = Fast rate selected (10ms).
- 0 = Slow rate selected (20ms).

VOLTAGE REGULATOR

The 908E626 chip contains a low power, low drop voltage regulator to provide internal power and external power for the MCU. The V_{DD} regulator accepts a unregulated input supply and provides a regulated V_{DD} supply to all digital sections of the device. The output of the regulator is also connected to the VDD pin to provide the 5.0V to the microcontroller.

Note: Under loss of power conditions, the discharge of the V_{DD} capacitor may occur relatively slow. Based on the selected external components and external V_{DD} load, additional external load may be required guarantee the MCU POR threshold being reached before the next power up.

RUN Mode

During RUN mode, the main voltage regulator is on. It provides a regulated supply to all digital sections.

STOP Mode

During STOP mode the STOP mode regulator supplies a regulated output voltage. The STOP mode regulator has a very limited output current capability. The output voltage will be lower than the output voltage of the main voltage regulator.

FACTORY TRIMMING AND CALIBRATION

To enhance the ease-of-use of the 908E626, various parameters (e.g. ICG trim value) are stored in the flash memory of the device. The following flash memory locations are reserved for this purpose and might have a value different from the *empty* (0xFF) state:

- 0xFD80:0xFDDF Trim and Calibration Values
- 0xFFFE:0xFFFF Reset Vector

In the event the application uses these parameters, one has to take care not to erase or override these values. If these parameters are not used, these flash locations can be erased and otherwise used.

Trim Values

Below the usage of the trim values located in the flash memory is explained

Internal Clock Generator (ICG) Trim Value

The internal clock generator (ICG) module is used to create a stable clock source for the microcontroller without using any external components. The untrimmed frequency of the low frequency base clock (IBASE), will vary as much as ±25 percent due to process, temperature, and voltage dependencies. To compensate this dependencies a ICG trim values is located at address $FDC2. After trimming the ICG is a range of typ. ±2% (±3% max.) at nominal conditions (filtered (100nF) and stabilized (4.7uF) V_{DD} = 5V, $T_{Ambient}$~25°C) and will vary over temperature and voltage (VDD) as indicated in the 68HC908EY16 datasheet.

To trim the ICG this values has to be copied to the ICG Trim Register ICGTR at address $38 of the MCU.

Important The value has to be copied after every reset.

TYPICAL APPLICATIONS

DEVELOPMENT SUPPORT

As the 908E626 has the MC68HC908EY16 MCU embedded typically all the development tools available for the MCU also apply for this device, however due to the fact of the additional analog die circuitry and the nominal +12V supply voltage some additional items have to be considered:

- nominal 12V rather than 5V or 3V supply
- high voltage V_{TST} might be applied not only to $\overline{IRQ}$ pin, but $\overline{IRQ\_A}$ pin

For a detailed information on the MCU related development support see the MC68HC908EY16 datasheet - section development support.

The programming is principally possible at two stages in the manufacturing process - first on chip level, before the IC is soldered onto a pcb board and second after the IC is soldered onto the pcb board.

Chip level programming

On Chip level the easiest way is to only power the MCU with +5V (see Figure 16) and not to provide the analog chip with VSUP, in this setup all the analog pin should be left open (e.g. VSUP[1:3]) and interconnections between MCU and analog die have to be separated (e.g. $\overline{IRQ}$ - $\overline{IRQ\_A}$).

This mode is well described in the MC68HC908EY16 datasheet - section development support.

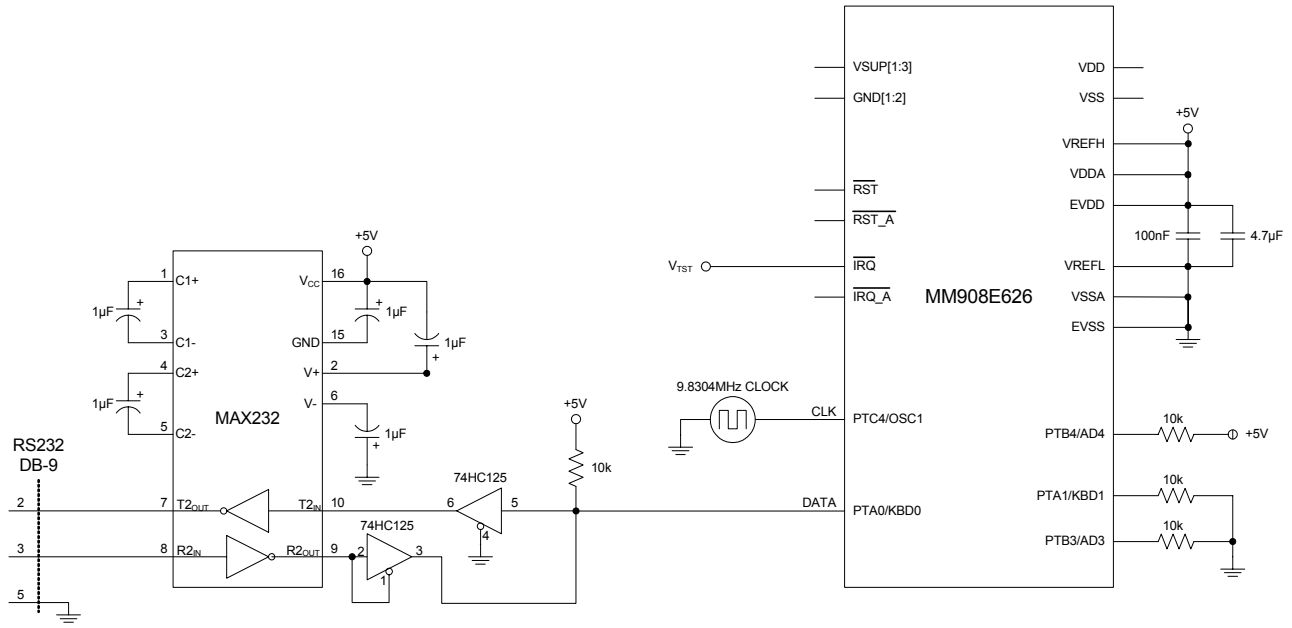


Figure 16. Normal Monitor Mode Circuit (MCU only)

Of course its also possible to supply the whole system with V_{SUP} (12V) instead as described in Figure 17, page 34.

PCB level programming

If the IC is soldered onto the pcb board its typically not possible to separately power the MCU with +5V, the whole system has to be powered up providing V_{SUP} (see Figure 17).

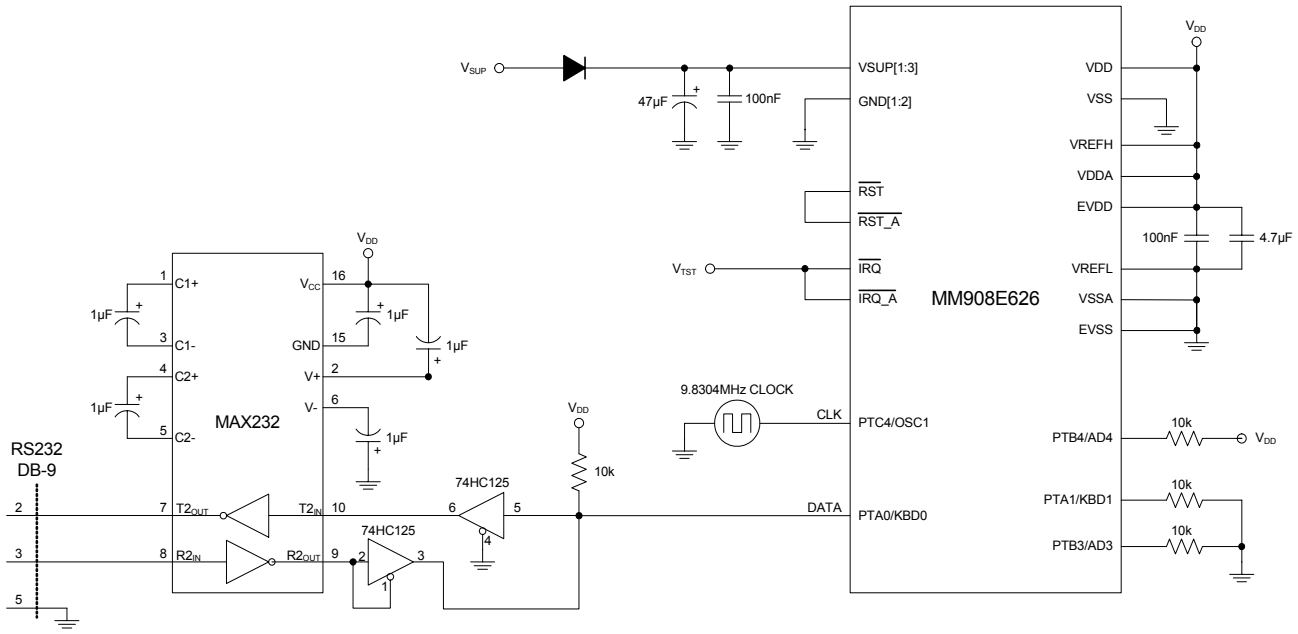


Figure 17. Normal Monitor Mode Circuit

Table 10 summarizes the possible configurations and the necessary setups.

Table 10. Monitor Mode Signal Requirements and Options

Mode	IRQ	RST	Reset Vector	Serial Communication		Mode Selection		ICG	COP	Normal Request Timeout	Communication Speed		
				PTA0	PTA1	PTB3	PTB4				External Clock	Bus Frequency	Baud Rate
Normal Monitor	V_{TST}	V_{DD}	X	1	0	0	1	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
Forced Monitor	V_{DD}	V_{DD}	$FFFF (blank)	1	0	X	X	OFF	disabled	disabled	9.8304 MHz	2.4576 MHz	9600
	GND							ON	disabled	disabled	—	Nominal 1.6MHz	Nominal 6300
User	V_{DD}	V_{DD}	not $FFFF (not blank)	X	X	X	X	ON	enabled	enabled	—	Nominal 1.6MHz	Nominal 6300

Notes

1. PTA0 must have a pull-up resistor to V_{DD} in monitor mode
2. External clock is a 4.9152MHz, 9.8304MHz or 19.6608MHz canned oscillator on OCS1
3. Communication speed with external clock is depending on external clock value. Baud rate is bus frequency / 256
4. X = don't care
5. V_{TST} is a high voltage $V_{DD} + 3.5V \leq V_{TST} \leq V_{DD} + 4.5V$

EMC/EMI RECOMMENDATIONS

This paragraph gives some device specific recommendations to improve EMC/EMI performance. Further generic design recommendations can be e.g. found on the Freescale web site www.freescale.com.

VSUP pins (VSUP1:VSUP3)

Its recommended to place a high quality ceramic decoupling capacitor close to the VSUP pins to improve EMC/EMI behavior.

LIN pin

For DPI (Direct Power Injection) and ESD (Electrostatic Discharge) its recommended to place a high quality ceramic decoupling capacitor near the LIN pin. An additional varistor will further increase the immunity against ESD. A ferrite in the LIN line will suppress some of the noise induced.

Voltage regulator output pins (VDD and AGND)

Use a high quality ceramic decoupling capacitor to stabilize the regulated voltage.

MCU digital supply pins (EVDD and EVSS)

Fast signal transitions on MCU pins place high, short duration current demands on the power supply. To prevent noise problems, take special care to provide power supply bypassing at the MCU. It is recommended that a high quality ceramic decoupling capacitor be placed between these pins.

MCU analog supply pins (VREFH, VDDA and VREFL, VSSA)

To avoid noise on the analog supply pins its important to take special care on the layout. The MCU digital and analog supplies should be tied to the same potential via separate traces and connected to the voltage regulator output.

Figure 18 and Figure 19 show the recommendations on schematics and layout level and Table 11 indicates recommended external components and layout considerations.

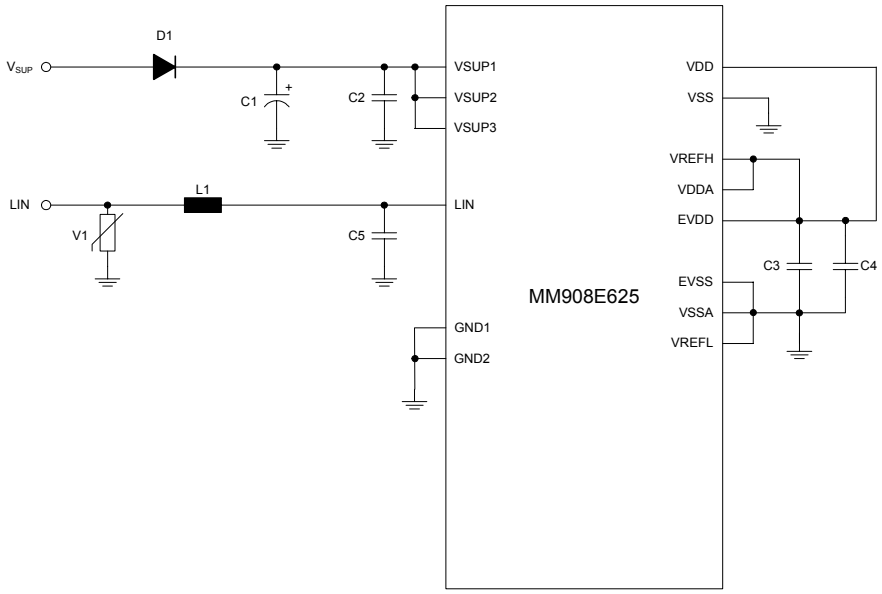


Figure 18. EMC/EMI Recommendations

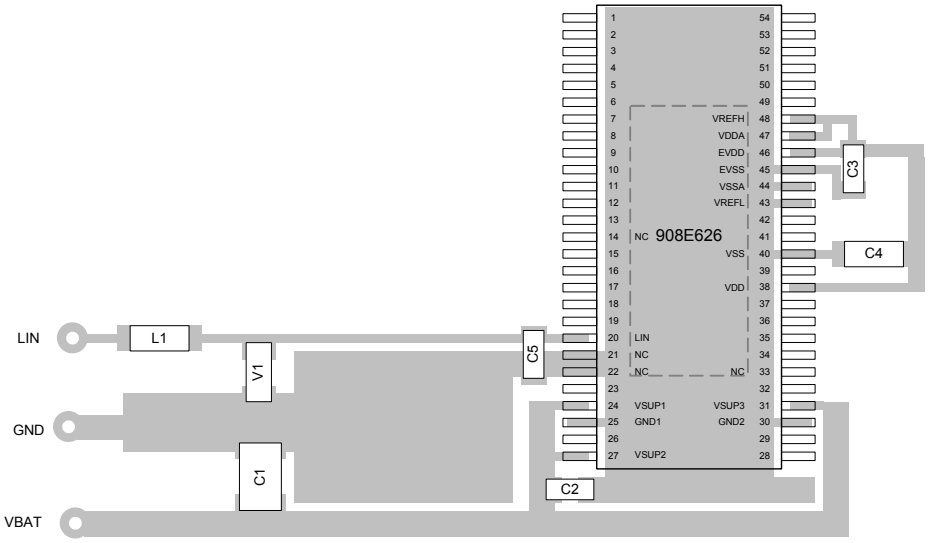


Figure 19. PCB Layout Recommendations

Table 11. Component Value Recommendation

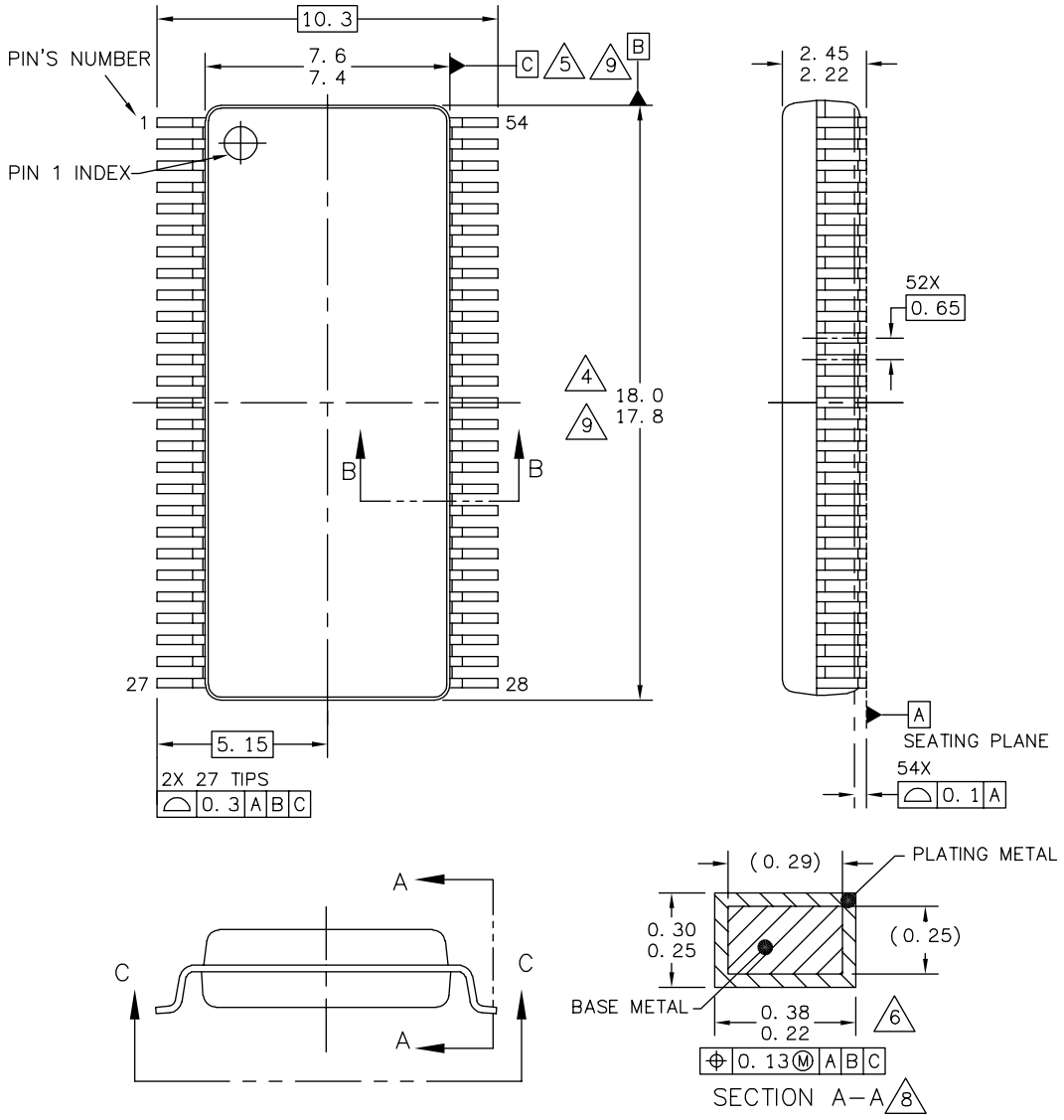
Component	Recommended Value[1]	Comments / Signal routing
C1	Bulk Capacitor	
C2	100nF, SMD Ceramic, Low ESR	Close (<5mm) to VSUP1, VSUP2 pins with good ground return
C3	100nF, SMD Ceramic, Low ESR	Close (<3mm) to digital supply pins (EVDD, EVSS) with good ground return. The positive analog (VREFH, VDDA) and the digital (EVDD) supply should be connected right at the C3.
C4	4,7uF, SMD Ceramic, Low ESR	Bulk Capacitor
C5	180pF, SMD Ceramic, Low ESR	Close (<5mm) to LIN pin. Total Capacitance on LIN has to be below 220pF. (C_{total} = $C_{LIN-Pin}$ + C5 + $C_{Varistor}$ ~ 10pF + 180pF + 15pF)
V1[2]	Varistor Type TDK AVR-M1608C270MBAAB	Optional (close to LIN connector)
L1[2]	SMD Ferrite Bead Type TDK MMZ2012Y202B	Optional, (close to LIN connector)

Notes
1. Freescale does not assume liability, endorse, or want components from external manufactures that are referenced in circuit drawings or tables. While Freescale offers component recommendations in this configuration, it is the customer's responsibility to validate their application.
2. Components are recommended to improve EMC and ESD performance.

PACKAGING

PACKAGING DIMENSIONS

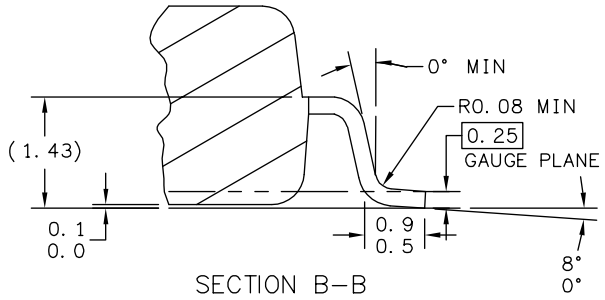
Important: For the most current revision of the package, visit www.freescale.com and perform a keyword search on 98ARL10519D.



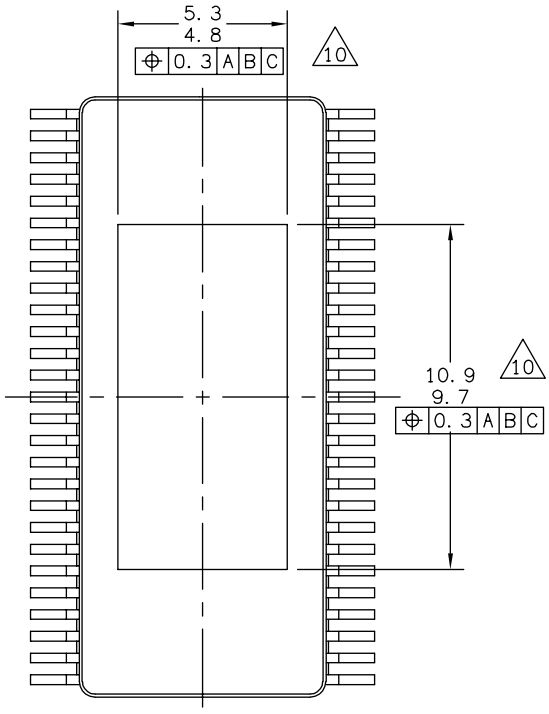
© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE
TITLE: 54LD SOIC W/B, 0.65 PITCH 5.1 X 10.3 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ARL10519D	REV: D
	CASE NUMBER: 1400–03	02 MAY 2008
	STANDARD: NON–JEDEC	

DWB SUFFIX
EK SUFFIX (PB-FREE)
54-PIN
98ARL10519D
ISSUE D

908E626



SECTION B–B



VIEW C–C

© FREESCALE SEMICONDUCTOR, INC. ALL RIGHTS RESERVED.	**MECHANICAL OUTLINE**	PRINT VERSION NOT TO SCALE	
TITLE: 54LD SOIC W/B, 0.65 PITCH 5.1 X 10.3 EXPOSED PAD, CASE–OUTLINE	DOCUMENT NO: 98ARL10519D		REV: D
	CASE NUMBER: 1400–03		02 MAY 2008
	STANDARD: NON–JEDEC		

DWB SUFFIX
EK SUFFIX (PB-FREE)
54-PIN
98ARL10519D
ISSUE D

908E626

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.
3. DATUMS B AND C TO BE DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
4. THIS DIMENSION DOES NOT INCLUDE MOLD FLASH, PROTRUSION OR GATE BURRS. MOLD FLASH, PROTRUSION OR GATE BURRS SHALL NOT EXCEED 0.15 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
5. THIS DIMENSION DOES NOT INCLUDE INTER–LEAD FLASH OR PROTRUSIONS. INTER–LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25 MM PER SIDE. THIS DIMENSION IS DETERMINED AT THE PLANE WHERE THE BOTTOM OF THE LEADS EXIT THE PLASTIC BODY.
6. THIS DIMENSION DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL NOT CAUSE THE LEAD WIDTH TO EXCEED 0.46 mm. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSION AND ADJACENT LEAD SHALL NOT BE LESS THAN 0.07 mm.
7. EXACT SHAPE OF EACH CORNER IS OPTIONAL.
8. THESE DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.1 mm AND 0.3 mm FROM THE LEAD TIP.
9. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. THIS DIMENSION IS DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTER–LEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
10. THESE DIMENSIONS RANGES DEFINE THE PRIMARY KEEP–OUT AREA. MOLD LOCKING AND RESIN BLEED CONTROL FEATURES MAY BE VISIBLE AND THEY MAY EXTEND TO 0.4mm FROM MAXIMUM EXPOSED PAD SIZE

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE:	DOCUMENT NO: 98ARL10519D	REV: D
54LD SOIC W/B, 0.65 PITCH 5.1 X 10.3 EXPOSED PAD, CASE–OUTLINE	CASE NUMBER: 1400–03	02 MAY 2008
	STANDARD: NON–JEDEC	

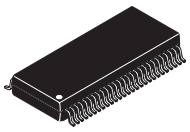
DWB SUFFIX
EK SUFFIX (PB-FREE)
54-PIN
98ARL10519D
ISSUE D

ADDITIONAL DOCUMENTATION

THERMAL ADDENDUM (REV 1.0)

908E626

54-PIN
SOICW-EP



DWB SUFFIX
98ARL10519D
54-PIN SOICW-EP

Note For package dimensions, refer to the 908E626 device datasheet.

Introduction

This thermal addendum ia provided as a supplement to the MM908E626 technical data sheet. The addendum provides thermal performance information that may be critical in the design and development of system applications. All electrical, application and packaging information is provided in the data sheet.

Package and Thermal Considerations

This MM908E626 is a dual die package. There are two heat sources in the package independently heating with P_1 and P_2. This results in two junction temperatures, T_{J1} and T_{J2}, and a thermal resistance matrix with $R_{\theta JAmn}$.

For *m*, *n* = 1, $R_{\theta JA11}$ is the thermal resistance from Junction 1 to the reference temperature while only heat source 1 is heating with P_1.

For *m* = 1, *n* = 2, $R_{\theta JA12}$ is the thermal resistance from Junction 1 to the reference temperature while heat source 2 is heating with P_2. This applies to $R_{\theta J21}$ and $R_{\theta J22}$, respectively.

$$\begin{Bmatrix} T_{J1} \\ T_{J2} \end{Bmatrix} = \begin{bmatrix} R_{\theta JA11} & R_{\theta JA12} \\ R_{\theta JA21} & R_{\theta JA22} \end{bmatrix} \cdot \begin{Bmatrix} P_1 \\ P_2 \end{Bmatrix}$$

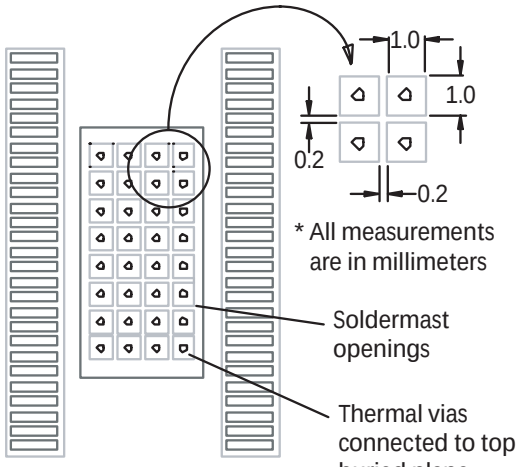
The stated values are solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment. Stated values were obtained by measurement and simulation according to the standards listed below.

Standards

Table 12. Thermal Performance Comparison

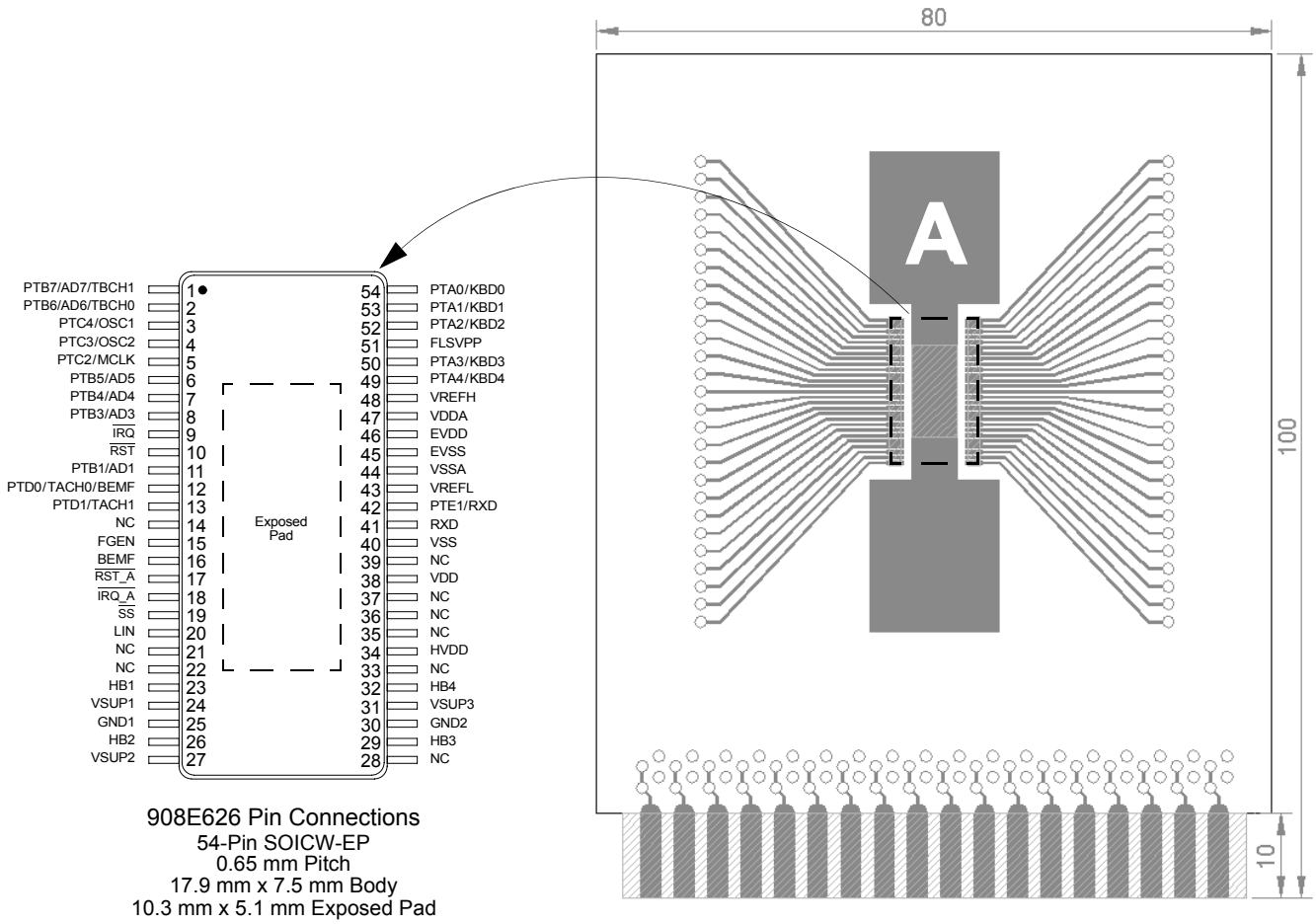
Thermal Resistance	1 = Power Chip, 2 = Logic Chip [°C/W]		
	m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$ (1)(2)	23	20	24
$R_{\theta JBmn}$ (2)(3)	9.0	6.0	10
$R_{\theta JAmn}$ (1)(4)	52	47	52
$R_{\theta JCmn}$ (5)	1.0	0	2.0

Notes:
1. Per JEDEC JESD51-2 at natural convection, still air condition.
2. 2s2p thermal test board per JEDEC JESD51-7and JESD51-5.
3. Per JEDEC JESD51-8, with the board temperature on the center trace near the power outputs.
4. Single layer thermal test board per JEDEC JESD51-3 and JESD51-5.
5. Thermal resistance between the die junction and the exposed pad, “infinite” heat sink attached to exposed pad.



54 Terminal SOIC-EP
0.65 mm Pitch
17.9 mm x 7.5 mm Body
10.3 mm x 5.1 mm Exposed Pad

Figure 20. Thermal Land Pattern for Direct Thermal Attachment Per JEDEC JESD51-5Thermal Test Board



908E626 Pin Connections
54-Pin SOICW-EP
0.65 mm Pitch
17.9 mm x 7.5 mm Body
10.3 mm x 5.1 mm Exposed Pad

Figure 21. Thermal Test Board

Device on Thermal Test Board

Material:	Single layer printed circuit board FR4, 1.6 mm thickness Cu traces, 0.07 mm thickness
Outline:	80 mm x 100 mm board area, including edge connector for thermal testing
Area **A**:	Cu heat-spreading areas on board surface
Ambient Conditions:	Natural convection, still air

Table 13. Thermal Resistance Performance

Thermal Resistance	Area A (mm^2)	1 = Power Chip, 2 = Logic Chip (°C/W)		
		m **= 1,** ***n*** **= 1**	***m*** **= 1,** ***n*** **= 2** ***m*** **= 2,** ***n*** **= 1**	***m*** **= 2,** ***n*** **= 2**
$R_{\theta JAmn}$	0	53	48	53
	300	39	34	38
	600	35	30	34
$R_{\theta JSmn}$	0	21	16	20
	300	15	11	15
	600	14	9.0	13

$R_{\theta JA}$ is the thermal resistance between die junction and ambient air.

$R_{\theta JSmn}$ is the thermal resistance between die junction and the reference location on the board surface near a center lead of the package.

This device is a dual die package. Index *m* indicates the die that is heated. Index *n* refers to the number of the die where the junction temperature is sensed.

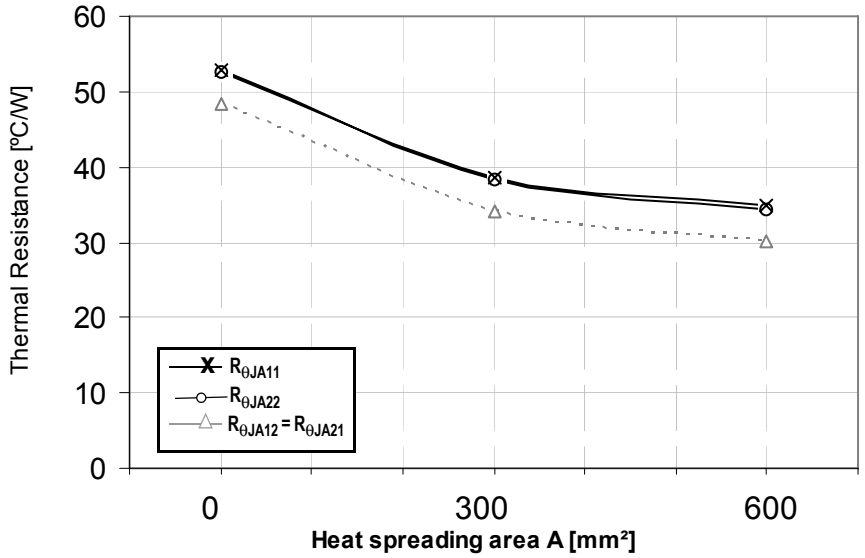


Figure 22. Device on Thermal Test Board $R_{\theta JA}$

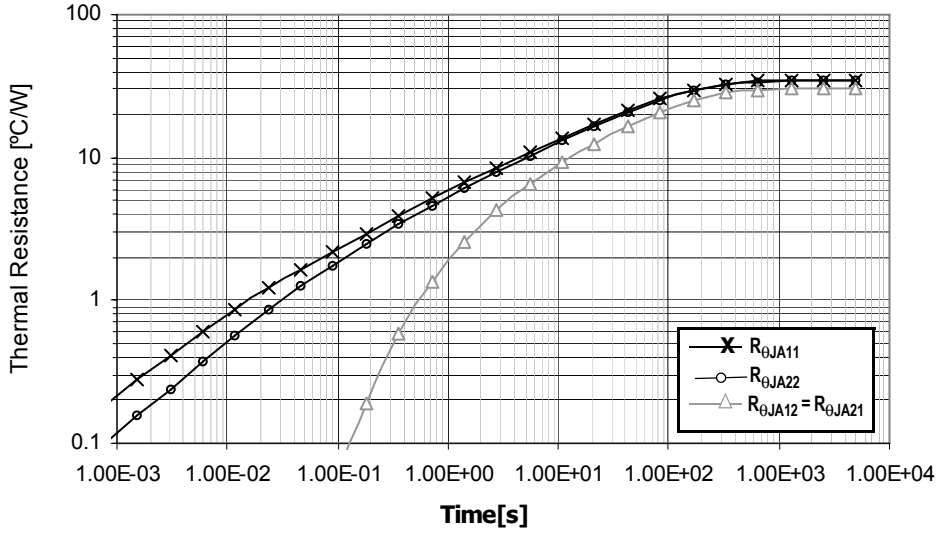


Figure 23. Transient Thermal Resistance $R_{\theta JA}$ (1.0W Step Response)
Device on Thermal Test Board Area A = 600 (mm^2)

REVISION HISTORY

	DATE	DESCRIPTION OF CHANGES
4.0	9/2008	• Implemented Revision History page • Minor corrections throughout the document • Updated to current Freescale format and style • Added MM908E626AVEK to the ordering information • Corrected package drawing designation • Added STOP mode
	7/2009	• Corrected several non-technical cross-references.

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Japan:
Freescale Semiconductor Japan Ltd.
Headquarters
ARCO Tower 15F
1-8-1, Shimo-Meguro, Meguro-ku,
Tokyo 153-0064
Japan
0120 191014 or +81 3 5437 9125
support.japan@freescale.com

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MM908E626
Rev. 5.0
7/2009