FUJITSU MICROELECTRONICS
DATA SHEET

DS07-16617-2E

32-bit Microcontroller

CMOS

FR60 MB91460S Series

MB91F467SA

■ DESCRIPTION

MB91460S series is a line of general-purpose 32-bit RISC microcontrollers designed for embedded control applications which require high-speed real-time processing, such as consumer devices and on-board vehicle systems. This series uses the FR60 CPU, which is compatible with the FR family* of CPUs.

This series contains the LIN-USART, CAN and APIX^{fi} controllers.

* : FR, the abbreviation of FUJITSU RISC controller, is a line of products of FUJITSU Microelectronics Limited.

■ FEATURES

1. FR60 CPU core

32-bit RISC, load/store architecture, five-stage pipeline
16-bit fixed-length instructions (basic instructions)
Instruction execution speed: 1 instruction per cycle
Instructions including memory-to-memory transfer, bit manipulation, and barrel shift instructions: Instructions suitable for embedded applications
Function entry/exit instructions and register data multi-load store instructions : Instructions supporting C language
Register interlock function: Facilitating assembly-language coding
Built-in multiplier with instruction-level support
Signed 32-bit multiplication: 5 cycles
Signed 16-bit multiplication: 3 cycles
Interrupts (save PC/PS) : 6 cycles (16 priority levels)
Harvard architecture enabling program access and data access to be performed simultaneously
Instructions compatible with the FR family

For the information for microcontroller supports, see the following web site.
This web site includes the **"Customer Design Review Supplement"** which provides the latest cautions on system development and the minimal requirements to be checked to prevent problems before the system development.

http://edevice.fujitsu.com/micom/en-support/

Copyright' 2009 FUJITSU MICROELECTRONICS LIMITED All rights reserved
2009.9

2. Internal peripheral resources

General-purpose ports : Maximum 133 ports
DMAC (DMA Controller)
Maximum of 5 channels able to operate simultaneously.
2 transfer sources (internal peripheral/software)
Activation source can be selected using software.
Addressing mode specifies full 32-bit addresses (increment/decrement/fixed)
Transfer mode (demand transfer/burst transfer/step transfer/block transfer)
Transfer data size selectable from 8/16/32-bit
Multi-byte transfer enabled (by software)
DMAC descriptor in I/O areas (200_H to 240_H, 1000_H to 1024_H)
A/D converter (successive approximation type)
10-bit resolution: 16 channels
Conversion time: minimum 1 µs
External interrupt inputs : 16 channels
Shares the CAN RX pin and I^2C SDA pin
Bit search module (for REALOS)
Function to search from the MSB (most significant bit) for the position of the first "0", "1", or changed bit in a word
LIN-USART (full duplex double buffer): 6 channels
Clock synchronous/asynchronous selectable
Sync-break detection
Internal dedicated baud rate generator
I^2C bus interface (supports 400 kbps): 3 channels
Master/slave transmission and reception
Arbitration function, clock synchronization function
CAN controller (C-CAN): 2 channels
Maximum transfer speed: 1 Mbps
32 transmission/reception message buffers
APIX^{fi} controller
APIX^{fi} link (105Mbit / 6Mbit): 1 channel
Automotive Interconnect links (5Mbit / 6Mbit): 2 links
Sound generator : 1 channel
Tone frequency : PWM frequency divide-by-two (reload value + 1)
Alarm comparator : 1 channel
Monitor external voltage
Generate an interrupt in case of voltage lower/higher than the defined thresholds (reference voltage)
16-bit PPG timer : 16 channels
16-bit PFM timer : 1 channel
16-bit reload timer: 8 channels
16-bit free-run timer: 8 channels (1 channel each for ICU and OCU)
Input capture: 8 channels (operates in conjunction with the free-run timer)
Output compare: 4 channels (operates in conjunction with the free-run timer)
Up/Down counter: 4 channels (4×8-bit or 2×16 bit)
Watchdog timer
Real-time clock
Low-power consumption modes : Sleep/stop mode function
Low voltage detection circuit
Clock monitor

Clock supervisor
Monitors the sub-clock (32 kHz) and the main clock (4 MHz) , and switches to a recovery clock (CR oscillator, etc.) when the oscillations stop.
Clock modulator *
Sub-clock calibration
Corrects the real-time clock timer when operating with the 32 kHz or CR oscillator
Main oscillator stabilization timer
Generates an interrupt in sub-clock mode after the stabilization wait time has elapsed on the 23-bit stabilization wait time counter
Sub-oscillator stabilization timer
Generates an interrupt in main clock mode after the stabilization wait time has elapsed on the 15-bit stabilization wait time counter

3. Package and technology

Package : LQFP-176
CMOS 0.18 µm technology
Power supply range 3 V to 5 V (1.8 V internal logic provided by a step-down voltage converter)
Operating temperature range: between Š40°C and + 105°C

* : The clock modulator is currently being evaluated and should not be used for other purpose than testing.

Note APIX^{fi} is a registered mark of INOVA Semiconductors GmbH

■ PRODUCT LINEUP

Feature	MB91V460A	MB91F467SA
Max. core frequency (CLKB)	80MHz	100MHz
Max. resource frequency (CLKP)	40MHz	50MHz
Max. external bus freq. (CLKT)	40MHz	50MHz
Max. CAN frequency (CLKCAN)	20MHz	40MHz
Max. FlexRay frequency (SCLK)	-	-
Technology	0.35µm	0.18µm
Watchdog	yes	yes
Watchdog (RC osc. based)	yes (disengageable)	yes
Bit Search	yes	yes
Reset input (INITX)	yes	yes
Hardware Standby input (HSTX)	yes	no
Clock Modulator	yes	yes
Clock Monitor	yes	yes
Low Power Mode	yes	yes
DMA	5 ch	5 ch
MAC (µDSP)	no	no
MMU/MPU	MPU (16 ch) [1)]	MPU (8 ch) [1)]
Flash	Emulation SRAM 32bit read data	1088 KByte
Satellite Flash	-	no
Flash Protection	-	yes
D-RAM	64 KByte	32 KByte
ID-RAM	64 KByte	32 KByte
Flash-Cache (Instruction cache)	16 KByte	8 KByte
Boot-ROM / BI-ROM	4 KByte fixed	4 KByte
RTC	1 ch	1 ch
Free Running Timer	8 ch	8 ch
ICU	8 ch	8 ch
OCU	8 ch	4 ch
Reload Timer	8 ch	8 ch
PPG 16-bit	16 ch	16 ch
PFM 16-bit	1 ch	1 ch
Sound Generator	1 ch	1 ch
Up/Down Counter (8/16-bit)	4 ch (8-bit) / 2 ch (16-bit)	4 ch (8-bit) / 2 ch (16-bit)

(Continued)

(Continued)

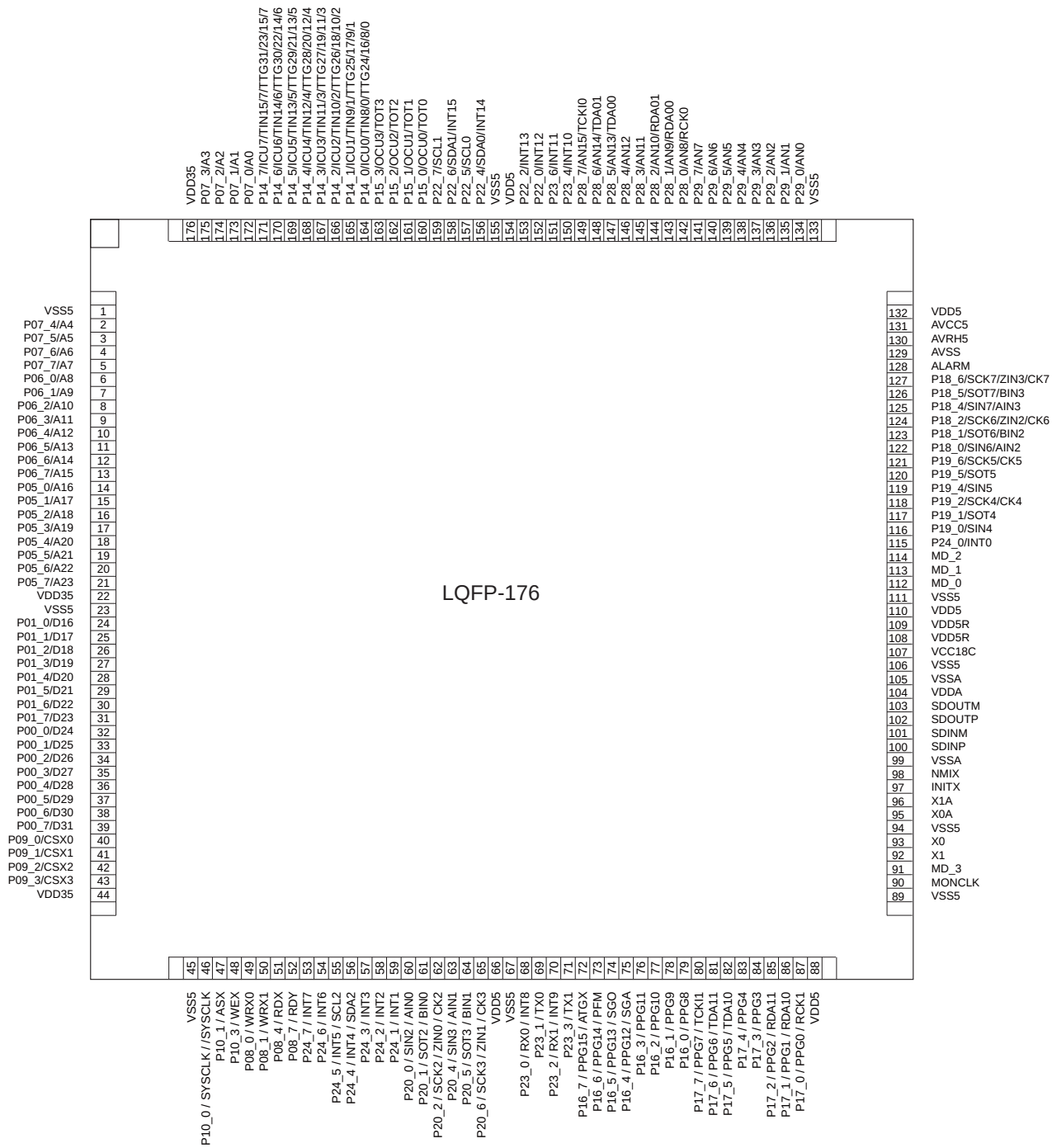
Feature	MB91V460A	MB91F467SA
C_CAN	6 ch (128msg)	2 ch (32msg)
LIN-USART	4 ch + 4 ch FIFO + 8 ch	2 ch + 4 ch FIFO
I²C (400k)	4 ch	3 ch
APIX[fi]	-	2ch (1ch physical)
FR external bus	yes (32bit addr, 32bit data)	yes (24bit addr, 16bit data)
External Interrupts	16 ch	16 ch
NMI Interrupts	1 ch	1 ch
SMC	6 ch	-
LCD controller (40x4)	1 ch	-
ADC (10 bit)	32 ch	16 ch
Alarm Comparator	2 ch	1 ch
Supply Supervisor	yes	yes
Clock Supervisor	yes	yes
Main clock oscillator	4MHz	4MHz
Sub clock oscillator	32kHz	32kHz
RC Oscillator	100kHz	100kHz / 2MHz
PLL	x 20	x 25
DSU4	yes	-
EDSU	yes (32 BP) *1	yes (16 BP) *1
Supply Voltage	3V / 5V	3V / 5V
Regulator	yes	yes
Power Consumption	n.a.	< 1 W
Temperature Range (Ta)	0..70 C	-40..105 C
Package	BGA660	LQFP176
Power on to PLL run	< 20 ms	< 20 ms
Flash Download Time	n.a.	< 30 sec (2M)

*1 : MPU channels use EDSU breakpoint registers (shared operation between MPU and EDSU).

■ PIN ASSIGNMENT

1. MB91F467SA

(TOP VIEW)



(FPT-176P-M07)

Pin no.	Pin name	I/O	I/O circuit type*	Function
56	P24_4	I/O	C	General-purpose input/output port
	INT4			External interrupt input pin
	SDA2			I^2C bus DATA input/output pin
57	P24_3	I/O	A	General-purpose input/output port
	INT3			External interrupt input pin
58	P24_2	I/O	A	General-purpose input/output port
	INT2			External interrupt input pin
59	P24_1	I/O	A	General-purpose input/output port
	INT1			External interrupt input pin
60	P20_0	I/O	A	General-purpose input/output port
	SIN2			Data input pin of USART2
	AIN0			Up/down counter input pin
61	P20_1	I/O	A	General-purpose input/output port
	SOT2			Data output pin of USART2
	BIN0			Up/down counter input pin
62	P20_2	I/O	A	General-purpose input/output port
	SCK2			Clock input/output pin of USART2
	ZIN0			Up/down counter input pin
	CK2			External clock input pin of free-run timer 2
63	P20_4	I/O	A	General-purpose input/output port
	SIN3			Data input pin of USART3
	AIN1			Up/down counter input pin
64	P20_5	I/O	A	General-purpose input/output port
	SOT3			Data output pin of USART3
	BIN1			Up/down counter input pin
65	P20_6	I/O	A	General-purpose input/output port
	SCK3			Clock input/output pin of USART3
	ZIN1			Up/down counter input pin
	CK3			External clock input pin of free-run timer 3
68	P23_0	I/O	A	General-purpose input/output port
	RX0			RX input/output pin of CAN0
	INT8			External interrupt input pin
69	P23_1	I/O	A	General-purpose input/output port
	TX0			TX output pin of CAN0

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
82	P17_5	I/O	A	General-purpose input/output port
	PPG5			Output pin of PPG timer
	TDA10			AIC downlink data of Apix^{fi} link1
83	P17_4	I/O	A	General-purpose input/output port
	PPG4			Output pin of PPG timer
84	P17_3	I/O	A	General-purpose input/output port
	PPG3			Output pin of PPG timer
85	P17_2	I/O	A	General-purpose input/output port
	PPG2			Output pin of PPG timer
	RDA11			AIC uplink data of Apix^{fi} link1
86	P17_1	I/O	A	General-purpose input/output port
	PPG1			Output pin of PPG timer
	RDA10			AIC uplink data of Apix^{fi} link1
87	P17_0	I/O	A	General-purpose input/output port
	PPG0			Output pin of PPG timer
	RCK1			AIC uplink clock of Apix^{fi} link1
90	MONCLK	O	M	Clock monitor pin
91	MD_3	I	G00	Fast clock input pin
92	X1		J1	Clock (oscillation) output
93	X0		J1	Clock (oscillation) input
95	X0A		J2	Sub clock (oscillation) input
96	X1A		J2	Sub clock (oscillation) output
97	INITX	I	H	External reset input pin
98	NMIX	I	H	Non-maskable interrupt input pin
100	SDINP		N1	Apix^{fi} uplink
101	SDINM		N1	Apix^{fi} uplink
102	SDOUTP		N2	Apix^{fi} downlink
103	SDOUTM		N2	Apix^{fi} downlink
112 to 114	MD_0 to MD_2	I	G01	Mode setting pins
115	P24_0	I/O	A	General-purpose input/output port
	INT0			External interrupt input pin

(Continued)

Pin no.	Pin name	I/O	I/O circuit type*	Function
116	P19_0	I/O	A	General-purpose input/output port
	SIN4			Data input pin of USART4
117	P19_1	I/O	A	General-purpose input/output port
	SOT4			Data output pin of USART4
118	P19_2	I/O	A	General-purpose input/output port
	SCK4			Clock input/output pin of USART4
	CK4			External clock input pin of free-run timer 4
119	P19_4	I/O	A	General-purpose input/output port
	SIN5			Data input pin of USART5
120	P19_5	I/O	A	General-purpose input/output port
	SOT5			Data output pin of USART5
121	P19_6	I/O	A	General-purpose input/output port
	SCK5			Clock input/output pin of USART5
	CK5			External clock input pin of free-run timer 5
122	P18_0	I/O	A	General-purpose input/output port
	SIN6			Data input pin of USART6
	AIN2			Up/down counter input pin
123	P18_1	I/O	A	General-purpose input/output port
	SOT6			Data output pin of USART6
	BIN2			Up/down counter input pin
124	P18_2	I/O	A	General-purpose input/output port
	SCK6			Clock input/output pin of USART6
	ZIN2			Up/down counter input pin
	CK6			External clock input pin of free-run timer 6
125	P18_4	I/O	A	General-purpose input/output port
	SIN7			Data input pin of USART7
	AIN3			Up/down counter input pin
126	P18_5	I/O	A	General-purpose input/output port
	SOT7			Data output pin of USART7
	BIN3			Up/down counter input pin

(Continued)

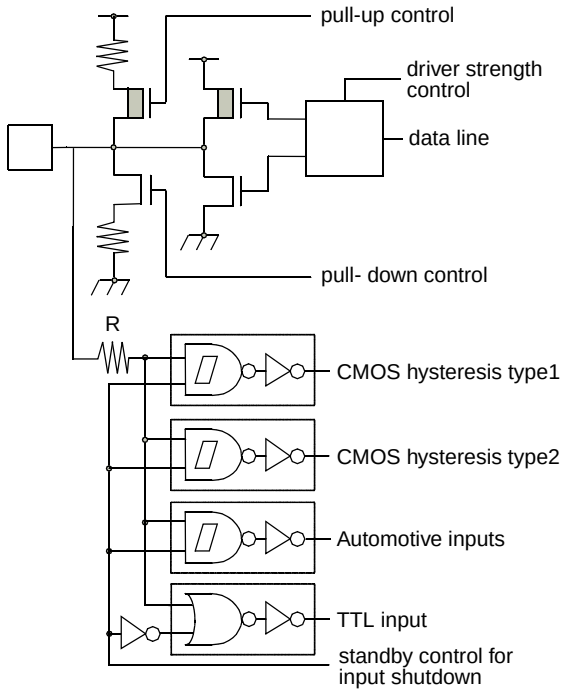
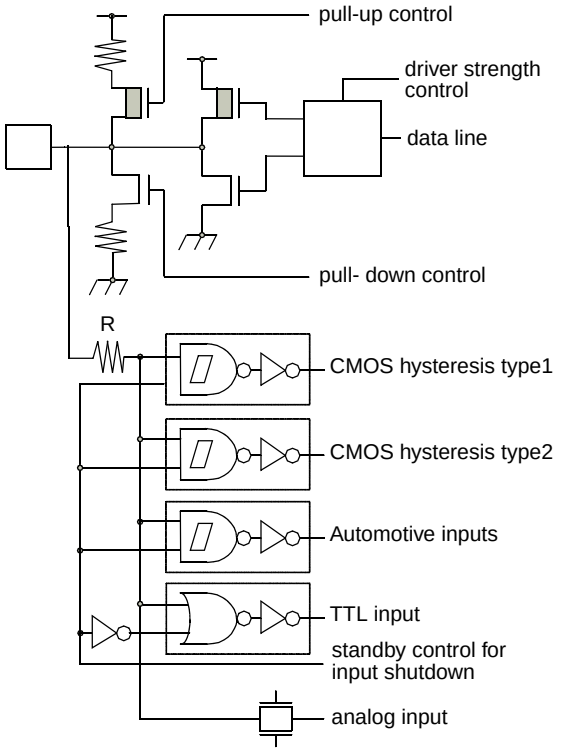
(Continued)

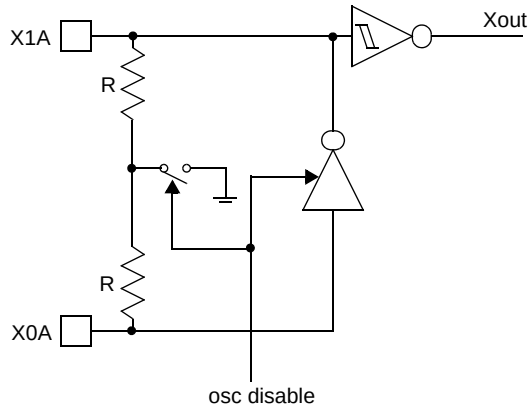
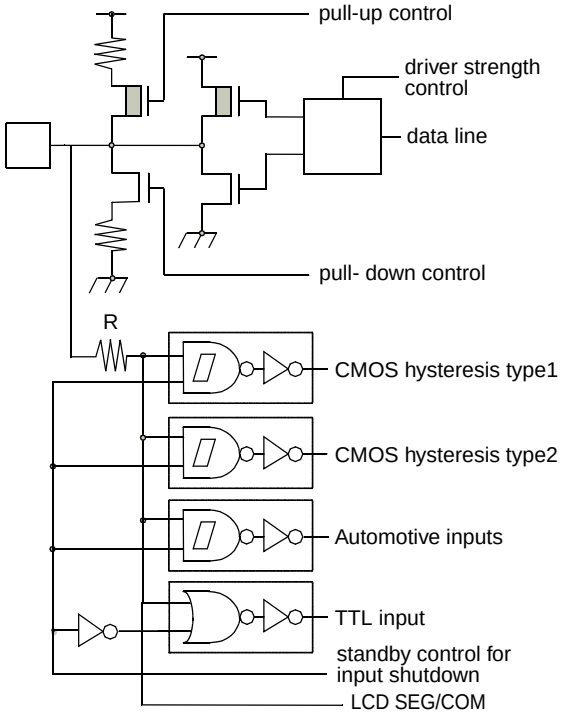
Pin no.	Pin name	I/O	I/O circuit type*	Function
151	P23_6	I/O	A	General-purpose input/output port
	INT11			External interrupt input pin
152	P22_0	I/O	A	General-purpose input/output port
	INT12			External interrupt input pin
153	P22_2	I/O	A	General-purpose input/output port
	INT13			External interrupt input pin
156	P22_4	I/O	C	General-purpose input/output port
	SDA0			I^2C bus data input/output pin
	INT14			External interrupt input pin
157	P22_5	I/O	C	General-purpose input/output port
	SCL0			I^2C bus clock input/output pin
158	P22_6	I/O	C	General-purpose input/output port
	SDA1			I^2C bus data input/output pin
	INT15			External interrupt input pin
159	P22_7	I/O	C	General-purpose input/output port
	SCL1			I^2C bus clock input/output pin
160 to 163	P15_0 to P15_3	I/O	A	General-purpose input/output ports
	OCU0 to OCU3			Output compare output pins
	TOT0 to TOT3			Reload timer output pins
164 to 171	P14_0 to P14_7	I/O	A	General-purpose input/output ports
	ICU0 to ICU7			Input capture input pins
	TIN8/0 to TIN 15/7			External trigger input pins of reload timer
	TTG24/16/8/0 to TTG31/23/15/7			External trigger input pins of PPG timer
172 to 175	P07_0 to P07_3	I/O	A	General-purpose input/output ports
	A0 to A3			Signal pins of external address bus (bit0 to bit3)

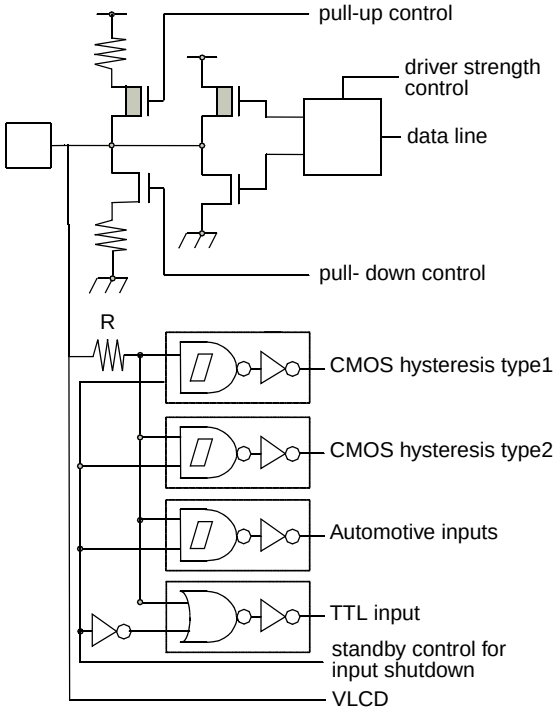
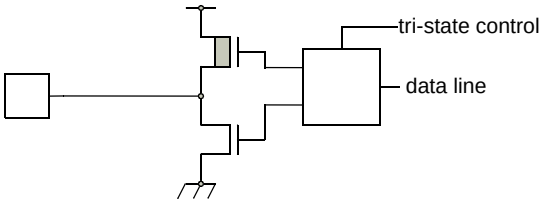
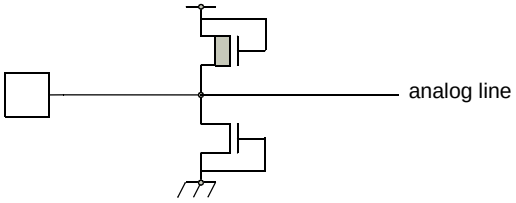
[Power supply/Ground pins]

Pin no.	Pin name	I/O	Function
1, 23, 45, 67, 89, 94, 106, 111, 133, 155	VSS5	Supply	Ground pins
66, 88, 110, 132, 154	VDD5		Power supply pins
108, 109	VDD5R		Power supply pins for internal regulator
129	AVSS		Analog ground pin for A/D converter
131	AVCC5		Power supply pin for A/D converter
130	AVRH5		Reference power supply pin for A/D converter
107	VCC18C		Capacitor connection pin for internal regulator
22, 44, 176	VDD35		Power supply pins for external bus part of I/O ring
99, 105	VSSA		Apix^{fi} ground supply pins
104	VDDA		Apix^{fi} power supply pin

* : For information about the I/O circuit type, refer to I/O CIRCUIT TYPES .

Type	Circuit	Remarks
E		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50k approx.
F		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA, and I_{OL} = 30mA, I_{OH} = -30mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50k approx. Analog input

Type	Circuit	Remarks
J2		Low-speed oscillation circuit: Feedback resistor = approx. 2 * 5 M . Feedback resistor is grounded in the center when the oscillator is disabled.
K		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function TTL input with input shutdown function Programmable pull-up resistor: 50k approx. LCD SEG/COM output

Type	Circuit	Remarks
L		CMOS level output (programmable I_{OL} = 5mA, I_{OH} = -5mA and I_{OL} = 2mA, I_{OH} = -2mA) 2 different CMOS hysteresis inputs with input shutdown function Automotive input with input shutdown function) TTL input with input shutdown function Programmable pull-up resistor: 50k approx. Analog input LCD Voltage input
M		CMOS level tri-state output (I_{OL} = 5mA, I_{OH} = -5mA)
N1/N2		Analog terminal Type N1: Analog input pin with protection Type N2: Analog output line with protection

■ HANDLING DEVICES

1. Preventing Latch-up

Latch-up may occur in a CMOS IC if a voltage higher than ($V_{DD}5$ or $V_{DD}35$) or less than ($V_{SS}5$) is applied to an input or output pin or if a voltage exceeding the rating is applied between the power supply pins and ground pins. If latch-up occurs, the power supply current increases rapidly, sometimes resulting in thermal breakdown of the device. Therefore, be very careful not to apply voltages in excess of the absolute maximum ratings.

2. Handling of unused input pins

If unused input pins are left open, abnormal operation may result. Any unused input pins should be connected to pull-up or pull-down resistor (2K to 10K) or enable internal pullup or pulldown resisters (PPER/PPCR) before the input enable (PORTEN) is activated by software. The mode pins MD_x can be connected to $V_{SS}5$ or $V_{DD}5$ directly. Unused ALARM input pins can be connected to AV_{SS} directly.

3. Power supply pins

In MB91460S series, devices including multiple power supply pins and ground pins are designed as follows; pins necessary to be at the same potential are interconnected internally to prevent malfunctions such as latch-up. All of the power supply pins and ground pins must be externally connected to the power supply and ground respectively in order to reduce unnecessary radiation, to prevent strobe signal malfunctions due to the ground level rising and to follow the total output current ratings. Furthermore, the power supply pins and ground pins of the MB91460S series must be connected to the current supply source via a low impedance.
It is also recommended to connect a ceramic capacitor of approximately 0.1 µF as a bypass capacitor between power supply pin and ground pin near this device.
This series has a built-in step-down regulator. Connect a bypass capacitor of 4.7 µF (use a X7R ceramic capacitor) to VCC18C pin for the regulator.

4. Crystal oscillator circuit

Noise in proximity to the X0 (X0A) and X1 (X1A) pins can cause the device to operate abnormally. Printed circuit boards should be designed so that the X0 (X0A) and X1 (X1A) pins, and crystal oscillator, as well as bypass capacitors connected to ground, are located near the device and ground.
It is recommended that the printed circuit board layout be designed such that the X0 and X1 pins or X0A and X1A pins are surrounded by ground plane for the stable operation.
Please request the oscillator manufacturer to evaluate the oscillational characteristics of the crystal and this device.

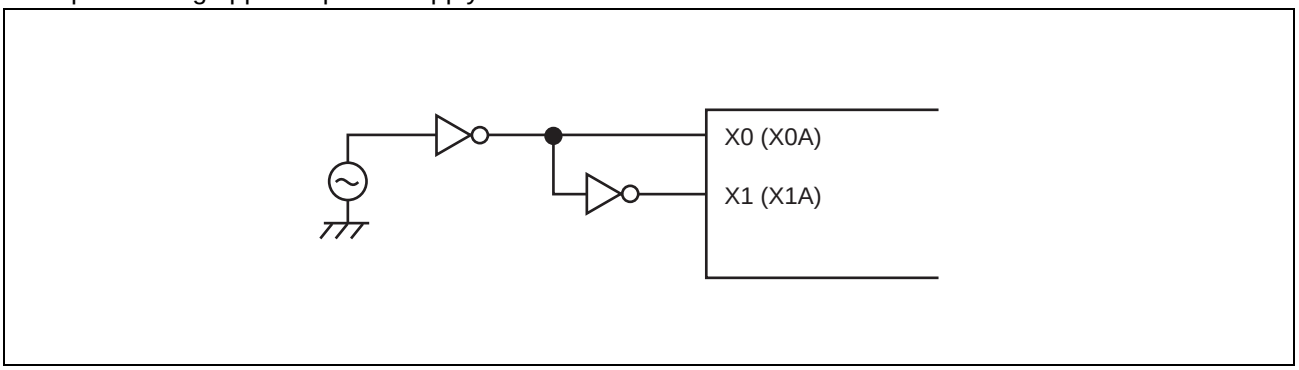
5. Notes on using external clock

5.1. Opposite phase clock supply

When using the external clock, it is possible to simultaneously supply the X0 (X0A) and the X1 (X1A) pins. In the described combination X0 (X0A) should be supplied with a clock signal which has the opposite phase to the X1 (X1A) pins. However, in this case the stop mode (oscillation stop mode) must not be used (This is because the X1 (X1A) pin stops at H output in STOP mode).

With opposite phase supply at X0 and X1, a frequency up to 16 MHz is possible.

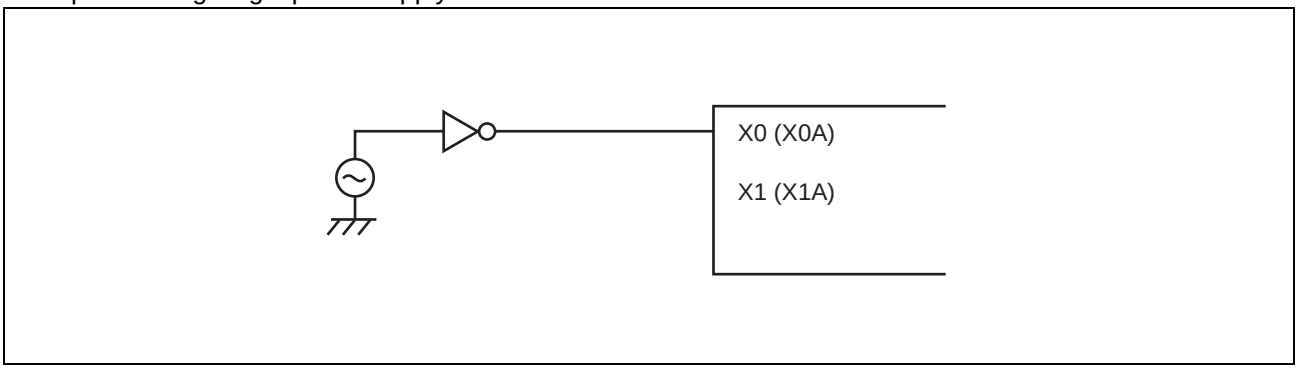
Example of using opposite phase supply



5.2. Single phase clock supply

For lower frequencies, up to 4 MHz, it is possible to supply a single phase clock at X0 (X0A).

Example of using single phase supply



6. Mode pins (MD_x)

These pins should be connected directly to the power supply or ground pins. To prevent the device from entering test mode accidentally due to noise, minimize the lengths of the patterns between each mode pin and power supply pin or ground pin on the printed circuit board as possible and connect them with low impedance.

MD_3 pin should be connected directly to ground.

7. Notes on operating in PLL clock mode

If the oscillator is disconnected or the clock input stops when the PLL clock is selected, the microcontroller may continue to operate at the free-running frequency of the self-oscillating circuit of the PLL. However, this self-running operation cannot be guaranteed.

8. Pull-up control

The AC standard is not guaranteed in case a pull-up resistor is connected to the pin serving as an external bus pin.

9. Notes on PS register

As the PS register is processed in advance by some instructions, when the debugger is being used, the exception handling may result in execution breaking in an interrupt handling routine or the displayed values of the flags in the PS register being updated.
As the microcontroller is designed to carry out reprocessing correctly upon returning from such an EIT event, the operation before and after the EIT always proceeds according to specification.

1) The following behavior may occur if any of the following occurs in the instruction immediately after a DIV0U/DIV0S instruction:
(a) a user interrupt or NMI is accepted; (b) single-step execution is performed; or (c) execution breaks due to a data event or from the emulator menu.

- D0 and D1 flags are updated in advance.
- An EIT handling routine (user interrupt/NMI or emulator) is executed.
- Upon returning from the EIT, the DIV0U/DIV0S instruction is executed and the D0 and D1 flags are updated to the same values as those in 1).

2) The following behavior occurs when an ORCCR, STILM, MOV Ri, PS instruction is executed to enable a user interrupt or NMI source while that interrupt is in the active state.

- The PS register is updated in advance.
- An EIT handling routine (user interrupt/NMI or emulator) is executed.
- Upon returning from the EIT, the above instructions are executed and the PS register is updated to the same value as in 1).

■ NOTES ON DEBUGGER

1. Execution of the RETI Command

If single-step execution is used in an environment where an interrupt occurs frequently, the corresponding interrupt handling routine will be executed repeatedly to the exclusion of other processing. This will prevent the main routine and the handlers for low priority level interrupts from being executed (For example, if the time-base timer interrupt is enabled, stepping over the RETI instruction will always break on the first line of the time-base timer interrupt handler).

Disable the corresponding interrupts when the corresponding interrupt handling routine no longer needs debugging.

2. Break function

If the range of addresses that cause a hardware break (including event breaks) is set to the address of the current system stack pointer or to an area that contains the stack pointer, execution will break after each instruction regardless of whether the user program actually contains data access instructions.

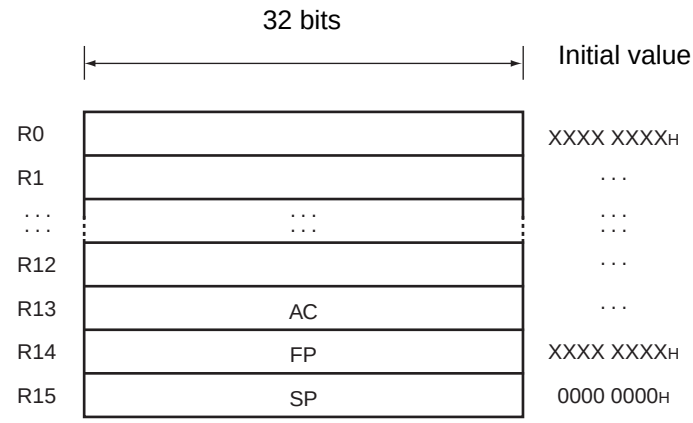
To prevent this, do not set (word) access to the area containing the address of the system stack pointer as the target of the hardware break (including an event breaks).

3. Operand break

It may cause malfunctions if a stack pointer exists in the area which is set as the DSU operand break. Do not set the access to the areas containing the address of system stack pointer as a target of data event break.

4. Registers

4.1. General-purpose register



Registers R0 to R15 are general-purpose registers. These registers can be used as accumulators for computation operations and as pointers for memory access.

Of the 16 registers, enhanced commands are provided for the following registers to enable their use for particular applications.

R13 : Virtual accumulator

R14 : Frame pointer

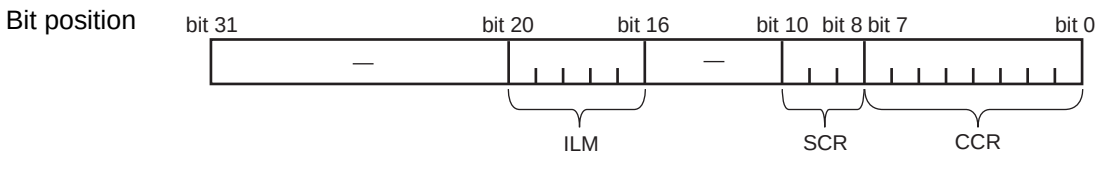
R15 : Stack pointer

Initial values at reset are undefined for R0 to R14. The value for R15 is 00000000H (SSP value).

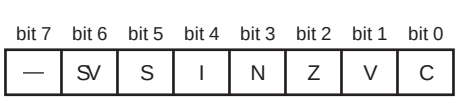
4.2. PS (Program Status)

This register holds the program status, and is divided into three parts, ILM, SCR, and CCR.

All undefined bits (-) in the diagram are reserved bits. The read values are always 0 . Write access to these bits is invalid.



4.3. CCR (Condition Code Register)



SV : Supervisor flag

S : Stack flag

I : Interrupt enable flag

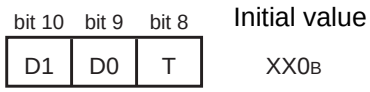
N : Negative enable flag

Z : Zero flag

V : Overflow flag

C : Carry flag

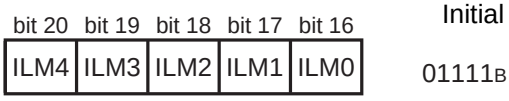
4.4. SCR (System Condition Register)



Flag for step multiplication (D1, D0)
This flag stores interim data during execution of step multiplication.

Step trace trap flag (T)
This flag indicates whether the step trace trap is enabled or disabled.
The step trace trap function is used by emulators. When an emulator is in use, it cannot be used in execution of user programs.

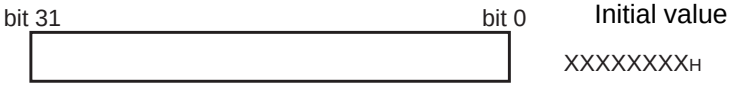
4.5. ILM (Interrupt Level Mask register)



This register stores interrupt level mask values, and the values stored in ILM4 to ILM0 are used for level masking.

The register is initialized to value 01111B at reset.

4.6. PC (Program Counter)



The program counter indicates the address of the instruction that is being executed.

The initial value at reset is undefined.

3. Flash access in CPU mode

3.1. Flash configuration

3.1.1. Flash memory map MB91F467SA

Address									
0014:FFFFh 0014:C000h	SA6 (8KB)				SA7 (8KB)				ROMS7
0014:BFFFh 0014:8000h	SA4 (8KB)				SA5 (8KB)				
0014:7FFFh 0014:4000h	SA2 (8KB)				SA3 (8KB)				
0014:3FFFh 0014:0000h	SA0 (8KB)				SA1 (8KB)				
0013:FFFFh 0012:0000h	SA22 (64KB)				SA23 (64KB)				ROMS6
0011:FFFFh 0010:0000h	SA20 (64KB)				SA21 (64KB)				
000F:FFFFh 000E:0000h	SA18 (64KB)				SA19 (64KB)				ROMS5
000D:FFFFh 000C:0000h	SA16 (64KB)				SA17 (64KB)				ROMS4
000B:FFFFh 000A:0000h	SA14 (64KB)				SA15 (64KB)				ROMS3
0009:FFFFh 0008:0000h	SA12 (64KB)				SA13 (64KB)				ROMS2
0007:FFFFh 0006:0000h	SA10 (64KB)				SA11 (64KB)				ROMS1
0005:FFFFh 0004:0000h	SA8 (64KB)				SA9 (64KB)				ROMS0
	addr+0	addr+1	addr+2	addr+3	addr+4	addr+5	addr+6	addr+7	
16bit read/write	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
32bit read/write	dat[31:0]				dat[31:0]				
64bit read	dat[63:0]								

3.2. Flash access timing settings in CPU mode

The following tables list all settings for a given maximum Core Frequency (through the setting of CLKB or maximum clock modulation) for Flash read and write access.

3.2.1. Flash read timing settings (synchronous read)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 24 MHz	0	0	0	0	1	
to 48 MHz	0	0	1	0	2	
to 96 MHz	1	1	3	0	4	
to 100 MHz	1	1	3	0	4	

3.2.2. Flash write timing settings (synchronous write)

Core clock (CLKB)	ATD	ALEH	EQ	WEXH	WTC	Remark
to 32 MHz	1	0	1	0	4	
to 48 MHz	1	0	3	0	5	
to 64 MHz	1	1	3	0	6	
to 96 MHz	1	1	3	0	7	
to 100 MHz	1	1	3	0	7	

3.3. Address mapping from CPU to parallel programming mode

The following tables show the calculation from CPU addresses to flash macro addresses which are used in parallel programming.

3.3.1. Address mapping MB91F467SA

CPU Address (addr)	Condition	Flash sectors	FA (flash address) Calculation
14:0000h to 14:FFFFh	addr[2]==0	SA0, SA2, SA4, SA6 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 05:0000h
14:0000h to 14:FFFFh	addr[2]==1	SA1, SA3, SA5, SA7 (8 Kbyte)	FA := addr - addr%00:4000h + (addr%00:4000h)/2 - (addr/2)%4 + addr%4 - 05:0000h + 00:2000h
04:0000h to 13:FFFFh	addr[2]==0	SA8, SA10, SA12, SA14, SA16, SA18, SA20, SA22 (64 Kbyte)	FA := addr - addr%02:0000 + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 0C:0000h
04:0000h to 13:FFFFh	addr[2]==1	SA9, SA11, SA13, SA15, SA17, SA19, SA21, SA23 (64 Kbyte)	FA := addr - addr%02:0000h + (addr%02:0000h)/2 - (addr/2)%4 + addr%4 + 0C:0000h + 01:0000h

Note: FA result is without 20:0000h offset for parallel Flash programming .
Set offset by keeping FA[21] = 1 as described in section Parallel Flash programming mode .

4. Parallel Flash programming mode

4.1. Flash configuration in parallel Flash programming mode

Parallel Flash programming mode (MD_[2:0] = 111):

MB91F467SA

FA[21:0]		
003F:FFFFh 003F:0000h	SA23 (64KB)	
003E:FFFFh 003E:0000h	SA22 (64KB)	
003D:FFFFh 003D:0000h	SA21 (64KB)	
003C:FFFFh 003C:0000h	SA20 (64KB)	
003B:FFFFh 003B:0000h	SA19 (64KB)	
003A:FFFFh 003A:0000h	SA18 (64KB)	
0039:FFFFh 0039:0000h	SA17 (64KB)	
0038:FFFFh 0038:0000h	SA16 (64KB)	
0037:FFFFh 0037:0000h	SA15 (64KB)	
0036:FFFFh 0036:0000h	SA14 (64KB)	
0035:FFFFh 0035:0000h	SA13 (64KB)	
0034:FFFFh 0034:0000h	SA12 (64KB)	
0033:FFFFh 0033:0000h	SA11 (64KB)	
0032:FFFFh 0032:0000h	SA10 (64KB)	
0031:FFFFh 0031:0000h	SA9 (64KB)	
0030:FFFFh 0030:0000h	SA8 (64KB)	
002F:FFFFh 002F:E000h	SA7 (8KB)	
002F:DFFFh 002F:C000h	SA6 (8KB)	
002F:BFFFh 002F:A000h	SA5 (8KB)	
002F:9FFFh 002F:8000h	SA4 (8KB)	
002F:7FFFh 002F:6000h	SA3 (8KB)	
002F:5FFFh 002F:4000h	SA2 (8KB)	
002F:3FFFh 002F:2000h	SA1 (8KB)	
002F:1FFFh 002F:0000h	SA0 (8KB)	
	FA[1:0]=00	FA[1:0]=10
16bit write mode	DQ[15:0]	DQ[15:0]

Remark: Always keep FA[0] = 0 and FA[21] = 1

5. Flash Security

5.1. Vector addresses

Two Flash Security Vectors (FSV1, FSV2) are located parallel to the Boot Security Vectors (BSV1, BSV2) controlling the protection functions of the Flash Security Module:

FSV1: 0x14:8000 BSV1: 0x14:8004
FSV2: 0x14:8008 BSV2: 0x14:800C

5.2. Security Vector FSV1

The setting of the Flash Security Vector FSV1 is responsible for the read and write protection modes and the individual write protection of the 8 Kbytes sectors.

5.2.1. FSV1 (bit31 to bit16)

The setting of the Flash Security Vector FSV1 bits [31:16] is responsible for the read and write protection modes.

Explanation of the bits in the Flash Security Vector FSV1 [31:16]

FSV1[31:19]	FSV1[18] Write Protection Level	FSV1[17] Write Protection	FSV1[16] Read Protection	Flash Security Mode
set all to 0	set to 0	set to 0	set to 1	Read Protection (all device modes, except INTVEC mode MD_[2:0] = 000)
set all to 0	set to 0	set to 1	set to 0	Write Protection (all device modes, without exception)
set all to 0	set to 0	set to 1	set to 1	Read Protection (all device modes, except INTVEC mode MD_[2:0] = 000) and Write Protection (all device modes)
set all to 0	set to 1	set to 0	set to 1	Read Protection (all device modes, except INTVEC mode MD_[2:0] = 000)
set all to 0	set to 1	set to 1	set to 0	Write Protection (all device modes, except INTVEC mode MD_[2:0] = 000)
set all to 0	set to 1	set to 1	set to 1	Read Protection (all device modes, except INTVEC mode MD_[2:0] = 000) and Write Protection (all device modes except INTVEC mode MD_[2:0] = 000)

5.2.2. FSV1 (bit15 to bit0)

The setting of the Flash Security Vector FSV1 bits [15:0] is responsible for the individual write protection of the 8 Kbytes sectors. It is only evaluated if write protection bit FSV1[17] is set.

Explanation of the bits in the Flash Security Vector FSV1 [15:0]

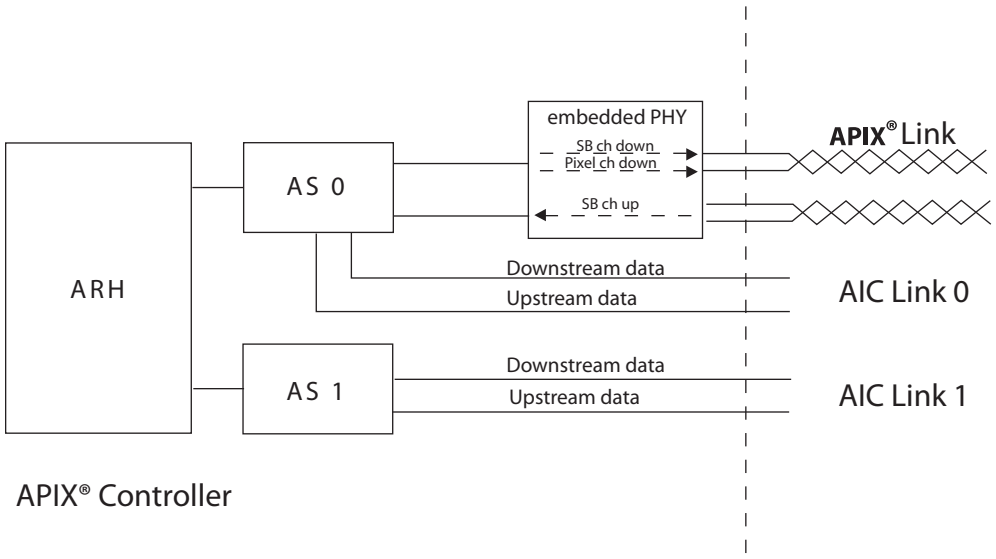
FSV1 bit	Sector	Enable Write Protection	Disable Write Protection	Comment
FSV1[0]	SA0	set to 0	set to 1	
FSV1[1]	SA1	set to 0	set to 1	
FSV1[2]	SA2	set to 0	set to 1	
FSV1[3]	SA3	set to 0	set to 1	
FSV1[4]	SA4	set to 0		Write protection is mandatory!
FSV1[5]	SA5	set to 0	set to 1	
FSV1[6]	SA6	set to 0	set to 1	
FSV1[7]	SA7	set to 0	set to 1	
FSV1[8]		set to 0	set to 1	not available
FSV1[9]		set to 0	set to 1	not available
FSV1[10]		set to 0	set to 1	not available
FSV1[11]		set to 0	set to 1	not available
FSV1[12]		set to 0	set to 1	not available
FSV1[13]		set to 0	set to 1	not available
FSV1[14]		set to 0	set to 1	not available
FSV1[15]		set to 0	set to 1	not available

Note : It is mandatory to always set the sector where the Flash Security Vectors FSV1 and FSV2 are located to write protected (here sector SA4). Otherwise it is possible to overwrite the Security Vector to a setting where it is possible to either read out the Flash content or manipulate data by writing.
See section Flash access in CPU mode for an overview about the sector organization of the Flash Memory.

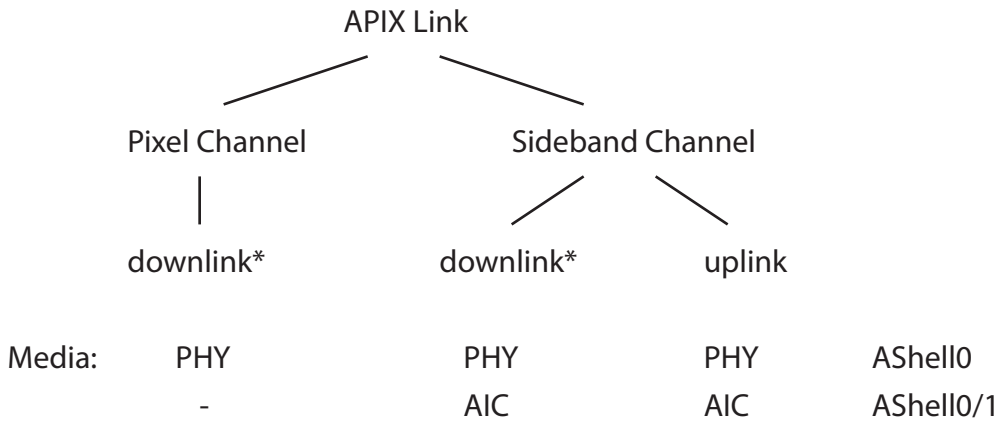
■ APIX® CONTROLLER

1. Overview

The integrated APIX[fi] controller provides 2 links. Link 0 can be configured as an APIX[fi] link or an Automotive Interconnect (AIC) link. Link 1 only supports AIC link.



*Remark: Link 1 can be used only if Link 0 is activated (CHCTRL: TXCFG = 0)



*Remark: MB91460S series provides either downlink over Pixelchannel or over Sidebandchannel

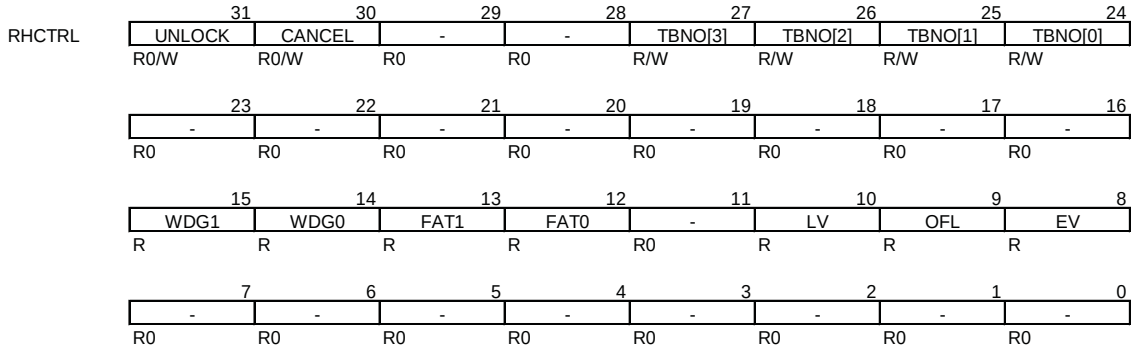
2. Automotive Remote Handler

The Automotive Remote Handler provides an Interface to the APIX[fi] controller.

2.1. Register Description

2.1.1. General Control

RHCTRL: Address 07200h



UNLOCK	0(def)	Transaction on buffer TBNO is requested
	1	Request unlock on waiting buffer TBNO Caution: Requested data gets lost or data is being received after using this buffer with same IDX
CANCEL	0(def)	Transaction on buffer TBNO is requested
	1	Request cancel on pending buffer TBNO
TBNO[3:0]	0-15	Writing starts transaction on buffer number TBNO
WDG1		readonly flag of enabled and selected CHWDG1.WDTXIRQx or enabled and selected CHWDG1.WDRXIRQx
WDG0		readonly flag of enabled and selected CHWDG0.WDTXIRQx or enabled and selected CHWDG0.WDRXIRQx
FAT0		readonly flag of enabled CHCTRL0.FATIRQ
FAT1		readonly flag of enabled CHCTRL1.FATIRQ
LV		readonly flag of enabled EVCTRL.LVIRQ
EV		readonly flag of enabled EVCTRL.EVIRQ
OFL		readonly flag of enabled EVCTRL.OFLIRQ

2.1.2. Channel Control and Status

CHCTRL0 (Link 0): Address 07208h
CHCTRL1 (Link 1): Address 07214h

CHCTRL0-1

31	30	29	28	27	26	25	24
-	-	-	reserved	BYPASS	-	-	-
R0/WX	R0/WX	R0/WX	R/W0	R/W	R/W	R/W	R/W

23	22	21	20	19	18	17	16
FATAL	UPHSK	DNHSK	-	-	-	FATIEN	FATIRQ
R	R	R	RX/W	RX/W	RX/W	R/W	R(RM1)/W

15	14	13	12	11	10	9	8
PLLGOOD	UPRDY	CONNECTED	CRCERR	CRCTOUT	PERROR	READY	REMOTERST
R	R	R	R(RM1)/W	R(RM1)/W	R(RM1)/W	R(RM1)/W	R(RM1)/W

7	6	5	4	3	2	1	0
-	-	UPVALID	DNVALID	-	TXCFG	RSTRTA	INITRH
RX/WX	RX/WX	R/(W)	R/(W)	R0	R/W	R/W	R/W

Bit28 reserved Bit

Always write 0 to this bit. The read value is the value written.

BYPASS: 0 Remote Handler active

1 Remote Handler inactive

In BYPASS mode Transaction Buffer 2 (for AShell 1) is used for downstream data (outbound) and Transaction Buffer 3 (for AShell 1) is used for upstream data (inbound).

Valid written data in Transaction Buffer 0/2 is delivered to AShell by setting DNVALID.

Valid received data in Transaction Buffer 1/3 from AShell is marked by setting UPVALID.

FATAL 1 indicates that AShell has encountered conditions where AShell can not continue to deliver and receive transactions. FATAL is only one CLKB cycle active.

UPHSK 1 indicates inbound handshake is performed

DNHSK 1 indicates outbound handshake is performed

FATIEN 0(def) FATAL Interrupt disabled

1 FATAL Interrupt enabled

FATIRQ 0(def) FATAL Interrupt not active

1 FATAL Interrupt active, triggered by FATAL

*Remark: On a RMW instruction a 1 is read; write 0 clears the interrupt; write 1 is ignored

*Remark: While Fatal Interrupt is active, the corresponding channel is deactivated and the triggered buffers are canceled.

UPRDY 1 indicates that upstream serial channel (APIX^{fi} PHY) is operational

CONNECTED 1 a connection to remote APIX^{fi} is established

CRCERR 1 indicates occurrence of CRC error in upstream data (inbound)

*Remark: On a RMW instruction a 1 is read; write 0 clears the flag; write 1 is ignored

CRCTOUT 1 indicates occurrence of CRC timeout in upstream data (inbound)

*Remark: On a RMW instruction a 1 is read; write 0 clears the flag; write 1 is ignored

PERROR 1 indicates occurrence of a protocol error

*Remark: On a RMW instruction a 1 is read; write 0 clears the flag; write 1 is ignored

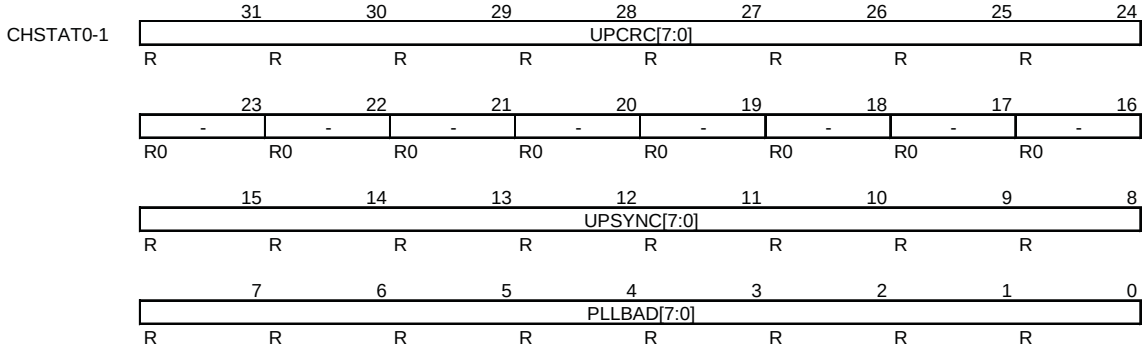
READY	1	indicates that AShell is ready to accept outbound transactions
REMOTERST	1	indicates a restart of remote AShell was performed

*Remark: On a RMW instruction a 1 is read; write 0 clears the flag; write 1 is ignored

UPVALID	BYPASS==0		read only Read only status (ap_data_out_valid)
	BYPASS==1	0(def)	Cleared by SW after successful reception (read) of upstream data
		1	Set by HW to mark upstream data as valid (ap_data_out_valid)
DNVALID	BYPASS==0		read only DNVALID is only operational in BYPASS mode (always read 0)
	BYPASS==1	0(def)	Cleared by HW after successful transfer to AShell
		1	Set by SW to mark downstream data as valid (ap_data_in_valid)
TXCFG	0		AShell and PHY running (write protection on APCFG registers)
	1(def)		AShell and PHY configuration (possible to change APCFG registers)
RSTRTA	0		AShell running Level
	1(def)		AShell initialization
INITRH	0		Remote Handler running Level
	1(def)		Remote Handler initialization (no change of TB* and TF* registers)

*Remark: PENDING requests (set while INIT==1) will be started with INIT==0

CHSTAT0 (Link 0): Address 0720Ch
CHSTAT1 (Link 1): Address 07218h



UPCRC	0-255	Inbound CRC errors
UPSYNC	0-255	Synchronization losses
PLLBAD	0-255	PLL synchronization losses

2.1.3. Channel Watchdog

CHWDG0 (Link 0): Address 07210h
CHWDG1 (Link 1): Address 0721Ch

CHWDG

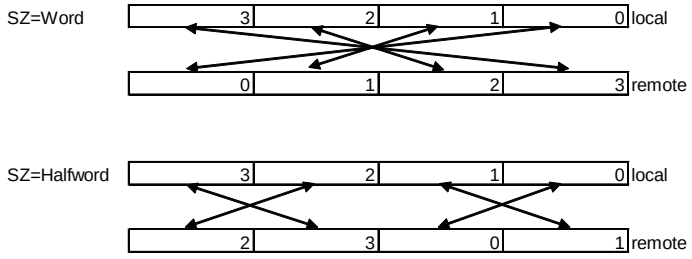
31	30	29	28	27	26	25	24
WDTXIEN	WDRXIEN	-	-	WTTX1	WTTX0	WTRX1	WTRX0
R/W	R/W	R0	R0	R/W	R/W	R/W	R/W

23	22	21	20	19	18	17	16
WDTXIRQ3	WDTXIRQ2	WDTXIRQ1	WDTXIRQ0	WDRXIRQ3	WDRXIRQ2	WDRXIRQ1	WDRXIRQ0
R(RM1)/W	R(RM1)/W	R(RM1)/W	R(RM1)/W	R(RM1)/W	R(RM1)/W	R(RM1)/W	R(RM1)/W

15	14	13	12	11	10	9	8
CNT19	CNT18	CNT17	CNT16	CNT15	CNT14	CNT13	CNT12
R	R	R	R	R	R	R	R

7	6	5	4	3	2	1	0
CNT11	CNT10	CNT9	CNT8	CNT7	CNT6	CNT5	CNT4
R	R	R	R	R	R	R	R

WDTXIEN	0(def)	Watchdog interrupt for TX is disabled
	1	Watchdog interrupt for TX is enabled
WDRXIEN	0(def)	Watchdog interrupt for RX is disabled
	1	Watchdog interrupt for RX is enabled
WTTX	0	select WDTXIRQ0
	1	select WDTXIRQ1
	2	select WDTXIRQ2
	3	select WDTXIRQ3
WTRX	0	select WDRXIRQ0
	1	select WDRXIRQ1
	2	select WDRXIRQ2
	3	select WDRXIRQ3
WDTXIRQ3	0(def)	interrupt for TX at 2^{19} is not active
	1	interrupt for TX at 2^{19} is active
WDTXIRQ2	0(def)	interrupt for TX at 2^{16} is not active
	1	interrupt for TX at 2^{16} is active
WDTXIRQ1	0(def)	interrupt for TX at 2^{14} is not active
	1	interrupt for TX at 2^{14} is active
WDTXIRQ0	0(def)	interrupt for TX at 2^{13} is not active
	1	interrupt for TX at 2^{13} is active
WDRXIRQ3	0(def)	interrupt for RX at 2^{19} is not active
	1	interrupt for RX at 2^{19} is active
WDRXIRQ2	0(def)	interrupt for RX at 2^{18} is not active
	1	interrupt for RX at 2^{18} is active
WDRXIRQ1	0(def)	interrupt for RX at 2^{17} is not active
	1	interrupt for RX at 2^{17} is active



TFIDX00 (Transaction Buffer 00): Address 07251h
TFIDX01 (Transaction Buffer 01): Address 07253h
TFIDX02 (Transaction Buffer 02): Address 07255h
TFIDX03 (Transaction Buffer 03): Address 07257h
TFIDX04 (Transaction Buffer 04): Address 07259h
TFIDX05 (Transaction Buffer 05): Address 0725Bh
TFIDX06 (Transaction Buffer 06): Address 0725Dh
TFIDX07 (Transaction Buffer 07): Address 0725Fh
TFIDX08 (Transaction Buffer 08): Address 07261h
TFIDX09 (Transaction Buffer 09): Address 07263h
TFIDX10 (Transaction Buffer 10): Address 07265h
TFIDX11 (Transaction Buffer 11): Address 07267h
TFIDX12 (Transaction Buffer 12): Address 07269h
TFIDX13 (Transaction Buffer 13): Address 0726Bh
TFIDX14 (Transaction Buffer 14): Address 0726Dh
TFIDX15 (Transaction Buffer 15): Address 0726Fh

TFIDX00-15

7	6	5	4	3	2	1	0
IDX[7]	IDX[6]	IDX[5]	IDX[4]	IDX[3]	IDX[2]	IDX[1]	IDX[0]
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

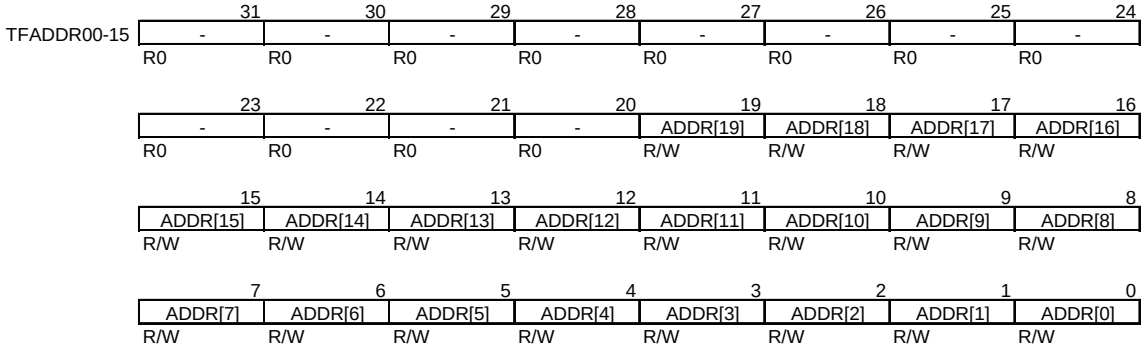
IDX[7:0] Any number between 0 and 255

*Remark: Index is used for read request. Received data from a read request will be stored in an active Transaction Buffer with matching index.

If there is no active Transaction Buffer with matching index (e.g. by using UNLOCK), the received data is discarded.

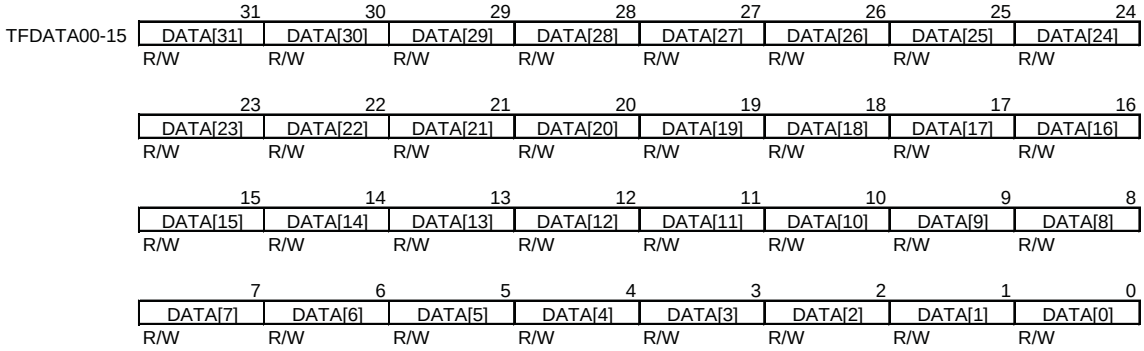
TFADDR00 (Transaction Buffer 00): Address 07270h
TFADDR01 (Transaction Buffer 01): Address 07274h
TFADDR02 (Transaction Buffer 02): Address 07278h
TFADDR03 (Transaction Buffer 03): Address 0727Ch
TFADDR04 (Transaction Buffer 04): Address 07280h
TFADDR05 (Transaction Buffer 05): Address 07284h
TFADDR06 (Transaction Buffer 06): Address 07288h
TFADDR07 (Transaction Buffer 07): Address 0728Ch
TFADDR08 (Transaction Buffer 08): Address 07290h
TFADDR09 (Transaction Buffer 09): Address 07294h
TFADDR10 (Transaction Buffer 10): Address 07298h
TFADDR11 (Transaction Buffer 11): Address 0729Ch

TFADDR12 (Transaction Buffer 12): Address 072A0h
TFADDR13 (Transaction Buffer 13): Address 072A4h
TFADDR14 (Transaction Buffer 14): Address 072A8h
TFADDR15 (Transaction Buffer 15): Address 072ACh



ADDR[19:0] Address in remote system

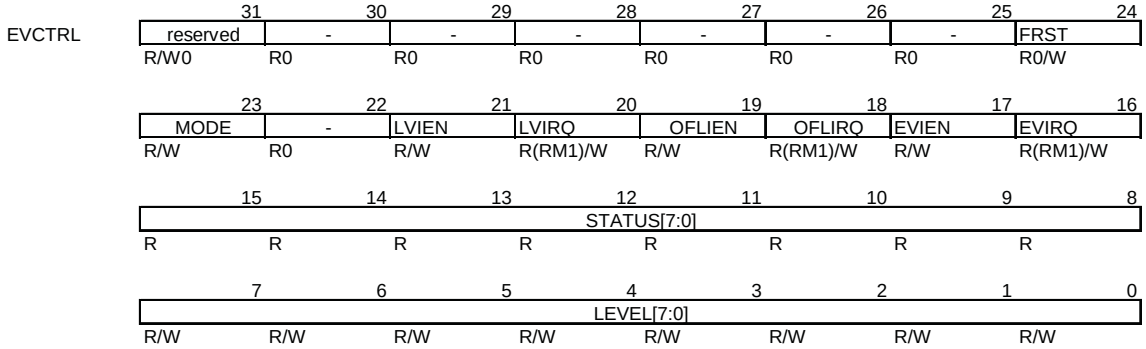
TFDATA00 (Transaction Buffer 00): Address 072B0h
TFDATA01 (Transaction Buffer 01): Address 072B4h
TFDATA02 (Transaction Buffer 02): Address 072B8h
TFDATA03 (Transaction Buffer 03): Address 072BCh
TFDATA04 (Transaction Buffer 04): Address 072C0h
TFDATA05 (Transaction Buffer 05): Address 072C4h
TFDATA06 (Transaction Buffer 06): Address 072C8h
TFDATA07 (Transaction Buffer 07): Address 072CCh
TFDATA08 (Transaction Buffer 08): Address 072D0h
TFDATA09 (Transaction Buffer 09): Address 072D4h
TFDATA10 (Transaction Buffer 10): Address 072D8h
TFDATA11 (Transaction Buffer 11): Address 072DCh
TFDATA12 (Transaction Buffer 12): Address 072E0h
TFDATA13 (Transaction Buffer 13): Address 072E4h
TFDATA14 (Transaction Buffer 14): Address 072E8h
TFDATA15 (Transaction Buffer 15): Address 076ECh



DATA[31:0] Payload data

2.1.7. Event Control

EVCTRL: Address 072F0h



Bit31		reserved Bit
		Always write 0 to this bit. The read value is the value written.
FRST	0(def)	FIFO in normal operation
	1	FIFO pointers are reset pulse (set to 0 after 1 cycle)
MODE	0 (def)	level mode On full FIFO new Events are discarded
	1	ring mode
LVIEN	0(def)	Level Interrupt disabled
	1	Level Interrupt enabled
LVIRQ	0(def)	Level Interrupt not active
	1	Level Interrupt active (if STATUS>=LEVEL)

*Remark: On a RMW instruction a 1 is read; write 0 clears the interrupt; write 1 is ignored

OFLIEN	0(def)	Event Buffer Overflow Interrupt disabled
	1	Event Buffer Overflow Interrupt enabled
OFLIRQ	0(def)	Event Buffer Overflow Interrupt not active
	1	Event Buffer Overflow Interrupt active

*Remark: On a RMW instruction a 1 is read; write 0 clears the interrupt; write 1 is ignored

EVIEN	0(def)	Event Buffer Interrupt disabled
	1	Event Buffer Interrupt enabled
EVIRQ	0(def)	Event Buffer Interrupt not active
	1	Event Buffer Interrupt active

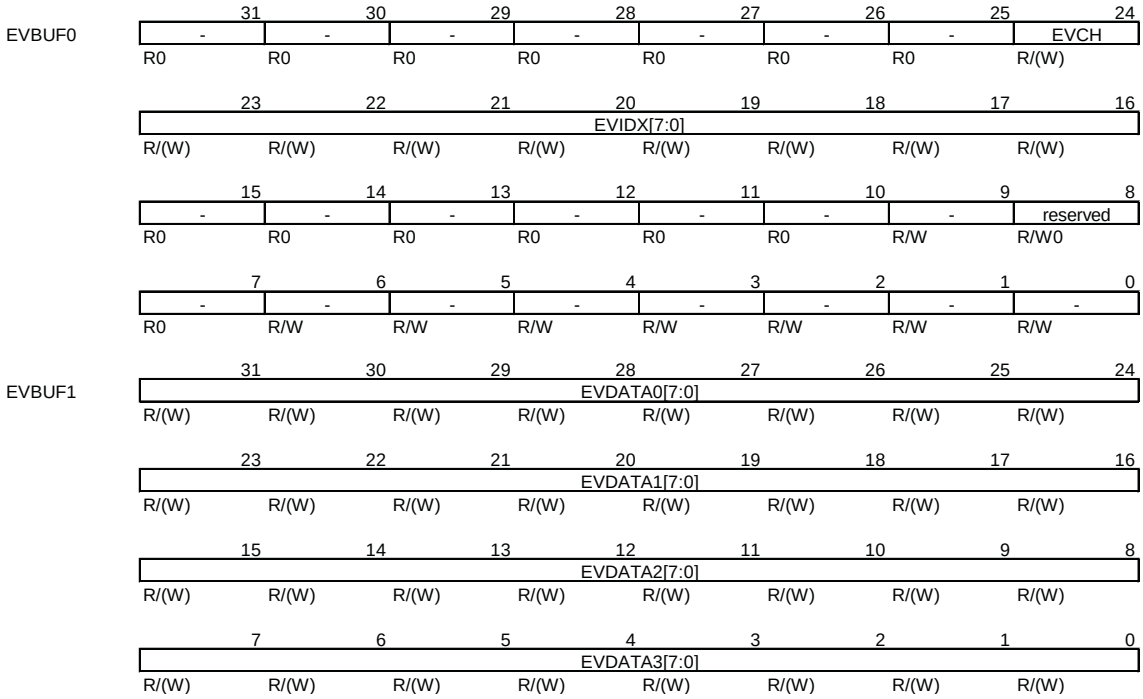
*Remark: On a RMW instruction a 1 is read; write 0 clears the interrupt; write 1 is ignored

Set by hardware, reset by software

STATUS[7:0]	0-128	Current FIFO filling status read only
LEVEL[7:0]	0-128	FIFO interrupt level (128 default)

2.1.8. Eventbuffer

EVBUF0: Address 072F8h
EVBUF1: Address 072FCh



EVCH	Holds channel number from Remote Handler RX event
EVIDX[7:0]	0-255 Holds index number from Remote Handler RX event
Bit8	reserved Bit Always write 0 to this bit. The read value is the value written.
EVDATA0-3	4 bytes of payload data

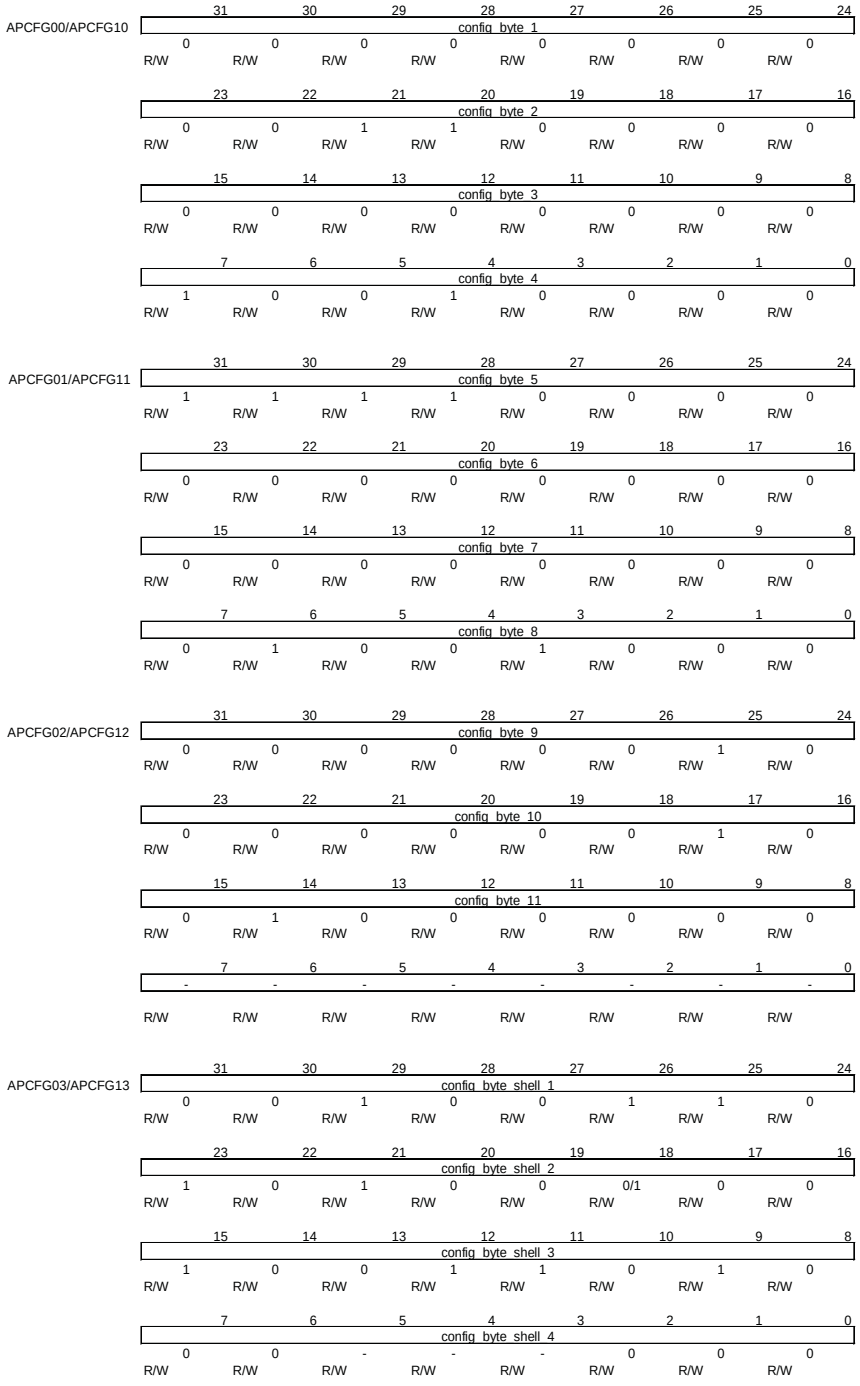
*Remark: It is recommended to read first EVBUF0 and

A read access to EVBUF0 triggers a retrieve of the current event message from the event buffer fifo and returns the channel number and event index.

A read access to EVBUF1 returns the data part of the a event message

2.1.9. Apix® configuration

APCFG0x (Link 0)
APCFG1x (Link 1)



AShell and PHY configuration.

2.1.10. Module ID

MODULEID: Address 07320h

MODULEID[31:0]: Version of the APIX[fi] controller

3. APIX¼® PHY Configuration

3.1. Powerdown

Configuration Vector:		APCFG 00
Bit	**Default**	**Description**
31	0	global power down (upstream, downstream and PLL) 1: power down 0: power up
29	0	power down serializer and output driver (diff amp) 1: power down 0: power up
28	0	power down upstream path 1: power down 0: power up

3.2. Nominal Current

Configuration Vector:		APCFG 01
Bit	**Default**	**Description**
19	0	nominal current setting (64 steps) 000000: min (0 mA - power down output driver) 111111: max
18	0	
17	0	
16	0	
15	0	
14	0	

3.3. Pre-emphasis

Configuration Vector:		APCFG 00
Bit	**Default**	**Description**
26	0	pre-emphasis configuration: reduce output current (pre-emphasis) after N equal serial bits (N = 0..7)
25	0	
24	0	

Configuration Vector:		APCFG 01
Bit	**Default**	**Description**
13	0	pre-emphasis current setting (64 steps) 000000: min (0 mA - power down output driver) 111111: max
12	0	
11	0	
10	0	
9	0	
8	0	

3.4. Sampling Offset

Configuration Vector:		APCFG 00
Bit	**Default**	**Description**
11	0	upstream sampling point configuration 0000: optimum sampling point when operating in 62.50 Mbit/s mode 0010: optimum sampling point when operating in 41.67 Mbit/s or 31.25 Mbit/s mode 0100: optimum sampling point when operating in 20.83 Mbit/s mode
10	0	
9	0	
8	0	

3.5. Charge Pump Control

Configuration Vector:		APCFG 01
Bit	**Default**	**Description**
23	1	charge pump current control
22	0	
21	0	
20	0	

4. DMA transfer request

To request a DMA transfer by a Transaction Buffer, please configure the transfer request source in DMACAx as follows.

IS	EIS(DDNO)	RN	Function	Transfer stop request
10000	1010	160	APIX^{fi} Transaction Buffer 0	available
10001	1010	161	APIX^{fi} Transaction Buffer 1	available
10010	1010	162	APIX^{fi} Transaction Buffer 2	available
10011	1010	163	APIX^{fi} Transaction Buffer 3	available
10100	1010	164	APIX^{fi} Transaction Buffer 4	available
10101	1010	165	APIX^{fi} Transaction Buffer 5	available
10110	1010	166	APIX^{fi} Transaction Buffer 6	available
10111	1010	167	APIX^{fi} Transaction Buffer 7	available
11000	1010	168	APIX^{fi} Transaction Buffer 8	available
11001	1010	169	APIX^{fi} Transaction Buffer 9	available
11010	1010	170	APIX^{fi} Transaction Buffer 10	available
11011	1010	171	APIX^{fi} Transaction Buffer 11	available
11100	1010	172	APIX^{fi} Transaction Buffer 12	available
11101	1010	173	APIX^{fi} Transaction Buffer 13	available
11110	1010	174	APIX^{fi} Transaction Buffer 14	available
11111	1010	175	APIX^{fi} Transaction Buffer 15	available

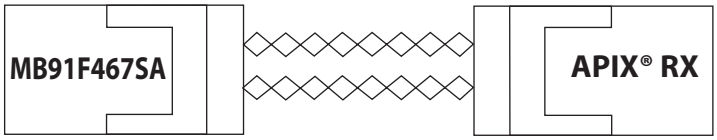
5. Automotive Interconnect Pins

The AIC Pins also serve as general ports.

Pin name	Pin function	I/O format	Pull-up Pull-down	Standby control	Setting required to use
RCK0	AIC uplink clock of Apix® link0	CMOS output and CMOS hysteresis, CMOS Automotive hysteresis, TTL input	Programmable	Provided	Set port function mode PFR28: Bit0 = 1, EPFR28: Bit0 = 1
RDA00	AIC uplink data of Apix® link0				Set port function mode PFR28: Bit1 = 1, EPFR28: Bit1 = 1
RDA01					Set port function mode PFR28: Bit2 = 1, EPFR28: Bit2 = 1
TDA00	AIC downlink data of Apix® link0				Set port function mode PFR28: Bit5 = 1, EPFR28: Bit5 = 1
TDA01					Set port function mode PFR28: Bit6 = 1, EPFR28: Bit6 = 1
TCLI0	AIC downlink clock of Apix® link0				Set port function mode PFR28: Bit7 = 1, EPFR28: Bit7 = 1
RCK1	AIC uplink clock of Apix® link1				Set port function mode PFR17: Bit0 = 1, EPFR17: Bit0 = 1
RDA10	AIC uplink data of Apix® link1				Set port function mode PFR17: Bit1 = 1, EPFR17: Bit1 = 1
RDA11					Set port function mode PFR17: Bit2 = 1, EPFR17: Bit2 = 1
TDA10	AIC downlink data of Apix® link1				Set port function mode PFR17: Bit5 = 1, EPFR17: Bit5 = 1
TDA11					Set port function mode PFR17: Bit6 = 1, EPFR17: Bit6 = 1
TCLI1	AIC downlink clock of Apix® link1				Set port function mode PFR17: Bit7 = 1, EPFR17: Bit7 = 1

6. USECASES

6.1. Communication over APIX® link



6.1.1. Downlink over Pixelchannel

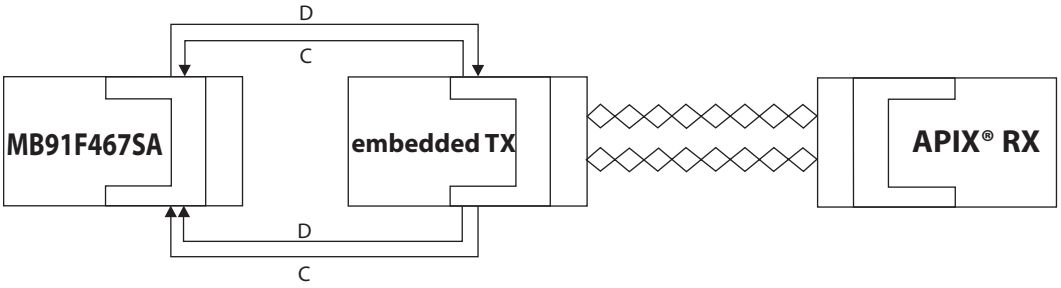
Downlink over Pixelchannel is provided by default configuration. Please configure the PHY according to Chapter APIX…fi PHY Configuration on page 52

6.1.2. Downlink over Sidebandchannel

Register	Bit	Default	Value	Description
APCFG01	31	1	0	0: disable data mode / enable pixel stream mode 1: enable data mode / disable pixel stream mode

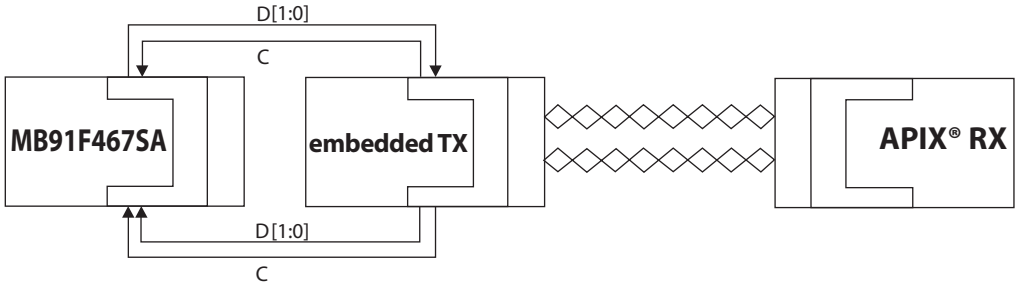
6.2. Communication over Automotive Interconnect to external AShell

6.2.1. 1Bit Datawidth



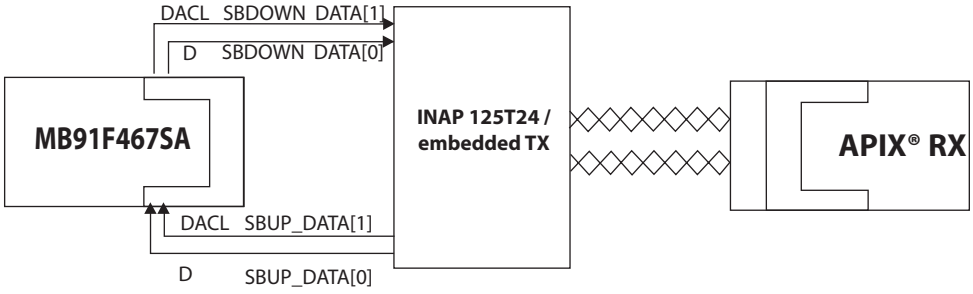
Register	Bit	Default	Value	Description
APCFGn1	31	1	0	0: disable data mode / enable pixel stream mode 1: enable data mode / disable pixel stream mode
APCFGn1	29	1	0	1: enable core clock of APIXfi PHY 0: disable
APCFGn3	23	1	0	1: sbup_data[1:0] 0: sbup_data[0]
APCFGn3	21	1	0	1: sbdown_data[1:0] 0: sbdown_data[0]
APCFGn3	18	0	1	AShell: connect internal Ashell to external APIXfi PHY through GPIO interface 1: enable 0: disable

6.2.2. 2Bit Datawidth



Register	Bit	Default	Value	Description
APCFGn1	31	1	0	0: disable data mode / enable pixel stream mode 1: enable data mode / disable pixel stream mode
APCFGn1	29	1	0	1: enable core clock of APIX[fi] PHY 0: disable
APCFGn3	18	0	1	AShell: connect internal Ashell to external APIX[fi] PHY through GPIO interface 1: enable 0: disable

6.3. Communication over Automotive Interconnect to external PHY



Register	Bit	Default	Value	Description
APCFGn1	31	1	0	0: disable data mode / enable pixel stream mode 1: enable data mode / disable pixel stream mode
APCFGn1	29	1	0	1: enable core clock of APIXfi PHY 0: disable
APCFGn3	22	0	1	AShell: validate sbup_data with 1: sbup_data[1] 0: sbup_valid
APCFGn3	20	0	1	AShell: generate sbdown clock and transmit as sbdown_data[1] 11: disable 10: with use of internal counter (asynchronous to core_clk of APIX^{fi} PHY) 01: with use of sbdown_trigger (synchronous to core_clk of APIX^{fi} PHY) 00: disable
APCFGn3	19	0	0	
APCFGn3	18	0	1	AShell: connect internal Ashell to external APIX^{fi} PHY through GPIO interface 1: enable 0: disable
APCFGn3	2	0	t.b.d.	AShell: configures cycle time of sbdown clock (multiples of Ashell core clock) when sbdown_data are asynchronous (sbdown_data[1] is used as sbdown clock) or cfg_spi_over_sb is enabled 0x0B: recommended minimum (no low bandwidth mode, AShell and APIX^{fi} PHY operate at same core clock frequency) 0x14: recommended minimum (low bandwidth mode 2, AShell and APIX^{fi} PHY operate at 62.5 MHz) 0x26: recommended minimum (low bandwidth mode 1, AShell and APIX^{fi} PHY operate at 62.5 MHz)
	1	0		
	0	0		
	30	0		
	29	1		
	28	0		
	27	0		
	26	1		
	25	1		
	24	0		

6.4. Caution

Up to now only the usecases Downlink over Pixelchannel on page 56 and Communication over Automotive Interconnect to external PHY on page 57 are guaranteed.

■ MEMORY SPACE

The FR family has 4 Gbytes of logical address space (2^{32} addresses) available to the CPU by linear access.

Direct addressing area

The following address space area is used for I/O.

This area is called direct addressing area, and the address of an operand can be specified directly in an instruction.

The size of directly addressable area depends on the length of the data being accessed as shown below.

Byte data access : 000_H to $0FF_H$

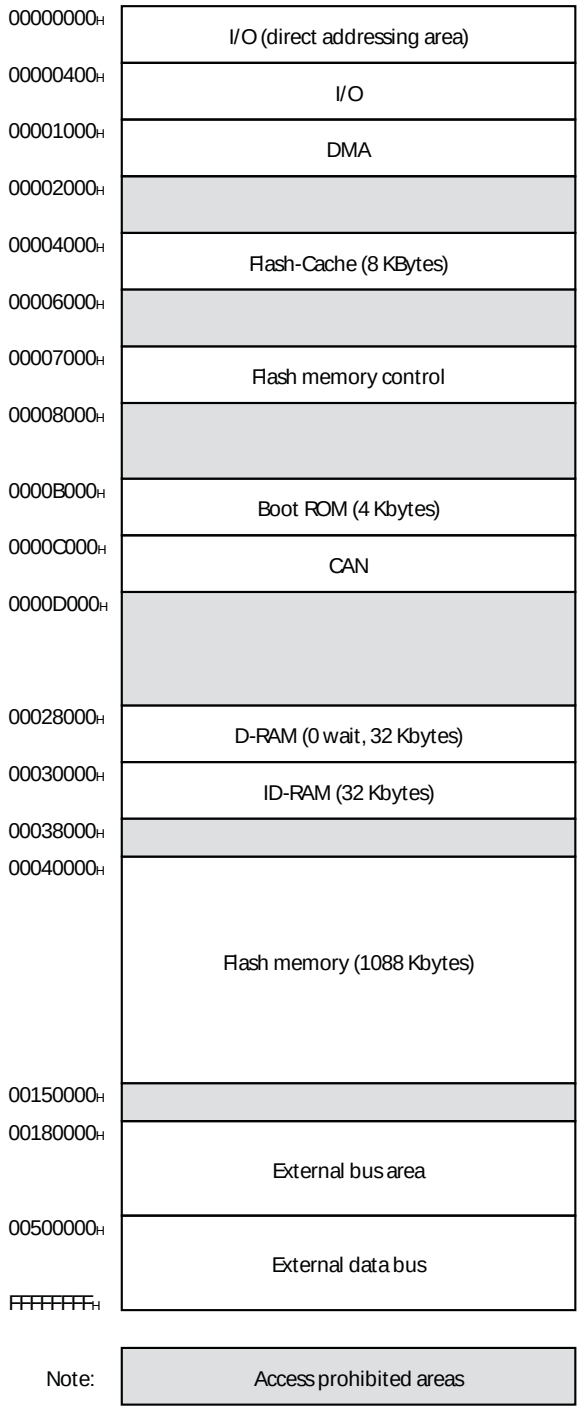
Half word access : 000_H to $1FF_H$

Word data access : 000_H to $3FF_H$

■ MEMORY MAPS

1. MB91F467SA

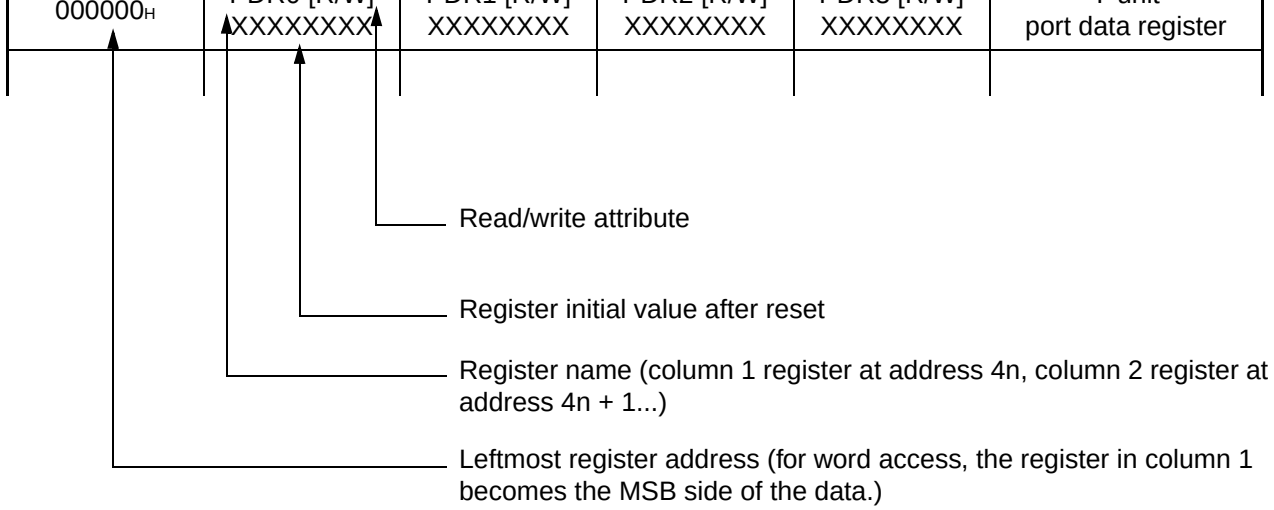
MB91F467SA



■ I/O MAP

1. MB91F467SA

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000H	PDR0 [R/W] XXXXXXXX	PDR1 [R/W] XXXXXXXX	PDR2 [R/W] XXXXXXXX	PDR3 [R/W] XXXXXXXX	T-unit port data register



Note : Initial values of register bits are represented as follows:
- 1 : Initial value 1
- 0 : Initial value 0
- X : Initial value undefined
- - : No physical register at this location

Access is barred with an undefined data access attribute.

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000000H	PDR00 [R/W] XXXXXXXX	PDR01 [R/W] XXXXXXXX	Reserved		R-bus Port Data Register
000004H	Reserved	PDR05 [R/W] XXXXXXXX	PDR06 [R/W] XXXXXXXX	PDR07 [R/W] XXXXXXXX	
000008H	PDR08 [R/W] X - - X - - XX	PDR09 [R/W] - - - - XXXX	PDR10 [R/W] - - - - X - XX	Reserved	
00000CH	Reserved		PDR14 [R/W] XXXXXXXX	PDR15 [R/W] - - - - XXXX	
000010H	PDR16 [R/W] XXXXXXXX	PDR17 [R/W] XXXXXXXX	PDR18 [R/W] - XXX - XXX	PDR19 [R/W] - XXX - XXX	
000014H	PDR20 [R/W] - XXX - XXX	Reserved	PDR22 [R/W] XXXX - X - X	PDR23 [R/W] - X - XXXXX	
000018H	PDR24 [R/W] XXXXXXXX	Reserved			
00001CH	PDR28 [R/W] XXXXXXXX	PDR29 [R/W] XXXXXXXX	Reserved		
000024H to 00002CH	Reserved				
000030H	EIRR0 [R/W] XXXXXXXX	ENIR0 [R/W] 00000000	ELVR0 [R/W] 00000000 00000000		External interrupt (INT 0 to INT 7)
000034H	EIRR1 [R/W] XXXXXXXX	ENIR1 [R/W] 00000000	ELVR1 [R/W] 00000000 00000000		External interrupt (INT 8 to INT 15)
000038H	DICR [R/W] - - - - - - - 0	HRCL [R/W] 0 - - 11111	RBSYNC*1		Delay Interrupt
00003CH to 00004CH	Reserved				
000050H	SCR02 [R/W, W] 00000000	SMR02 [R/W, W] 00000000	SSR02 [R/W, R] 00001000	RDR02/TDR02 [R/W] 00000000	LIN-USART 2
000054H	ESCR02 [R/W] 00000X00	ECCR02 [R/W, R, W] -00000XX	Reserved		
000058H	SCR03 [R/W, W] 00000000	SMR03 [R/W, W] 00000000	SSR03 [R/W, R] 00001000	RDR03/TDR03 [R/W] 00000000	LIN-USART 3
00005CH	ESCR03 [R/W] 00000X00	ECCR03 [R/W, R, W] -00000XX	Reserved		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000060H	SCR04 [R/W, W] 00000000	SMR04 [R/W, W] 00000000	SSR04 [R/W, R] 00001000	RDR04/TDR04 [R/W] 00000000	LIN-USART 4 with FIFO
000064H	ESCR04 [R/W] 00000X00	ECCR04 [R/W, R, W] -00000XX	FSR04 [R] - - - 00000	FCR04 [R/W] 0001 - 000	
000068H	SCR05 [R/W, W] 00000000	SMR05 [R/W, W] 00000000	SSR05 [R/W, R] 00001000	RDR05/TDR05 [R/W] 00000000	LIN-USART 5 with FIFO
00006CH	ESCR05 [R/W] 00000X00	ECCR05 [R/W, R, W] -00000XX	FSR05 [R] - - - 00000	FCR05 [R/W] 0001 - 000	
000070H	SCR06 [R/W, W] 00000000	SMR06 [R/W, W] 00000000	SSR06 [R/W, R] 00001000	RDR06/TDR06 [R/W] 00000000	LIN-USART 6 with FIFO
000074H	ESCR06 [R/W] 00000X00	ECCR06 [R/W, R, W] -00000XX	FSR06 [R] - - - 00000	FCR06 [R/W] 0001 - 000	
000078H	SCR07 [R/W, W] 00000000	SMR07 [R/W, W] 00000000	SSR07 [R/W, R] 00001000	RDR07/TDR07 [R/W] 00000000	LIN-USART 7 with FIFO
00007CH	ESCR07 [R/W] 00000X00	ECCR07 [R/W, R, W] -00000XX	FSR07 [R] - - - 00000	FCR07 [R/W] 0001 - 000	
000080H	Reserved				
000084H	BGR102 [R/W] 00000000	BGR002 [R/W] 00000000	BGR103 [R/W] 00000000	BGR003 [R/W] 00000000	Baud rate Generator LIN-USART 2 to 7
000088H	BGR104 [R/W] 00000000	BGR004 [R/W] 00000000	BGR105 [R/W] 00000000	BGR005 [R/W] 00000000	
00008CH	BGR106 [R/W] 00000000	BGR006 [R/W] 00000000	BGR107 [R/W] 00000000	BGR007 [R/W] 00000000	
000090H to 0000CCH	Reserved				
0000D0H	IBCR0 [R/W] 00000000	IBSR0 [R] 00000000	ITBAH0 [R/W] - - - - - - 00	ITBAL0 [R/W] 00000000	I²C 0
0000D4H	ITMKH0 [R/W] 00 - - - - 11	ITMKL0 [R/W] 11111111	ISMK0 [R/W] 01111111	ISBA0 [R/W] - 0000000	
0000D8H	Reserved	IDAR0 [R/W] 00000000	ICCR0 [R/W] - 0011111	Reserved	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0000DC$_H$	IBCR1 [R/W] 00000000	IBSR1 [R] 00000000	ITBAH1[R/W] - - - - - - 00	ITBAL1 [R/W] 00000000	I^2C 1
0000E0$_H$	ITMKH1 [R/W] 00 - - - - 11	ITMKL1 [R/W] 11111111	ISMK1 [R/W] 01111111	ISBA1 [R/W] - 0000000	
0000E4$_H$	Reserved	IDAR1 [R/W] 00000000	ICCR1 [R/W] - 0011111	Reserved	
0000E8$_H$ to 0000FC$_H$	Reserved				
000100$_H$	GCN10 [R/W] 00110010 00010000		Reserved	GCN20 [R/W] - - - - 0000	PPG Control 0 to 3
000104$_H$	GCN11 [R/W] 00110010 00010000		Reserved	GCN21 [R/W] - - - - 0000	PPG Control 4 to 7
000108$_H$	GCN12 [R/W] 00110010 00010000		Reserved	GCN22 [R/W] - - - - 0000	PPG Control 8 to 11
00010C$_H$	Reserved				
000110$_H$	PTMR00 [R] 11111111 11111111		PCSR00 [W] XXXXXXXX XXXXXXXX		PPG 0
000114$_H$	PDUT00 [W] XXXXXXXX XXXXXXXX		PCNH00 [R/W] 0000000 -	PCNL00 [R/W] 000000 - 0	
000118$_H$	PTMR01 [R] 11111111 11111111		PCSR01 [W] XXXXXXXX XXXXXXXX		PPG 1
00011C$_H$	PDUT01 [W] XXXXXXXX XXXXXXXX		PCNH01 [R/W] 0000000 -	PCNL01 [R/W] 000000 - 0	
000120$_H$	PTMR02 [R] 11111111 11111111		PCSR02 [W] XXXXXXXX XXXXXXXX		PPG2
000124$_H$	PDUT02 [W] XXXXXXXX XXXXXXXX		PCNH02 [R/W] 0000000 -	PCNL02 [R/W] 000000 - 0	
000128$_H$	PTMR03 [R] 11111111 11111111		PCSR03 [W] XXXXXXXX XXXXXXXX		PPG3
00012C$_H$	PDUT03 [W] XXXXXXXX XXXXXXXX		PCNH03 [R/W] 0000000 -	PCNL03 [R/W] 000000 - 0	
000130$_H$	PTMR04 [R] 11111111 11111111		PCSR04 [W] XXXXXXXX XXXXXXXX		PPG 4
000134$_H$	PDUT04 [W] XXXXXXXX XXXXXXXX		PCNH04 [R/W] 0000000 -	PCNL04 [R/W] 000000 - 0	
000138$_H$	PTMR05 [R] 11111111 11111111		PCSR05 [W] XXXXXXXX XXXXXXXX		PPG 5
00013C$_H$	PDUT05 [W] XXXXXXXX XXXXXXXX		PCNH05 [R/W] 0000000 -	PCNL05 [R/W] 000000 - 0	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000140H	PTMR06 [R] 11111111 11111111		PCSR06 [W] XXXXXXXX XXXXXXXX		PPG 6
000144H	PDUT06 [W] XXXXXXXX XXXXXXXX		PCNH06 [R/W] 0000000 -	PCNL06 [R/W] 000000 - 0	
000148H	PTMR07 [R] 11111111 11111111		PCSR07 [W] XXXXXXXX XXXXXXXX		PPG 7
00014CH	PDUT07 [W] XXXXXXXX XXXXXXXX		PCNH07 [R/W] 0000000 -	PCNL07 [R/W] 000000 - 0	
000150H	PTMR08 [R] 11111111 11111111		PCSR08 [W] XXXXXXXX XXXXXXXX		PPG 8
000154H	PDUT08 [W] XXXXXXXX XXXXXXXX		PCNH08 [R/W] 0000000 -	PCNL08 [R/W] 000000 - 0	
000158H	PTMR09 [R] 11111111 11111111		PCSR09 [W] XXXXXXXX XXXXXXXX		PPG 9
00015CH	PDUT09 [W] XXXXXXXX XXXXXXXX		PCNH09 [R/W] 0000000 -	PCNL09 [R/W] 000000 - 0	
000160H	PTMR10 [R] 11111111 11111111		PCSR10 [W] XXXXXXXX XXXXXXXX		PPG 10
000164H	PDUT10 [W] XXXXXXXX XXXXXXXX		PCNH10 [R/W] 0000000 -	PCNL10 [R/W] 000000 - 0	
000168H	PTMR11 [R] 11111111 11111111		PCSR11 [W] XXXXXXXX XXXXXXXX		PPG 11
00016CH	PDUT11 [W] XXXXXXXX XXXXXXXX		PCNH11 [R/W] 0000000 -	PCNL11 [R/W] 000000 - 0	
000170H	P0TMCSRH [R/W] - 0 - 000 - 0	P0TMCSRL [R/W] - - - 00000	P1TMCSRH [R/W] - 0 - 000 - 0	P1TMCSRL [R/W] - - - 00000	Pulse Frequency Modulator
000174H	P0TMRLR [W] XXXXXXXX XXXXXXXX		P0TMR [R] XXXXXXXX XXXXXXXX		
000178H	P1TMRLR [W] XXXXXXXX XXXXXXXX		P1TMR [R] XXXXXXXX XXXXXXXX		
00017CH	Reserved				
000180H	Reserved	ICS01 [R/W] 00000000	Reserved	ICS23 [R/W] 00000000	Input Capture 0 to 3
000184H	IPCP0 [R] XXXXXXXX XXXXXXXX		IPCP1 [R] XXXXXXXX XXXXXXXX		
000188H	IPCP2 [R] XXXXXXXX XXXXXXXX		IPCP3 [R] XXXXXXXX XXXXXXXX		

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00018CH	OCS01 [R/W] - - - 0 - - 00 0000 - - 00		OCS23 [R/W] - - - 0 - - 00 0000 - - 00		Output Compare 0 to 3
000190H	OCCP0 [R/W] XXXXXXXX XXXXXXXX		OCCP1 [R/W] XXXXXXXX XXXXXXXX		
000194H	OCCP2 [R/W] XXXXXXXX XXXXXXXX		OCCP3 [R/W] XXXXXXXX XXXXXXXX		
000198H	SGCRH [R/W] 0000 - - 00	SGCRL [R/W] - - 0 - - 000	SGFR [R/W, R] XXXXXXXX XXXXXXXX		Sound Generator
00019CH	SGAR [R/W] 00000000	Reserved	SGTR [R/W] XXXXXXXX	SGDR [R/W] XXXXXXXX	
0001A0H	ADERH [R/W] 00000000 00000000		ADERL [R/W] 00000000 00000000		A/D Converter
0001A4	ADCS1 [R/W] 00000000	ADCS0 [R/W] 00000000	ADCR1 [R] 000000XX	ADCR0 [R] XXXXXXXX	
0001A8H	ADCT1 [R/W] 00010000	ADCT0 [R/W] 00101100	ADSCH [R/W] - - - 00000	ADECH [R/W] - - - 00000	
0001ACH	Reserved	ACSR0 [R/W] - 11XXX00	Reserved		Alarm Comparator 0
0001B0H	TMRLR0 [W] XXXXXXXX XXXXXXXX		TMR0 [R] XXXXXXXX XXXXXXXX		Reload Timer 0 (PPG 0, PPG 1)
0001B4H	Reserved		TMCSRH0 [R/W] - - - 00000	TMCSRL0 [R/W] 0 - 000000	
0001B8H	TMRLR1 [W] XXXXXXXX XXXXXXXX		TMR1 [R] XXXXXXXX XXXXXXXX		Reload Timer 1 (PPG 2, PPG 3)
0001BCH	Reserved		TMCSRH1 [R/W] - - - 00000	TMCSRL1 [R/W] 0 - 000000	
0001C0H	TMRLR2 [W] XXXXXXXX XXXXXXXX		TMR2 [R] XXXXXXXX XXXXXXXX		Reload Timer 2 (PPG 4, PPG 5)
0001C4H	Reserved		TMCSRH2 [R/W] - - - 00000	TMCSRL2 [R/W] 0 - 000000	
0001C8H	TMRLR3 [W] XXXXXXXX XXXXXXXX		TMR3 [R] XXXXXXXX XXXXXXXX		Reload Timer 3 (PPG 6, PPG 7)
0001CCH	Reserved		TMCSRH3 [R/W] - - - 00000	TMCSRL3 [R/W] 0 - 000000	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0001D0H	TMRLR4 [W] XXXXXXXX XXXXXXXX		TMR4 [R] XXXXXXXX XXXXXXXX		Reload Timer 4 (PPG 8, PPG 9)
0001D4H	Reserved		TMCSRH4 [R/W] - - - 00000	TMCSRL4 [R/W] 0 - 000000	
0001D8H	TMRLR5 [W] XXXXXXXX XXXXXXXX		TMR5 [R] XXXXXXXX XXXXXXXX		Reload Timer 5 (PPG 10, PPG 11)
0001DCH	Reserved		TMCSRH5 [R/W] - - - 00000	TMCSRL5 [R/W] 0 - 000000	
0001E0H	TMRLR6 [W] XXXXXXXX XXXXXXXX		TMR6 [R] XXXXXXXX XXXXXXXX		Reload Timer 6 (PPG 12, PPG 13)
0001E4H	Reserved		TMCSRH6 [R/W] - - - 00000	TMCSRL6 [R/W] 0 - 000000	
0001E8H	TMRLR7 [W] XXXXXXXX XXXXXXXX		TMR7 [R] XXXXXXXX XXXXXXXX		Reload Timer 7 (PPG 14, PPG 15) (A/D Converter)
0001ECH	Reserved		TMCSRH7 [R/W] - - - 00000	TMCSRL7 [R/W] 0 - 000000	
0001F0H	TCDT0 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS0 [R/W] 00000000	Free Running Timer 0 (ICU 0, ICU 1)
0001F4H	TCDT1 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS1 [R/W] 00000000	Free Running Timer 1 (ICU 2, ICU 3)
0001F8H	TCDT2 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS2 [R/W] 00000000	Free Running Timer 2 (OCU 0, OCU 1)
0001FCH	TCDT3 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS3 [R/W] 00000000	Free Running Timer 3 (OCU 2, OCU 3)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000200H	DMACA0 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				DMAC
000204H	DMACB0 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000208H	DMACA1 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00020CH	DMACB1 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000210H	DMACA2 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000214H	DMACB2 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000218H	DMACA3 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
00021CH	DMACB3 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000220H	DMACA4 [R/W] 00000000 0000XXXX XXXXXXXX XXXXXXXX				
000224H	DMACB4 [R/W] 00000000 00000000 XXXXXXXX XXXXXXXX				
000228H to 00023CH	Reserved				
000240H	DMACR [R/W] 00 - - 0000	Reserved			
000244H to 0002CCH	Reserved				
0002D0H	Reserved	ICS045 [R/W] 00000000	Reserved	ICS67 [R/W] 00000000	Input Capture 4 to 7
0002D4H	IPCP4 [R] XXXXXXXX XXXXXXXX		IPCP5 [R] XXXXXXXX XXXXXXXX		
0002D8H	IPCP6 [R] XXXXXXXX XXXXXXXX		IPCP7 [R] XXXXXXXX XXXXXXXX		
0002DCH to 0002ECH	Reserved				
0002F0H	TCDT4 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS4 [R/W] 00000000	Free Running Timer 4 (ICU 4, ICU 5)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0002F4H	TCDT5 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS5 [R/W] 00000000	Free Running Timer 5 (ICU 6, ICU 7)
0002F8H	TCDT6 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS6 [R/W] 00000000	Free Running Timer 6
0002FCH	TCDT7 [R/W] XXXXXXXX XXXXXXXX		Reserved	TCCS7 [R/W] 00000000	Free Running Timer 7
000300H	UDRC1 [W] 00000000	UDRC0 [W] 00000000	UDCR1 [R] 00000000	UDCR0 [R] 00000000	Up/Down Counter 0/1
000304H	UDCCH0 [R/W] 00000000	UDCCL0 [R/W] 00000000	Reserved	UDCS0 [R/W] 00000000	
000308H	UDCCH1 [R/W] 00000000	UDCCL1[R/W] 00000000	Reserved	UDCS1 [R/W] 00000000	
00030CH	Reserved				
000310H	UDRC3 [W] 00000000	UDRC2 [W] 00000000	UDCR3 [R] 00000000	UDCR2 [R] 00000000	Up/Down Counter 2/3
000314H	UDCCH2 [R/W] 00000000	UDCCL2 [R/W] 00000000	Reserved	UDCS2 [R/W] 00000000	
000318H	UDCCH3 [R/W] 00000000	UDCCL3 [R/W] 00000000	Reserved	UDCS3 [R/W] 00000000	
00031CH	Reserved				
000320H	GCN13 [R/W] 00110010 00010000		Reserved	GCN23 [R/W] - - - - 0000	PPG Control 12 to 15
000324H to 00032CH	Reserved				
000330H	PTMR12 [R] 11111111 11111111		PCSR12 [W] XXXXXXXX XXXXXXXX		PPG 12
000334H	PDUT12 [W] XXXXXXXX XXXXXXXX		PCNH12 [R/W] 0000000 -	PCNL12 [R/W] 000000 - 0	
000338H	PTMR13 [R] 11111111 11111111		PCSR13 [W] XXXXXXXX XXXXXXXX		PPG 13
00033CH	PDUT13 [W] XXXXXXXX XXXXXXXX		PCNH13 [R/W] 0000000 -	PCNL13 [R/W] 000000 - 0	
000340H	PTMR14 [R] 11111111 11111111		PCSR14 [W] XXXXXXXX XXXXXXXX		PPG 14
000344H	PDUT14 [W] XXXXXXXX XXXXXXXX		PCNH14 [R/W] 0000000 -	PCNL14 [R/W] 000000 - 0	

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000348H	PTMR15 [R] 11111111 11111111		PCSR15 [W] XXXXXXXX XXXXXXXX		PPG 15
00034CH	PDUT15 [W] XXXXXXXX XXXXXXXX		PCNH15 [R/W] 0000000 -	PCNL15 [R/W] 000000 - 0	
000350H to 000364H	Reserved				
000368H	IBCR2 [R/W] 00000000	IBSR2 [R] 00000000	ITBAH2 [R/W] - - - - - - 00	ITBAL2 [R/W] 00000000	I²C 2
00036CH	ITMKH2 [R/W] 00 - - - - 11	ITMKL2 [R/W] 11111111	ISMK2 [R/W] 01111111	ISBA2 [R/W] - 0000000	
000370H	Reserved	IDAR2 [R/W] 00000000	ICCR2 [R/W] - 0011111	Reserved	
000374H to 00038CH	Reserved				
000390H	ROMS [R] 11111111 00000000		Reserved		ROM Select Register
000394H to 0003ECH	Reserved				
0003F0H	BSD0 [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				Bit Search Module
0003F4H	BSD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003F8H	BSDC [W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
0003FCH	BSRR [R] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
000400H to 00043CH	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000440H	ICR00 [R/W] ---11111	ICR01 [R/W] ---11111	ICR02 [R/W] ---11111	ICR03 [R/W] ---11111	Interrupt Controller
000444H	ICR04 [R/W] ---11111	ICR05 [R/W] ---11111	ICR06 [R/W] ---11111	ICR07 [R/W] ---11111	
000448H	ICR08 [R/W] ---11111	ICR09 [R/W] ---11111	ICR10 [R/W] ---11111	ICR11 [R/W] ---11111	
00044CH	ICR12 [R/W] ---11111	ICR13 [R/W] ---11111	ICR14 [R/W] ---11111	ICR15 [R/W] ---11111	
000450H	ICR16 [R/W] ---11111	ICR17 [R/W] ---11111	ICR18 [R/W] ---11111	ICR19 [R/W] ---11111	
000454H	ICR20 [R/W] ---11111	ICR21 [R/W] ---11111	ICR22 [R/W] ---11111	ICR23 [R/W] ---11111	
000458H	ICR24 [R/W] ---11111	ICR25 [R/W] ---11111	ICR26 [R/W] ---11111	ICR27 [R/W] ---11111	
00045CH	ICR28 [R/W] ---11111	ICR29 [R/W] ---11111	ICR30 [R/W] ---11111	ICR31 [R/W] ---11111	
000460H	ICR32 [R/W] ---11111	ICR33 [R/W] ---11111	ICR34 [R/W] ---11111	ICR35 [R/W] ---11111	
000464H	ICR36 [R/W] ---11111	ICR37 [R/W] ---11111	ICR38 [R/W] ---11111	ICR39 [R/W] ---11111	
000468H	ICR40 [R/W] ---11111	ICR41 [R/W] ---11111	ICR42 [R/W] ---11111	ICR43 [R/W] ---11111	
00046CH	ICR44 [R/W] ---11111	ICR45 [R/W] ---11111	ICR46 [R/W] ---11111	ICR47 [R/W] ---11111	
000470H	ICR48 [R/W] ---11111	ICR49 [R/W] ---11111	ICR50 [R/W] ---11111	ICR51 [R/W] ---11111	
000474H	ICR52 [R/W] ---11111	ICR53 [R/W] ---11111	ICR54 [R/W] ---11111	ICR55 [R/W] ---11111	
000478H	ICR56 [R/W] ---11111	ICR57 [R/W] ---11111	ICR58 [R/W] ---11111	ICR59 [R/W] ---11111	
00047CH	ICR60 [R/W] ---11111	ICR61 [R/W] ---11111	ICR62 [R/W] ---11111	ICR63 [R/W] ---11111	
000480H	RSRR [R/W] 10000000	STCR [R/W] 00110011	TBCR [R/W] 00XXX - 00	CTBR [W] XXXXXXXX	Clock Control
000484H	CLKR [R/W] ---- 0000	WPR [W] XXXXXXXX	DIVR0 [R/W] 00000011	DIVR1 [R/W] 00000000	
000488H	Reserved				
00048CH	PLLDIVM [R/W] - - - - 0000	PLLDIVN [R/W] - - 000000	PLLDIVG [R/W] - - - - 0000	PLLDIVG [W] 00000000	PLL Interface
000490H	PLLCTRL [R/W] - - - - 0000	Reserved			

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000494H	OSCC1 [R/W] - - - - - 010	OSCS1 [R/W] 00001111	OSCC2 [R/W] - - - - - 010	OSCS2 [R/W] 00001111	Main/Sub Oscillator Control
000498H	PORTEN [R/W] - - - - - - 00	Reserved			Port Input Enable Control
00049CH	Reserved				
0004A0H	Reserved	WTCER [R/W] - - - - - - 00	WTCR [R/W] 00000000 000 - 00 - 0		Real Time Clock (Watch Timer)
0004A4H	Reserved	WTBR [R/W] - - - XXXXX XXXXXXXX XXXXXXXX			
0004A8H	WTHR [R/W] - - - 00000	WTMR [R/W] - - 000000	WTSR [R/W] - - 000000	Reserved	
0004ACH	CSVTR [R/W] - - - 00010	CSVCR [R/W] 00011100	CSCFG [R/W] 0X000000	CMCFG [R/W] 00000000	Clock-Supervisor / Selector / Monitor
0004B0H	CUCR [R/W] - - - - - - - - - - - - 0 - - 00		CUTD [R/W] 10000000 00000000		Calibration of Sub Clock
0004B4H	CUTR1 [R] - - - - - - - - 00000000		CUTR2 [R] 00000000 00000000		
0004B8H	CMPR [R/W] - - 000010 11111101		Reserved	CMCR [R/W] - 001 - - 00	Clock Modulator
0004BCH	CMT1 [R/W] 00000000 1 - - - 0000		CMT2 [R/W] - - 000000 - - 000000		
0004C0H	CANPRE [R/W] - - 000000	CANCKD [R/W] - - - - - - 00*3	Reserved		CAN Clock Control
0004C4H	LVSEL [R/W] 00000111	LVDET [R/W] 0000 0 - 00	HWWDE [R/W] - - - - - - 00	HWWD [R/W, W] 00011000	Low Voltage Detection/ Hardware Watchdog
0004C8H	OSCRH [R/W] 000 - - 001	OSCRL [R/W] - - - - - 000	WPCRH [R/W] 00 - - - 000	WPCRL [R/W] - - - - - - 00	Main-/Sub-Oscillation Stabilization Timer
0004CCH	OSCCR [R/W] - - - - - - - 0	Reserved	REGSEL [R/W] - - 000100	REGCTR [R/W] - - - 0 - - 00	Main- Oscillation Standby Control Main-/Subregulator Control
0004D0H to 00063CH	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000640H	ASR0 [R/W] 00000000 00000000		ACR0 [R/W] 1111**00 00100000*4		External Bus
000644H	ASR1 [R/W] XXXXXXXX XXXXXXXX		ACR1 [R/W] XXXXXXXX XXXXXXXX		
000648H	ASR2 [R/W] XXXXXXXX XXXXXXXX		ACR2 [R/W] XXXXXXXX XXXXXXXX		
00064CH	ASR3 [R/W] XXXXXXXX XXXXXXXX		ACR3 [R/W] XXXXXXXX XXXXXXXX		
000650H	ASR4 [R/W] XXXXXXXX XXXXXXXX		ACR4 [R/W] XXXXXXXX XXXXXXXX		
000654H	ASR5 [R/W] XXXXXXXX XXXXXXXX		ACR5 [R/W] XXXXXXXX XXXXXXXX		
000658H	ASR6 [R/W] XXXXXXXX XXXXXXXX		ACR6 [R/W] XXXXXXXX XXXXXXXX		
00065CH	ASR7 [R/W] XXXXXXXX XXXXXXXX		ACR7 [R/W] XXXXXXXX XXXXXXXX		
000660H	AWR0 [R/W] 01001111 11111011		AWR1 [R/W] XXXXXXXX XXXXXXXX		
000664H	AWR2 [R/W] XXXXXXXX XXXXXXXX		AWR3 [R/W] XXXXXXXX XXXXXXXX		
000668H	AWR4 [R/W] XXXXXXXX XXXXXXXX		AWR5 [R/W] XXXXXXXX XXXXXXXX		
00066CH	AWR6 [R/W] XXXXXXXX XXXXXXXX		AWR7 [R/W] XXXXXXXX XXXXXXXX		
000670H	MCRA [R/W] XXXXXXXX	MCRB [R/W] XXXXXXXX	Reserved		
000674H	Reserved				
000678H	IORW0 [R/W] XXXXXXXX	IORW1 [R/W] XXXXXXXX	IORW2 [R/W] XXXXXXXX	Reserved	
00067CH	Reserved				
000680H	CSER [R/W] 00000001	CHER [R/W] 11111111	Reserved	TCR [R/W] 0000**** *5	
000684H	RCRH [R/W] 00XXXXXX	RCRL [R/W] XXXX0XXX	Reserved		
000688H to 0007F8H	Reserved				
0007FCH	Reserved	MODR [W] XXXXXXXX	Reserved		Mode Register

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000800H to 000CFCH	Reserved				
000D00H	PDRD00 [R] XXXXXXXX	PDRD01 [R] XXXXXXXX	Reserved		R-bus Port Data Direct Read Register
000D04H	Reserved	PDRD05 [R] XXXXXXXX	PDRD06 [R] XXXXXXXX	PDRD07 [R] XXXXXXXX	
000D08H	PDRD08 [R] X - - X - - XX	PDRD09 [R] - - - - XXXX	PDRD10 [R] - - - - X - XX	Reserved	
000D0CH	Reserved		PDRD14 [R] XXXXXXXX	PDRD15 [R] - - - - XXXX	
000D10H	PDRD16 [R] XXXXXXXX	PDRD17 [R] XXXXXXXX	PDRD18 [R] - XXX - XXX	PDRD19 [R] - XXX - XXX	
000D14H	PDRD20 [R] - XXX - XXX	Reserved	PDRD22 [R] XXXX - X - X	PDRD23 [R] -X - XXXXX	
000D18H	PDRD24 [R] XXXXXXXX	Reserved	Reserved		
000D1CH	PDRD28 [R] XXXXXXXX	PDRD29 [R] XXXXXXXX	Reserved		
000D20H to 000D3CH	Reserved				
000D40H	DDR00 [R/W] 00000000	DDR01 [R/W] 00000000	Reserved		R-bus Port Direction Register
000D44H	Reserved	DDR05 [R/W] 00000000	DDR06 [R/W] 00000000	DDR07 [R/W] 00000000	
000D48H	DDR08 [R/W] 0 - - 0 - -00	DDR09 [R/W] - - - - 0000	DDR10 [R/W] - - - - 0 - 00	Reserved	
000D4CH	Reserved	Reserved	DDR14 [R/W] 00000000	DDR15 [R/W] - - - - 0000	
000D50H	DDR16 [R/W] 00000000	DDR17 [R/W] 00000000	DDR18 [R/W] - 000 - 000	DDR19 [R/W] - 000 - 000	
000D54H	DDR20 [R/W] - 000 - 000	Reserved	DDR22 [R/W] 0000 - 0 - 0	DDR23 [R/W] - 0 - 00000	
000D58H	DDR24 [R/W] 00000000	Reserved	Reserved	Reserved	
000D5CH	DDR28 [R/W] 00000000	DDR29 [R/W] 00000000	Reserved		
000D60H to 000D7CH	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000D80H	PFR00 [R/W] 00000000	PFR01 [R/W] 00000000	Reserved		R-bus Port Function Register
000D84H	Reserved	PFR05 [R/W] 00000000	PFR06 [R/W] 00000000	PFR07 [R/W] 00000000	
000D88H	PFR08 [R/W] 0 - - 0 - - 00	PFR09 [R/W] - - - - 0000	PFR10 [R/W] - - - - 0 - 00	Reserved	
000D8CH	Reserved		PFR14 [R/W] 00000000	PFR15 [R/W] - - - - 0000	
000D90H	PFR16 [R/W] 00000000	PFR17 [R/W] 00000000	PFR18 [R/W] - 000 - 000	PFR19 [R/W] - 000 - 000	
000D94H	PFR20 [R/W] - 000 - 000	Reserved	PFR22 [R/W] 0000 - 0 - 0	PFR23 [R/W] - 0 - 00000	
000D98H	PFR24 [R/W] 00000000	Reserved			
000D9CH	PFR28 [R/W] 00000000	PFR29 [R/W] 00000000	Reserved		
000DA0H to 000DBCH	Reserved				
000DC0H	EPFR00 [R/W] - - - - - - - -	EPFR01 [R/W] - - - - - - - -	Reserved		R-bus Extra Port Function Register
000DC4H	Reserved	EPFR05 [R/W] - - - - - - - -	EPFR06 [R/W] - - - - - - - -	EPFR07 [R/W] - - - - - - - -	
000DC8H	EPFR08 [R/W] - - - - - - - -	EPFR09 [R/W] - - - - - - - -	EPFR10 [R/W] - - - - - - - 0	Reserved	
000DCCH	Reserved		EPFR14 [R/W] 00000000	EPFR15 [R/W] - - - - 0000	
000DD0H	EPFR16 [R/W] 0000 - - - -	EPFR17 [R/W] - 000 - 000	EPFR18 [R/W] - 000 - 000	EPFR19 [R/W] - 0- - - 0- -	
000DD4H	EPFR20 [R/W] - 000 - 000	Reserved	EPFR22 [R/W] - - - - - - - -	EPFR23 [R/W] - - - - - - - -	
000DD8H	EPFR24 [R/W] - - - - - - - -	Reserved			
000DDCH	EPFR28 [R/W] - 000 - 000	EPFR29 [R/W] - - - - - - - -	Reserved		
000DE0H to 000DFCH	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000E00H	PODR00 [R/W] 00000000	PODR01 [R/W] 00000000	Reserved		R-bus Port Output Drive Select Register
000E04H	Reserved	PODR05 [R/W] 00000000	PODR06 [R/W] 00000000	PODR07 [R/W] 00000000	
000E08H	PODR08 [R/W] 0 - - 0 - - 00	PODR09 [R/W] - - - - 0000	PODR10 [R/W] - - - - 0 - 00	Reserved	
000E0CH	Reserved		PODR14 [R/W] 00000000	PODR15 [R/W] - - - - 0000	
000E10H	PODR16 [R/W] 00000000	PODR17 [R/W] 0000 - - - -	PODR18 [R/W] - 000 - 000	PODR19 [R/W] - 000 - 000	
000E14H	PODR20 [R/W] - 000 - 000	Reserved	PODR22 [R/W] 0000 - 0 - 0	PODR23 [R/W] - 0 - 00000	
000E18H	PODR24 [R/W] 00000000	Reserved			
000E1CH	PODR28 [R/W] 00000000	PODR29 [R/W] 00000000	Reserved		
000E20H to 000E3CH	Reserved				
000E40H	PILR00 [R/W] 00000000	PILR01 [R/W] 00000000	Reserved		R-bus Port Input Level Select Register
000E44H	Reserved	PILR05 [R/W] 00000000	PILR06 [R/W] 00000000	PILR07 [R/W] 00000000	
000E48H	PILR08 [R/W] 0 - - 0 - - 00	PILR09 [R/W] - - - - 0000	PILR10 [R/W] - - - - 0 - 00	Reserved	
000E4CH	Reserved		PILR14 [R/W] 00000000	PILR15 [R/W] - - - - 0000	
000E50H	PILR16 [R/W] 00000000	PILR17 [R/W] 0000 - - - -	PILR18 [R/W] - 000 - 000	PILR19 [R/W] - 000 - 000	
000E54H	PILR20 [R/W] - 000 - 000	Reserved	PILR22 [R/W] 0000 - 0 - 0	PILR23 [R/W] - 0 - 00000	
000E58H	PILR24 [R/W] 00000000	Reserved			
000E5CH	PILR28 [R/W] 00000000	PILR29 [R/W] 00000000	Reserved		
000E60H to 000E7CH	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000E80H	EPILR00 [R/W] 00000000	EPILR01 [R/W] 00000000	Reserved		R-bus Extra Port Input Level Select Register
000E84H	Reserved	EPILR05 [R/W] 00000000	EPILR06 [R/W] 00000000	EPILR07 [R/W] 00000000	
000E88H	EPILR08 [R/W] 0 - - 0 - - 00	EPILR09 [R/W] - - - - 0000	EPILR10 [R/W] - - - - 0 - 00	Reserved	
000E8CH	Reserved		EPILR14 [R/W] 00000000	EPILR15 [R/W] - - - - 0000	
000E90H	EPILR16 [R/W] 00000000	EPILR17 [R/W] 0000 - - - -	EPILR18 [R/W] - 000 - 000	EPILR19 [R/W] - 000 - 000	
000E94H	EPILR20 [R/W] - 000 - 000	Reserved	EPILR22 [R/W] 0000 - 0 - 0	EPILR23 [R/W] - 0 - 00000	
000E98H	EPILR24 [R/W] 00000000	Reserved			
000E9CH	EPILR28 [R/W] 00000000	EPILR29 [R/W] 00000000	Reserved		
000EA0H to 000EBCH	Reserved				
000EC0H	PPER00 [R/W] 00000000	PPER01 [R/W] 00000000	Reserved		R-bus Port Pull-Up/Down Enable Register
000EC4H	Reserved	PPER05 [R/W] 00000000	PPER06 [R/W] 00000000	PPER07 [R/W] 00000000	
000EC8H	PPER08 [R/W] 0 - - 0 - - 00	PPER09 [R/W] - - - - 0000	PPER10 [R/W] - - - - 0 - 00	Reserved	
000ECCH	Reserved		PPER14 [R/W] 00000000	PPER15 [R/W] - - - - 0000	
000ED0H	PPER16 [R/W] 00000000	PPER17 [R/W] 0000 - - - -	PPER18 [R/W] - 000 - 000	PPER19 [R/W] - 000 - 000	
000ED4H	PPER20 [R/W] - 000 - 000	Reserved	PPER22 [R/W] 0000 - 0 - 0	PPER23 [R/W] - 0 - 00000	
000ED8H	PPER24 [R/W] 00000000	Reserved			
000EDCH	PPER28 [R/W] 00000000	PPER29 [R/W] 00000000	Reserved		
000EE0H to 000EFCH	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
000F00H	PPCR00 [R/W] 11111111	PPCR01 [R/W] 11111111	Reserved		R-bus Port Pull-Up/Down Control Register
000F04H	Reserved	PPCR05 [R/W] 11111111	PPCR06 [R/W] 11111111	PPCR07 [R/W] 11111111	
000F08H	PPCR08 [R/W] 1 - - 1- - 11	PPCR09 [R/W] - - - - 1111	PPCR10 [R/W] - - - - 1 - 11	Reserved	
000F0CH	Reserved		PPCR14 [R/W] 11111111	PPCR15 [R/W] - - - - 1111	
000F10H	PPCR16 [R/W] 11111111	PPCR17 [R/W] 11111111	PPCR18 [R/W] - 111 - 111	PPCR19 [R/W] - 111 - 111	
000F14H	PPCR20 [R/W] - 111 - 111	Reserved	PPCR22 [R/W] 1111 - 1 - 1	PPCR23 [R/W] - 1 - 11111	
000F18H	PPCR24 [R/W] 11111111	Reserved			
000F1CH	PPCR28 [R/W] 11111111	PPCR29 [R/W] 11111111	Reserved		
000F20H to 000F3CH	Reserved				
001000H	DMASA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				DMAC
001004H	DMADA0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001008H	DMASA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00100CH	DMADA1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001010H	DMASA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001014H	DMADA2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001018H	DMASA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00101CH	DMADA3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001020H	DMASA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
001024H	DMADA4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
001028H to 001FFCH	Reserved				
002000H to 006FFCH	MB91F467SA Flash-cache size is 8 Kbytes : 004000H to 005FFCH				Flash-cache / I-RAM area
007000H	FMCS [R/W] 01101000	FMCR [R] - - - 00000	FCHCR [R/W] - - - - - - 00 10000011		Flash Memory/ Flash-cache/ I-RAM Control Register
007004H	FMWT [R/W] 11111111 11111111		FMWT2 [R] - 001 - - - -	FMPS [R/W] - - - - - 000	
007008H	FMAC [R] 00000000 00000000 00000000 00000000				
00700CH	FCHA0 [R/W] - - - - - - - - - - - 00000 00000000 00000000				Flash-cache Non-cacheable area setting Register
007010H	FCHA1 [R/W] - - - - - - - - - - - 00000 00000000 00000000				
007014H to 0071FCH	Reserved				
007200H	RHCTRL[R/W] 00 - - 0000 - - - - - - - - 0000 - 000 - - - - - - - -				Automotive Remote Handler Control
007204H	Reserved				
007208H	CHCTRL0[R/W] - - - - 0 - - - 000 - - - 00 00000000 - - 00 - - 000				APIXfi Control/Status
00720CH	CHSTAT0[R] 00000000 - - - - - - - - 00000000 00000000				
007210H	CHWDG0[R/W] 00 - - 0000 00000000 xxxxxxxx xxxxxxxx				
007214H	CHCTRL1[R/W] - - - - 0 - - - 000 - - - 00 00000000 - - 00 - - 000				
007218H	CHSTAT1[R] 00000000 - - - - - - - - 00000000 00000000				
00721CH	CHWDG1[R/W] 00 - - 0000 00000000 xxxxxxxx xxxxxxxx				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
007220H	TBCTRL00[R/W] - - - 00000 0000 - 000		TBCTRL01[R/W] - - - 00000 0000 - 000		Automotive Remote Handler Transaction Buffer Control
007224H	TBCTRL02[R/W] - - - 00000 0000 - 000		TBCTRL03[R/W] - - - 00000 0000 - 000		
007228H	TBCTRL04[R/W] - - - 00000 0000 - 000		TBCTRL05[R/W] - - - 00000 0000 - 000		
00722CH	TBCTRL06[R/W] - - - 00000 0000 - 000		TBCTRL07[R/W] - - - 00000 0000 - 000		
007230H	TBCTRL08[R/W] - - - 00000 0000 - 000		TBCTRL09[R/W] - - - 00000 0000 - 000		
007234H	TBCTRL10[R/W] - - - 00000 0000 - 000		TBCTRL11[R/W] - - - 00000 0000 - 000		
007238H	TBCTRL12[R/W] - - - 00000 0000 - 000		TBCTRL13[R/W] - - - 00000 0000 - 000		
00723CH	TBCTRL14[R/W] - - - 00000 0000 - 000		TBCTRL15[R/W] - - - 00000 0000 - 000		
007240H	TBIRQ[R] 00000000 00000000		Reserved		Automotive Remote Handler Interrupt
007244H to 00724CH	Reserved				
007250H	TFCRTL00[R/W] 00 - 00000	TFIDX00[R/W] 00000000	TFCRTL01[R/W] 00 - 00000	TFIDX01[R/W] 00000000	Transaction Frame
007254H	TFCRTL02[R/W] 00 - 00000	TFIDX02[R/W] 00000000	TFCRTL03[R/W] 00 - 00000	TFIDX03[R/W] 00000000	
007258H	TFCRTL04[R/W] 00 - 00000	TFIDX04[R/W] 00000000	TFCRTL05[R/W] 00 - 00000	TFIDX05[R/W] 00000000	
00725CH	TFCRTL06[R/W] 00 - 00000	TFIDX06[R/W] 00000000	TFCRTL07[R/W] 00 - 00000	TFIDX07[R/W] 00000000	
007260H	TFCRTL08[R/W] 00 - 00000	TFIDX08[R/W] 00000000	TFCRTL09[R/W] 00 - 00000	TFIDX09[R/W] 00000000	
007264H	TFCRTL10[R/W] 00 - 00000	TFIDX10[R/W] 00000000	TFCRTL11[R/W] 00 - 00000	TFIDX11[R/W] 00000000	
007268H	TFCRTL12[R/W] 00 - 00000	TFIDX12[R/W] 00000000	TFCRTL13[R/W] 00 - 00000	TFIDX13[R/W] 00000000	
00726CH	TFCRTL14[R/W] 00 - 00000	TFIDX14[R/W] 00000000	TFCRTL15[R/W] 00 - 00000	TFIDX15[R/W] 00000000	
007270H	TFADDR00[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
007274H	TFADDR01[R/W] - - - - - - - - - - - - 0000 00000000 00000000				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
007278H	TFADDR02[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
00727CH	TFADDR03[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
007280H	TFADDR04[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
007284H	TFADDR05[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
007288H	TFADDR06[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
00728CH	TFADDR07[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
007290H	TFADDR08[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
007294H	TFADDR09[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
007298H	TFADDR10[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
00729CH	TFADDR11[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
0072A0H	TFADDR12[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
0072A4H	TFADDR13[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
0072A8H	TFADDR14[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
0072ACH	TFADDR15[R/W] - - - - - - - - - - - - 0000 00000000 00000000				
0072B0H	TFDATA00[R/W] 00000000 00000000 00000000 00000000				
0072B4H	TFDATA01[R/W] 00000000 00000000 00000000 00000000				
0072B8H	TFDATA02[R/W] 00000000 00000000 00000000 00000000				
0072BCH	TFDATA03[R/W] 00000000 00000000 00000000 00000000				
0072C0H	TFDATA04[R/W] 00000000 00000000 00000000 00000000				
0072C4H	TFDATA05[R/W] 00000000 00000000 00000000 00000000				
0072C8H	TFDATA06[R/W] 00000000 00000000 00000000 00000000				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
0072CC$_H$	TFDATA07[R/W] 00000000 00000000 00000000 00000000				
0072D0$_H$	TFDATA08[R/W] 00000000 00000000 00000000 00000000				
0072D4$_H$	TFDATA09[R/W] 00000000 00000000 00000000 00000000				
0072D8$_H$	TFDATA10[R/W] 00000000 00000000 00000000 00000000				
0072DC$_H$	TFDATA11[R/W] 00000000 00000000 00000000 00000000				
0072E0$_H$	TFDATA12[R/W] 00000000 00000000 00000000 00000000				
0072E4$_H$	TFDATA13[R/W] 00000000 00000000 00000000 00000000				
0072E8$_H$	TFDATA14[R/W] 00000000 00000000 00000000 00000000				
0072EC$_H$	TFDATA15[R/W] 00000000 00000000 00000000 00000000				
0072F0$_H$	EVCTRL[R/W] - - - - - - - 0 0 - 000000 00000000 00000000				Automotive Remote Handler Eventcontrol
0072F4$_H$	Reserved				
0072F8$_H$	EVBUF0[R/W] - - - - - - - 0 00000000 - - - - - - - - - - - - - - - -				Automotive Remote Handler Eventqueue
0072FC$_H$	EVBUF1[R/W] 00000000 00000000 00000000 00000000				
007300$_H$	APCFG00[R/W] 00000000 00110000 00000000 10010000				APIX^{fi} Configuration
007304$_H$	APCFG01[R/W] 11110000 10000000 00000000 01001000				
007308$_H$	APCFG02[R/W] 00000010 00000010 01000000 - - - - - - - -				
00730C$_H$	APCFG03[R/W] 00100110 10100000 10011010 00 - - - 000				
007310$_H$	APCFG10[R/W] 00000000 00110000 00000000 10010000				
007314$_H$	APCFG11[R/W] 11110000 00000000 00000000 01001000				
007318$_H$	APCFG12[R/W] 00000010 00000010 01000000 - - - - - - - -				
00731C$_H$	APCFG13[R/W] 00100110 10100100 10011010 00 - - - 000				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
007320H	MODULEID[R] 0 - - - - - - - ******** ******** ******** *6				Version of APIXfi Controller
007324H to 007FFCH	Reserved				
008000H to 00BFFCH	MB91F467SA Boot-ROM size is 4 Kbytes : 00B000H to 00BFFCH (instruction access is 1 wait cycle, data access is 1 wait cycle)				Boot ROM area
00C000H	CTRLR0 [R/W] 00000000 00000001		STATR0 [R/W] 00000000 00000000		CAN 0 Control Register
00C004H	ERRCNT0 [R] 00000000 00000000		BTR0 [R/W] 00100011 00000001		
00C008H	INTR0 [R] 00000000 00000000		TESTR0 [R/W] 00000000 X0000000		
00C00CH	BRPE0 [R/W] 00000000 00000000		CBSYNC*2		
00C010H	IF1CREQ0 [R/W] 00000000 00000001		IF1CMSK0 [R/W] 00000000 00000000		CAN 0 IF 1 Register
00C014H	IF1MSK20 [R/W] 11111111 11111111		IF1MSK10 [R/W] 11111111 11111111		
00C018H	IF1ARB20 [R/W] 00000000 00000000		IF1ARB10 [R/W] 00000000 00000000		
00C01CH	IF1MCTR0 [R/W] 00000000 00000000		Reserved		
00C020H	IF1DTA10 [R/W] 00000000 00000000		IF1DTA20 [R/W] 00000000 00000000		CAN 0 IF 1 Register
00C024H	IF1DTB10 [R/W] 00000000 00000000		IF1DTB20 [R/W] 00000000 00000000		
00C028H, 00C02CH	Reserved				
00C030H	IF1DTA20 [R/W] 00000000 00000000		IF1DTA10 [R/W] 00000000 00000000		
00C034H	IF1DTB20 [R/W] 00000000 00000000		IF1DTB10 [R/W] 00000000 00000000		
00C038H, 00C03CH	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00C040H	IF2CREQ0 [R/W] 00000000 00000001		IF2CMSK0 [R/W] 00000000 00000000		CAN 0 IF 2 Register
00C044H	IF2MSK20 [R/W] 11111111 11111111		IF2MSK10 [R/W] 11111111 11111111		
00C048H	IF2ARB20 [R/W] 00000000 00000000		IF2ARB10 [R/W] 00000000 00000000		
00C04CH	IF2MCTR0 [R/W] 00000000 00000000		Reserved		
00C050H	IF2DTA10 [R/W] 00000000 00000000		IF2DTA20 [R/W] 00000000 00000000		
00C054H	IF2DTB10 [R/W] 00000000 00000000		IF2DTB20 [R/W] 00000000 00000000		
00C058H, 00C05CH	Reserved				
00C060H	IF2DTA20 [R/W] 00000000 00000000		IF2DTA10 [R/W] 00000000 00000000		
00C064H	IF2DTB20 [R/W] 00000000 00000000		IF2DTB10 [R/W] 00000000 00000000		
00C068H to 00C07CH	Reserved				
00C080H	TREQR20 [R] 00000000 00000000		TREQR10 [R] 00000000 00000000		CAN 0 Status Flags
00C084H to 00C08CH	Reserved				
00C090H	NEWDT20 [R] 00000000 00000000		NEWDT10 [R] 00000000 00000000		
00C094H to 00C09CH	Reserved				
00C0A0H	INTPND20 [R] 00000000 00000000		INTPND10 [R] 00000000 00000000		
00C0A4H to 00C0ACH	Reserved				
00C0B0H	MSGVAL20 [R] 00000000 00000000		MSGVAL10 [R] 00000000 00000000		
00C0B4H to 00C0FCH	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00C100H	CTRLR1 [R/W] 00000000 00000001		STATR1 [R/W] 00000000 00000000		CAN 1 Control Register
00C104H	ERRCNT1 [R] 00000000 00000000		BTR1 [R/W] 00100011 00000001		
00C108H	INTR1 [R] 00000000 00000000		TESTR1 [R/W] 00000000 X0000000		
00C10CH	BRPE1 [R/W] 00000000 00000000		Reserved		
00C110H	IF1CREQ1 [R/W] 00000000 00000001		IF1CMSK1 [R/W] 00000000 00000000		CAN 1 IF 1 Register
00C114H	IF1MSK21 [R/W] 11111111 11111111		IF1MSK11 [R/W] 11111111 11111111		
00C118H	IF1ARB21 [R/W] 00000000 00000000		IF1ARB11 [R/W] 00000000 00000000		
00C11CH	IF1MCTR1 [R/W] 00000000 00000000		Reserved		
00C120H	IF1DTA11 [R/W] 00000000 00000000		IF1DTA21 [R/W] 00000000 00000000		
00C124H	IF1DTB11 [R/W] 00000000 00000000		IF1DTB21 [R/W] 00000000 00000000		
00C128H, 00C12CH	Reserved				CAN 1 IF 1 Register
00C130H	IF1DTA21 [R/W] 00000000 00000000		IF1DTA11 [R/W] 00000000 00000000		
00C134H	IF1DTB21 [R/W] 00000000 00000000		IF1DTB11 [R/W] 00000000 00000000		
00C138H, 00C13CH	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00C140H	IF2CREQ1 [R/W] 00000000 00000001		IF2CMSK1 [R/W] 00000000 00000000		CAN 1 IF 2 Register
00C144H	IF2MSK21 [R/W] 11111111 11111111		IF2MSK11 [R/W] 11111111 11111111		
00C148H	IF2ARB21 [R/W] 00000000 00000000		IF2ARB11 [R/W] 00000000 00000000		
00C14CH	IF2MCTR1 [R/W] 00000000 00000000		Reserved		
00C150H	IF2DTA11 [R/W] 00000000 00000000		IF2DTA21 [R/W] 00000000 00000000		
00C154H	IF2DTB11 [R/W] 00000000 00000000		IF2DTB21 [R/W] 00000000 00000000		
00C158H, 00C15CH	Reserved				
00C160H	IF2DTA21 [R/W] 00000000 00000000		IF2DTA11 [R/W] 00000000 00000000		
00C164H	IF2DTB21 [R/W] 00000000 00000000		IF2DTB11 [R/W] 00000000 00000000		
00C168H to 00C17CH	Reserved				
00C180H	TREQR21 [R] 00000000 00000000		TREQR11 [R] 00000000 00000000		CAN 1 Status Flags
00C184H to 00C18CH	Reserved				
00C190H	NEWDT21 [R] 00000000 00000000		NEWDT11 [R] 00000000 00000000		
00C194H to 00C19CH	Reserved				
00C1A0H	INTPND21 [R] 00000000 00000000		INTPND11 [R] 00000000 00000000		CAN 1 Status Flags
00C1A4H to 00C1ACH	Reserved				
00C1B0H	MSGVAL21 [R] 00000000 00000000		MSGVAL11 [R] 00000000 00000000		
00C1B4H to 00C1FCH	Reserved				

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00C200H to 00EFFCH	Reserved				
00F000H	BCTRL [R/W] - - - - - - - - - - - - - - - - 11111100 00000000				EDSU / MPU
00F004H	BSTAT [R/W] - 000 00000000 10 - - 0000				
00F008H	BIAC [R] - - - - - - - - - - - - - - - - 00000000 00000000				
00F00CH	BOAC [R] - - - - - - - - - - - - - - - - 00000000 00000000				
00F010H	BIRQ [R/W] - - - - - - - - - - - - - - - - 00000000 00000000				
00F014H to 00F01CH	Reserved				
00F020H	BCR0 [R/W] - - - - - - - - 00000000 00000000 00000000				
00F024H	BCR1 [R/W] - - - - - - - - 00000000 00000000 00000000				
00F028H	BCR2 [R/W] - - - - - - - - 00000000 00000000 00000000				
00F02CH	BCR3 [R/W] - - - - - - - - 00000000 00000000 00000000				
00F030H to 00F07CH	Reserved				
00F080H	BAD0 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
00F084H	BAD1 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F088H	BAD2 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F08CH	BAD3 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F090H	BAD4 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F094H	BAD5 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F098H	BAD6 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				

(Continued)

(Continued)

Address	Register				Block
	+ 0	+ 1	+ 2	+ 3	
00F09C$_H$	BAD7 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				EDSU / MPU
00F0A0$_H$	BAD8 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A4$_H$	BAD9 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0A8$_H$	BAD10 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0AC$_H$	BAD11 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B0$_H$	BAD12 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B4$_H$	BAD13 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0B8$_H$	BAD14 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0BC$_H$	BAD15 [R/W] XXXXXXXX XXXXXXXX XXXXXXXX XXXXXXXX				
00F0C0$_H$ to 01FFFC$_H$	Reserved				
020000$_H$ to 02FFFC$_H$	MB91F467SA D-RAM size is 32 Kbytes : 028000$_H$ to 02FFFC$_H$ (data access is 0 wait cycles)				D-RAM area
030000$_H$ to 037FFC$_H$	MB91F467SA ID-RAM size is 32 Kbytes : 030000$_H$ to 037FFC$_H$ (instruction access is 0 wait cycles, data access is 1 wait cycle)				ID-RAM area
038000$_H$ to 03FFFC$_H$	Reserved				

*1 : Use a read access (byte or halfword) to this address to synchronize the CPU operation (e.g. the interrupt acceptance of the CPU) to a preceding write access to the resources on R-bus (e.g. to an interrupt flag) on following address (0x0000-0x01FF, 0x0280-0x037F, 0x0400-0x063F and 0x0C00-0x0FFF).

*2 : Use a read access (byte or halfword) to this address to synchronize the CPU operation (e.g. the interrupt acceptance of the CPU) to a preceding write access to the CANS on D-bus (e.g. to an interrupt flag) on following address (0x0000-0xFFFF).

*3 : depends on the number of available CAN channels

*4 : ACR0 [11 : 10] depends on Mode vector fetch information on bus width

*5 **:** TCR [3 **:** 0] INIT value = 0000**,** keeps value after RST

*6 **:** Datecode of APIX^{fi} controller version

2. Flash memory and external bus area

32bit write mode	dat[31:0]				dat[31:0]				
16bit write mode	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
040000H to 05FFF8H	SA8 (64kB)				SA9 (64kB)				ROMS0
060000H to 07FFF8H	SA10 (64kB)				SA11 (64kB)				ROMS1
080000H to 09FFF8H	SA12 (64kB)				SA13 (64kB)				ROMS2
0A0000H to 0BFFF8H	SA14 (64kB)				SA15 (64kB)				ROMS3
0C0000H to 0DFFF8H	SA16 (64kB)				SA17 (64kB)				ROMS4
0E0000H to 0FFFF0H	SA18 (64kB)				SA19 (64kB)				ROMS5
0FFFF8H	FMV [R] 06 00 00 00H				FRV [R] 00 00 BF F8H				
100000H to 11FFF8H	SA20 (64kB)				SA21 (64kB)				ROMS6
120000H to 13FFF8H	SA22 (64kB)				SA23 (64kB)				
140000H to 143FF8H	SA0 (8kB)				SA1 (8kB)				ROMS7
144000H to 17FF8H	SA2 (8kB)				SA3 (8kB)				
148000H to 14BFF8H	SA4 (8kB)				SA5 (8kB)				
14C000H to 14FFF8H	SA6 (8kB)				SA7 (8kB)				
150000H to 17FFF8H	Reserved								

(Continued)

(Continued)

32bit write mode	dat[31:0]				dat[31:0]				
16bit write mode	dat[31:16]		dat[15:0]		dat[31:16]		dat[15:0]		
Address	Register								Block
	+ 0	+ 1	+ 2	+ 3	+ 4	+ 5	+ 6	+ 7	
180000H to 1BFFF8H	External Bus Area								ROMS8
1C0000H to 1FFFF8H									ROMS9
200000H to 27FFF8H									ROMS10
280000H to 2FFFF8H									ROMS11
300000H to 37FFF8H									ROMS12
380000H to 3FFFF8H									ROMS13
400000H to 47FFF8H									ROMS14
480000H to 4FFFF8H									ROMS15

Note: Write operations to address 0FFFF8H and 0FFFFCH are not possible. When reading these addresses, the values shown above will be read.

■ INTERRUPT VECTOR TABLE

Interrupt	Interrupt number		Interrupt level*1		Interrupt vector*2		DMA	
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default Vector address	RN*5	Stop*6
Reset	0	00			3FC$_H$	000FFFFC$_H$		
Mode vector	1	01			3F8$_H$	000FFFF8$_H$		
System reserved	2	02			3F4$_H$	000FFFF4$_H$		
System reserved	3	03			3F0$_H$	000FFFF0$_H$		
System reserved	4	04			3EC$_H$	000FFFEC$_H$		
CPU supervisor mode (INT #5 instruction) *7	5	05			3E8$_H$	000FFFE8$_H$		
Memory Protection exception *7	6	06			3E4$_H$	000FFFE4$_H$		
System reserved	7	07			3E0$_H$	000FFFE0$_H$		
System reserved	8	08			3DC$_H$	000FFFDC$_H$		
System reserved	9	09			3D8$_H$	000FFFD8$_H$		
System reserved	10	0A			3D4$_H$	000FFFD4$_H$		
System reserved	11	0B			3D0$_H$	000FFFD0$_H$		
System reserved	12	0C			3CC$_H$	000FFFCC$_H$		
System reserved	13	0D			3C8$_H$	000FFFC8$_H$		
Undefined instruction exception	14	0E			3C4$_H$	000FFFC4$_H$		
NMI request	15	0F	F$_H$ fixed		3C0$_H$	000FFFC0$_H$		
External Interrupt 0	16	10	ICR00	440$_H$	3BC$_H$	000FFFBC$_H$	0, 16	
External Interrupt 1	17	11			3B8$_H$	000FFFB8$_H$	1, 17	
External Interrupt 2	18	12	ICR01	441$_H$	3B4$_H$	000FFFB4$_H$	2, 18	
External Interrupt 3	19	13			3B0$_H$	000FFFB0$_H$	3, 19	
External Interrupt 4	20	14	ICR02	442$_H$	3AC$_H$	000FFFAC$_H$	20	
External Interrupt 5	21	15			3A8$_H$	000FFFA8$_H$	21	
External Interrupt 6	22	16	ICR03	443$_H$	3A4$_H$	000FFFA4$_H$	22	
External Interrupt 7	23	17			3A0$_H$	000FFFA0$_H$	23	
External Interrupt 8	24	18	ICR04	444$_H$	39C$_H$	000FFF9C$_H$		
External Interrupt 9	25	19			398$_H$	000FFF98$_H$		
External Interrupt 10	26	1A	ICR05	445$_H$	394$_H$	000FFF94$_H$		
External Interrupt 11	27	1B			390$_H$	000FFF90$_H$		
External Interrupt 12	28	1C	ICR06	446$_H$	38C$_H$	000FFF8C$_H$		
External Interrupt 13	29	1D			388$_H$	000FFF88$_H$		

(Continued)

Interrupt	Interrupt number		Interrupt level[*1]		Interrupt vector[*2]		DMA	
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default Vector address	RN[*5]	Stop[*6]
External Interrupt 14	30	1E	ICR07	447H	384H	000FFF84H		
External Interrupt 15	31	1F			380H	000FFF80H		
Reload Timer 0	32	20	ICR08	448H	37CH	000FFF7CH	4, 32	
Reload Timer 1	33	21			378H	000FFF78H	5, 33	
Reload Timer 2	34	22	ICR09	449H	374H	000FFF74H	34	
Reload Timer 3	35	23			370H	000FFF70H	35	
Reload Timer 4	36	24	ICR10	44AH	36CH	000FFF6CH	36	
Reload Timer 5	37	25			368H	000FFF68H	37	
Reload Timer 6	38	26	ICR11	44BH	364H	000FFF64H	38	
Reload Timer 7	39	27			360H	000FFF60H	39	
Free Run Timer 0	40	28	ICR12	44CH	35CH	000FFF5CH	40	
Free Run Timer 1	41	29			358H	000FFF58H	41	
Free Run Timer 2	42	2A	ICR13	44DH	354H	000FFF54H	42	
Free Run Timer 3	43	2B			350H	000FFF50H	43	
Free Run Timer 4	44	2C	ICR14	44EH	34CH	000FFF4CH	44	
Free Run Timer 5	45	2D			348H	000FFF48H	45	
Free Run Timer 6	46	2E	ICR15	44FH	344H	000FFF44H	46	
Free Run Timer 7	47	2F			340H	000FFF40H	47	
CAN 0	48	30	ICR16	450H	33CH	000FFF3CH		
CAN 1	49	31			338H	000FFF38H		
System reserved	50	32	ICR17	451H	334H	000FFF34H		
System reserved	51	33			330H	000FFF30H		
System reserved	52	34	ICR18	452H	32CH	000FFF2CH		
System reserved	53	35			328H	000FFF28H		
System reserved	54	36	ICR19	453H	324H	000FFF24H	6, 48	
System reserved	55	37			320H	000FFF20H	7, 49	
System reserved	56	38	ICR20	454H	31CH	000FFF1CH	8, 50	
System reserved	57	39			318H	000FFF18H	9, 51	
LIN-USART 2 RX	58	3A	ICR21	455H	314H	000FFF14H	52	
LIN-USART 2 TX	59	3B			310H	000FFF10H	53	
LIN-USART 3 RX	60	3C	ICR22	456H	30CH	000FFF0CH	54	
LIN-USART 3 TX	61	3D			308H	000FFF08H	55	

(Continued)

Interrupt	Interrupt number		Interrupt level*1		Interrupt vector*2		DMA	
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default Vector address	RN*5	Stop*6
System reserved	62	3E	ICR23 *3	457H	304H	000FFF04H		
Delayed Interrupt	63	3F			300H	000FFF00H		
System reserved *4	64	40	(ICR24)	(458H)	2FCH	000FFEFCH		
System reserved *4	65	41			2F8H	000FFEF8H		
LIN-USART (FIFO) 4 RX	66	42	ICR25	459H	2F4H	000FFEF4H	10, 56	10, 56
LIN-USART (FIFO) 4 TX	67	43			2F0H	000FFEF0H	11, 57	
LIN-USART (FIFO) 5 RX	68	44	ICR26	45AH	2ECH	000FFEECH	12, 58	12, 58
LIN-USART (FIFO) 5 TX	69	45			2E8H	000FFEE8H	13, 59	
LIN-USART (FIFO) 6 RX	70	46	ICR27	45BH	2E4H	000FFEE4H	60	60
LIN-USART (FIFO) 6 TX	71	47			2E0H	000FFEE0H	61	
LIN-USART (FIFO) 7 RX	72	48	ICR28	45CH	2DCH	000FFEDCH	62	62
LIN-USART (FIFO) 7 TX	73	49			2D8H	000FFED8H	63	
I²C 0 / I²C 2	74	4A	ICR29	45DH	2D4H	000FFED4H	28, 30	28, 30
I²C 1	75	4B			2D0H	000FFED0H	29	29
APIXfi Event/ Eventlevel/ Eventbufferoverflow/ Fatal Error/ Watchdog	76	4C	ICR30	45EH	2CCH	000FFECCH		
System reserved	77	4D			2C8H	000FFEC8H	65	
System reserved	78	4E	ICR31	45FH	2C4H	000FFEC4H	66	
System reserved	79	4F			2C0H	000FFEC0H	67	
APIXfi Transaction Buffer	80	50	ICR32	460H	2BCH	000FFEBCH	160-175	160-175
System reserved	81	51			2B8H	000FFEB8H	69	
System reserved	82	52	ICR33	461H	2B4H	000FFEB4H	70	
System reserved	83	53			2B0H	000FFEB0H	71	
System reserved	84	54	ICR34	462H	2ACH	000FFEACH	72	
System reserved	85	55			2A8H	000FFEA8H	73	
System reserved	86	56	ICR35	463H	2A4H	000FFEA4H	74	
System reserved	87	57			2A0H	000FFEA0H	75	
System reserved	88	58	ICR36	464H	29CH	000FFE9CH	76	
System reserved	89	59			298H	000FFE98H	77	
System reserved	90	5A	ICR37	465H	294H	000FFE94H	78	
System reserved	91	5B			290H	000FFE90H	79	

(Continued)

Interrupt	Interrupt number		Interrupt level*1		Interrupt vector*2		DMA	
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default Vector address	RN*5	Stop*6
Input Capture 0	92	5C	ICR38	466H	28CH	000FFE8CH	80	
Input Capture 1	93	5D			288H	000FFE88H	81	
Input Capture 2	94	5E	ICR39	467H	284H	000FFE84H	82	
Input Capture 3	95	5F			280H	000FFE80H	83	
Input Capture 4	96	60	ICR40	468H	27CH	000FFE7CH	84	
Input Capture 5	97	61			278H	000FFE78H	85	
Input Capture 6	98	62	ICR41	469H	274H	000FFE74H	86	
Input Capture 7	99	63			270H	000FFE70H	87	
Output Compare 0	100	64	ICR42	46AH	26CH	000FFE6CH	88	
Output Compare 1	101	65			268H	000FFE68H	89	
Output Compare 2	102	66	ICR43	46BH	264H	000FFE64H	90	
Output Compare 3	103	67			260H	000FFE60H	91	
System reserved	104	68	ICR44	46CH	25CH	000FFE5CH	92	
System reserved	105	69			258H	000FFE58H	93	
System reserved	106	6A	ICR45	46DH	254H	000FFE54H	94	
System reserved	107	6B			250H	000FFE50H	95	
Sound Generator	108	6C	ICR46	46EH	24CH	000FFE4CH		
Phase Frequency Modulator	109	6D			248H	000FFE48H		
System reserved	110	6E	ICR47 *3	46FH	244H	000FFE44H		
System reserved	111	6F			240H	000FFE40H		
PPG0	112	70	ICR48	470H	23CH	000FFE3CH	15, 96	
PPG1	113	71			238H	000FFE38H	97	
PPG2	114	72	ICR49	471H	234H	000FFE34H	98	
PPG3	115	73			230H	000FFE30H	99	
PPG4	116	74	ICR50	472H	22CH	000FFE2CH	100	
PPG5	117	75			228H	000FFE28H	101	
PPG6	118	76	ICR51	473H	224H	000FFE24H	102	
PPG7	119	77			220H	000FFE20H	103	
PPG8	120	78	ICR52	474H	21CH	000FFE1CH	104	
PPG9	121	79			218H	000FFE18H	105	
PPG10	122	7A	ICR53	475H	214H	000FFE14H	106	
PPG11	123	7B			210H	000FFE10H	107	

(Continued)

(Continued)

Interrupt	Interrupt number		Interrupt level*1		Interrupt vector*2		DMA	
	Decimal	Hexadecimal	Setting Register	Register address	Offset	Default Vector address	RN*5	Stop*6
PPG12	124	7C	ICR54	476H	20CH	000FFE0CH	108	
PPG13	125	7D			208H	000FFE08H	109	
PPG14	126	7E	ICR55	477H	204H	000FFE04H	110	
PPG15	127	7F			200H	000FFE00H	111	
Up/Down Counter 0	128	80	ICR56	478H	1FCH	000FFDFCH		
Up/Down Counter 1	129	81			1F8H	000FFDF8H		
Up/Down Counter 2	130	82	ICR57	479H	1F4H	000FFDF4H		
Up/Down Counter 3	131	83			1F0H	000FFDF0H		
Real Time Clock	132	84	ICR58	47AH	1ECH	000FFDECH		
Calibration Unit	133	85			1E8H	000FFDE8H		
A/D Converter 0	134	86	ICR59	47BH	1E4H	000FFDE4H	14, 112	
System reserved	135	87			1E0H	000FFDE0H		
Alarm Comparator 0	136	88	ICR60	47CH	1DCH	000FFDDCH		
System reserved	137	89			1D8H	000FFDD8H		
Low Voltage Detection	138	8A	ICR61	47DH	1D4H	000FFDD4H		
SMC Comparator 0 to 5	139	8B			1D0H	000FFDD0H		
Timebase Overflow	140	8C	ICR62	47EH	1CCH	000FFDCCH		
PLL Clock Gear	141	8D			1C8H	000FFDC8H		
DMA Controller	142	8E	ICR63	47FH	1C4H	000FFDC4H		
Main/Sub OSC stability wait	143	8F			1C0H	000FFDC0H		
Security vector	144	90			1BCH	000FFDBCH		
Used by the INT instruction.	145 to 255	91 to FF			1B8H to 000H	000FFDB8H to 000FFC00H		

*1 : The ICRs are located in the interrupt controller and set the interrupt level for each interrupt request. An ICR is provided for each interrupt request.

*2 : The vector address for each EIT (exception, interrupt or trap) is calculated by adding the listed offset to the table base register value (TBR) . The TBR specifies the top of the EIT vector table. The addresses listed in the table are for the default TBR value (000FFC00H) . The TBR is initialized to this value by a reset. The TBR is set to 000FFC00H after the internal boot ROM is executed.

*3 : ICR23 and ICR47 can be exchanged by setting the REALOS compatibility bit (addr 0C03H : IOS[0])

*4 : Used by REALOS

*5 :DMA RN is the resource number used for DMA operation. No number means that this resource interrupt cannot be used to trigger a DMA transfer.

*6 :DMA Stop shows the DMA Transfer Stop Request feature.

*7 :Memory Protection Unit (MPU) support

■ RECOMMENDED SETTINGS

1. PLL and Clockgear settings

Please note that for MB91F467SA the core base clock frequencies are valid in the 1.8V operation mode of the Main regulator and Flash.

Recommended PLL divider and clockgear settings

PLL Input (CLK) [MHz]	Frequency Parameter		Clockgear Parameter		PLL Output (X) [MHz]	Core Base Clock [MHz]	Remarks
	DIVM	DIVN	DIVG	MULG	MULG		
4	2	25	16	24	200	100	
4	2	24	16	24	192	96	
4	2	23	16	24	184	92	
4	2	22	16	24	176	88	
4	2	21	16	20	168	84	
4	2	20	16	20	160	80	
4	2	19	16	20	152	76	
4	2	18	16	20	144	72	
4	2	17	16	16	136	68	
4	2	16	16	16	128	64	
4	2	15	16	16	120	60	
4	2	14	16	16	112	56	
4	2	13	16	12	104	52	
4	2	12	16	12	96	48	
4	2	11	16	12	88	44	
4	4	10	16	24	160	40	
4	4	9	16	24	144	36	
4	4	8	16	24	128	32	
4	4	7	16	24	112	28	
4	6	6	16	24	144	24	
4	8	5	16	28	160	20	
4	10	4	16	32	160	16	
4	12	3	16	32	144	12	

2. Clock Modulator settings

The clock modulator is currently being evaluated and should not be used for other purpose than testing.

The following table shows all possible settings for the Clock Modulator in a base clock frequency range from 32MHz up to 88MHz.

The Flash access time settings need to be adjusted according to Fmax while the PLL and clockgear settings should be set according to base clock frequency.

Clock Modulator settings, frequency range and supported supply voltage

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	3	026F	88	79.5	98.5	
1	3	026F	84	76.1	93.8	
1	3	026F	80	72.6	89.1	
1	5	02AE	80	68.7	95.8	
2	3	046E	80	68.7	95.8	
1	3	026F	76	69.1	84.5	
1	5	02AE	76	65.3	90.8	
1	7	02ED	76	62	98.1	
2	3	046E	76	65.3	90.8	
3	3	066D	76	62	98.1	
1	3	026F	72	65.5	79.9	
1	5	02AE	72	62	85.8	
1	7	02ED	72	58.8	92.7	
2	3	046E	72	62	85.8	
3	3	066D	72	58.8	92.7	
1	3	026F	68	62	75.3	
1	5	02AE	68	58.7	80.9	
1	7	02ED	68	55.7	87.3	
1	9	032C	68	53	95	
2	3	046E	68	58.7	80.9	
2	5	04AC	68	53	95	
3	3	066D	68	55.7	87.3	
4	3	086C	68	53	95	
1	3	026F	64	58.5	70.7	
1	5	02AE	64	55.3	75.9	
1	7	02ED	64	52.5	82	
1	9	032C	64	49.9	89.1	
1	11	036B	64	47.6	97.6	
2	3	046E	64	55.3	75.9	

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
2	5	04AC	64	49.9	89.1	
3	3	066D	64	52.5	82	
4	3	086C	64	49.9	89.1	
5	3	0A6B	64	47.6	97.6	
1	3	026F	60	54.9	66.1	
1	5	02AE	60	51.9	71	
1	7	02ED	60	49.3	76.7	
1	9	032C	60	46.9	83.3	
1	11	036B	60	44.7	91.3	
2	3	046E	60	51.9	71	
2	5	04AC	60	46.9	83.3	
3	3	066D	60	49.3	76.7	
4	3	086C	60	46.9	83.3	
5	3	0A6B	60	44.7	91.3	
1	3	026F	56	51.4	61.6	
1	5	02AE	56	48.6	66.1	
1	7	02ED	56	46.1	71.4	
1	9	032C	56	43.8	77.6	
1	11	036B	56	41.8	84.9	
1	13	03AA	56	39.9	93.8	
2	3	046E	56	48.6	66.1	
2	5	04AC	56	43.8	77.6	
2	7	04EA	56	39.9	93.8	
3	3	066D	56	46.1	71.4	
3	5	06AA	56	39.9	93.8	
4	3	086C	56	43.8	77.6	
5	3	0A6B	56	41.8	84.9	
6	3	0C6A	56	39.9	93.8	
1	3	026F	52	47.8	57	
1	5	02AE	52	45.2	61.2	
1	7	02ED	52	42.9	66.1	
1	9	032C	52	40.8	71.8	
1	11	036B	52	38.8	78.6	
1	13	03AA	52	37.1	86.8	
1	15	03E9	52	35.5	96.9	

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
2	3	046E	52	45.2	61.2	
2	5	04AC	52	40.8	71.8	
2	7	04EA	52	37.1	86.8	
3	3	066D	52	42.9	66.1	
3	5	06AA	52	37.1	86.8	
4	3	086C	52	40.8	71.8	
5	3	0A6B	52	38.8	78.6	
6	3	0C6A	52	37.1	86.8	
7	3	0E69	52	35.5	96.9	
1	3	026F	48	44.2	52.5	
1	5	02AE	48	41.8	56.4	
1	7	02ED	48	39.6	60.9	
1	9	032C	48	37.7	66.1	
1	11	036B	48	35.9	72.3	
1	13	03AA	48	34.3	79.9	
1	15	03E9	48	32.8	89.1	
2	3	046E	48	41.8	56.4	
2	5	04AC	48	37.7	66.1	
2	7	04EA	48	34.3	79.9	
3	3	066D	48	39.6	60.9	
3	5	06AA	48	34.3	79.9	
4	3	086C	48	37.7	66.1	
5	3	0A6B	48	35.9	72.3	
6	3	0C6A	48	34.3	79.9	
7	3	0E69	48	32.8	89.1	
1	3	026F	44	40.6	48.1	
1	5	02AE	44	38.4	51.6	
1	7	02ED	44	36.4	55.7	
1	9	032C	44	34.6	60.4	
1	11	036B	44	33	66.1	
1	13	03AA	44	31.5	73	
1	15	03E9	44	30.1	81.4	
2	3	046E	44	38.4	51.6	
2	5	04AC	44	34.6	60.4	
2	7	04EA	44	31.5	73	

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
2	9	0528	44	28.9	92.1	
3	3	066D	44	36.4	55.7	
3	5	06AA	44	31.5	73	
4	3	086C	44	34.6	60.4	
4	5	08A8	44	28.9	92.1	
5	3	0A6B	44	33	66.1	
6	3	0C6A	44	31.5	73	
7	3	0E69	44	30.1	81.4	
8	3	1068	44	28.9	92.1	
1	3	026F	40	37	43.6	
1	5	02AE	40	34.9	46.8	
1	7	02ED	40	33.1	50.5	
1	9	032C	40	31.5	54.8	
1	11	036B	40	30	59.9	
1	13	03AA	40	28.7	66.1	
1	15	03E9	40	27.4	73.7	
2	3	046E	40	34.9	46.8	
2	5	04AC	40	31.5	54.8	
2	7	04EA	40	28.7	66.1	
2	9	0528	40	26.3	83.3	
3	3	066D	40	33.1	50.5	
3	5	06AA	40	28.7	66.1	
3	7	06E7	40	25.3	95.8	
4	3	086C	40	31.5	54.8	
4	5	08A8	40	26.3	83.3	
5	3	0A6B	40	30	59.9	
6	3	0C6A	40	28.7	66.1	
7	3	0E69	40	27.4	73.7	
8	3	1068	40	26.3	83.3	
9	3	1267	40	25.3	95.8	
1	3	026F	36	33.3	39.2	
1	5	02AE	36	31.5	42	
1	7	02ED	36	29.9	45.3	
1	9	032C	36	28.4	49.2	
1	11	036B	36	27.1	53.8	

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
1	13	03AA	36	25.8	59.3	
1	15	03E9	36	24.7	66.1	
2	3	046E	36	31.5	42	
2	5	04AC	36	28.4	49.2	
2	7	04EA	36	25.8	59.3	
2	9	0528	36	23.7	74.7	
3	3	066D	36	29.9	45.3	
3	5	06AA	36	25.8	59.3	
3	7	06E7	36	22.8	85.8	
4	3	086C	36	28.4	49.2	
4	5	08A8	36	23.7	74.7	
5	3	0A6B	36	27.1	53.8	
6	3	0C6A	36	25.8	59.3	
7	3	0E69	36	24.7	66.1	
8	3	1068	36	23.7	74.7	
9	3	1267	36	22.8	85.8	
1	3	026F	32	29.7	34.7	
1	5	02AE	32	28	37.3	
1	7	02ED	32	26.6	40.2	
1	9	032C	32	25.3	43.6	
1	11	036B	32	24.1	47.7	
1	13	03AA	32	23	52.5	
1	15	03E9	32	22	58.6	
2	3	046E	32	28	37.3	
2	5	04AC	32	25.3	43.6	
2	7	04EA	32	23	52.5	
2	9	0528	32	21.1	66.1	
2	11	0566	32	19.5	89.1	
3	3	066D	32	26.6	40.2	
3	5	06AA	32	23	52.5	
3	7	06E7	32	20.3	75.9	
4	3	086C	32	25.3	43.6	
4	5	08A8	32	21.1	66.1	
5	3	0A6B	32	24.1	47.7	
5	5	0AA6	32	19.5	89.1	

(Continued)

(Continued)

Modulation Degree (k)	Random No (N)	CMPR [hex]	Baseclk [MHz]	Fmin [MHz]	Fmax [MHz]	Remarks
6	3	0C6A	32	23	52.5	
7	3	0E69	32	22	58.6	
8	3	1068	32	21.1	66.1	
9	3	1267	32	20.3	75.9	
10	3	1466	32	19.5	89.1	

2. Recommended operating conditions

($V_{SS}5 = AV_{SS}5 = 0.0$ V)

Parameter	Symbol	Value			Unit	Remarks
		Min	Typ	Max		
Power supply voltage	$V_{DD}5$	3.0		5.5	V	
	$V_{DD}5R$	3.0		5.5	V	Internal regulator
	$V_{DD}35$	3.0		5.5	V	External bus
	$V_{DD}A$	1.7		1.9	V	APIX[fi]
	$V_{PP}A$			50	mV	$V_{DD}A$, $V_{SS}A$ peak-peak supply noise
	$AV_{CC}5$	3.0		5.5	V	A/D converter
Smoothing capacitor	C_S		4.7		µ F	Use a X7R ceramic capacitor or a capacitor that has similar frequency characteristics. Use a capacitor with a capacitance greater than Cs as the smoothing capacitor on the supply pin.
Power supply slew rate				50	V/ms	
Operating temperature	T_A	Š 40		+ 105	°C	
Main Oscillation stabilization time		10			ms	
Lock-up time PLL (4 MHz ->16 ...100MHz)				0.6	ms	
ESD Protection (Human body model)	Vsurge	2			kV	$R_{discharge}$ = 1.5k $C_{discharge}$ = 100pF
RC Oscillator	$f_{RC100kHz}$ f_{RC2MHz}	50 1	100 2	200 4	kHz MHz	VDD_{CORE} 1.65V

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges. Operation outside these ranges may adversely affect reliability and could result in device failure.

No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS5} = AV_{SS}5 = 0$ V, T_A = Š40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input L voltage	V_{ILXDF}	X0		V_{SS5} Š 0.3		0.2 × V_{DD}	V	External clock in Fast Clock Input mode
Output H voltage	V_{OH2}	Normal outputs	4.5V V_{DD} 5.5V, I_{OH} = Š 2mA	V_{DD} Š 0.5			V	Driving strength set to 2 mA
			3.0V V_{DD} < 4.5V, I_{OH} = Š 1.6mA					
	V_{OH5}	Normal outputs	4.5V V_{DD} 5.5V, I_{OH} = Š 5mA	V_{DD} Š 0.5			V	Driving strength set to 5 mA
			3.0V V_{DD} < 4.5V, I_{OH} = Š 3mA					
	V_{OH3}	I^2C outputs	3.0V V_{DD} 5.5V, I_{OH} = Š 3mA	V_{DD} Š 0.5			V	
	V_{OH30}	High current outputs	4.5V V_{DD} 5.5V, T_A = -40 °C, I_{OH} = -40mA	V_{DD} Š 0.5			V	Driving strength set to 30mA
			4.5V V_{DD} 5.5V, I_{OH} = -30mA					
			3.0V V_{DD} < 4.5V, I_{OH} = -20mA					
Output L voltage	V_{OL2}	Normal outputs	4.5V V_{DD} 5.5V, I_{OL} = + 2mA			0.4	V	Driving strength set to 2 mA
			3.0V V_{DD} < 4.5V, I_{OL} = + 1.6mA					
	V_{OL5}	Normal outputs	4.5V V_{DD} 5.5V, I_{OL} = + 5mA			0.4	V	Driving strength set to 5 mA
			3.0V V_{DD} < 4.5V, I_{OL} = + 3mA					
	V_{OL3}	I^2C outputs	3.0V V_{DD} 5.5V, I_{OL} = + 3mA			0.4	V	
	V_{OL30}	High current outputs	4.5V V_{DD} 5.5V, T_A = -40 °C, I_{OL} = +40mA			0.5	V	Driving strength set to 30mA
			4.5V V_{DD} 5.5V, I_{OL} = +30mA					
			3.0V V_{DD} < 4.5V, I_{OL} = +20mA					

(Continued)

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS5} = AV_{SS}5 = 0$ V, T_A = Š40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Input leakage current	I_{IL}	Pnn_m *1	3.0V V_{DD} 5.5V $V_{SS5} < V_I < V_{DD}$ T_A = 25 °C	Š 1		+ 1	µA	
			3.0V V_{DD} 5.5V $V_{SS5} < V_I < V_{DD}$ T_A = 105 °C	Š 3		+ 3		
Analog input leakage current	I_{AIN}	ADIN	3.0V V_{DD} 5.5V AV_{SS5} V_I AV_{CC5} T_A = 25 °C	Š 1		+ 1	µA	
			3.0V V_{DD} 5.5V AV_{SS5} V_I AV_{CC5} T_A = 105 °C	Š 3		+ 3		
Sum input leakage	I_L	Pnn_m ALARM	V_{DD5} V_{IN} V_{SS5} A_{VCC5}, A_{VRH5} V_{IN} AV_{SS5} (1 to n) [max (|ILHi|, |ILLi|)] (n = number of IO = 133 GPIO + 1 ALARM)		13	130	µA	
Pull-up resistance	R_{UP}	Pnn_m *1, INITX	3.0V VDD 3.6V	40	100	160	k	
			4.5V VDD 5.5V	25	50	100		
Pull-down resistance	R_{DOWN}	Pnn_m *1	3.0V VDD 3.6V	40	100	160	k	
			4.5V VDD 5.5V	25	50	100		
APIX^{fi} terminal resistance	R_{TERM}	SDINM SDINP SD-OUTM SD-OUT-MP		35		65		

(Continued)

(Continued)

($V_{DD}5$ = $AV_{CC}5$ = 3.0 V to 5.5 V, V_{SS5} = $AV_{SS}5$ = 0 V, T_A = Š40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	Value			Unit	Remarks
				Min	Typ	Max		
Power supply current	I_{CC}	$V_{DD5}R$			125	155	mA	(Conditions at MB91F467SA) CLKB: 100 MHz CLKP: 50 MHz CLKT: 50 MHz CLKCAN: 40 MHz Code fetch from Flash
		V_{DDA}			12	60		APIX^{fi}
	I_{CCH}	$V_{DD5}R$	T_A = + 25 °C		30	150	µA	At stop mode *2
			T_A = + 105 °C		400	2000	µA	
			T_A = + 25 °C		100	500	µA	RTC : 4 MHz mode *2
			T_A = + 105 °C		500	2400	µA	
			T_A = + 25 °C		50	250	µA	RTC : 100 kHz mode *2
			T_A = + 105 °C		450	2200	µA	
		V_{DDA}			10	50	µA	APIX^{fi} power-down
	I_{LVE}	V_{DD5}			70	150	µA	External low voltage detection
	I_{LVI}	$V_{DD5}R$			50	100	µA	Internal low voltage detection
	I_{OSC}	V_{DD5}			250	500	µA	Main clock (4 MHz)
					20	40	µA	Sub clock (32 kHz)
Input capacitance	C_{IN}	All except V_{DD5}, $V_{DD5}R$, V_{SS5}, AV_{CC5}, AV_{SS}, V_{DDA}, V_{SSA},	f = 1 MHz		5	15	pF	

*1 Pnn_m includes all pins unless the pins, which include analog inputs.

*2 Main regulator OFF, sub regulator set to 1.2V, Low voltage detection disabled.

4. A/D converter characteristics

($V_{DD}5 = AV_{CC}5 = 3.0$ V to 5.5 V, $V_{SS}5 = AV_{SS}5 = 0$ V, T_A = Š40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Resolution					10	bit	
Total error			Š 3		+ 3	LSB	
Nonlinearity error			Š 2.5		+ 2.5	LSB	
Differential nonlinearity error			Š 1.9		+ 1.9	LSB	
Zero reading voltage	V_{OT}	ANn	AVRLŠ 1.5 LSB	AVRL + 0.5 LSB	AVRL + 2.5 LSB	V	
Full scale reading voltage	V_{FST}	ANn	AVRHŠ 3.5 LSB	AVRHŠ 1.5 LSB	AVRH + 0.5 LSB	V	
Compare time	T_{comp}		1.0		16,500	µs	4.5 V AV $_{CC}$5 5.5 V
			2.0		µ	s	3.0 V AV $_{CC}$5 < 4.5 V
Sampling time	T_{samp}		0.4		µ	s	4.5 V AV $_{CC}$5 5.5 V, R_{EXT} < 2 k
			1.0		µ	s	3.0 V AV $_{CC}$5 < 4.5 V, R_{EXT} < 1 k
Conversion time	T_{conv}		1.4		µ	s	4.5 V AV $_{CC}$5 5.5 V
			3.0		µ	s	3.0 V AV $_{CC}$5 < 4.5 V
Input capacitance	C_{IN}	ANn			11	pF	
Input resistance	R_{IN}	ANn			2.6	k	4.5 V AV $_{CC}$5 5.5 V
					12.1	k	3.0 V AV $_{CC}$5 < 4.5 V
Analog input leakage current	I_{AIN}	ANn	Š 1		+ 1	µA	T_A = + 25 °C
			Š 3		+ 3	µA	T_A = + 105 °C
Analog input voltage range	V_{AIN}	ANn	AVRL		AVRH	V	
Offset between input channels		ANn			4	LSB	

(Continued)

Note : The accuracy gets worse as AVRH - AVRL becomes smaller

(Continued)

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Reference voltage range	AVRH	AVRH5	0.75 × $AV_{CC}5$		$AV_{CC}5$	V	
	AVRL	$AV_{SS}5$	$AV_{SS}5$		$AV_{CC}5$ × 0.25	V	
Power supply current per ADC macro *3	I_A	$AV_{CC}5$		2.5	5	mA	A/D Converter active
	I_{AH}	$AV_{CC}5$			5	µA	A/D Converter not operated *1
Reference voltage current per ADC macro *3	I_R	AVRH5		0.7	1	mA	A/D Converter active
	I_{RH}	AVRH5			5	µA	A/D Converter not operated *2

*1 : Supply current at $AV_{CC}5$, if A/D converter and ALARM comparator are not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)

*2 : Input current at AVRH5, if A/D converter is not operating, ($V_{DD}5 = AV_{CC}5 = AVRH = 5.0$ V)

*3 : The current consumption per ADC macro is given here. On devices having more then one A/D converter, the current values have to be multiplied by the number of macros.

Sampling Time Calculation

T_{samp} = (2.6 kOhm + R_{EXT}) × 11pF × 7; for 4.5V $AV_{CC}5$ 5.5V

T_{samp} = (12.1 kOhm + R_{EXT}) × 11pF × 7; for 3.0V $AV_{CC}5 < 4.5$V

Conversion Time Calculation

$T_{conv} = T_{samp} + T_{comp}$

Definition of A/D converter terms

Resolution

Analog variation that is recognizable by the A/D converter.

Nonlinearity error

Deviation between actual conversion characteristics and a straight line connecting the zero transition point ($00\ 0000\ 0000_B$ $00\ 0000\ 0001_B$) and the full scale transition point ($11\ 1111\ 1110_B$ $11\ 1111\ 1111_B$).

Differential nonlinearity error

Deviation of the input voltage from the ideal value that is required to change the output code by 1 LSB.

Total error

This error indicates the difference between actual and theoretical values, including the zero transition error, full scale transition error, and nonlinearity error.

5. Alarm comparator characteristics

Parameter	Symbol	Pin name	Value			Unit	Remarks
			Min	Typ	Max		
Power supply current	I_{A5ALMF}	$AV_{CC}5$		25	40	µA	Alarm comparator enabled in fast mode (one channel)
	I_{A5ALMS}			7	10	µA	Alarm comparator enabled in fast mode (one channel)
	I_{A5ALMH}				5	µA	Alarm comparator disabled
ALARM pin input current	I_{ALIN}	ALARM	Š 1		+ 1	µA	T_A = + 25 °C
			Š 3		+ 3		T_A = + 105 °C
ALARM pin input voltage range	V_{ALIN}		0		$AV_{CC}5$	V	
Alarm upper limit voltage	V_{IAH}		$AV_{CC}5 \times 0.78$ Š 3%	$AV_{CC}5 \times 0.78$	$AV_{CC}5 \times 0.78$ + 3%	V	
Alarm lower limit voltage	V_{IAL}		$AV_{CC}5 \times 0.36$ Š 5%	$AV_{CC}5 \times 0.36$	$AV_{CC}5 \times 0.36$ + 5%	V	
Alarm hysteresis voltage	V_{IAHYS}		50		250	mV	
Alarm input resistance	R_{IN}		5			M	
Comparison time	t_{COMPF}			0.1	0.2	µs	ACSR.MD=1
	t_{COMPS}			1	2	µs	ACSR.MD=0

6. FLASH memory program/erase characteristics

6.1. MB91F467SA

(T_A = 25°C, Vcc = 5.0V)

Parameter	Value			Unit	Remarks
	Min	Typ	Max		
Sector erase time	-	0.5	2.0	s	Erasure programming time not included
Chip erase time	-	n*0.5	n*2.0	s	n is the number of Flash sector of the device
Word (16-bit width) programming time	-	6	100	µs	System overhead time not included
Programme/Erase cycle	10 000			cycle	
Flash data retention time	20			year	*1

*1: This value was converted from the results of evaluating the reliability of the technology (using Arrhenius equation to convert high temperature measurements into normalized value at 85°C)

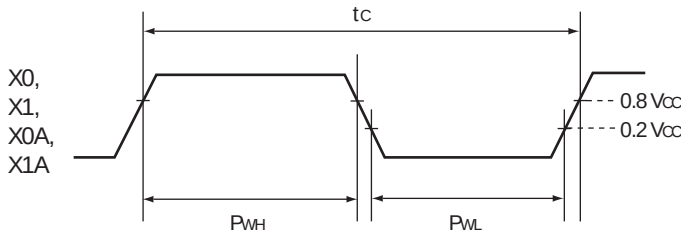
7. AC characteristics

7.1. Clock timing

($V_{DD}5$ = 3.0 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = Š40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value			Unit	Condition
			Min	Typ	Max		
Clock frequency	f_C	X0 X1	3.5	4	16	MHz	Opposite phase external supply or crystal
		X0A X1A	32	32.768	100	kHz	

€ Clock timing condition



7.3. LIN-USART Timings at $V_{DD}5$ = 3.0 to 5.5 V

Conditions during AC measurements

All AC tests were measured under the following conditions:

- IO_{drive} = 5 mA
- $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
- $V_{SS}5$ = 0 V
- T_a = -40 °C to +105 °C
- C_l = 50 pF (load capacity value of pins when testing)
- VOL = 0.2 x $V_{DD}5$,
- VOH = 0.8 x $V_{DD}5$
- EPILR = 0, PILR = 1 (Automotive Level = worst case)

($V_{DD}5$ = 3.0 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = Š40 °C to + 105 °C)

Parameter	Symbol	Pin name	Condition	$V_{DD}5$ = 3.0 V to 4.5 V		$V_{DD}5$ = 4.5 V to 5.5 V		Unit
				Min	Max	Min	Max	
Serial clock cycle time	t_{SCYCI}	SCKn	Internal clock operation (master mode)	4 t_{CLKP}		4 t_{CLKP}		ns
SCK SOT delay time	t_{SLOVI}	SCKn SOTn		Š 30	30	Š 20	20	ns
SOT SCK delay time	t_{OVSHI}	SCKn SOTn		m × t_{CLKP} Š 30*		m × t_{CLKP} Š 20*		ns
Valid SIN SCK setup time	t_{IVSHI}	SCKn SINn		t_{CLKP} + 55		t_{CLKP} + 45		ns
SCK valid SIN hold time	t_{SHIXI}	SCKn SINn		0		0		ns
Serial clock H pulse width	t_{SHSLE}	SCKn	External clock operation (slave mode)	t_{CLKP} + 10		t_{CLKP} + 10		ns
Serial clock L pulse width	t_{SLSHE}	SCKn		t_{CLKP} + 10		t_{CLKP} + 10		ns
SCK SOT delay time	t_{SLOVE}	SCKn SOTn			2 t_{CLKP} + 55		2 t_{CLKP} + 45	ns
Valid SIN SCK setup time	t_{IVSHE}	SCKn SINn		10		10		ns
SCK valid SIN hold time	t_{SHIXE}	SCKn SINn		t_{CLKP} + 10		t_{CLKP} + 10		ns
SCK rising time	t_{FE}	SCKn			20		20	ns
SCK falling time	t_{RE}	SCKn			20		20	ns

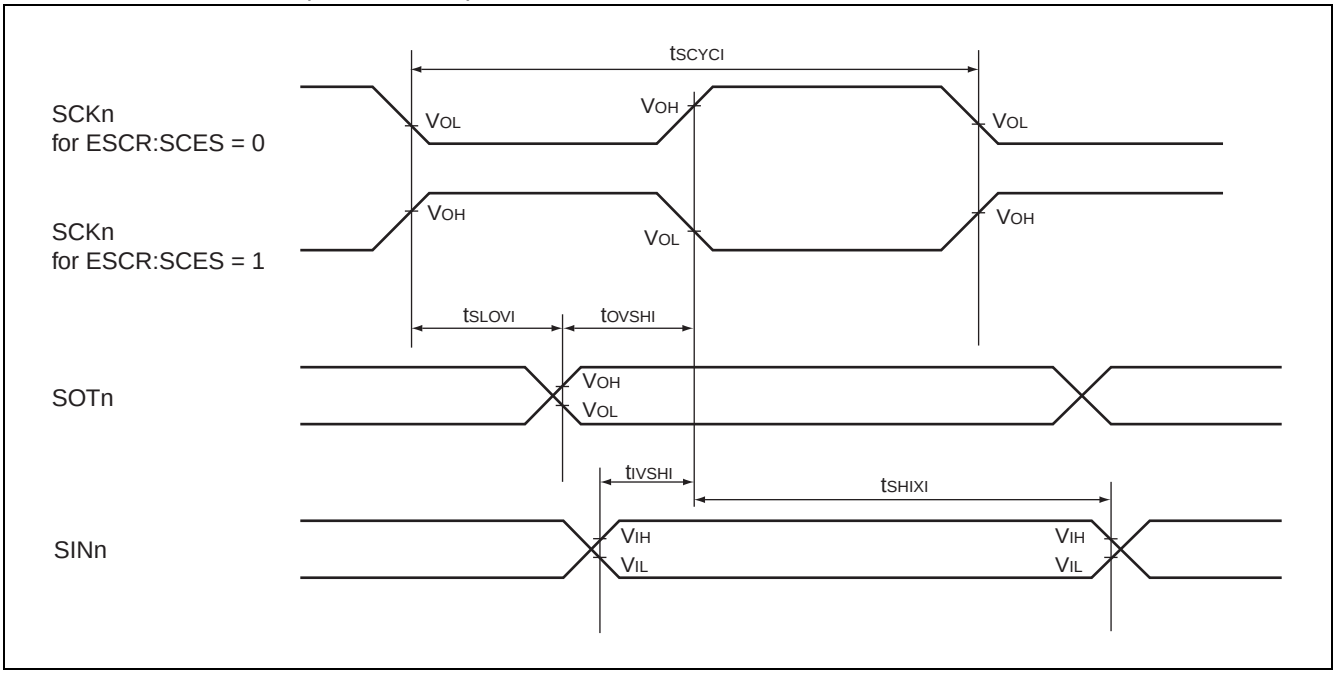
* : Parameter m depends on t_{SCYCI} and can be calculated as :

- € if t_{SCYCI} = 2*k*t_{CLKP}, then m = k, where k is an integer > 2
- € if t_{SCYCI} = (2*k + 1)*t_{CLKP}, then m = k + 1, where k is an integer > 1

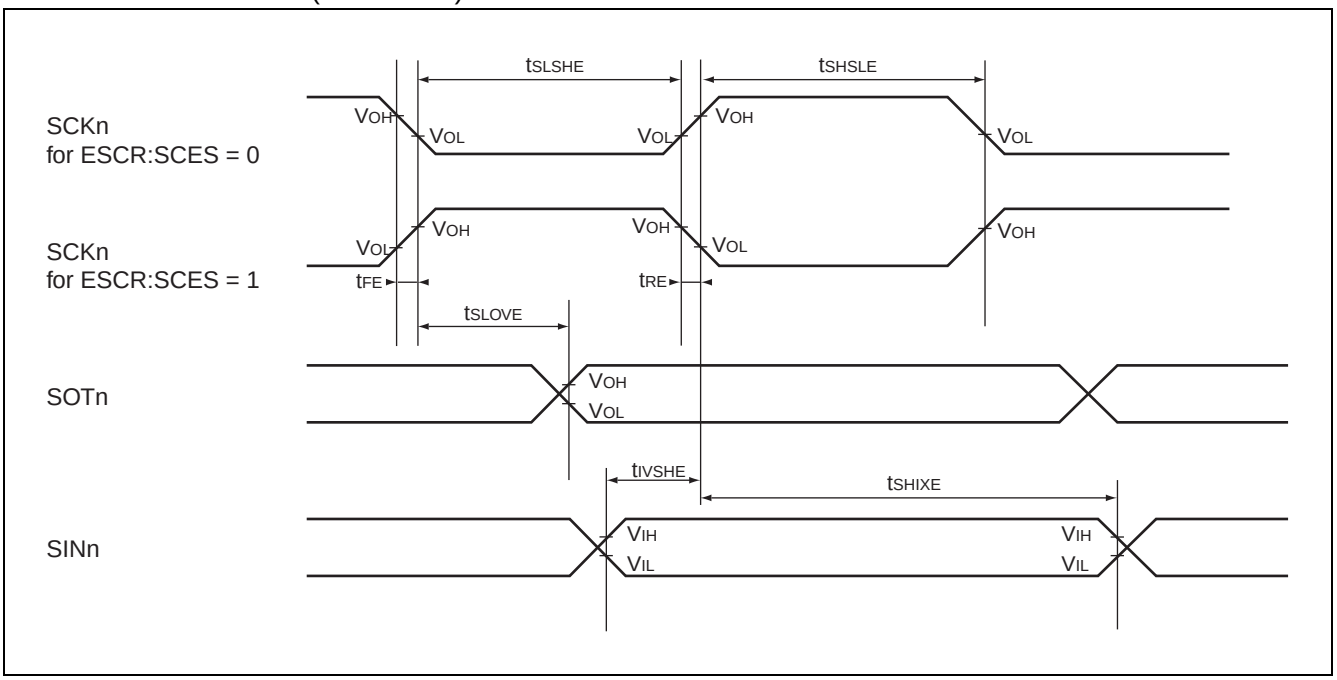
Notes :

- € The above values are AC characteristics for CLK synchronous mode.
- € t_{CLKP} is the cycle time of the peripheral clock.

Internal clock mode (master mode)



External clock mode (slave mode)



7.4. I²C AC Timings at $V_{DD}5$ = 3.0 to 5.5 V

Conditions during AC measurements

All AC tests were measured under the following conditions:

- IO_{drive} = 3 mA
- $V_{DD}5$ = 3.0 V to 5.5 V, I_{load} = 3 mA
- $V_{SS}5$ = 0 V
- Ta = Š 40 °C to + 105 °C
- C_l = 50 pF
- VOL = 0.3 × $V_{DD}5$,
  VOH = 0.7 × $V_{DD}5$
- EPILR = 0, PILR = 0 (CMOS Hysteresis 0.3 × $V_{DD}5$/0.7 × $V_{DD}5$)

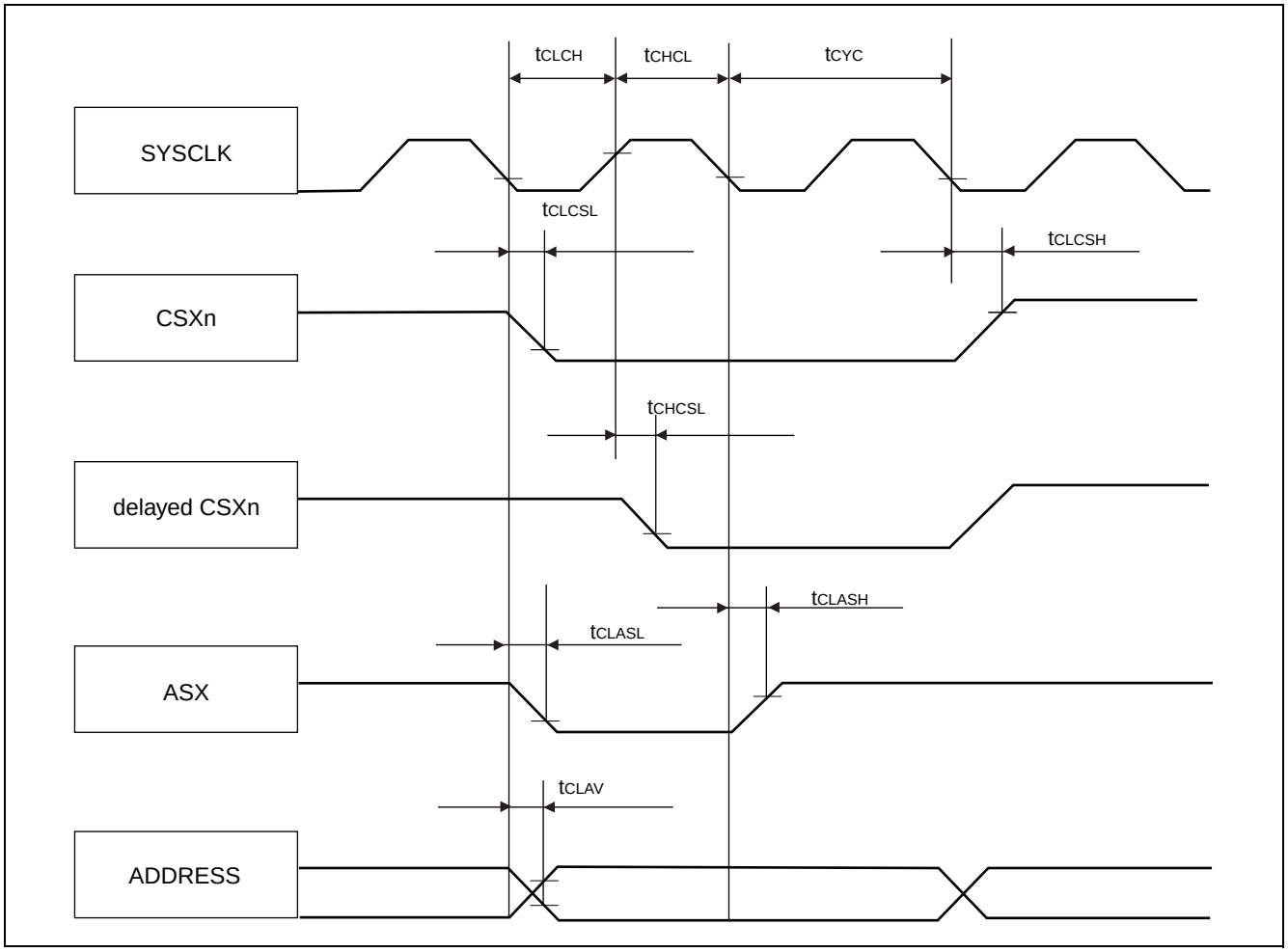
Fast mode:

($V_{DD}5$ = 3.5 V to 5.5 V, $V_{SS}5$ = $AV_{SS}5$ = 0 V, T_A = Š40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit	Remark
			Min	Max		
SCL clock frequency	f_{SCL}	SCLn	0	400	kHz	
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD;STA}$	SCLn, SDAn	0.6		µ s	
LOW period of the SCL clock	t_{LOW}	SCLn	1.3		µ s	
HIGH period of the SCL clock	t_{HIGH}	SCLn	0.6		µ s	
Setup time for a repeated START condition	$t_{SU;STA}$	SCLn, SDAn	0.6		µ s	
Data hold time for I²C-bus devices	$t_{HD;DAT}$	SCLn, SDAn	0	0.9	µs	
Data setup time	$t_{SU;DAT}$	SCLn SDAn	100		ns	
Rise time of both SDA and SCL signals	t_r	SCLn, SDAn	20 + 0.1Cb	300	ns	
Fall time of both SDA and SCL signals	t_f	SCLn, SDAn	20 + 0.1Cb	300	ns	
Setup time for STOP condition	$t_{SU;STO}$	SCLn, SDAn	0.6		µ s	
Bus free time between a STOP and START condition	t_{BUF}	SCLn, SDAn	1.3		µ s	
Capacitive load for each bus line	C_b	SCLn, SDAn		400	pF	
Pulse width of spike suppressed by input filter	t_{SP}	SCLn, SDAn	0	(1..1.5) × t_{CLKP}	ns	*1

*1 The noise filter will suppress single spikes with a pulse width of 0ns and between (1 to 1.5) cycles of peripheral clock, depending on the phase relationship between I²C signals (SDA, SCL) and peripheral clock.

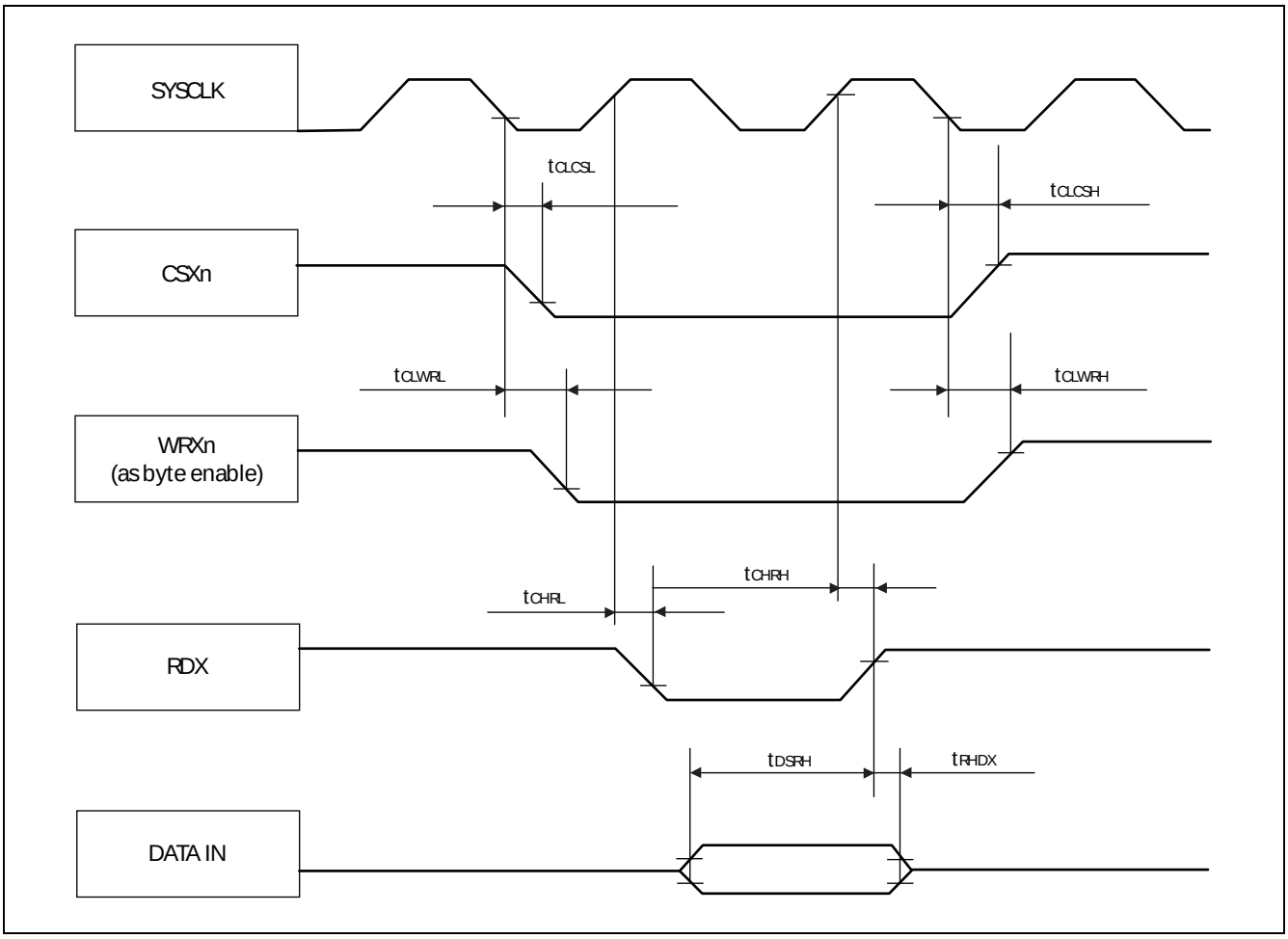
Note: t_{CLKP} is the cycle time of the peripheral clock.


tCLCH
tCHCL
tCYC
SYSCLK
tCLCSL
tCLCSH
CSXn
tCHCSL
delayed CSXn
tCLASH
tCLASL
ASX
tCLAV
ADDRESS

7.7.2. Synchronous/Asynchronous read access

(V_{DD}35 = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = Š40 °C to + 105 °C)

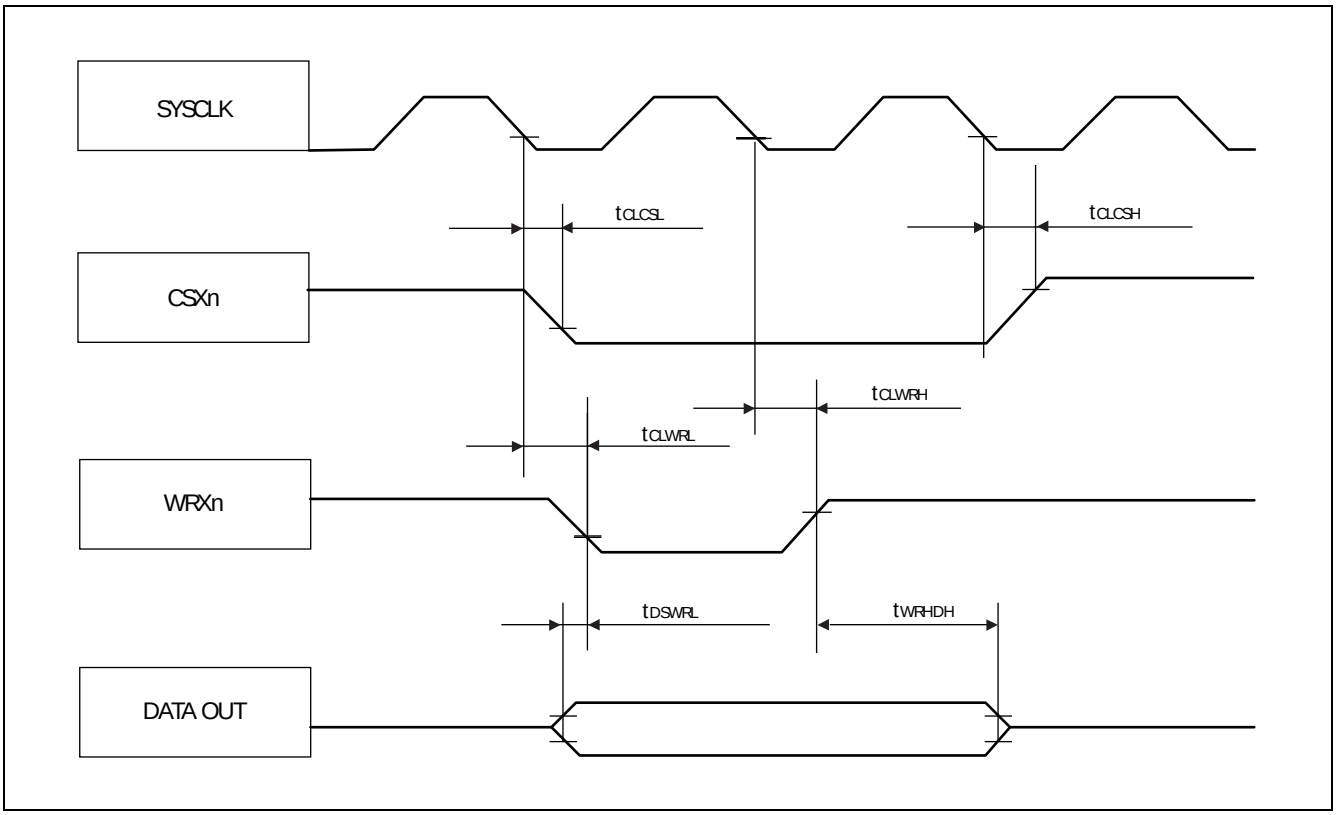
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK to RDX delay time	TCHRL	SYSCLK RDX	2	5	ns
	TCHRH		2	5	ns
Data valid to RDX setup time	TDSRH	RDX D31 to D16	12		ns
RDX to Data valid hold time	TRHDX	RDX D31 to D16	0		ns
SYSCLK to WRXn (as byte enable) delay time	TCLWRL	SYSCLK WRXn		5	ns
	TCLWRH		2		ns
SYSCLK to CSXn delay time	TCLCSL	SYSCLK CSXn		5	ns
	TCLCSH			5	ns



7.7.4. Synchronous write access - no byte control type

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = Š40 °C to + 105 °C)

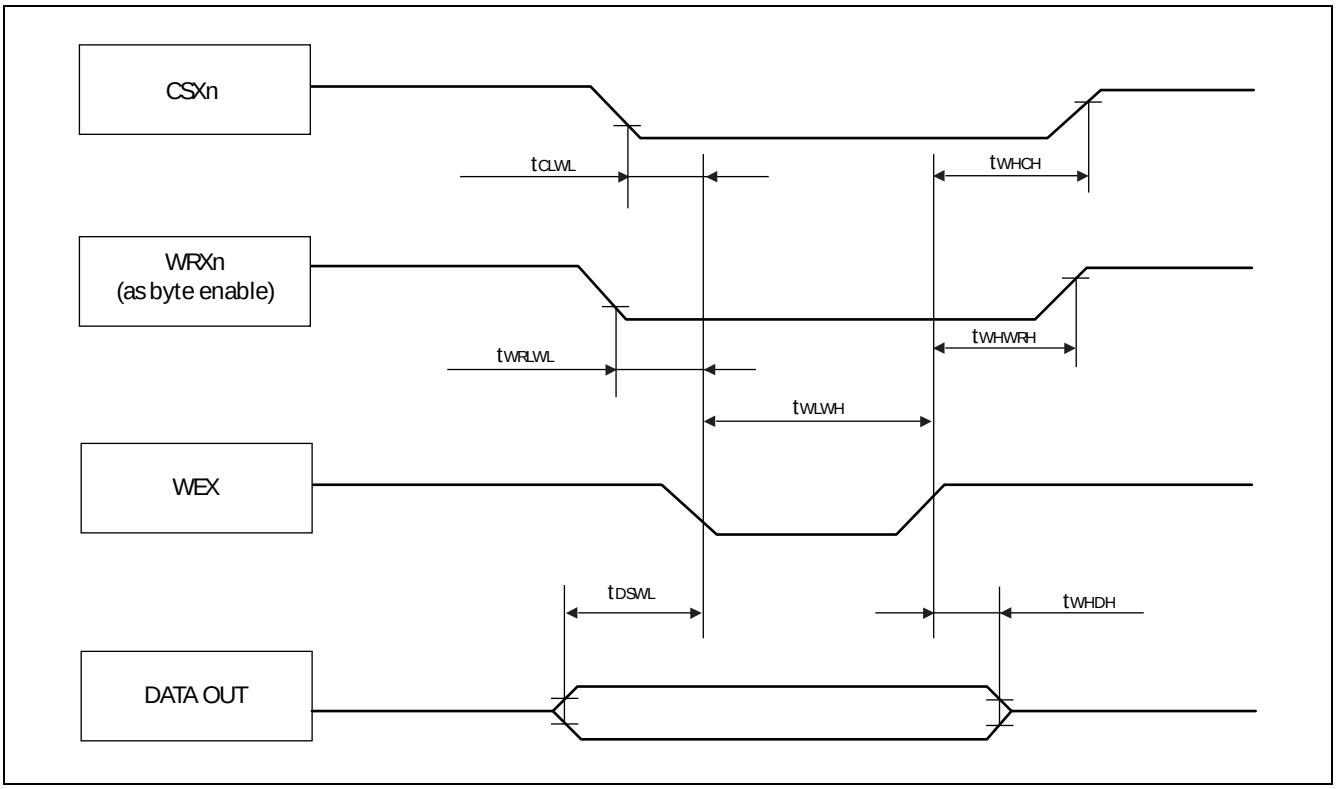
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK to WRXn delay time	TCLWRL	SYSCLK WRXn		5	ns
	TCLWRH		2		ns
Data valid to WRXn setup time	TDSWRL	WRXn D31 to D16	Š 1		ns
WRXn to Data valid hold time	TWRHDH	WRXn D31 to D16	t_{CLKT} Š 1		ns
SYSCLK to CSXn delay time	TCLCSL	SYSCLK CSXn		5	ns
	TCLCSH			5	ns



7.7.5. Asynchronous write access - byte control type

(V_{DD}35 = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = Š40 °C to + 105 °C)

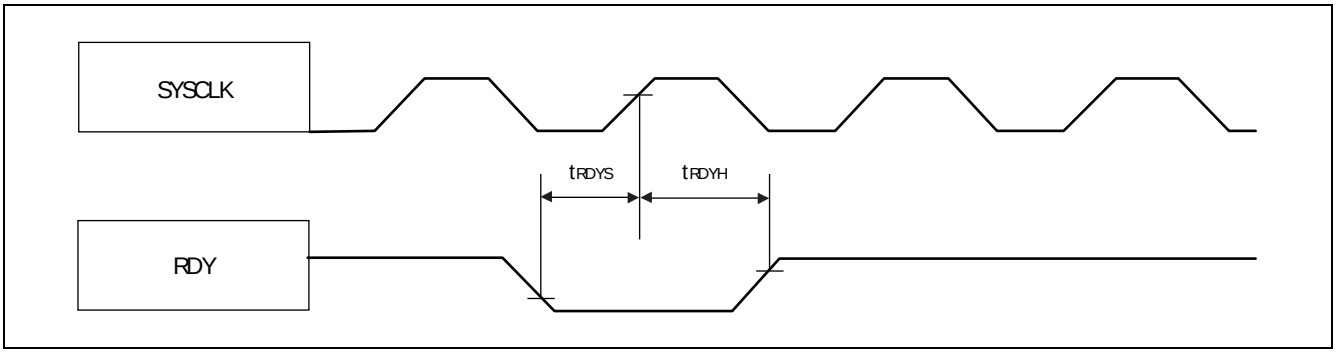
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WEX to WEX pulse width	TWLWH	WEX	t_{CLKT} Š 1		ns
Data valid to WEX setup time	TDSWL	WEX D31 to D16	1/2 × t_{CLKT} Š 1		ns
WEX to Data valid hold time	TWHDH	WEX D31 to D16	1/2 × t_{CLKT} Š 1		ns
WEX to WRXn delay time	TWRLWL	WEX WRXn		1/2 × t_{CLKT} + 1	ns
	TWHWRH		1/2 × t_{CLKT} Š 1		ns
WEX to CSXn delay time	TCLWL	WEX CSXn		1/2 × t_{CLKT} + 1	ns
	TWHCH		1/2 × t_{CLKT} Š 1		ns



7.7.7. RDY waitcycle insertion

($V_{DD}35$ = 4.5 V to 5.5 V, Vss5 = AVss5 = 0 V, T_A = Š40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
RDY setup time	TRDYS	SYSCLK RDY	8		ns
RDY hold time	TRDYH	SYSCLK RDY	0		ns



7.8. External Bus AC Timings at $V_{DD}35$ = 3.0 to 4.5 V

Conditions during AC measurements

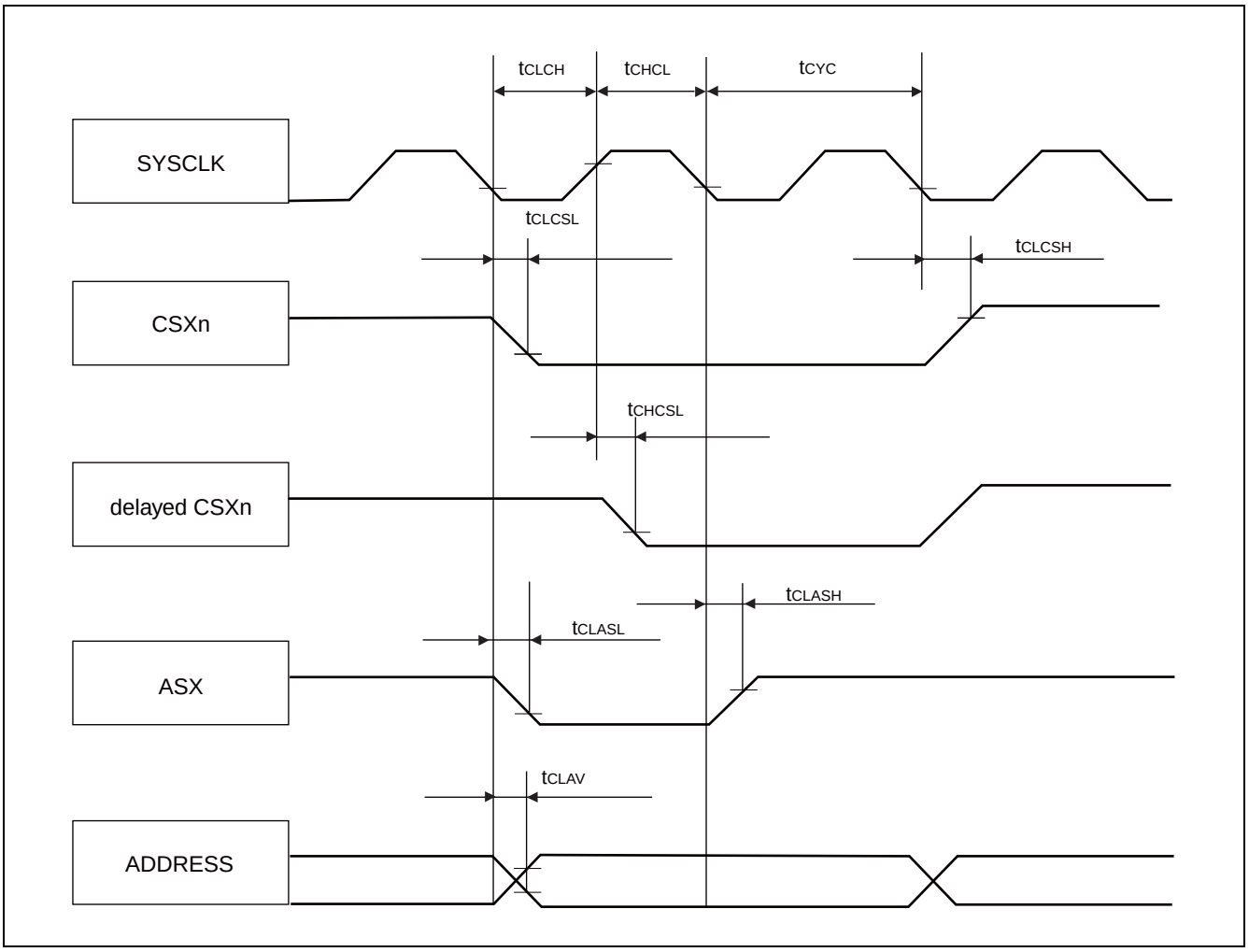
All AC tests were measured under the following conditions:

- IO_{drive} = 5 mA
- $V_{DD}35$ = 3.0 V to 4.5 V, I_{load} = 3 mA
- $V_{SS}5$ = 0 V
- Ta = Š 40 °C to + 105 °C
- C_l = 50 pF
- VOL = 0.2 × $V_{DD}35$,
  VOH = 0.8 × $V_{DD}35$
- EPILR = 0, PILR = 1 (Automotive Level = worst case)

7.8.1. Basic Timing

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = Š40 °C to + 105 °C)

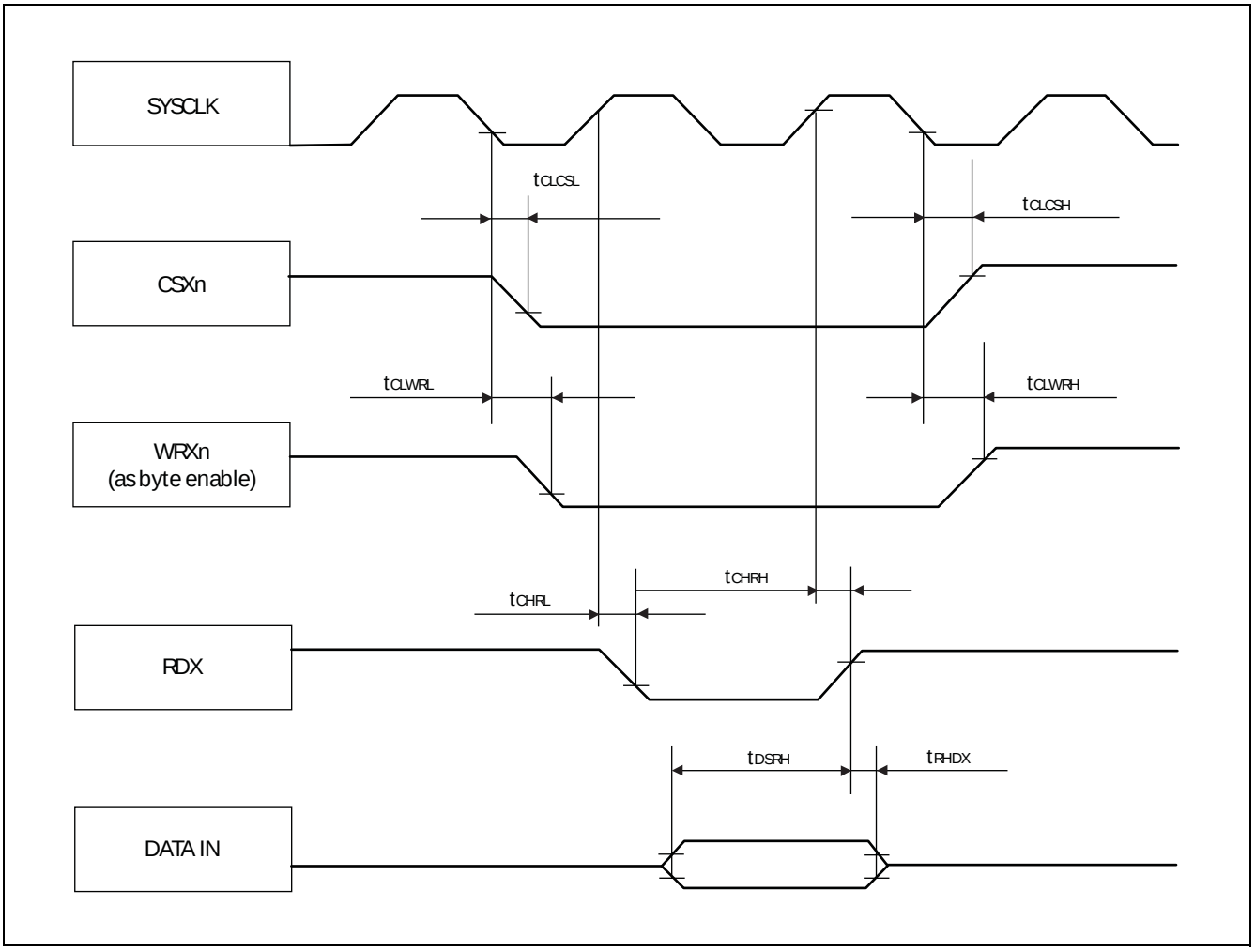
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK	TCLCH	SYSCLK	1/2 × t_{CLKT}	1/2 × t_{CLKT} + 2	ns
	TCHCL		1/2 × t_{CLKT} Š 2	1/2 × t_{CLKT}	ns
SYSCLK to CSXn delay time	TCLCSL	SYSCLK CSXn		11	ns
	TCLCSH			7	ns
SYSCLK to CSXn delay time (Addr CS delay)	TCHCSL		2	6	ns
SYSCLK to ASX delay time	TCLASL	SYSCLK ASX		6	ns
	TCLASH			7	ns
SYSCLK to Address valid delay time	TCLAV	SYSCLK A23 to A0		13	ns


tCLCH
tCHCL
tCYC
SYSCLK
tCLCSL
tCLCSH
CSXn
tCHCSL
delayed CSXn
tCLASH
tCLASL
ASX
tCLAV
ADDRESS

7.8.2. Synchronous/Asynchronous read access

(V_{DD}35 = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = Š40 °C to + 105 °C)

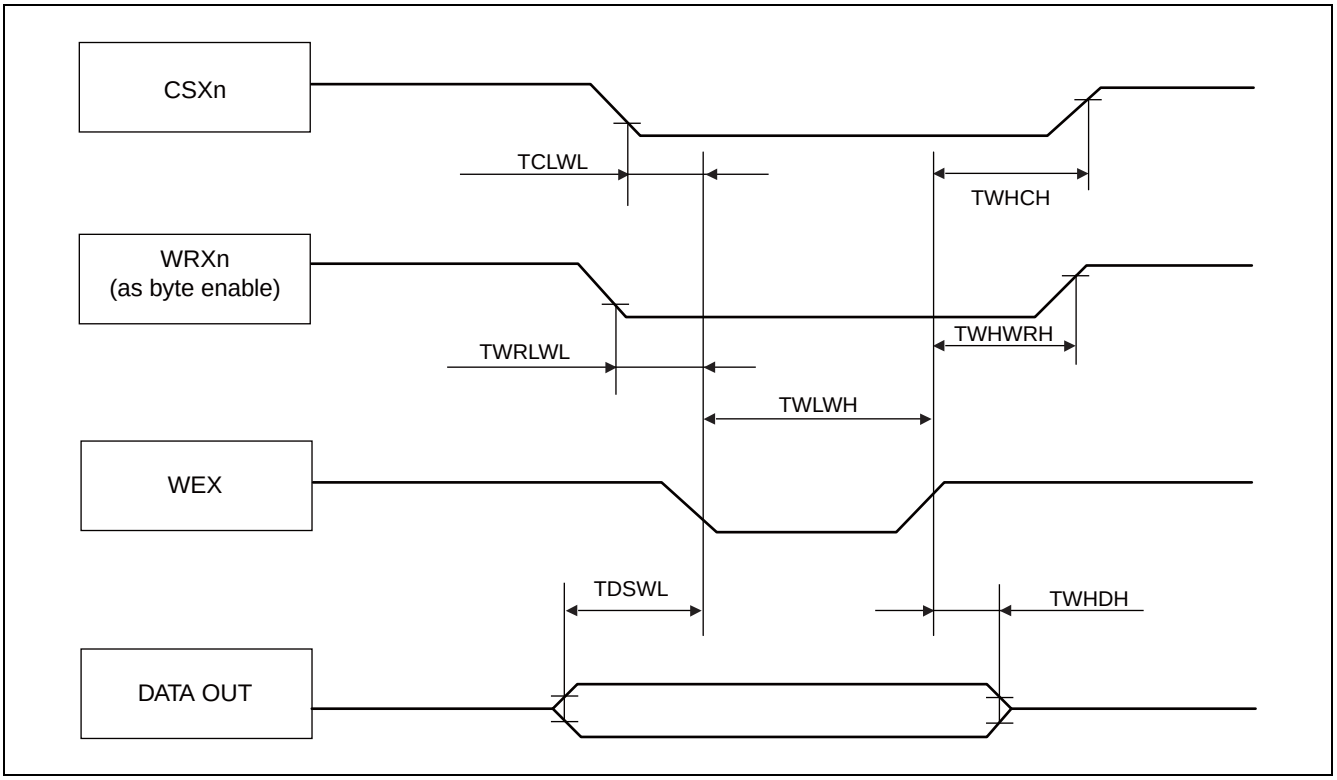
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
SYSCLK to RDX delay time	TCHRL	SYSCLK RDX	1	4	ns
	TCHRH		2	6	ns
Data valid to RDX setup time	TDSRH	RDX D31 to D16	16		ns
RDX to Data valid hold time	TRHDX	RDX D31 to D16	0		ns
SYSCLK to WRXn (as byte enable) delay time	TCLWRL	SYSCLK WRXn		6	ns
	TCLWRH		3		ns
SYSCLK to CSXn delay time	TCLCSL	SYSCLK CSXn		11	ns
	TCLCSH			7	ns



7.8.5. Asynchronous write access - byte control type

(V_{DD}35 = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = Š40 °C to + 105 °C)

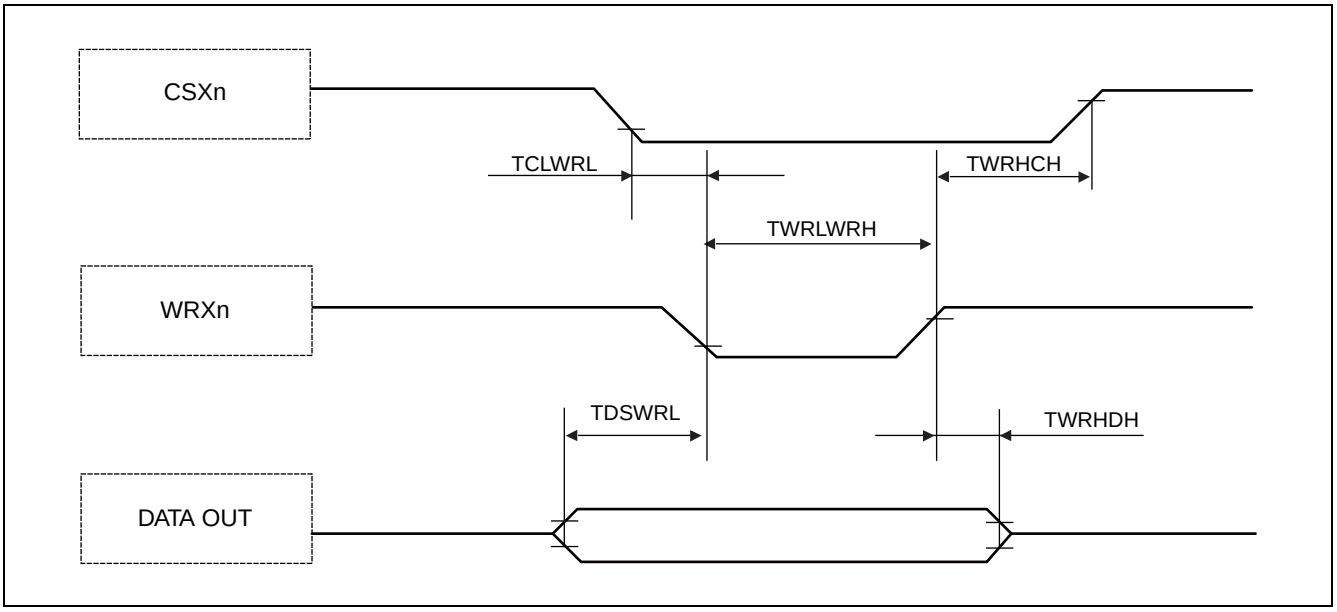
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WEX to WEX pulse width	TWLWH	WEX	t_{CLKT}		ns
Data valid to WEX setup time	TDSWL	WEX D31 to D16	1/2 × t_{CLKT} Š 7		ns
WEX to Data valid hold time	TWHDH	WEX D31 to D16	1/2 × t_{CLKT} Š 3		ns
WEX to WRXn delay time	TWRLWL	WEX WRXn		1/2 × t_{CLKT} + 1	ns
	TWHWRH		1/2 × t_{CLKT} Š 1		ns
WEX to CSXn delay time	TCLWL	WEX CSXn		1/2 × t_{CLKT} Š 1	ns
	TWHCH		1/2 × t_{CLKT} Š 1		ns



7.8.6. Asynchronous write access - no byte control type

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = Š40 °C to + 105 °C)

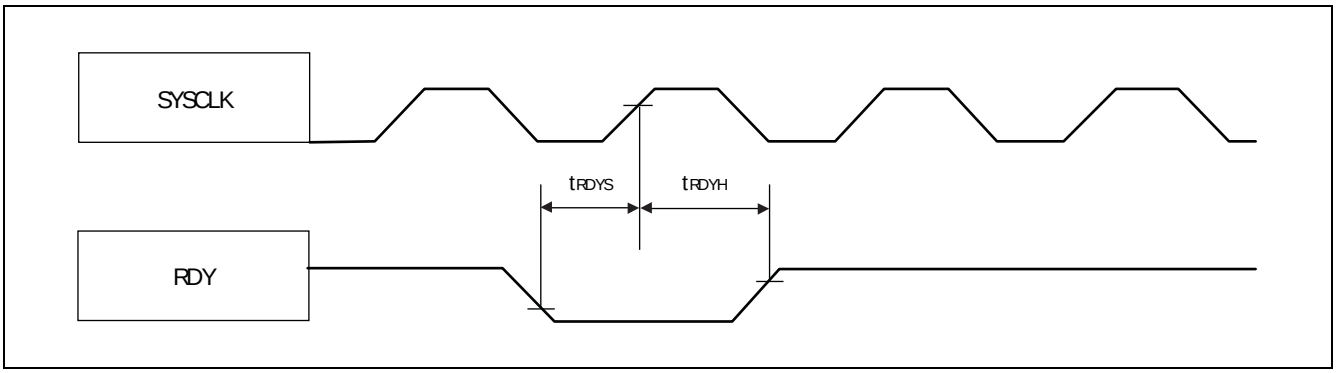
Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
WRXn to WRXn pulse width	TWRLWRH	WRXn	t_{CLKT}		ns
Data valid to WRXn setup time	TDSWRL	WRXn D31 to D16	1/2 × t_{CLKT} Š 7		ns
WRXn to Data valid hold time	TWRHDH	WRXn D31 to D16	1/2 × t_{CLKT} Š 3		ns
WRXn to CSXn delay time	TCLWRL	WRXn CSXn		1/2 × t_{CLKT}+1	ns
	TWRHCH		1/2 × t_{CLKT} Š 1		ns



7.8.7. RDY waitcycle insertion

($V_{DD}35$ = 3.0 V to 4.5 V, Vss5 = AVss5 = 0 V, T_A = Š40 °C to + 105 °C)

Parameter	Symbol	Pin name	Value		Unit
			Min	Max	
RDY setup time	TRDYS	SYSCLK RDY	12		ns
RDY hold time	TRDYH	SYSCLK RDY	0		ns

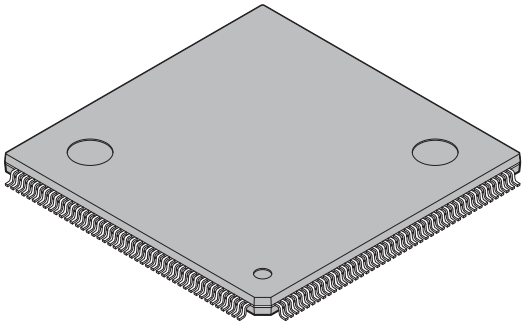


■ ORDERING INFORMATION

Part number	Package	Remarks
MB91F467SAPMC-GSE2	176-pin plastic LQFP (FPT-176P-M07)	Lead-free package

PACKAGE DIMENSION

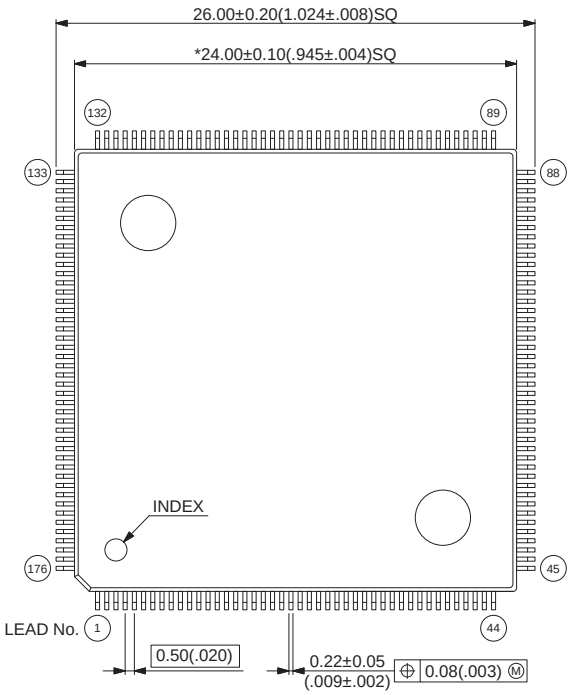
176-pin plastic LQFP



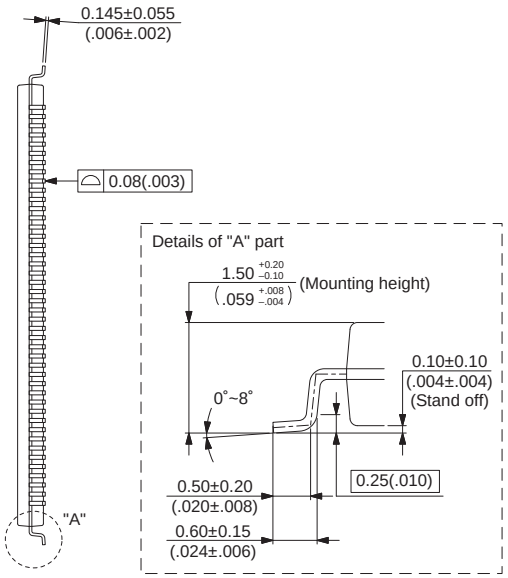
(FPT-176P-M07)

Lead pitch	0.50 mm
Package width × package length	24.0 × 24.0 mm
Lead shape	Gullwing
Sealing method	Plastic mold
Mounting height	1.70 mm MAX
Code (Reference)	P-LQFP-0176-2424-0.50

176-pin plastic LQFP
(FPT-176P-M07)



Note 1) * : Values do not include resin protrusion.
Resin protrusion is +0.25(.010)Max(each side).
Note 2) Pins width and pins thickness include plating thickness
Note 3) Pins width do not include tie bar cutting remainder.



©2004-2008 FUJITSU MICROELECTRONICS LIMITED F176013S-c-1-2

Dimensions in mm (inches).
Note: The values in parentheses are reference values.

Please check the latest package dimension at the following URL.
http://edevice.fujitsu.com/package/en-search/

■ MAIN CHANGES IN THIS EDITION

Page	Section	Change Results
		Preliminary Data Sheet Data Sheet

The vertical lines marked in the left side of the page show the changes.

FUJITSU MICROELECTRONICS LIMITED

Shinjuku Dai-Ichi Seimei Bldg., 7-1, Nishishinjuku 2-chome,
Shinjuku-ku, Tokyo 163-0722, Japan
Tel: +81-3-5322-3329
http://jp.fujitsu.com/fml/en/

For further information please contact:

North and South America
FUJITSU MICROELECTRONICS AMERICA, INC.
1250 E. Arques Avenue, M/S 333
Sunnyvale, CA 94085-5401, U.S.A.
Tel: +1-408-737-5600 Fax: +1-408-737-5999
http://www.fma.fujitsu.com/

Europe
FUJITSU MICROELECTRONICS EUROPE GmbH
Pittlerstrasse 47, 63225 Langen, Germany
Tel: +49-6103-690-0 Fax: +49-6103-690-122
http://emea.fujitsu.com/microelectronics/

Korea
FUJITSU MICROELECTRONICS KOREA LTD.
206 Kosmo Tower Building, 1002 Daechi-Dong,
Gangnam-Gu, Seoul 135-280, Republic of Korea
Tel: +82-2-3484-7100 Fax: +82-2-3484-7111
http://kr.fujitsu.com/fmk/

Asia Pacific
FUJITSU MICROELECTRONICS ASIA PTE. LTD.
151 Lorong Chuan,
#05-08 New Tech Park 556741 Singapore
Tel : +65-6281-0770 Fax : +65-6281-0220
http://www.fmal.fujitsu.com/

FUJITSU MICROELECTRONICS SHANGHAI CO., LTD.
Rm. 3102, Bund Center, No.222 Yan An Road (E),
Shanghai 200002, China
Tel : +86-21-6146-3688 Fax : +86-21-6335-1605
http://cn.fujitsu.com/fmc/

FUJITSU MICROELECTRONICS PACIFIC ASIA LTD.
10/F., World Commerce Centre, 11 Canton Road,
Tsimshatsui, Kowloon, Hong Kong
Tel : +852-2377-0226 Fax : +852-2376-3269
http://cn.fujitsu.com/fmc/en/

Specifications are subject to change without notice. For further information please contact each office.

All Rights Reserved.
The contents of this document are subject to change without notice.
Customers are advised to consult with sales representatives before ordering.
The information, such as descriptions of function and application circuit examples, in this document are presented solely for the purpose of reference to show examples of operations and uses of FUJITSU MICROELECTRONICS device; FUJITSU MICROELECTRONICS does not warrant proper operation of the device with respect to use based on such information. When you develop equipment incorporating the device based on such information, you must assume any responsibility arising out of such use of the information.
FUJITSU MICROELECTRONICS assumes no liability for any damages whatsoever arising out of the use of the information.
Any information in this document, including descriptions of function and schematic diagrams, shall not be construed as license of the use or exercise of any intellectual property right, such as patent right or copyright, or any other right of FUJITSU MICROELECTRONICS or any third party or does FUJITSU MICROELECTRONICS warrant non-infringement of any third-party's intellectual property right or other right by using such information. FUJITSU MICROELECTRONICS assumes no liability for any infringement of the intellectual property rights or other rights of third parties which would result from the use of information contained herein.
The products described in this document are designed, developed and manufactured as contemplated for general use, including without limitation, ordinary industrial use, general office use, personal use, and household use, but are not designed, developed and manufactured as contemplated (1) for use accompanying fatal risks or dangers that, unless extremely high safety is secured, could have a serious effect to the public, and could lead directly to death, personal injury, severe physical damage or other loss (i.e., nuclear reaction control in nuclear facility, aircraft flight control, air traffic control, mass transport control, medical life support system, missile launch control in weapon system), or (2) for use requiring extremely high reliability (i.e., submersible repeater and artificial satellite).
Please note that FUJITSU MICROELECTRONICS will not be liable against you and/or any third party for any claims or damages arising in connection with above-mentioned uses of the products.
Any semiconductor devices have an inherent chance of failure. You must protect against injury, damage or loss from such failures by incorporating safety design measures into your facility and equipment such as redundancy, fire protection, and prevention of over-current levels and other abnormal operating conditions.
Exportation/release of any products described in this document may require necessary procedures in accordance with the regulations of the Foreign Exchange and Foreign Trade Control Law of Japan and/or US export control laws.
The company names and brand names herein are the trademarks or registered trademarks of their respective owners.

Edited: Sales Promotion Department