

2K SPI Bus Serial EEPROM with EUI-48™ Node Identity

Device Selection Table

Part Number	Vcc Range	Page Size	Temp. Ranges	Packages
25AA02E48	1.8-5.5V	16 Bytes	I	SN, OT

Features:

- Pre-programmed Globally Unique, 48-bit Node Address
- Compatible with EUI-48™ and EUI-64™
- 10 MHz max. Clock Frequency
- Low-Power CMOS Technology:
 - Max. Write Current: 5 mA at 5.5V
 - Read Current: 5 mA at 5.5V, 10 MHz
 - Standby Current: 1 μ A at 2.5V
- 256 x 8-bit Organization
- Write Page mode (up to 16 bytes)
- Sequential Read
- Self-Timed Erase and Write Cycles (5 ms max.)
- Block Write Protection:
 - Protect none, 1/4, 1/2 or all of array
- Built-in Write Protection:
 - Power-on/off data protection circuitry
 - Write enable latch
 - Write-protect pin
- High Reliability:
 - Endurance: 1,000,000 erase/write cycles
 - Data retention: >200 years
 - ESD protection: >4000V
- Temperature Ranges Supported:
 - Industrial (I): -40°C to +85°C
- Pb-Free and RoHS Compliant

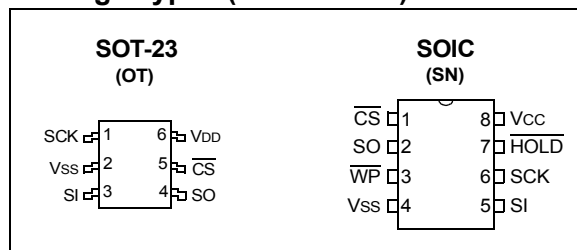
Description:

The Microchip Technology Inc. 25AA02E48 is a 2 Kbit Serial Electrically Erasable Programmable Read-Only Memory (EEPROM). The memory is accessed via a simple Serial Peripheral Interface (SPI) compatible serial bus. The bus signals required are a clock input (SCK) plus separate data in (SI) and data out (SO) lines. Access to the device is controlled through a Chip Select (\overline{CS}) input.

Communication to the device can be paused via the hold pin (HOLD). While the device is paused, transitions on its inputs will be ignored, with the exception of Chip Select, allowing the host to service higher priority interrupts.

The 25AA02E48 is available in the standard 8-lead SOIC and 6-lead SOT-23 packages.

Package Types (not to scale)



Pin Function Table

Name	Function
\overline{CS}	Chip Select Input
SO	Serial Data Output
\overline{WP}	Write-Protect
Vss	Ground
SI	Serial Data Input
SCK	Serial Clock Input
\overline{HOLD}	Hold Input
Vcc	Supply Voltage

25AA02E48

1.0 ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings^(†)

V _{CC}	6.5V
All inputs and outputs w.r.t. V _{SS}	-0.6V to V _{CC} +1.0V
Storage temperature	-65°C to 150°C
Ambient temperature under bias	-40°C to 85°C
ESD protection on all pins	4 kV

† NOTICE: Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for an extended period of time may affect device reliability.

TABLE 1-1: DC CHARACTERISTICS

DC CHARACTERISTICS			Industrial (I): TA = -40°C to +85°C V _{CC} = 1.8V to 5.5V			
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Test Conditions
D001	V _{IH1}	High-level Input voltage	0.7 V _{CC}	V _{CC} +1	V	
D002	V _{IL1}	Low-level Input Voltage	-0.3	0.3 V _{CC}	V	V _{CC} ≥ 2.7V (Note 1)
D003	V _{IL2}		-0.3	0.2 V _{CC}	V	V _{CC} < 2.7V (Note 1)
D004	V _{OL}	Low-level Output Voltage	—	0.4	V	I _{OL} = 2.1 mA
D005	V _{OL}		—	0.2	V	I _{OL} = 1.0 mA, V _{CC} < 2.5V
D006	V _{OH}	High-level Output Voltage	V _{CC} -0.5	—	V	I _{OH} = -400 μA
D007	I _{LI}	Input Leakage Current	—	±1	μA	$\overline{CS} = V_{CC}$, V _{IN} = V _{SS} TO V _{CC}
D008	I _{LO}	Output Leakage Current	—	±1	μA	$\overline{CS} = V_{CC}$, V _{OUT} = V _{SS} TO V _{CC}
D009	C _{INT}	Internal Capacitance (all inputs and outputs)	—	7	pF	TA = 25°C, CLK = 1.0 MHz, V _{CC} = 5.0V (Note 1)
D010	I _{CC} Read	Operating Current	—	5	mA	V _{CC} = 5.5V; F _{CLK} = 10.0 MHz; SO = Open
			—	2.5	mA	V _{CC} = 2.5V; F _{CLK} = 5.0 MHz; SO = Open
D011	I _{CC} Write		—	5	mA	V _{CC} = 5.5V
			—	3	mA	V _{CC} = 2.5V
D012	I _{CCS}	Standby Current	—	1	μA	$\overline{CS} = V_{CC} = 2.5V$, Inputs tied to V _{CC} or V _{SS} , TA = +85°C

Note: This parameter is periodically sampled and not 100% tested.

TABLE 1-2: AC CHARACTERISTICS

AC CHARACTERISTICS			Industrial (I): $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ $V_{CC} = 1.8\text{V}$ to 5.5V			
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Test Conditions
1	FCLK	Clock Frequency	—	10	MHz	$4.5\text{V} \leq V_{CC} < 5.5\text{V}$
			—	5	MHz	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
			—	3	MHz	$1.8\text{V} \leq V_{CC} < 2.5\text{V}$
2	T _{CSS}	$\overline{\text{CS}}$ Setup Time	50	—	ns	$4.5\text{V} \leq V_{CC} < 5.5\text{V}$
			100	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
			150	—	ns	$1.8\text{V} \leq V_{CC} < 2.5\text{V}$
3	T _{CSH}	$\overline{\text{CS}}$ Hold Time	100	—	ns	$4.5\text{V} \leq V_{CC} < 5.5\text{V}$
			200	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
			250	—	ns	$1.8\text{V} \leq V_{CC} < 2.5\text{V}$
4	T _{CSD}	$\overline{\text{CS}}$ Disable Time	50	—	ns	—
5	T _{SU}	Data Setup Time	10	—	ns	$4.5\text{V} \leq V_{CC} < 5.5\text{V}$
			20	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
			30	—	ns	$1.8\text{V} \leq V_{CC} < 2.5\text{V}$
6	T _{HD}	Data Hold Time	20	—	ns	$4.5\text{V} \leq V_{CC} < 5.5\text{V}$
			40	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
			50	—	ns	$1.8\text{V} \leq V_{CC} < 2.5\text{V}$
7	T _R	CLK Rise Time	—	100	ns	(Note 1)
8	T _F	CLK Fall Time	—	100	ns	(Note 1)
9	T _{HI}	Clock High Time	50	—	ns	$4.5\text{V} \leq V_{CC} < 5.5\text{V}$
			100	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
			150	—	ns	$1.8\text{V} \leq V_{CC} < 2.5\text{V}$
10	T _{LO}	Clock Low Time	50	—	ns	$4.5\text{V} \leq V_{CC} < 5.5\text{V}$
			100	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
			150	—	ns	$1.8\text{V} \leq V_{CC} < 2.5\text{V}$
11	T _{CLD}	Clock Delay Time	50	—	ns	—
12	T _{CLE}	Clock Enable Time	50	—	ns	—
13	T _V	Output Valid from Clock Low	—	50	ns	$4.5\text{V} \leq V_{CC} < 5.5\text{V}$
			—	100	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
			—	160	ns	$1.8\text{V} \leq V_{CC} < 2.5\text{V}$
14	T _{HO}	Output Hold Time	0	—	ns	(Note 1)
15	T _{DIS}	Output Disable Time	—	40	ns	$4.5\text{V} \leq V_{CC} < 5.5\text{V}$ (Note 1)
			—	80	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$ (Note 1)
			—	160	ns	$1.8\text{V} \leq V_{CC} < 2.5\text{V}$ (Note 1)
16	T _{HS}	$\overline{\text{HOLD}}$ Setup Time	20	—	ns	$4.5\text{V} \leq V_{CC} < 5.5\text{V}$
			40	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
			80	—	ns	$1.8\text{V} \leq V_{CC} < 2.5\text{V}$

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at www.Microchip.com.

3: T_{WC} begins on the rising edge of $\overline{\text{CS}}$ after a valid write sequence and ends when the internal write cycle is complete.

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TABLE 1-2: AC CHARACTERISTICS (CONTINUED)

AC CHARACTERISTICS			Industrial (I): $T_A = -40^{\circ}\text{C}$ to $+85^{\circ}\text{C}$ $V_{CC} = 1.8\text{V}$ to 5.5V			
Param. No.	Sym.	Characteristic	Min.	Max.	Units	Test Conditions
17	THH	$\overline{\text{HOLD}}$ Hold Time	20	—	ns	$4.5\text{V} \leq V_{CC} < 5.5\text{V}$
			40	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
			80	—	ns	$1.8\text{V} \leq V_{CC} < 2.5\text{V}$
18	THZ	$\overline{\text{HOLD}}$ Low to Output High-Z	30	—	ns	$4.5\text{V} \leq V_{CC} < 5.5\text{V}$ (Note 1)
			60	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$ (Note 1)
			160	—	ns	$1.8\text{V} \leq V_{CC} < 2.5\text{V}$ (Note 1)
19	THV	$\overline{\text{HOLD}}$ High to Output Valid	30	—	ns	$4.5\text{V} \leq V_{CC} < 5.5\text{V}$
			60	—	ns	$2.5\text{V} \leq V_{CC} < 4.5\text{V}$
			160	—	ns	$1.8\text{V} \leq V_{CC} < 2.5\text{V}$
20	Twc	Internal Write Cycle Time (byte or page)	—	5	ms	(Note 3)
21	—	Endurance	1M	—	E/W Cycles	(NOTE 2)

Note 1: This parameter is periodically sampled and not 100% tested.

2: This parameter is not tested but ensured by characterization. For endurance estimates in a specific application, please consult the Total Endurance™ Model which can be obtained from Microchip's web site at www.Microchip.com.

3: Twc begins on the rising edge of $\overline{\text{CS}}$ after a valid write sequence and ends when the internal write cycle is complete.

TABLE 1-3: AC TEST CONDITIONS

AC Waveform:	
$V_{LO} = 0.2\text{V}$	—
$V_{HI} = V_{CC} - 0.2\text{V}$	(Note 1)
$V_{HI} = 4.0\text{V}$	(Note 2)
$C_L = 100\text{ pF}$	—
Timing Measurement Reference Level	
Input	0.5 V_{CC}
Output	0.5 V_{CC}

Note 1: For $V_{CC} \leq 4.0\text{V}$

2: For $V_{CC} > 4.0\text{V}$

FIGURE 1-1: HOLD TIMING



FIGURE 1-2: SERIAL INPUT TIMING

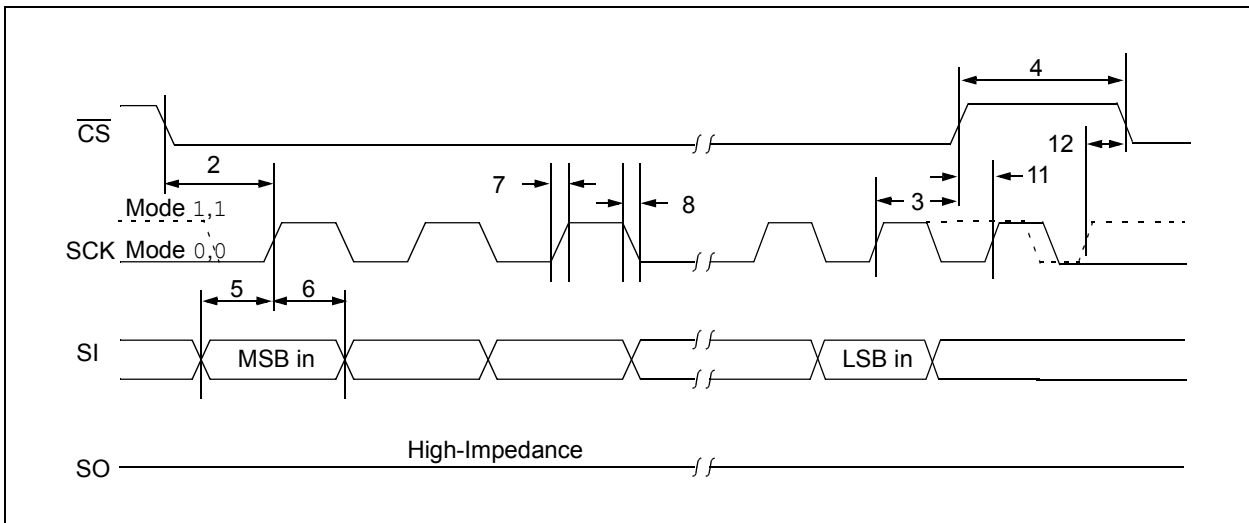
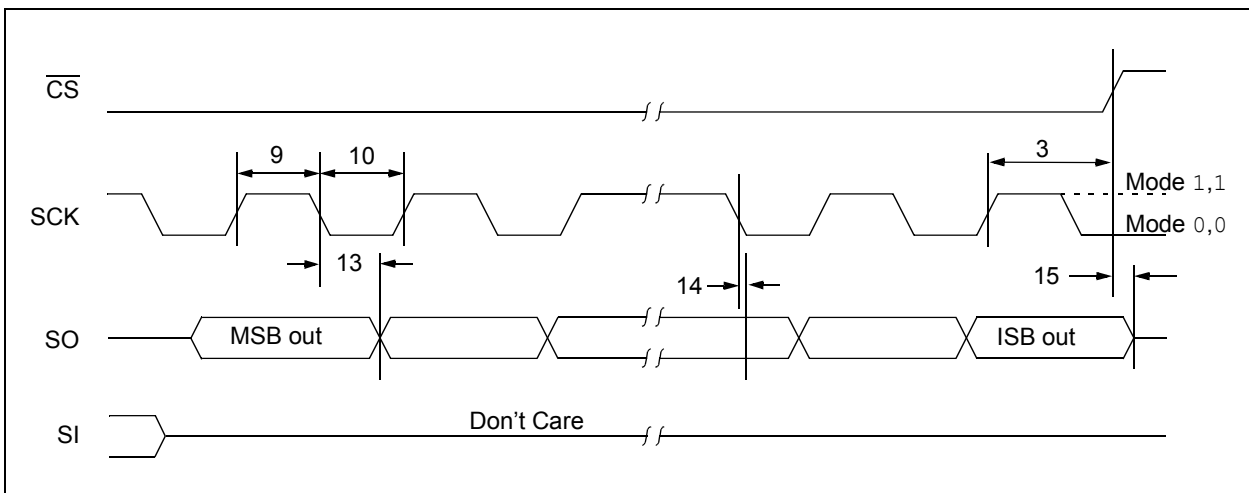


FIGURE 1-3: SERIAL OUTPUT TIMING



25AA02E48

2.0 FUNCTIONAL DESCRIPTION

2.1 Principles of Operation

The 25AA02E48 is a 256-byte Serial EEPROM designed to interface directly with the Serial Peripheral Interface (SPI) port of many of today's popular microcontroller families, including Microchip's PIC[®] microcontrollers. It may also interface with microcontrollers that do not have a built-in SPI port by using discrete I/O lines programmed properly in software to match the SPI protocol.

The 25AA02E48 contains an 8-bit instruction register. The device is accessed via the SI pin, with data being clocked in on the rising edge of SCK. The $\overline{\text{CS}}$ pin must be low and the HOLD pin must be high for the entire operation.

Table 2-1 contains a list of the possible instruction bytes and format for device operation. All instructions, addresses, and data are transferred MSb first, LSb last.

Data (SI) is sampled on the first rising edge of SCK after $\overline{\text{CS}}$ goes low. If the clock line is shared with other peripheral devices on the SPI bus, the user can assert the HOLD input and place the 25AA02E48 in 'HOLD' mode. After releasing the HOLD pin, operation will resume from the point when the HOLD was asserted.

2.2 Read Sequence

The device is selected by pulling $\overline{\text{CS}}$ low. The 8-bit READ instruction is transmitted to the 25AA02E48 followed by an 8-bit address. See Figure 2-1 for more details.

After the correct READ instruction and address are sent, the data stored in the memory at the selected address is shifted out on the SO pin. Data stored in the memory at the next address can be read sequentially by continuing to provide clock pulses to the slave. The internal Address Pointer automatically increments to the next higher address after each byte of data is shifted out. When the highest address is reached (FFh), the address counter rolls over to address 00h allowing the read cycle to be continued indefinitely. The read operation is terminated by raising the $\overline{\text{CS}}$ pin (Figure 2-1).

2.3 Write Sequence

Prior to any attempt to write data to the 25AA02E48, the write enable latch must be set by issuing the WREN instruction (Figure 2-4). This is done by setting $\overline{\text{CS}}$ low and then clocking out the proper instruction into the 25AA02E48. After all eight bits of the instruction are transmitted, $\overline{\text{CS}}$ must be driven high to set the write enable latch. If the write operation is initiated immediately after the WREN instruction without $\overline{\text{CS}}$ driven high, data will not be written to the array since the write enable latch was not properly set.

After setting the write enable latch, the user may proceed by driving $\overline{\text{CS}}$ low, issuing a WRITE instruction, followed by the remainder of the address, and then the data to be written. Up to 16 bytes of data can be sent to the device before a write cycle is necessary. The only restriction is that all of the bytes must reside in the same page. Additionally, a page address begins with XXXX 0000 and ends with XXXX 1111. If the internal address counter reaches XXXX 1111 and clock signals continue to be applied to the chip, the address counter will roll back to the first address of the page and overwrite any data that previously existed in those locations.

Note: Page write operations are limited to writing bytes within a single physical page, **regardless** of the number of bytes actually being written. Physical page boundaries start at addresses that are integer multiples of the page buffer size (or 'page size') and, end at addresses that are integer multiples of page size - 1. If a Page Write command attempts to write across a physical page boundary, the result is that the data wraps around to the beginning of the current page (overwriting data previously stored there), instead of being written to the next page as might be expected. It is therefore necessary for the application software to prevent page write operations that would attempt to cross a page boundary.

For the data to be actually written to the array, the $\overline{\text{CS}}$ must be brought high after the Least Significant bit (D0) of the n^{th} data byte has been clocked in. If $\overline{\text{CS}}$ is driven high at any other time, the write operation will not be completed. Refer to Figure 2-2 and Figure 2-3 for more detailed illustrations on the byte write sequence and the page write sequence respectively. While the write is in progress, the STATUS register may be read to check the status of the WIP, WEL, BP1 and BP0 bits (Figure 2-6). Attempting to read a memory array location will not be possible during a write cycle. Polling the WIP bit in the STATUS register is recommended in order to determine if a write cycle is in progress. When the write cycle is completed, the write enable latch is reset.

BLOCK DIAGRAM



TABLE 2-1: INSTRUCTION SET

Instruction Name	Instruction Format	Description
READ	0000 x011	Read data from memory array beginning at selected address
WRITE	0000 x010	Write data to memory array beginning at selected address
WRDI	0000 x100	Reset the write enable latch (disable write operations)
WREN	0000 x110	Set the write enable latch (enable write operations)
RDSR	0000 x101	Read STATUS register
WRSR	0000 x001	Write STATUS register

x = don't care

FIGURE 2-1: READ SEQUENCE



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FIGURE 2-2: BYTE WRITE SEQUENCE

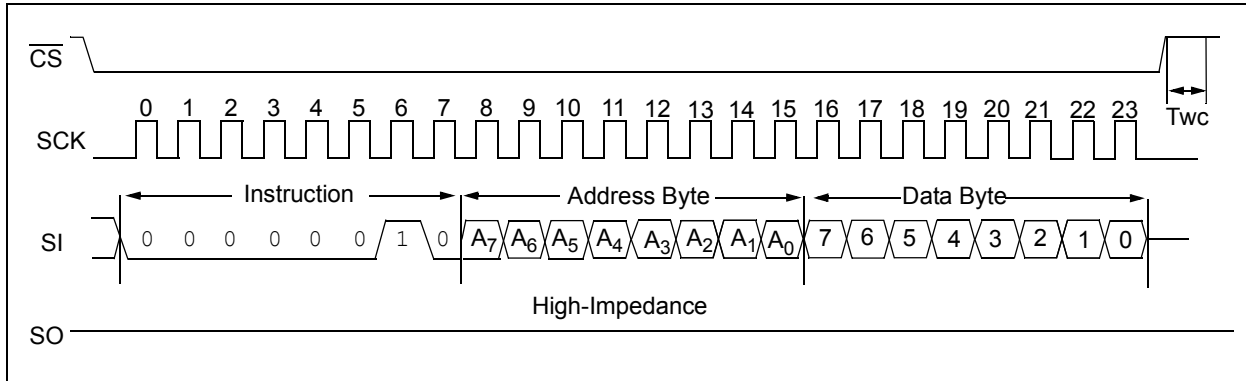
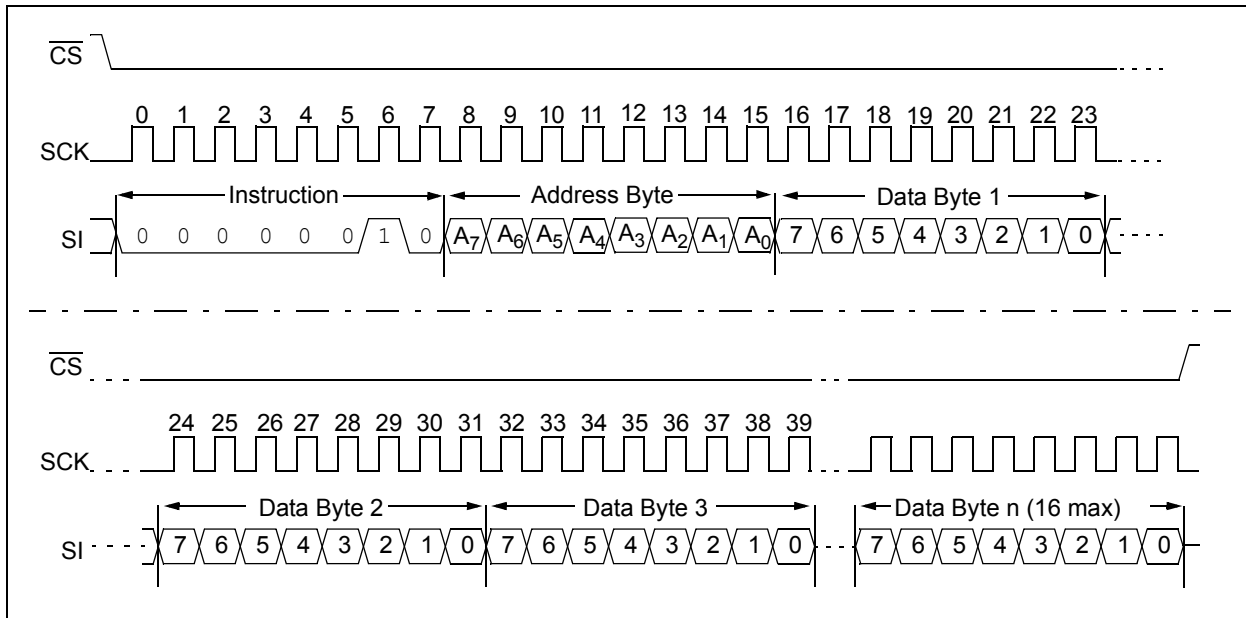


FIGURE 2-3: PAGE WRITE SEQUENCE



2.4 Write Enable (WREN) and Write Disable (WRDI)

The 25AA02E48 contains a write enable latch. See Table 2-4 for the Write-Protect Functionality Matrix. This latch must be set before any write operation will be completed internally. The WREN instruction will set the latch, and the WRDI will reset the latch.

The following is a list of conditions under which the write enable latch will be reset:

- Power-up
- WRDI instruction successfully executed
- WRSR instruction successfully executed
- WRITE instruction successfully executed
- \overline{WP} pin is brought low

FIGURE 2-4: WRITE ENABLE SEQUENCE (WREN)



FIGURE 2-5: WRITE DISABLE SEQUENCE (WRDI)



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2.5 Read Status Register Instruction (RDSR)

The Read Status Register instruction (RDSR) provides access to the STATUS register. See Figure 2-6 for the RDSR timing sequence. The STATUS register may be read at any time, even during a write cycle. The STATUS register is formatted as follows:

TABLE 2-2: STATUS REGISTER

7	6	5	4	3	2	1	0
–	–	–	–	W/R	W/R	R	R
X	X	X	X	BP1	BP0	WEL	WIP

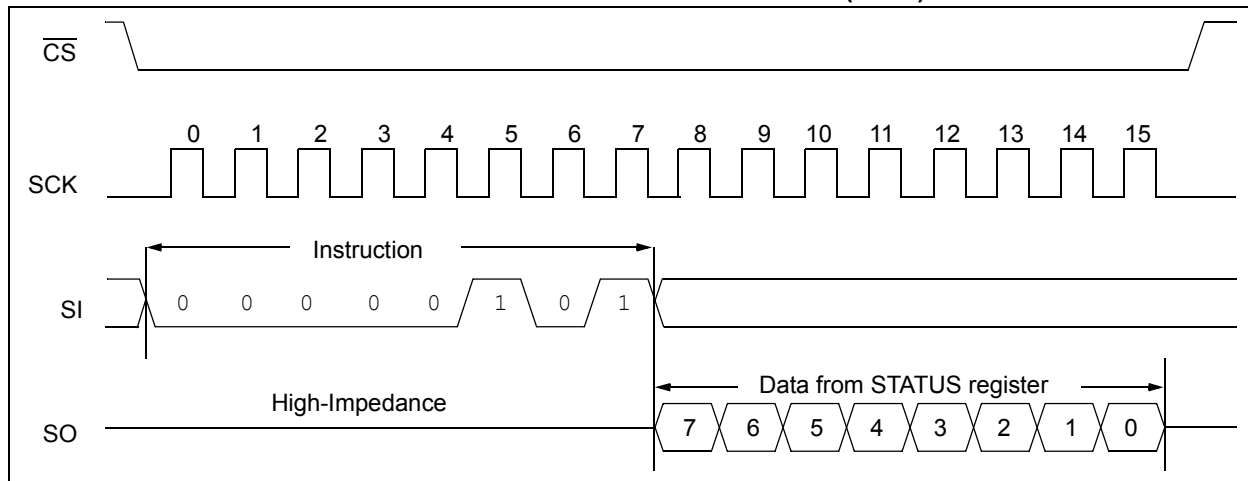
W/R = writable/readable. R = read-only.

The **Write-In-Process (WIP)** bit indicates whether the 25AA02E48 is busy with a write operation. When set to a '1', a write is in progress, when set to a '0', no write is in progress. This bit is read-only.

The **Write Enable Latch (WEL)** bit indicates the status of the write enable latch and is read-only. When set to a '1', the latch allows writes to the array, when set to a '0', the latch prohibits writes to the array. The state of this bit can always be updated via the WREN or WRDI commands regardless of the state of write protection on the STATUS register. These commands are shown in Figure 2-4 and Figure 2-5.

The **Block Protection (BP0 and BP1)** bits indicate which blocks are currently write-protected. These bits are set by the user issuing the WRSR instruction, which is shown in Figure 2-7. These bits are nonvolatile and are described in more detail in Table 2-3.

FIGURE 2-6: READ STATUS REGISTER TIMING SEQUENCE (RDSR)



2.6 Write Status Register Instruction (WRSR)

The Write Status Register instruction (WRSR) allows the user to write to the nonvolatile bits in the STATUS register as shown in Table 2-2. See Figure 2-7 for the WRSR timing sequence. Four levels of protection for the array are selectable by writing to the appropriate bits in the STATUS register. The user has the ability to write-protect none, one, two, or all four of the segments of the array as shown in Table 2-3.

TABLE 2-3: ARRAY PROTECTION

BP1	BP0	Array Addresses Write-Protected
0	0	none
0	1	upper 1/4 (C0h-FFh)
1	0	upper 1/2 (80h-FFh)
1	1	all (00h-FFh)

FIGURE 2-7: WRITE STATUS REGISTER TIMING SEQUENCE (WRSR)



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2.7 Data Protection

The following protection has been implemented to prevent inadvertent writes to the array:

- The write enable latch is reset on power-up
- A write enable instruction must be issued to set the write enable latch
- After a byte write, page write or STATUS register write, the write enable latch is reset
- \overline{CS} must be set high after the proper number of clock cycles to start an internal write cycle
- Access to the array during an internal write cycle is ignored and programming is continued

2.8 Power-On State

The 25AA02E48 powers on in the following state:

- The device is in low-power Standby mode ($\overline{CS} = 1$)
- The write enable latch is reset
- SO is in high-impedance state
- A high-to-low-level transition on \overline{CS} is required to enter active state

TABLE 2-4: WRITE-PROTECT FUNCTIONALITY MATRIX

\overline{WP} (pin 3)	WEL (SR bit 1)	Protected Blocks	Unprotected Blocks	STATUS Register
0 (low)	x	Protected	Protected	Protected
1 (high)	0	Protected	Protected	Protected
1 (high)	1	Protected	Writable	Writable

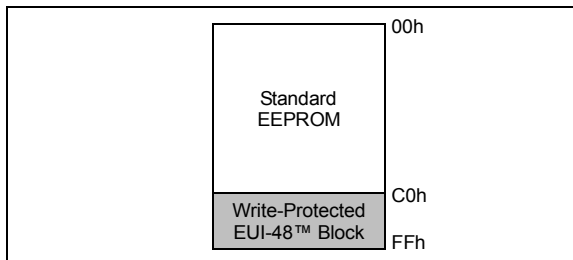
x = don't care

3.0 PRE-PROGRAMMED EUI-48™ NODE ADDRESS

The 25AA02E48 is programmed at the factory with a globally unique, EUI-48™ and EUI-64™ compatible node address stored in the upper 1/4 of the array and write-protected through the STATUS register. The remaining 1,536 bits are available for application use.

The 6-byte EUI-48™ node address value is stored in array locations 0xFA through 0xFF, as shown in Figure 3-2. The first 3 bytes are the Organizationally Unique Identifier (OUI) assigned to Microchip by the IEEE Registration Authority. Microchip's OUI is 0x0004A3. The remaining 3 bytes are the Extension Identifier, and are generated by Microchip to ensure a globally-unique, 48-bit value.

FIGURE 3-1: MEMORY ORGANIZATION



3.1 EUI-64™ Support

The pre-programmed EUI-48 node address can easily be encapsulated at the application level to form a globally unique, 64-bit node address for systems utilizing the EUI-64 standard. This is done by adding 0xFFFFE between the OUI and the Extension Identifier, as shown below.

FIGURE 3-2: EUI-48 NODE ADDRESS PHYSICAL MEMORY MAP EXAMPLE

Description	24-bit Organizationally Unique Identifier			24-bit Extension Identifier		
	Data	00h	04h	A3h	12h	34h
Array Address	FAh			FFh		

Corresponding EUI-48™ Node Address: 00-04-A3-12-34-56

Corresponding EUI-64™ Node Address: 00-04-A3-FF-FE-12-34-56

3.2 Factory-Programmed Write Protection

In order to help guard against accidental corruption of the EUI-48 node address, the BP1 and BP0 bits of the STATUS register are programmed at the factory to '0' and '1', respectively, as shown in the following table:

7	6	5	4	3	2	1	0
X	X	X	X	BP1	BP0	WEL	WIP
—	—	—	—	0	1	—	—

This protects the upper 1/4 of the array (0xC0 to 0xFF) from write operations. This array block can be utilized for writing by clearing the BP bits with a Write Status Register (WRSR) instruction. Note that if this is performed, care must be taken to prevent overwriting the EUI-48 value.

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4.0 PIN DESCRIPTIONS

The descriptions of the pins are listed in Table 4-1.

TABLE 4-1: PIN FUNCTION TABLE

Name	SOIC	SOT-23	Function
$\overline{\text{CS}}$	1	5	Chip Select Input
SO	2	4	Serial Data Output
$\overline{\text{WP}}$	3	—	Write-Protect Pin
Vss	4	2	Ground
SI	5	3	Serial Data Input
SCK	6	1	Serial Clock Input
$\overline{\text{HOLD}}$	7	—	Hold Input
Vcc	8	6	Supply Voltage

4.1 Chip Select ($\overline{\text{CS}}$)

A low level on this pin selects the device. A high level deselects the device and forces it into Standby mode. However, a programming cycle which is already initiated or in progress will be completed, regardless of the $\overline{\text{CS}}$ input signal. If $\overline{\text{CS}}$ is brought high during a program cycle, the device will go into Standby mode as soon as the programming cycle is complete. When the device is deselected, SO goes to the high-impedance state, allowing multiple parts to share the same SPI bus. A low-to-high transition on $\overline{\text{CS}}$ after a valid write sequence initiates an internal write cycle. After power-up, a low level on $\overline{\text{CS}}$ is required prior to any sequence being initiated.

4.2 Serial Output (SO)

The SO pin is used to transfer data out of the 25AA02E48. During a read cycle, data is shifted out on this pin after the falling edge of the serial clock.

4.3 Write-Protect ($\overline{\text{WP}}$)

The $\overline{\text{WP}}$ pin is a hardware write-protect input pin. When it is low, all writes to the array or STATUS register are disabled, but any other operations function normally. When $\overline{\text{WP}}$ is high, all functions, including nonvolatile writes operate normally. At any time, when $\overline{\text{WP}}$ is low, the write enable Reset latch will be reset and programming will be inhibited. However, if a write cycle is already in progress, $\overline{\text{WP}}$ going low will not change or disable the write cycle. See Table 2-4 for the Write-Protect Functionality Matrix.

4.4 Serial Input (SI)

The SI pin is used to transfer data into the device. It receives instructions, addresses and data. Data is latched on the rising edge of the serial clock.

4.5 Serial Clock (SCK)

The SCK is used to synchronize the communication between a master and the 25AA02E48. Instructions, addresses or data present on the SI pin are latched on the rising edge of the clock input, while data on the SO pin is updated after the falling edge of the clock input.

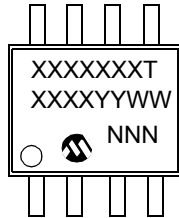
4.6 Hold ($\overline{\text{HOLD}}$)

The $\overline{\text{HOLD}}$ pin is used to suspend transmission to the 25AA02E48 while in the middle of a serial sequence without having to retransmit the entire sequence again. It must be held high any time this function is not being used. Once the device is selected and a serial sequence is underway, the $\overline{\text{HOLD}}$ pin may be pulled low to pause further serial communication without resetting the serial sequence. The $\overline{\text{HOLD}}$ pin must be brought low while SCK is low, otherwise the $\overline{\text{HOLD}}$ function will not be invoked until the next SCK high-to-low transition. The 25AA02E48 must remain selected during this sequence. The SI, SCK and SO pins are in a high-impedance state during the time the device is paused and transitions on these pins will be ignored. To resume serial communication, $\overline{\text{HOLD}}$ must be brought high while the SCK pin is low, otherwise serial communication will not resume. Lowering the $\overline{\text{HOLD}}$ line at any time will tri-state the SO line.

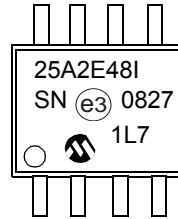
5.0 PACKAGING INFORMATION

5.1 Package Marking Information

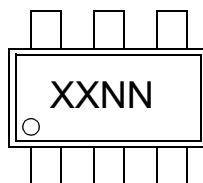
8-Lead SOIC



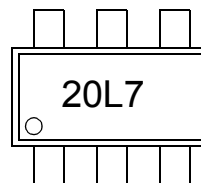
Example:



6-Lead SOT-23



Example:



Part Number	1st Line Marking Code
	SOT-23
	I Temp.
25AA02E48	20NN

Note: NN = Alphanumeric traceability code

Legend:	XX...X Part number or part number code
	T Temperature (I, E)
	Y Year code (last digit of calendar year)
	YY Year code (last 2 digits of calendar year)
	WW Week code (week of January 1 is week '01')
	NNN Alphanumeric traceability code (2 characters for small packages)
	e3 Pb-free JEDEC designator for Matte Tin (Sn)
Note:	For very small packages with no room for the Pb-free JEDEC designator e3, the marking will only appear on the outer carton or reel label.
Note:	In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

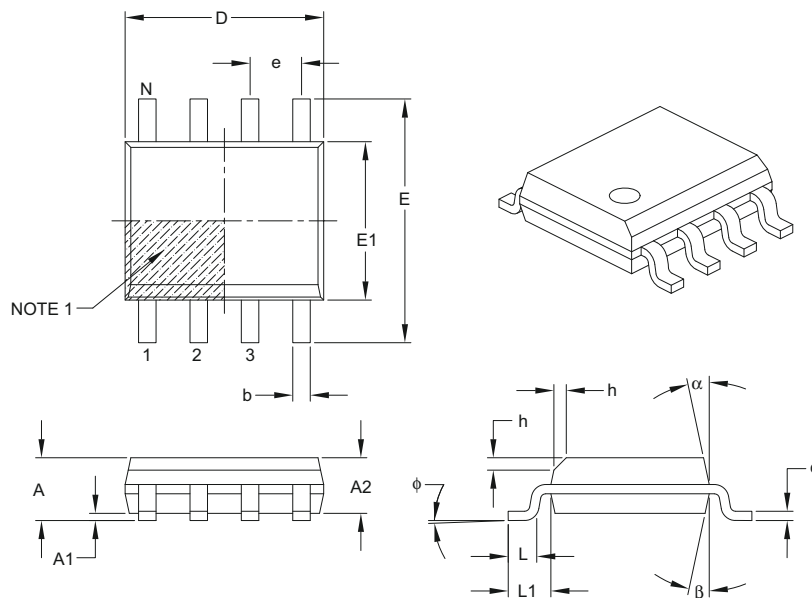
Note: Please visit www.microchip.com/Pbfree for the latest information on Pb-free conversion.

*Standard OTP marking consists of Microchip part number, year code, week code, and traceability code.

25AA02E48

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	8		
Pitch	e	1.27 BSC		
Overall Height	A	–	–	1.75
Molded Package Thickness	A2	1.25	–	–
Standoff §	A1	0.10	–	0.25
Overall Width	E	6.00 BSC		
Molded Package Width	E1	3.90 BSC		
Overall Length	D	4.90 BSC		
Chamfer (optional)	h	0.25	–	0.50
Foot Length	L	0.40	–	1.27
Footprint	L1	1.04 REF		
Foot Angle	ϕ	0°	–	8°
Lead Thickness	c	0.17	–	0.25
Lead Width	b	0.31	–	0.51
Mold Draft Angle Top	α	5°	–	15°
Mold Draft Angle Bottom	β	5°	–	15°

Notes:

- Pin 1 visual index feature may vary, but must be located within the hatched area.
- § Significant Characteristic.
- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.

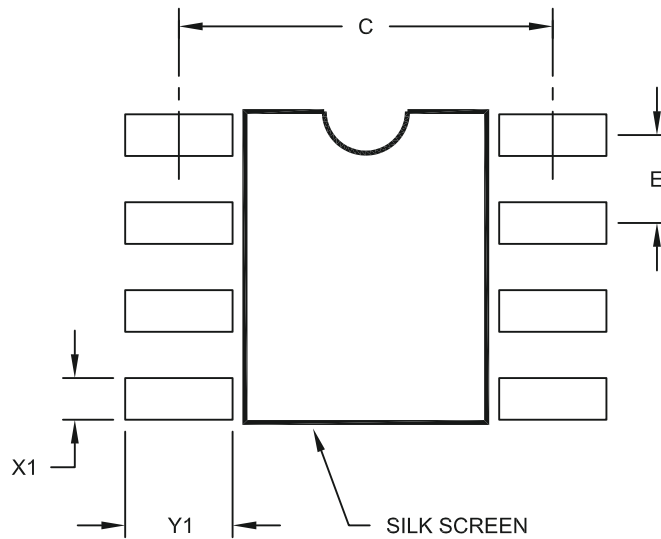
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-057B

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	1.27 BSC		
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

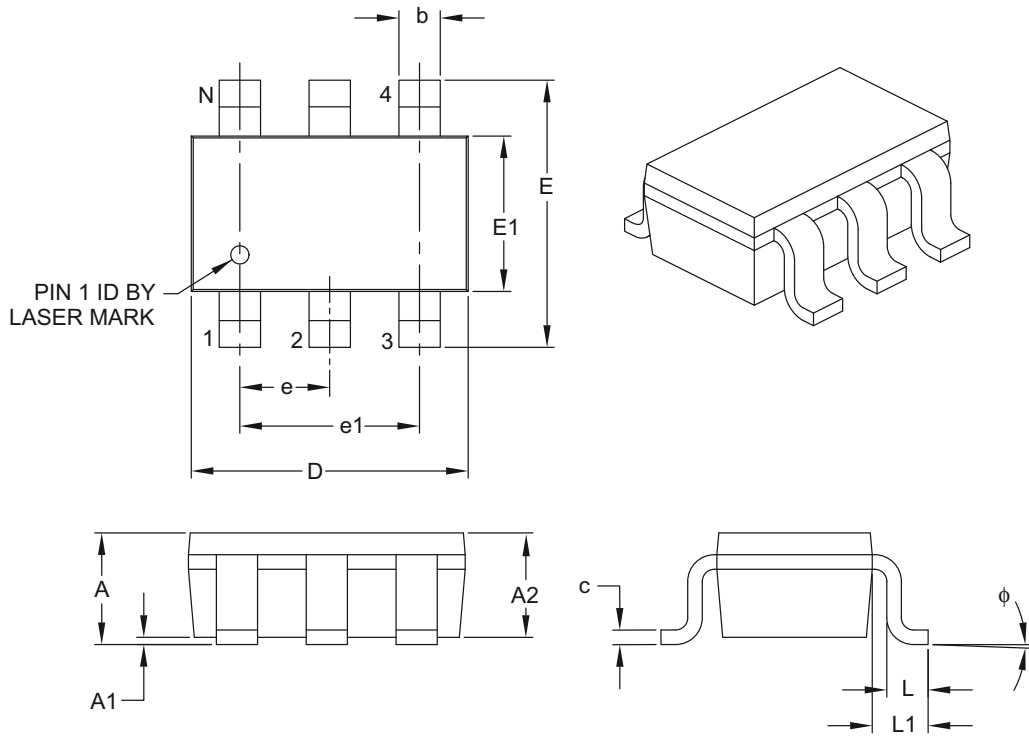
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2057A

25AA02E48

6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Number of Pins	N	6		
Pitch	e	0.95 BSC		
Outside Lead Pitch	e1	1.90 BSC		
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

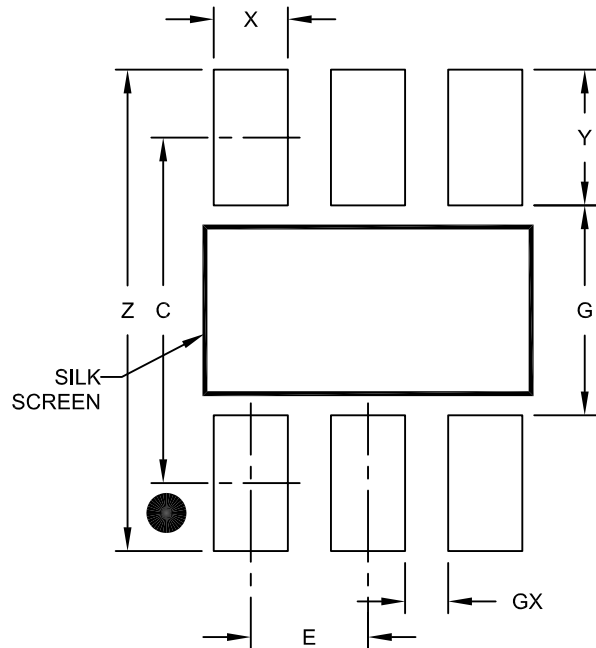
Notes:

- Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
- Dimensioning and tolerancing per ASME Y14.5M.
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-028B

6-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



RECOMMENDED LAND PATTERN

Dimension Limits	Units	MILLIMETERS		
		MIN	NOM	MAX
Contact Pitch	E	0.95 BSC		
Contact Pad Spacing	C		2.80	
Contact Pad Width (X6)	X			0.60
Contact Pad Length (X6)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2028A

25AA02E48

APPENDIX A: REVISION HISTORY

Revision A (12/08)

Original release of this document.

Revision B (04/10)

Removed Preliminary status; Revised Section 2.0; Add sentence to Section 3.0; Add SOT-23 Land Pattern.

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Device	Tape & Reel			Temperature	Package
Device:	25AA02E48				2k-Bit, 1.8V, 16 Byte Page, SPI Serial EEPROM with EUI-48™ Node Identity
Tape & Reel:	Blank =				Standard packaging
	T =				Tape & Reel
Temperature Range:	I =				-40°C to+85°C
Package:	SN =				Plastic SOIC (3.90 mm body), 8-lead
	OT =				SOT-23, 6-lead (Tape and Reel only)

Examples:

- a) 25AA02E48-I/SN = 2k-bit, 16-byte page, 1.8V Serial EEPROM, Industrial temp., SOIC package
- b) 25AA02E48T-I/SN = 2k-bit, 16-byte page, 1.8V Serial EEPROM, Industrial temp., Tape & Reel, SOIC package
- c) 25AA02E48T-I/OT = 2k-bit, 16-byte page, 1.8V Serial EEPROM, Industrial temp., Tape & Reel, SOT-23 package

25AA02E48

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