STRUCTURE Silicon Monolithic Integrated Circuit

PRODUCT SERIES Voltage Regulator with Watchdog Timer Reset

TYPE BD3021HFP—M

FEATURES 1. High output voltage precision: 5 V ±2% / low dropout voltage / low quiescent current：80μA(TYP)
2. INH for WDT(ON/OFF function) /built-in OCP/ built-in TSD

○ABSOLUTE MAXIMUM RATINGS(Ta=25℃)

Parameter	Symbol	Limits	Unit
Supply Voltage ※1	Vcc	-0.3～+50	V
INH pin voltage	INH	-0.3～+15	V
Regulator output pin voltage	VOUT	-0.3～+15	V
Reset output pin voltage	VRESET	-0.3～+15	V
Watchdog input pin voltage	VCLK	-0.3～+15	V
Reset delay setting pin voltage	VCT	-0.3～+15	V
Power dissipation ※2	Pd	1.6	W
Operating temperature range	Topr	-40～+125	℃
Storage temperature range	Tstg	-55～+150	℃
Maximum junction temperature	Tjmax	150	℃

※1 Not to exceed Pd.
※2 Reduced by 12.8mW / °C over Ta = 25°C, when mounted on glass epoxy board: 70mm×70mm×1.6mm.

○OPERATING CONDITIONS（Ta=-40～+125℃）

Parameter	Symbol	Min	Max	Unit
Supply Voltage ※3	Vcc	5.6	36.0	V
Output Current	Io	0	500	mA

※3 For the output voltage, consider the voltage drop (dropout voltage) due to the output current.

NOTE : This product is not designed for protection against radioactive rays.

Status of this document
The Japanese version of this document is the formal specification.
A customer may use this translation version only for a reference to help reading the formal version.
If there are any differences in translation version of this document, formal version takes priority.

○ELECTRICAL CHARACTERISTICS

（Unless otherwise specified, Ta=-40～+125℃, Vcc=13.5V, INH=5V, CLK=GND）

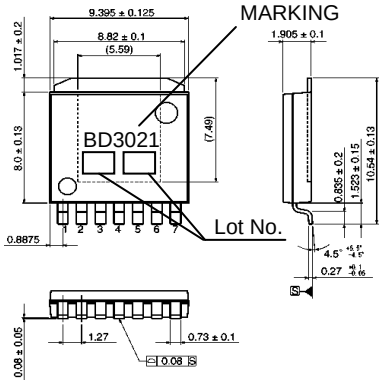
Parameter	Symbol	Limit			Unit	Conditions
		Min	Typ	Max		
Overall Device						
Bias current 1	Icc1	–	80	130	μA	Io=0mA
Bias current 2	Icc2	–	150	300	μA	Io=50mA（Ta=25℃）
Regulator						
Output voltage	VOUT	4.90	5.00	5.10	V	Io=200mA
Line regulation	Line.Reg	–	5	35	mV	Vcc=5.6～36V
Load regulation	Load.Reg	–	30	70	mV	Io=5～200mA
Dropout voltage	ΔVd	–	0.3	0.6	V	Vcc=4.75V, Io=200mA
Ripple rejection	R.R.	45	55	–	dB	f=120Hz, ein=1Vrms, Io=100mA
Reset						
Detection voltage	Vdet	4.40	4.50	4.60	V	
Hysteresis width	VHS	50	100	150	mV	
Output delay time Low → High (Power on reset time) ※1	TdLH	1.1	1.9	2.7	ms	Vdet±0.5V（Vcc=VOUT） CT=0.01μF
Low output voltage	VRST	–	0.1	0.2	V	VOUT=4.0V
Min. operating voltage	VOPL	1.5	–	–	V	
Watchdog timer						
CT switching threshold voltage High	VthH	1.08	1.15	1.25	V	WDT ON, INH=Open
CT switching threshold voltage Low	VthL	0.13	0.15	0.17	V	WDT ON, INH=Open
WDT Charge current	Ictc	3.5	6.0	8.5	μA	WDT ON, INH=Open, CT=0V
WDT Discharge current	Ictd	1.2	2.0	2.8	μA	WDT ON, INH=Open ,CT=1.3V
Watchdog monitor time Low ※2	TWH	3.0	5.0	7.0	ms	WDT ON, INH=Open CT=0.01μF（Ceramic Cap） ※Characteristics of ceramic cap not considered.
Watchdog reset time ※3	TWL	1.0	1.7	2.4	ms	
CLK Input pulse width	TWCLK	500	–	–	ns	
INH						
WDT OFF threshold voltage	VHINH	VOUT ×0.8	–	VOUT	V	
WDT ON threshold voltage	VLINH	0	–	VOUT ×0.3	V	
INH Input current	IINH	–	10	20	μA	INH=5V

※1 TdLH can be changed by varying the CT capacitance value.
TdLH(s)≒(1.15×CT(μF))/Ictc(μA) (TYP)

※2 TWH can be changed by varying the CT capacitance value.
TWH(s)≒(1.00×CT(μF))/Ictd(μA) (TYP)

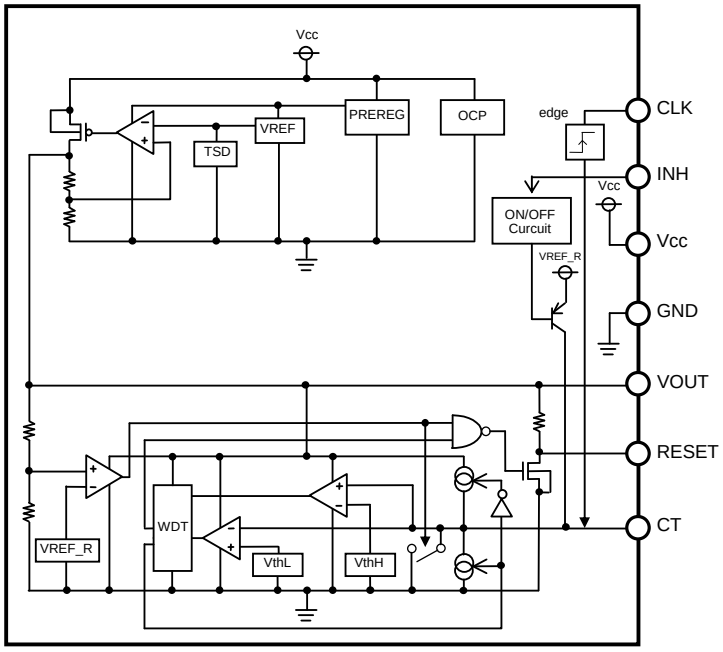
※3 TWL can be changed by varying the CT capacitance value.
TWL(s)≒(1.00×CT(μF))/Ictc(μA) (TYP)

○PHYSICAL DIMENSIONS, MARKING



HRP-7 (UNIT：mm)

○BLOCK DIAGRAM



○Pin Number, Pin Name

Pin Number	Pin Name	Function
1	CLK	Clock Input from Microcontroller
2	INH	WDT ON/OFF Function Pin
3	Vcc	Power Supply Pin
4	GND	GND
5	VOUT	Voltage Output Pin
6	RESET	Reset Output Pin
7	CT	External Capacitance for Reset Output Delay Time, WDT Monitor Time Setting Connection Pin
FIN	GND	GND

○Pin Settings / Precautions

1. Vcc pin

Insert a 0.33μF～1000μF capacitor between the Vcc and GND pins.The appropriate capacitance value varies by application. Be sure to allow a sufficient margin for input voltage levels.

2. Output pins

It is necessary to place capacitors between each output pin and GND to prevent oscillation on the output. Usable capacitance values range from 0.1μF～1000μF. Abrupt fluctuations in input voltage and load conditions may affect the output voltage. Output capacitance values should be determined only through sufficient testing of the actual application.

○Operation Notes

1. Absolute maximum ratings

Use of the IC in excess of absolute maximum ratings (such as the input voltage or operating temperature range) may result in damage to the IC. Assumptions should not be made regarding the state of the IC (e.g., short mode or open mode) when such damage is suffered. If operational values are expected to exceed the maximum ratings for the device, consider adding protective circuitry (such as fuses) to eliminate the risk of damaging the IC.

2. Electrical characteristics described in these specifications may vary, depending on temperature, supply voltage, external circuits and other conditions. Therefore, be sure to check all relevant factors, including transient characteristics.

3. GND potential

The potential of the GND pin must be the minimum potential in the system in all operating conditions. Ensure that no pins are at a voltage below the GND at any time, regardless of transient characteristics.

4. Ground wiring pattern

When using both small-signal and large-current GND traces, the two ground traces should be routed separately but connected to a single ground potential within the application in order to avoid variations in the small-signal ground caused by large currents. Also ensure that the GND traces of external components do not cause variations on GND voltage. The power supply and ground lines must be as short and thick as possible to reduce line impedance.

5. Inter-pin shorts and mounting errors

Use caution when orienting and positioning the IC for mounting on printed circuit boards. Improper mounting may result in damage to the IC. Shorts between output pins or between output pins and the power supply or GND pins (caused by poor soldering or foreign objects) may result in damage to the IC.

6. Operation in strong electromagnetic fields

Using this product in strong electromagnetic fields may cause IC malfunction. Caution should be exercised in applications where strong electromagnetic fields may be present.

7. Testing on application boards
When testing the IC on an application board, connecting a capacitor directly to a low-impedance pin may subject the IC to stress. Always discharge capacitors completely after each process or step. The IC's power supply should always be turned off completely before connecting or removing it from a jig or fixture during the evaluation process. To prevent damage from static discharge, ground the IC during assembly and use similar precautions during transport and storage.

8. Thermal consideration
Use a thermal design that allows for a sufficient margin in light of the Pd in actual operating conditions.
Consider Pc that does not exceed Pd in actual operating conditions.（Pd≧Pc）

（Tjmax : Maximum junction temperature=150℃, Ta : Peripheral temperature[℃] ,
θja : Thermal resistance of package-ambience[℃/W], Pd : Package Power dissipation [W],
Pc : Power dissipation [W], Vcc : Input Voltage, VOUT : Output Voltage, Io : Load, Icc2 : Bias Current2）

Package Power dissipation : Pd (W)＝(Tjmax－Ta)／θja
Power dissipation : Pc (W)＝(Vcc－VOUT)×Io＋Vcc×Icc2

9. Over current protection circuit (OCP)
The IC incorporates an integrated over-current protection circuit that operates in accordance with the rated output capacity. This circuit serves to protect the IC from damage when the load becomes shorted. It is also designed to limit output current (without latching) in the event of a large and instantaneous current flow from a large capacitor or other component. These protection circuits are effective in preventing damage due to sudden and unexpected accidents. However, the IC should not be used in applications characterized by the continuous or transitive operation of the protection circuits.

10. Thermal shutdown circuit (TSD)
The IC incorporates a built-in thermal shutdown circuit, which is designed to turn the IC off completely in the event of thermal overload. It is not designed to protect the IC from damage or guarantee its operation. ICs should not be used after this function has activated, or in applications where the operation of this circuit is assumed.

11. Applications or inspection processes where the potential of the Vcc pin or other pins may be reversed from their normal state may cause damage to the IC's internal circuitry or elements. Use an output pin capacitance of 1000μF or lower in case Vcc is shorted with the GND pin while the external capacitor is charged. Insert a diode in series with Vcc to prevent reverse current flow, or insert bypass diodes between Vcc and each pin.

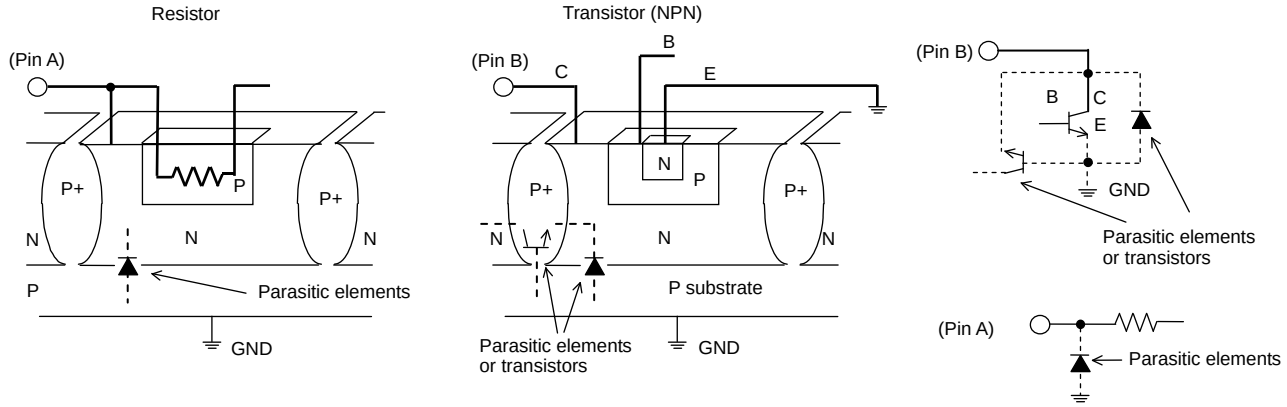
12. Positive voltage surges on VCC pin
A power zener diode should be inserted between VCC and GND for protection against voltage surges of more than 50V on the VCC pin.

13. Negative voltage surges on VCC pin
A schottky barrier diode should be inserted between VCC and GND for protection against voltages lower than GND on the VCC pin.

14. Output protection diode
Loads with large inductance components may cause reverse current flow during startup or shutdown. In such cases, a protection diode should be inserted on the output to protect the IC.

15. Regarding input pins of the IC
This monolithic IC contains P+ isolation and P substrate layers between adjacent elements in order to keep them isolated. PN junctions are formed at the intersection of these P layers with the N layers of other elements, creating parasitic diodes and/or transistors.
For example (refer to the figure below):
- ●When GND > Pin A and GND > Pin B, the PN junction operates as a parasitic diode
- ●When GND > Pin B, the PN junction operates as a parasitic transistor

Parasitic diodes occur inevitably in the structure of the IC, and the operation of these parasitic diodes can result in mutual interference among circuits, operational faults, or physical damage. Accordingly, conditions that cause these diodes to operate, such as applying a voltage lower than the GND voltage to an input pin (and thus to the P substrate) should be avoided.



Example of Simple Monolithic IC Architecture

Notes

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