# 4.5 Gb, DDR3, 64 M x 72 Integrated Module (IMOD)

## FEATURES

- DDR3 Integrated Module [iMOD]:
  - Vcc=VccQ=1.5V ± 0.075V
  - 1.5V center-terminated, push/pull I/O
  - Package: 25mm x 25mm, 16 x 16 matrix w/ 255 balls
  - Matrix ball pitch: 1.00mm
- Space saving footprint
- Thermally enhanced, Impedance matched, integrated packaging
- Differential, bidirectional data strobe
- 8n-bit prefetch architecture
- 8 internal banks (per word, 9 Bytes integrated in package)
- Nominal and dynamic on-die termination (ODT) for data, strobe, and mask signals.
- CAS (READ) latency (CL): 6, 8, and 10
- CAS (WRITE) latency (CWL): 6, 7 and 8
- Fixed burst length (BL) of 8 and burst chop (BC) of 4
- Selectable BC4 or BL8 on-the-fly (OTF)
- Self/Auto Refresh modes
- Operating Temperature Range (Case Temp=Tc)
  - Industrial: -40˚C to 85˚C supporting SELF & AUTO REFRESH
  - Extended: -40˚C to 105˚C; manual REFRESH only
  - Mil-Temp: -55˚C to 125˚C; manual REFRESH only
- CORE clocking frequencies:
  - Industrial: 667MHz, 533MHz and 400MHz
  - Extended: 533MHz and 400MHz
  - Mil-Temp: 400MHz
- Data Transfer Rates:
  - Industrial: 1333, 1066 and 800 Mbps
  - Extended: 1066 and 800 Mbps
  - Mil-Temp: 800 Mbps
- Write leveling
- Multipurpose register
- Output Driver Calibration

## Benefits

- 20% space savings while providing a surface mount friendly pitch (1.00mm)
- Reduced I/O (46%)
- 25% improvement in routings for your memory array
- Reduced trace lengths due to the highly integrated, impedance matched packaging
- Thermally enhanced packaging technology allow silicon integration without performance degradation due to power dissipation (heat)
- High TCE organic laminate interposer for improved glass stability over a wide operating temperature
- Suitability of use in High Reliability applications requiring Mil-temp, non-hermetic device operation

*Note: This integrated product is currently under consideration. Latest product status, information, and/or corresponding documents should be obtained from LDI prior to your design considerations.

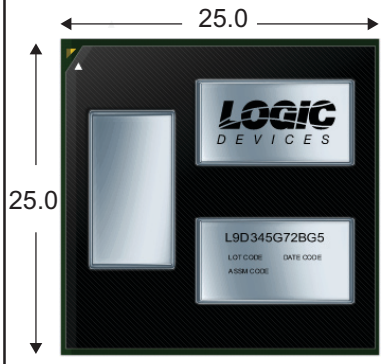
## iMOD Part Information

| Order Number | Speed Grade | Device Grade | Pkg Footprint | I/O | Pitch | Pkg No. |
|---|---|---|---|---|---|---|
| L9D345G72BG5I15 | DDR3-1333 | Industrial | 25mm x 25mm | 255 | 1.00mm | BG5 |
| L9D345G72BG5E19 | DDR3-1066 | Extended | | | | |
| L9D345G72BG5M25 | DDR3-800 | Mil-Temp | | | | |

iMOD
integrated module products

# 4.5 Gb, DDR3, 64 M x 72 Integrated Module (IMOD)

## Integrated vs. Monolithic Solutions - highlights

| OPTIONS | Monolithic Solution | IMOD Solution | SAVINGS |
|---|---|---|---|
| |  |  | |
| Area | 5 x 139.5mm$^2$ + component space = ~775mm$^2$ | 625 mm$^2$ | ~20% |
| I/O | 5 x 96 pins = 480 pins total | 255 Balls/Locations | 46% |

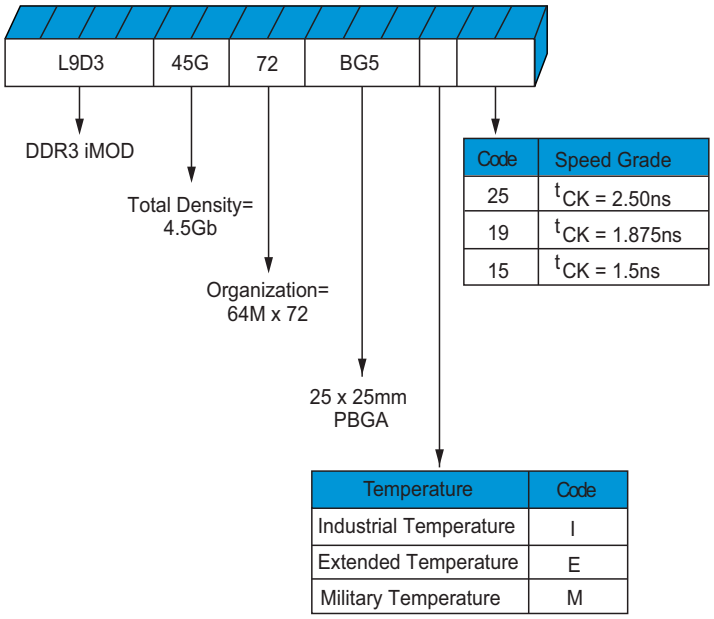
## Table 1: Key Timing Parameters

| Device Grade | Speed Grade | Speed Mark | Part Ordering Information | CORE Freq. [MHz] Support | Data Rate [Mbps] Support | Target $^t$RCD-$^t$RP-CL | $^t$RCD [ns] | $^t$RP [ns] | CL [ns] |
|---|---|---|---|---|---|---|---|---|---|
| INDUSTRIAL | DDR3-1333 | 15 | L9D345G72BG5I15 | 667/533/400 | 1333/1066/800 | 10-10-10/8-8-8/6-6-6 | 15 | 15 | 15 |
| EXTENDED | DDR3-1066 | 19 | L9D345G72BG5E19 | 533/400 | 1066/800 | 8-8-8/6-6-6 | 15 | 15 | 15 |
| MIL-TEMP | DDR3-800 | 25 | L9D345G72BG5M25 | 400 | 800 | 6-6-6 | 15 | 15 | 15 |

## FEATURES

### FIGURE 1 - 1Gb DDR3 PART NUMBERS

Sample Part Number: L9D345G72BG5M15




| Code | Speed Grade |
|---|---|
| 25 | $^{t}$CK = 2.50ns |
| 19 | $^{t}$CK = 1.875ns |
| 15 | $^{t}$CK = 1.5ns |

| Temperature | Code |
|---|---|
| Industrial Temperature | I |
| Extended Temperature | E |
| Military Temperature | M |

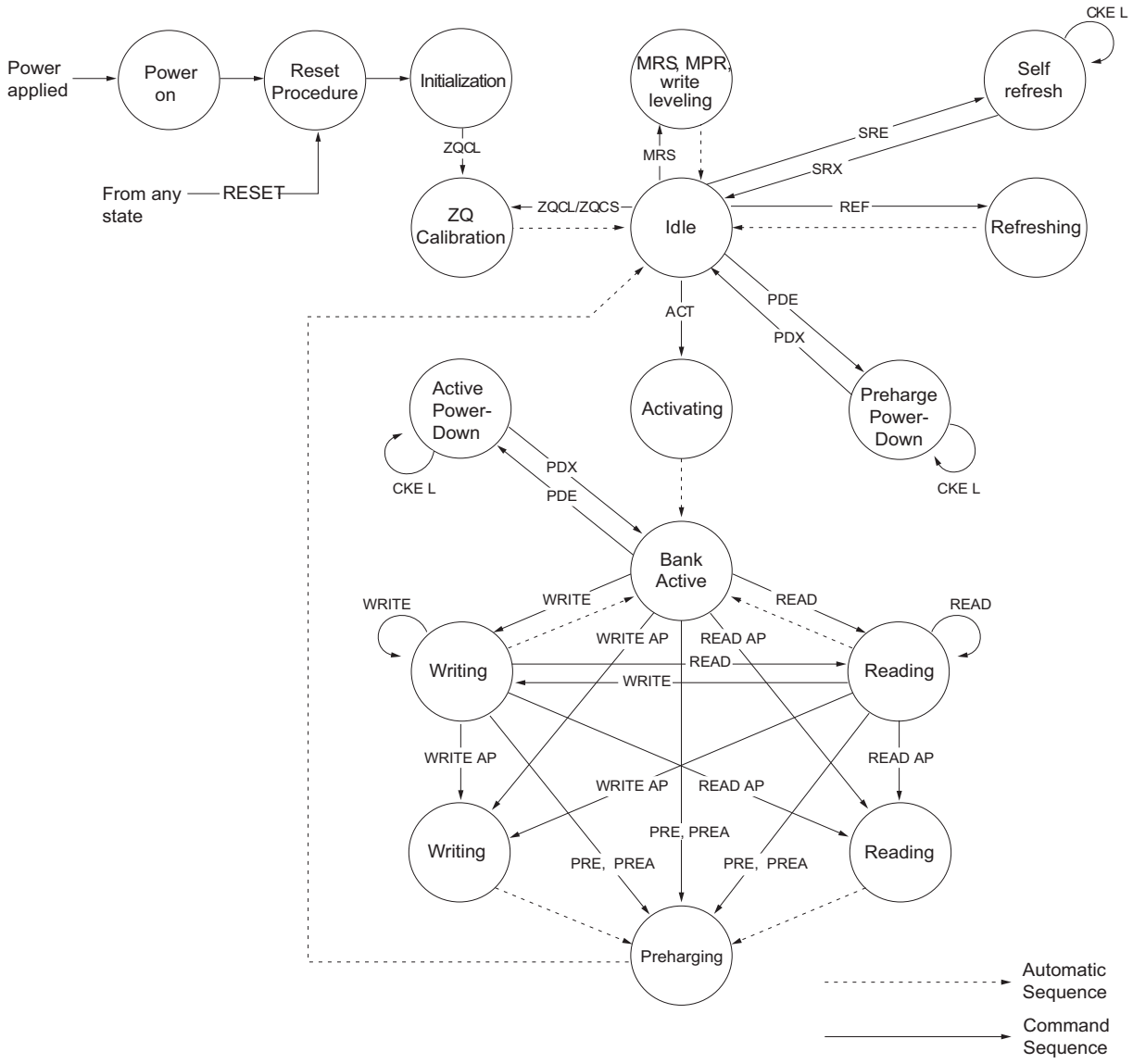
Note: Not all options can be combined. Please see our Part Catalog for available offerings.

### TABLE 2: ADDRESSING

| Parameter | 64 Meg x 72 |
|---|---|
| Configuration | [8 Meg x 8 banks x 16] x 4.5 |
| Refresh Count | 8K |
| ROW Addressing | 8K (A[12:0]) |
| Back Addressing | 8 (BA[2:0]) |
| Column Addressing | 1K (A[9:0]) |

## STATE DIAGRAM

### FIGURE 2 - SIMPLIFIED STATE DIAGRAM




ACT = ACTIVATE
MPR = Multipurpose register
MRS = Mode register set
PDE = Power-down entry
PDX = Power-down exit
PRE = PRECHARGE
PREA=PRECHARGE ALL
READ = RD, RDS4, RDS8
READ AP = RDAP, RDAPS4, RDAPS8
REF = REFRESH
RESET = START RESET PROCEDURE
SRE = Self refresh entry
SRX = Self refresh exit
WRITE = WR, WRS4, WRS8
WRITE AP = WRAP, WRAPS4, WRAPS8
ZQCL = ZQ LONG CALIBRATION
ZQCS = ZQ SHORT CALIBRATION

## FUNCTIONAL DESCRIPTION

The DDR3 SDRAM uses double data rate architecture to achieve high speed operation. The double data rate (DDR) architecture is an 8n prefetch with an interface designed to transfer two data words per clock cycle at the I/O pins. A single READ or WRITE access for the DDR3 SDRAM consists of a single 8n-bit-wide, one-clock-cycle data transfer at the internal memory core and eight corresponding n-bit-wide, one-half-clock-cycle data transfer at the I/O pin.

The differential strobes (LDQSx, LDQSx\, UDQSx, UDQSx\) is transmitted externally, along with data, for use in data capture at the DDR3 SDRAM input receiver. DQS is center-aligned with data for WRITEs. The READ data is transmitted by the DDR3 SDRAM and edge-aligned to the data strobes.

The DDR3 SDRAM operates from a differential clock (CKx, CKx\). The crossing of CK going HIGH and CK\ going LOW is referred to as the positive edge of Clock (CK). Control, Command, and Address signals are registered at every positive edge of CK. Input data is registered on the first rising edge of DQS after the WRITE preamble, and output data is referenced on the first rising edge of DQS after the READ preamble.

READ and WRITE accesses to the DDR3 SDRAM are burst-oriented. Accesses start at a selected location and continue for a programmed number of locations in a programmed sequence. Accesses begin with the registration of an ACTIVATE command, which is then followed by a READ or WRITE command. The address bits registered coincident with the ACTIVATE command are used to select the bank and the starting column location for the burst access.

DDR3 SDRAM devices use READ and WRITE BL8 and BC4. An AUTO PRECHARGE function may be enabled to provide a self-timed ROW PRECHARGE that is initiated at the end of the burst access.

As with standard DDR SDRAM devices, the pipelined, multi-bank architecture of the DDR3 SDRAM allows for concurrent operation, thereby providing high bandwidth by hiding ROW PRECHARGE and ACTIVATION time.

A SELF REFRESH mode is provided for all temperature grade offerings along with AUTO SELF REFRESH for Industrial product, as well as, power-saving, POWER-DOWN mode.

## INDUSTRIAL TEMPERATURE

The industrial temperature (I) device requires the case temperature not exceed -40˚C or +85˚C. JEDEC specifications require the REFRESH rate to double when Tc exceeds +85˚C; this also requires use of the high-temperature SELF REFRESH option. Additionally, ODT resistance and the INPUT/OUTPUT impedance must be derated when the Tc is <0˚C or >+85˚C.

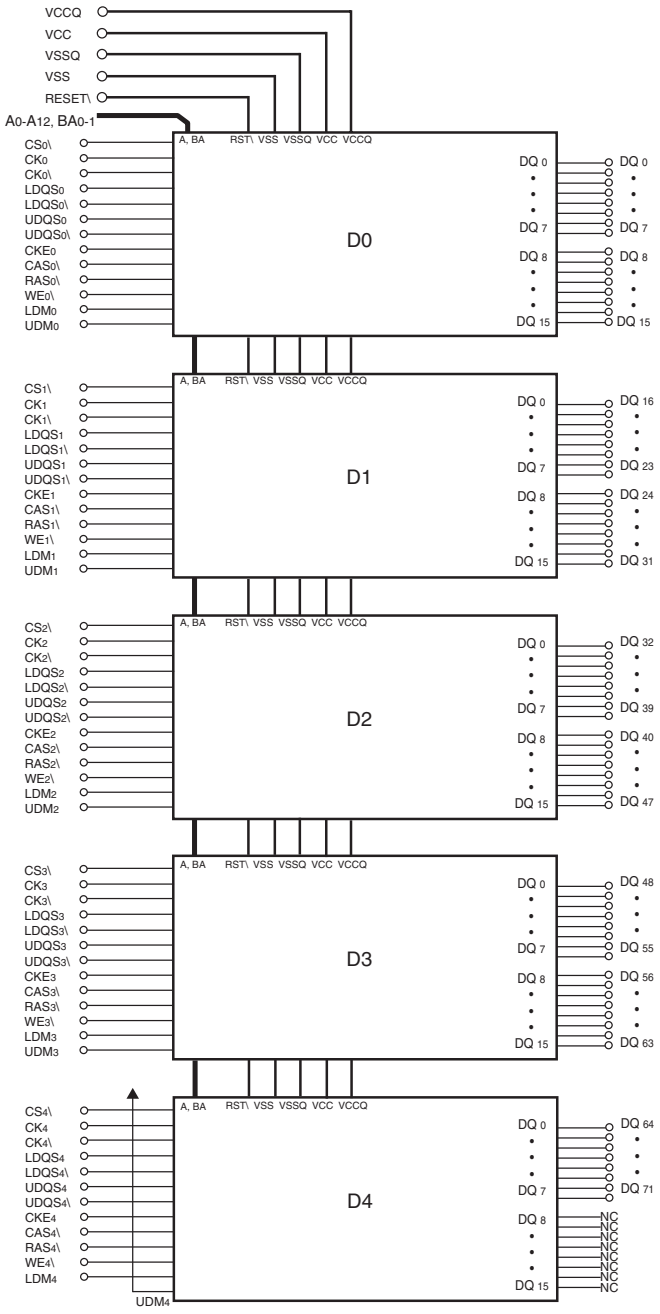
## EXTENDED TEMPERATURE

The Extended temperature (E) device requires the case temperature not exceed -40˚C or +105˚C. JEDEC specifications require the refresh rate to double when Tc exceeds +85˚C; this also requires use of the high-temperature SELF REFRESH option. Additionally, ODT resistance and the INPUT/OUTPUT impedance must be derated when the Tc is <0˚C or >85˚C.

## MILITARY, EXTREME OPERATING TEMPERATURE

The Mil-Temp (M) device requires the case temperature not exceed -55˚C or +125˚C. JEDEC requires the REFRESH rate double when Tc exceeds +85˚C and LDI recommends an additional derating as specified in this document as to properly maintain the DRAM core cell charge at temperatures above Tc>105˚C.

## FIGURE 3 - FUNCTIONAL BLOCK DIAGRAM



## BALL /SIGNAL LOCATION (PBGA)

### FIGURE 4 - SDRAM - DDR3 PINOUT TOP VIEW

| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| A | | DQ0 | DQ14 | DQ15 | VSS | VSS | A9 | A10 | A11 | A8 | VCCQ | VCCQ | DQ16 | DQ17 | DQ31 | VSS | A |
| B | DQ1 | DQ2 | DQ12 | DQ13 | VSS | VSS | A0 | A7 | A6 | A1 | VCC | VCC | DQ18 | DQ19 | DQ29 | DQ30 | B |
| C | DQ3 | DQ4 | DQ10 | DQ11 | VCC | VCC | A2 | A5 | A4 | A3 | VSS | VSS | DQ20 | DQ21 | DQ27 | DQ28 | C |
| D | DQ6 | DQ5 | DQ8 | DQ9 | VCCQ | VCCQ | A12 | RFU | BA2 | RFU | VSS | VSS | DQ22 | DQ23 | DQ26 | DQ25 | D |
| E | DQ7 | LDM0 | VCC | UDM0 | UDQS3 | LDQS0 | UDQS0 | BA0 | BA1 | LDQS1 | UDQS1 | VrefDA | LDM1 | VSS | NC | DQ24 | E |
| F | CAS0\ | WE0\ | VCC | CLK0 | LDQS3 | UDQS3\ | LDQS0\ | UDQS0\ | DNU | UDQS1\ | LDQS1\ | RAS1\ | WE1\ | VSS | UDM1 | CLK1 | F |
| G | CS0\ | RAS0\ | VCC | CKE0 | CLK0\ | LDQS3\ | VSSQ | VSSQ | VSSQ | VSSQ | RESET\ | CAS1\ | CS1\ | VSS | CLK1\ | CKE1 | G |
| H | VSS | VSS | VCC | VCCQ | VSS | ZQ0 | VSSQ | VSSQ | VSSQ | VSSQ | ZQ1 | VCC | VSS | VSS | VCCQ | VCC | H |
| J | VSS | VSS | VCC | VCCQ | VSS | VrefCA | VSSQ | VSSQ | VSSQ | VSSQ | ZQ2 | VCC | VSS | VSS | VCCQ | VCC | J |
| K | CLK3\ | CKE3 | VCC | CS3\ | LDQS4 | UDQS4\ | VSSQ | VSSQ | VSSQ | VSSQ | DNU | CLK2\ | CKE2 | VSS | RAS2\ | CS2\ | K |
| L | NC | CLK3 | VCC | CAS3\ | RAS3\ | ODT | LDQS4\ | ZQ3 | NC/ZQ4 | LDQS2\ | UDQS2\ | LDQS2 | CLK2 | VSS | WE2\ | CAS2\ | L |
| M | DQ56 | UDM3 | VCC | WE3\ | LDM3 | CKE4 | NC | CLK4 | CAS4\ | WE4\ | RAS4\ | CS4\ | UDM2 | VSS | LDM2 | DQ39 | M |
| N | DQ57 | DQ58 | DQ55 | DQ54 | UDQS4 | CLK4\ | NC | NC | DQ71 | DQ70 | LDM4 | UDQS2 | DQ41 | DQ40 | DQ37 | DQ38 | N |
| P | DQ60 | DQ59 | DQ53 | DQ52 | VSS | VSS | NC | NC | DQ69 | DQ68 | VCC | VCC | DQ43 | DQ42 | DQ36 | DQ35 | P |
| R | DQ62 | DQ61 | DQ51 | DQ50 | VCC | VCC | NC | NC | DQ67 | DQ66 | VSS | VSS | DQ45 | DQ44 | DQ34 | DQ33 | R |
| T | VSS | DQ63 | DQ49 | DQ48 | VCCQ | VCCQ | NC | NC | DQ65 | DQ64 | VSS | VSS | DQ47 | DQ46 | DQ32 | VCC | T |
| | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | 13 | 14 | 15 | 16 | |

GND (Core) | V+ (Core Power) | UNPOPULATED | Address

GND (I/O) | V+ (I/O Power) | NC | DNU

Data IO | CNTRL | Level REF

L9D345G72BG5

**ADVANCE INFORMATION**

## Table 3 - Ball/Signal Location and Description

| Ball Assignments | Symbol | Type | Description |
|---|---|---|---|
| B7, B10, C7, C10, C9, C8, B9, B8, A10, A7, A8, A9, D7 | **$A_0$, $A_1$, $A_2$, $A_3$, $A_4$, $A_5$, $A_6$, $A_7$, $A_8$, $A_9$, $A_{10}$/AP, $A_{11}$, $A_{12}$/BC** | **Input** | **Address Inputs:** Provide the ROW address for ACTIVATE commands, and the column address and auto precharge bit (A10) for READY/WRITE commands, to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one bank (A10 LOW), bank selected by BA[2:0] or all banks (A10 HIGH). The address inputs also provide the op-code during a LOAD MODE command. Address inputs are referenced to VrefCA. A12/BC#: when enabled in the mode register (MR), A12 is sampled during READ and WRITE commands to determine whether burst chop, LOW = BC4 burst chop). |
| E8, E9, D9 | **$BA_0$, $BA_1$, $BA_2$** | **Input** | **Bank Address Inputs:** BA[2:0] define the bank to which an ACTIVATE, READ, WRITE, or PRECHARGE command is being applied. BA[2:0] define which mode register (MR0, MR1, MRE, or MR3) is loaded during the LOAD MODE command. BA[2:0] are referenced to VrefCA. |
| D10, D8 | **RFU** | **Input** | Future Address: A13, A14 |
| F4, G5, F16, G15, L13, K12, L2, K1, M8, N6 | **$CLK_0$, $CLK_0$\, $CLK_1$, $CLK_1$\, $CLK_2$, $CLK_2$\, $CLK_3$, $CLK_3$\, $CLK_4$, $CLK_4$** | **Input** | **Clock:** CKx and CKx\ are differential clock inputs, one differential pair per WORD, five WORDs contained in the L9D3xxG72 product. All control and address input signals are sampled on the crossing of the positive edge of CKx and the negative edge of CKx\. Output data strobes (UDQSx/UDQSx\ and LDQSx/LDQSx\) is referenced to the crossing of CKx and CKx\. |
| G4, G16, K13, K2, M6 | **$CKE_0$, $CKE_1$, $CKE_2$, $CKE_3$, $CKE_4$** | **Input** | **Clock Enable:** CKE enables and disables internal circuitry and clocks on the SDRAM. The specific circuitry that is enabled/disabled is dependent upon the DDR3 SDRAM configuration and operating mode. Taking CKE LOW provides PRECHARGE power-down and SELF REFRESH operations (all banks idle), or active power-down (row active in any bank). CKE is synchronous for power-down entry and exit and for self refresh entry. CKE is asynchronous for self refresh exit. Input buffers (excluding CKx, CKx\, CKE, RESET#, and ODT) are disabled during SELF REFRESH. CKE is referenced to VrefCA. |
| G1, G13, K16, K4, M12 | **$CS_0$\, $CS_1$\, $CS_2$\, $CS_3$\, $CS_4$** | **Input** | **Chip Select:** CS\ enables (registered LOW) and disables the command decoder. All commands are masked when CS\ is registered HIGH. CS\ provides for external rank selection on systems with multiple ranks. CS\ is considered part of the command code. CS\ is referenced to VrefCA. |
| E2, E4, E13, F15, M15, M13, M5, M2, N11 | **LDMx, UDMx, LDMx, UDMx, LDMx, UDMx, LDMx, UDMx LDMx** | **Input** | **Input Data Mask:** LDMx is the Lower-byte of a WORD, UDMx is the Upperbyte of a WORD, the L9D3xxG72 contains five WORDS. The data mask input, masks WRITE data. Lower byte data masked when LDMx is sampled HIGH, upper byte data masked when UDMx is sampled HIGH. The UDMx and LDMx pins are structured as inputs only, the pins electrical loading is designed to match that of the DQ and LDQSx, LDQSx\, UDQSx, and UDQSx\ pins. |
| G2, F12, K15, L5, M11 | **RAS0\, RAS1\, RAS2\, RAS3\, RAS4** | **Input** | **ROW Address Strobe/Select:** Defines the command being entered along CAS\, WE\, and CS\. This input pin is referenced to VrefCA. |
| F1, G12, L16, L4, M9 | **CAS0\, CAS1\, CAS2\, CAS3\, CAS4** | **Input** | **COLUMN Address Strobe/Select:** Defines the command being entered along with RAS\, WE\, and CS\. This input pin is referenced to VrefCA. |
| F2, F13, L15, M4, M10 | **$WE_0$\, $WE_1$\, $WE_2$\, $WE_3$\, $WE_4$** | **Input** | **WRITE Enable Input:** Defines the command being entered along with CAS\, RAS\,, and CS\. This input pin is referenced to VrefCA. |

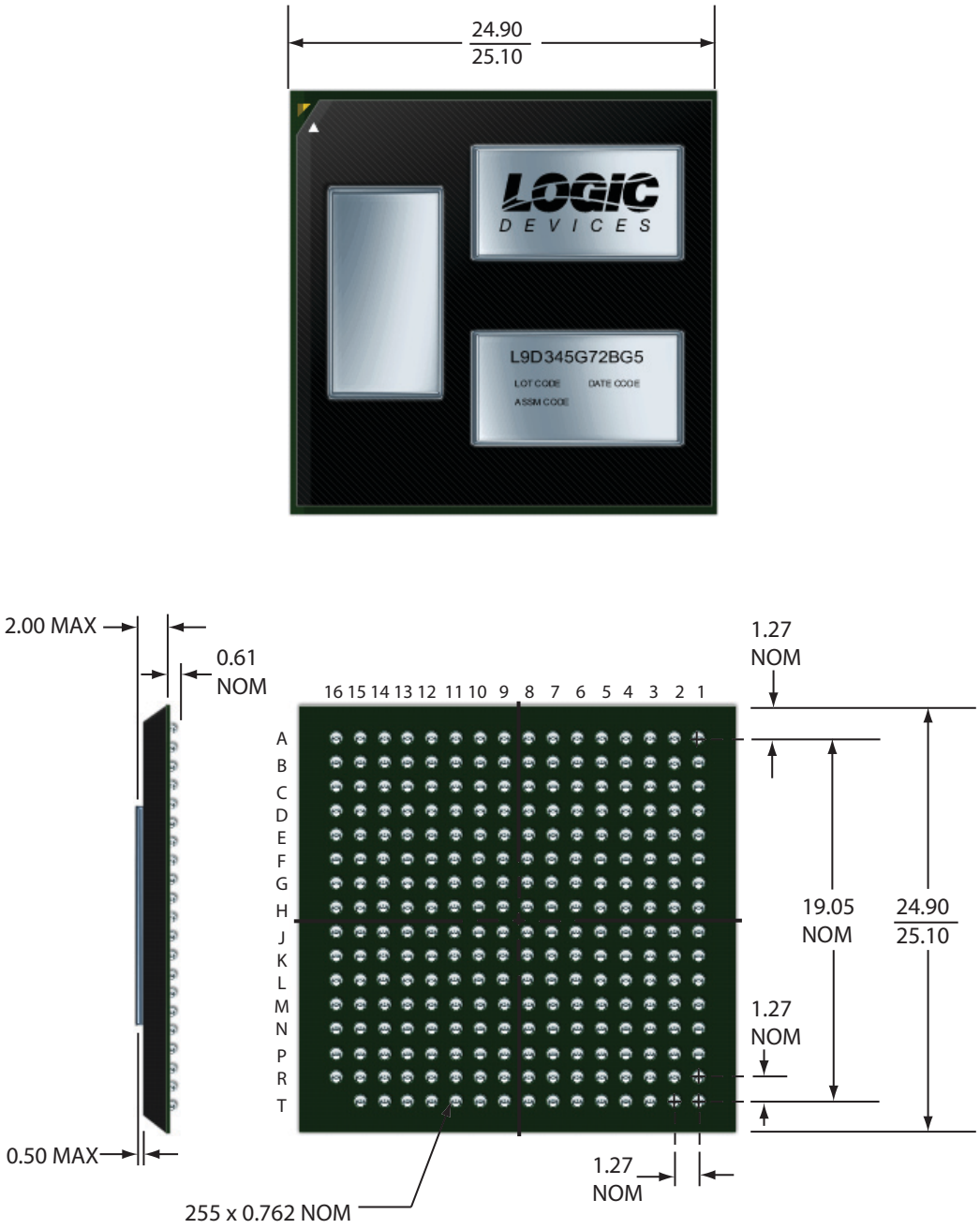
**TABLE 3 - BALL/SIGNAL LOCATION AND DESCRIPTION CONTINUED**

| Ball Assignments | Symbol | Type | Description |
|---|---|---|---|
| L6 | **ODT** | **Input** | **On-Die Termination:** ODT enables (when registered HIGH) and disables termination resistance internal to the DDR3 SDRAM. When enabled in normal operation, ODT is only applied to each of the following signals: DQ[63:0], LDQSx, LDQSx\, UDQSx, UDQSx\, UDMx and LDMx. The ODT input is ignored if disabled via the LOAD MODE register command. ODT is referenced to VrefCA. |
| G11 | **RESET** | **Input** | **RESET:** An input control pin, active LOW referenced to Vss. The RESET\ input receiver is a CMOS input defined as a rail to rail signal with DC HIGH ≥ 0.8 x Vcc and DC LOW ≤ 0.2 x VccQ. RESET\ assertion and de-assertion are asynchronous. |
| E6, E10, L12, F5, K5, F7, F11, L10, G6, L7 | **LDQSx, LDQSx** | **Input** | **Data Strobe, LOW Byte (per WORD):** Output, edge-aligned with READ data. Input, center-aligned with WRITE data. |
| E7, E11, N12, E5, N5, F8, F10, L11, F6, K6 | **UDQSx, UDQSx** | **Input** | **Data Strobe, HIGH Byte (per WORD):** Output, edge-aligned with READ data. Input, center-aligned with WRITE data. |
| A2, B1, B2, C1, C2, D2, D1, E1 | **$DQ_0$, $DQ_1$, $DQ_2$, $DQ_3$, $DQ_4$, $DQ_5$, $DQ_6$, $DQ_7$** | **I/O** | **Data Input/Output:** LOW Byte, LOW WORD (WORD 1). Pin referenced to VrefDQ. |
| D3, D4, C3, C4, B3, B4, A3, A4 | **$DQ_8$, $DQ_9$, $DQ_{10}$, $DQ_{11}$, $DQ_{12}$, $DQ_{13}$, $DQ_{14}$, $DQ_{15}$** | **I/O** | **Data Input/Output:** HIGH Byte, LOW WORD (WORD 1). Pin referenced to VrefDQ. |
| A13, A14, B13, B14, C13, C14, D13, D14 | **$DQ_{16}$, $DQ_{17}$, $DQ_{18}$, $DQ_{19}$, $DQ_{20}$, $DQ_{21}$, $DQ_{22}$, $DQ_{23}$** | **I/O** | **Data Input/Output:** LOW Byte, WORD 2. Pin referenced to VrefDQ. |
| E16, D16, D15, C15, C16, B15, B16, A15 | **$DQ_{24}$, $DQ_{25}$, $DQ_{26}$, $DQ_{27}$, $DQ_{28}$, $DQ_{29}$, $DQ_{30}$, $DQ_{31}$** | **I/O** | **Data Input/Output:** HIGH Byte, WORD 2. Pin referenced to VrefDQ. |
| T15, R16, R15, P16, P15, N15, N16, M16 | **$DQ_{32}$, $DQ_{33}$, $DQ_{34}$, $DQ_{35}$, $DQ_{36}$, $DQ_{37}$, $DQ_{38}$, $DQ_{39}$** | **I/O** | **Data Input/Output:** LOW Byte, WORD 3. Pin referenced to VrefDQ. |
| N14, N13, P14, P13, R14, R13, T14, T13 | **$DQ_{40}$, $DQ_{41}$, $DQ_{42}$, $DQ_{43}$, $DQ_{44}$, $DQ_{45}$, $DQ_{46}$, $DQ_{47}$** | **I/O** | **Data Input/Output:** HIGH Byte, WORD 3. Pin referenced to VrefDQ. |
| T4, T3, R4, R3, P4, P3, N4, N3 | **$DQ_{48}$, $DQ_{49}$, $DQ_{50}$, $DQ_{51}$, $DQ_{52}$, $DQ_{53}$, $DQ_{54}$, $DQ_{55}$** | **I/O** | **Data Input/Output:** LOW Byte, HIGH WORD (WORD 4). Pin referenced to VrefDQ. |

**TABLE 3 - BALL/SIGNAL LOCATION AND DESCRIPTION CONTINUED**

| Ball Assignments | Symbol | Type | Description |
|---|---|---|---|
| M1, N1, N2, P2, P1, R2, R1, T2 | **$DQ_{56}$, $DQ_{57}$, $DQ_{58}$, $DQ_{59}$, $DQ_{60}$, $DQ_{61}$, $DQ_{62}$, $DQ_{63}$** | **I/O** | **Data Input/Output:** HIGH Byte, HIGH WORD (WORD 4). Pin referenced to VrefDQ. |
| T10, T9, R10, R9, P10, P9, N10, N9 | **$DQ_{64}$, $DQ_{65}$, $DQ_{66}$, $DQ_{67}$, $DQ_{68}$, $DQ_{69}$, $DQ_{70}$, $DQ_{71}$** | **I/O** | **Data Input/Output:** HIGH Byte, HIGH WORD (WORD 5). Pin referenced to VrefDQ. |
| B11, B12, C5, C6, E3, F3, G3, H3, H12, H16, J3, J12, J16, K3, L3, M3, P11, P12, R5, R6, T16 | **$V_{CC}$** | **Supply** | Power Supply: 1.5V ± 0.075V |
| A11, A12, D5, D6, H4, H15, J4, J15, T5, T6 | **$V_{CC}Q$** | **Supply** | Data I/O Supply: 1.5V ± 0.075V |
| A5, A6, A16, B5, B6, C11, C12, D11, D12, E14, F14, G14, H1, H2, H5, H13, H14, J1, J2, J5, J13, J14, K14, L14, M14, P5, P6, R11, R12, T1, T11, T12 | **$V_{SS}$** | **Supply** | Ground |
| G7, G8, G9, G10, H7, H8, H9, H10, J7, J8, J9, J10, K7, K8, K9, K10 | **$V_{SS}Q$** | **Supply** | Data I/O Ground: Isolated from Core for improved noise immunity |
| J6 | **$V_{REFCA}$** | **Supply** | Voltage Reference CORE: VrefCA must be maintained at all times |
| E12 | **$V_{REFDQ}$** | **Supply** | Voltage Reference I/O: VrefDQ must be maintained at all times. |
| H6, H11, J11, L8, L9 | **ZQx** | **REF** | External Reference for output drive calibration |
| A1 | **UNPOPULATED** | | Unpopulated, un-plated matrix location(s) |
| E15, L1 | **NC** | **-** | No Connect: These ball locations have no electrical connection internally. Locations other than those indicating an upgrade or alternative function should be left isolated (non-connected) |

## FIGURE 5 - MECHANICAL DRAWING




Note: All dimensions in mm

## Table 5: Absolute Maximum Ratings

| Symbol | Parameter | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| $V_{CC}$ | $V_{CC}$ Supply Voltage relative to $V_{SS}$ | -0.4 | 1.975 | V | 1 |
| $V_{CC}Q$ | $V_{CC}$ Supply Voltage relative to $V_{SS}Q$ | -0.4 | 1.975 | V | 1 |
| $V_{IN}$, $V_{OUT}$ | Voltage on any pin relative to $V_{SS}$ | -0.4 | 1.975 | V | 1 |
| $T_C$Industrial | Operating Case Temperature | 0 | 85 | °C | 2,3 |
| $T_C$Extended | Operating Case Temperature | -40 | 105 | °C | 2,3 |
| $T_C$Miltemp | Operating Case Temperature | -55 | 125 | °C | 2,3 |
| $T_{STG}$ | Storage Temperature | -55 | 120 | °C | 2,3 |

NOTES:

1. $V_{CC}$ and $V_{CC}Q$ must be within 300mV of each other at all times and $V_{REF}$ must not be greater than 0.6 x $V_{CC}Q$. When $V_{CC}$ and $V_{CC}Q$ are less than 500MV, $V_{REF}$ may be ≤300mV.
2. Max operating case temperature. $T_C$ is measured in the center of the package.
3. Device Functionality is not guaranteed if the DRAM device exceeds the Maximum $T_C$ during operation.

## Table 6: Input/Output Capacitance

| | | DDR3-800 | | DDR3-1066 | | DDR3-1333 | | | |
|---|---|---|---|---|---|---|---|---|---|
| Capacitance Parameter | Symbol | MIN | MAX | MIN | MAX | MIN | MAX | UNITS | NOTES |
| CK and CK\ | $C_{CK}$ | 3.1 | 6.2 | 3.1 | 6.2 | 3.0 | 6.1 | pF | |
| ΔC: CK to CK\ | $C_{DCK}$ | 0 | 0.2 | 0 | 0.2 | 0 | 0.2 | pF | |
| Single-end I/O: DQ, DM | $C_{IO}$ | 1.5 | 3.0 | 1.5 | 3.0 | 1.5 | 2.5 | pF | 2 |
| Differential I/O: DQS, DQS\ | $C_{IO}$ | 1.5 | 3.0 | 1.5 | 3.0 | 1.5 | 2.5 | pF | 3 |
| ΔC: DQS to DQS\ | $C_{CCQS}$ | 0 | 0.2 | 0 | 0.2 | 0 | 0.2 | pF | 3 |
| ΔC: DQ to DQS | $C_{DIO}$ | -0.5 | 0.3 | -0.5 | 0.3 | -0.5 | 0.3 | pF | 4 |
| ΔC: CNTL to CK | $C_{DI\_CNTL}$ | -0.5 | 0.3 | -0.5 | 0.3 | -0.5 | 0.3 | pF | 6 |
| ΔC: cmd_ADDR to CK | $C_{DI\_CMD\_ADDR}$ | -0.5 | 0.3 | -0.5 | 0.3 | -0.5 | 0.3 | pF | 7 |
| Inputs (RAS\, CAS\, WE\, CS\, CKE, ADDR) | $C_{I\_Shared}$ | 2.9 | 5.5 | 2.9 | 5.3 | 2.9 | 5.1 | pF | 5 |

NOTES:

1. $V_{CC}$ = +1.5V± 0.075mV, $V_{CCQ}$ = $V_{CC}$, $V_{REF}$ = $V_{SS}$, f= 100MHz, $T_C$ = 25°C, $V_{OUT}$ (DC) = 0.5 x $V_{CCQ}$, $V_{OUT}$ (peak to peak) = 0.1V
2. DM input is grouped with I/O pins, reflecting the signal is grouped with DQ and therefore matched in loading.
3. $C_{CCQS}$ is for DQS vs. DQS\
4. $C_{DIO}$ = CIO (DQ) - 0.5 x (CIO [DQS] + CIO [DQS\])
5. Excludes CK, CK\
6. $C_{DI\_CNTL}$ = CI(CNTL) - 0.5 x (CCK[CK] + CCK [CK\]); CNTL = ODT, CS\ and CKE
7. $C_{DI\_CMD\_ADDR}$ = CI (CMD_ADDR) - 0.5 x (CCK [CK] + CCK [CK\]); CMD = RAS\, CAS\, and WE\ ADDR = [n:0]

**TABLE 8: TIMING PARAMETERS FOR ICC MEASUREMENTS - CLOCK UNITS**

| | | DDR3-800 -25 | DDR3-1066 -19 | DDR3-1333 -15 | |
|---|---|---|---|---|---|
| **ICC Parameter** | | **6-6-6** | **8-8-8** | **10-10-10** | **UNITS** |
| tCK (MIN) ICC | | 2.5 | 1.875 | 1.5 | ns |
| CL ICC | | 6 | 8 | 10 | CK |
| tRCD (MIN) ICC | | 6 | 8 | 10 | CK |
| tRC (MIN) ICC | | 21 | 28 | 34 | CK |
| tRAS (MIN) ICC | | 15 | 20 | 24 | CK |
| tRP (MIN) ICC | | 6 | 8 | 10 | CK |
| tFAW | x72 | 20 | 27 | 30 | CK |
| tRRD ICC | x72 | 4 | 6 | 5 | CK |
| tRFC | 64M x 16 (4.5X) | 44 | 59 | 74 | CK |

## TABLE 9: $I_{CC0}$ MEASUREMENT LOOP

| Cycle Number | Command | CS\ | RAS\ | CAS\ | WE\ | ODT | BA [2:0] | A [15:11] | A [10] | A [9:7] | A [6:3] | A [2:0] | Data | Sub-Loop | CKE | CK, CK\ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | ACT | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | 0 | Static HIGH | Toggling |
| 1 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | | |
| 2 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | | |
| 3 | D\ | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | | |
| 4 | D\ | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | | |
| - | | | | Repeat cycles 1 through 4 until *n*RAS - 1, truncate if needed | | | | | | | | | - | | | |
| *n*RAS | PRE | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | | |
| - | | | | Repeat cycles 1 through 4 until *n*RC - 1, truncate if needed | | | | | | | | | - | | | |
| *n*RC | ACT | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F | 0 | - | | | |
| *n*RC + 1 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | F | 0 | - | | | |
| *n*RC + 2 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | F | 0 | - | | | |
| *n*RC + 3 | D\ | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F | 0 | - | | | |
| *n*RC + 4 | D\ | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F | 0 | - | | | |
| - | | | | Repeat cycles *n*RC +1 through *n*RC +4 until *n*RC - 1 + *n*RAS - 1, truncate if needed | | | | | | | | | - | | | |
| *n*RC + *n*RAS | PRE | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | F | 0 | - | | | |
| - | | | | Repeat cycles *n*RC +1 through *n*RC +4 until 2 x *n*RC - 1, truncate if needed | | | | | | | | | - | 0 | | |
| 2 x *n*RC | | | | | | | | | | | | | | 1 | | |
| 4 x *n*RC | | | | | | | | | | | | | | 2 | | |
| 6 x *n*RC | | | | | | | | | | | | | | 3 | | |
| 8 x *n*RC | | | | | | | | | | | | | | 4 | | |
| 10 x *n*RC | | | | | | | | | | | | | | 5 | | |
| 12 x *n*RC | | | | | | | | | | | | | | 6 | | |
| 14 x *n*RC | | | | | | | | | | | | | | 7 | | |

| Repeat sub-loop 0, use BA [2:0] = 1 |
|---|
| Repeat sub-loop 0, use BA [2:0] = 2 |
| Repeat sub-loop 0, use BA [2:0] = 3 |
| Repeat sub-loop 0, use BA [2:0] = 4 |
| Repeat sub-loop 0, use BA [2:0] = 5 |
| Repeat sub-loop 0, use BA [2:0] = 6 |
| Repeat sub-loop 0, use BA [2:0] = 7 |

## TABLE 10: $I_{CC1}$ MEASUREMENT LOOP

| Cycle Number | Command | CS\ | RAS\ | CAS\ | WE\ | ODT | BA [2:0] | A [15:11] | A [10] | A [9:7] | A [6:3] | A [2:0] | Data | Sub-Loop | CKE | CK, CK\ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | ACT | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | 0 | Static HIGH | Toggling |
| 1 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | | |
| 2 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | | |
| 3 | D\ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | | |
| 4 | D\ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | | |
| - | - | Repeat cycles 1 through 4 until nRCD - 1, truncate if needed | | | | | | | | | | | | | | |
| nRCD | RD | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00000000 | | | |
| - | - | Repeat cycles 1 through 4 until nRAS - 1, truncate if needed | | | | | | | | | | | | | | |
| nRAS | PRE | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | | |
| - | - | Repeat cycles 1 through 4 until nRC - 1, truncate if needed | | | | | | | | | | | | | | |
| nRC | ACT | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F | 0 | - | | | |
| nRC +1 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | F | 0 | - | | | |
| nRC +2 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | F | 0 | - | | | |
| nRC +3 | D\ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F | 0 | - | | | |
| nRC +4 | D\ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F | 0 | - | | | |
| - | - | Repeat cycles nRC + 1 through nRC + 4 until nRCD - 1, truncate if needed | | | | | | | | | | | | | | |
| nRC + nRCD | RD | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | F | 0 | 00110011 | | | |
| - | - | Repeat cycles nRC + 1 through nRC + 4 until nRC + nRAS - 1, truncate if needed | | | | | | | | | | | | | | |
| nRC + nRAS | PRE | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | F | 0 | - | | | |
| - | - | Repeat cycle nRC + 1 through nRC + 4 until 2 x nRC - 1, truncate if needed | | | | | | | | | | | | | | |
| 2 x nRC | - | Repeat sub-loop 0, use BA [2:0] = 1 | | | | | | | | | | | | 1 | | |
| 2 x nRC | - | Repeat sub-loop 0, use BA [2:0] = 2 | | | | | | | | | | | | 2 | | |
| 2 x nRC | - | Repeat sub-loop 0, use BA [2:0] = 3 | | | | | | | | | | | | 3 | | |
| 2 x nRC | - | Repeat sub-loop 0, use BA [2:0] = 4 | | | | | | | | | | | | 4 | | |
| 2 x nRC | - | Repeat sub-loop 0, use BA [2:0] = 5 | | | | | | | | | | | | 5 | | |
| 2 x nRC | - | Repeat sub-loop 0, use BA [2:0] = 6 | | | | | | | | | | | | 6 | | |
| 2 x nRC | - | Repeat sub-loop 0, use BA [2:0] = 7 | | | | | | | | | | | | 7 | | |

**TABLE 11: IDD MEASUREMENT CONDITIONS FOR POWER-DOWN CURRENTS**

| Name | Idd2P0 Precharge Power-Down Current (Slow Exit) | Idd2P1 Precharge Power-Down Current (Fast Exit) | Idd2Q Precharge Quiet Standby Current | Idd3P Active Power-Down Current |
|---|---|---|---|---|
| Timing Pattern | n/a | n/a | n/a | n/a |
| CKE | LOW | LOW | HIGH | LOW |
| External Clock | Toggling | Toggling | Toggling | Toggling |
| $^{t}$CK | $^{t}$CK (MIN) IDD | $^{t}$CK (MIN) IDD | $^{t}$CK (MIN) IDD | $^{t}$CK (MIN) IDD |
| $^{t}$RC | n\a | n\a | n\a | n\a |
| $^{t}$RAS | n\a | n\a | n\a | n\a |
| $^{t}$RCD | n\a | n\a | n\a | n\a |
| $^{t}$RRD | n\a | n\a | n\a | n\a |
| $^{t}$RC | n\a | n\a | n\a | n\a |
| CL | n\a | n\a | n\a | n\a |
| AL | n\a | n\a | n\a | n\a |
| CS\ | HIGH | HIGH | HIGH | HIGH |
| Command Inputs | LOW | LOW | LOW | LOW |
| ROW/COLUMN Addr | LOW | LOW | LOW | LOW |
| Bank Address | LOW | LOW | LOW | LOW |
| DM | LOW | LOW | LOW | LOW |
| Data I/O | Mid-level | Mid-level | Mid-level | Mid-level |
| Output Buffer DQ, DQS | Enabled | Enabled | Enabled | Enabled |
| ODT | Enabled, OFF | Enabled, OFF | Enabled, OFF | Enabled, OFF |
| Burst Length | 8 | 8 | 8 | 8 |
| ACTIVE Bank(s) | None | None | None | None |
| IDLE Bank(s) | All | All | All | All |
| Special Notes | n\a | n\a | n\a | n\a |

## TABLE 12: $I_{CC}2N$ / $I_{CC}3N$ MEASUREMENT LOOP

| CK, CK\ | CKE | Sub-Loop | Cycle Number | Command | CS\ | RAS\ | CAS\ | WE\ | ODT | BA [2:0] | A [15:11] | A [10] | A [9:7] | A [6:3] | A [2:0] | Data |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Toggling | Static HIGH | 0 | 0 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - |
| | | | 1 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - |
| | | | 2 | D\ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F | 0 | - |
| | | | 3 | D\ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F | 0 | - |
| | | 1 | 4-7 | | | | | | | | | | | | | |
| | | 2 | 8-11 | | | | | | | | | | | | | |
| | | 3 | 12-15 | | | | | | | | | | | | | |
| | | 4 | 16-19 | | | | | | | | | | | | | |
| | | 5 | 20-23 | | | | | | | | | | | | | |
| | | 6 | 24-27 | | | | | | | | | | | | | |
| | | 7 | 28-31 | | | | | | | | | | | | | |

Repeat sub-loop 0, use BA [2:0] = 1
Repeat sub-loop 0, use BA [2:0] = 2
Repeat sub-loop 0, use BA [2:0] = 3
Repeat sub-loop 0, use BA [2:0] = 4
Repeat sub-loop 0, use BA [2:0] = 5
Repeat sub-loop 0, use BA [2:0] = 6
Repeat sub-loop 0, use BA [2:0] = 7

## TABLE 13: IDD2NT MEASUREMENT LOOP

| Cycle Number | Command | CS\ | RAS\ | CAS\ | WE\ | ODT | BA [2:0] | A [15:11] | A [10] | A [9:7] | A [6:3] | A [2:0] | Data | Sub-Loop |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | D | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | 0 |
| 1 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | |
| 2 | D\ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F | 0 | - | |
| 3 | D\ | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | F | 0 | - | |
| 4-7 | Repeat sub-loop 0, use BA [2:0] = 1; ODT = 0 | | | | | | | | | | | | | 1 |
| 8-11 | Repeat sub-loop 0, use BA [2:0] = 2; ODT = 1 | | | | | | | | | | | | | 2 |
| 12-15 | Repeat sub-loop 0, use BA [2:0] = 3; ODT = 1 | | | | | | | | | | | | | 3 |
| 16-19 | Repeat sub-loop 0, use BA [2:0] = 4; ODT = 0 | | | | | | | | | | | | | 4 |
| 20-23 | Repeat sub-loop 0, use BA [2:0] = 5; ODT = 0 | | | | | | | | | | | | | 5 |
| 24-27 | Repeat sub-loop 0, use BA [2:0] = 6; ODT = 1 | | | | | | | | | | | | | 6 |
| 28-31 | Repeat sub-loop 0, use BA [2:0] = 7; ODT = 1 | | | | | | | | | | | | | 7 |
| Static HIGH | | | | | | | | | | | | | | CKE |
| Toggling | | | | | | | | | | | | | | CK, CK\ |

## TABLE 14: IDD4R MEASUREMENT LOOP

| Cycle Number | Command | CS\ | RAS\ | CAS\ | WE\ | ODT | BA [2:0] | A [15:11] | A [10] | A [9:7] | A [6:3] | A [2:0] | Data | Sub-Loop | CKE | CK, CK\ |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | RD | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00000000 | 0 | Static HIGH | Toggling |
| 1 | D | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | | |
| 2 | D\ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | | |
| 3 | D\ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 00110011 | | | |
| 4 | RD | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | F | 0 | - | | | |
| 5 | D | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | F | 0 | - | | | |
| 6 | D\ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | | |
| 7 | D\ | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | | |
| 8-15 | Repeat sub-loop 0, use BA [2:0] = 1 | | | | | | | | | | | | | | | |
| 16-23 | Repeat sub-loop 0, use BA [2:0] = 2 | | | | | | | | | | | | | | | |
| 24-31 | Repeat sub-loop 0, use BA [2:0] = 3 | | | | | | | | | | | | | | | |
| 32-39 | Repeat sub-loop 0, use BA [2:0] = 4 | | | | | | | | | | | | | | | |
| 40-47 | Repeat sub-loop 0, use BA [2:0] = 5 | | | | | | | | | | | | | | | |
| 48-55 | Repeat sub-loop 0, use BA [2:0] = 6 | | | | | | | | | | | | | | | |
| 56-63 | Repeat sub-loop 0, use BA [2:0] = 7 | | | | | | | | | | | | | | | |

## TABLE 15: IDD4W MEASUREMENT LOOP

| Cycle Number | Sub-Loop | CKE | CK, CK\ | Command | CS\ | RAS\ | CAS\ | WE\ | ODT | BA [2:0] | A [15:11] | A [10] | A [9:7] | A [6:3] | A [2:0] | Data |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | Static HIGH | Toggling | WR | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 00000000 |
| 1 | 0 | | | D | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | - |
| 2 | 0 | | | D\ | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | - |
| 3 | 0 | | | D\ | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | F | 0 | 00110011 |
| 4 | 0 | | | WR | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | F | 0 | - |
| 5 | 0 | | | D | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | F | 0 | - |
| 6 | 0 | | | D\ | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | F | 0 | - |
| 7 | 0 | | | D\ | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | F | 0 | - |
| 8-15 | 1 | | | Repeat sub-loop 0, use BA [2:0] = 1 | | | | | | | | | | | | |
| 16-23 | 2 | | | Repeat sub-loop 0, use BA [2:0] = 2 | | | | | | | | | | | | |
| 24-31 | 3 | | | Repeat sub-loop 0, use BA [2:0] = 3 | | | | | | | | | | | | |
| 32-39 | 4 | | | Repeat sub-loop 0, use BA [2:0] = 4 | | | | | | | | | | | | |
| 40-47 | 5 | | | Repeat sub-loop 0, use BA [2:0] = 5 | | | | | | | | | | | | |
| 48-55 | 6 | | | Repeat sub-loop 0, use BA [2:0] = 6 | | | | | | | | | | | | |
| 56-63 | 7 | | | Repeat sub-loop 0, use BA [2:0] = 7 | | | | | | | | | | | | |

## TABLE 16: IDD5B MEASUREMENT LOOP

| Sub-Loop | Cycle Number | Command | CS\ | RAS\ | CAS\ | WE\ | ODT | BA [2:0] | A [15:11] | A [10] | A [9:7] | A [6:3] | A [2:0] | Data |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CK, CK\ | | Toggling | | | | | | | | | | | | |
| CKE | | Static HIGH | | | | | | | | | | | | |
| 0 | 0 | REF | | | | | | | | | | | | |
| 1a | 1 | D | | | | | | | | | | | | |
| | 2 | D | | | | | | | | | | | | |
| | 3 | D\ | | | | | | | | | | | | |
| | 4 | D\ | | | | | | | | | | | | |
| 1b | 5-8 | Repeat sub-loop 1a, use BA [2:0] = 1 | | | | | | | | | | | | |
| 1c | 9-12 | Repeat sub-loop 1a, use BA [2:0] = 2 | | | | | | | | | | | | |
| 1d | 13-16 | Repeat sub-loop 1a, use BA [2:0] = 3 | | | | | | | | | | | | |
| 1e | 17-20 | Repeat sub-loop 1a, use BA [2:0] = 4 | | | | | | | | | | | | |
| 1f | 21-24 | Repeat sub-loop 1a, use BA [2:0] = 5 | | | | | | | | | | | | |
| 1g | 25-28 | Repeat sub-loop 1a, use BA [2:0] = 6 | | | | | | | | | | | | |
| 1h | 29-32 | Repeat sub-loop 1a, use BA [2:0] = 7 | | | | | | | | | | | | |
| 2 | 33-nRFC-1 | Repeat sub-loop 1a through 1h until nRFC - 1, truncate if needed | | | | | | | | | | | | |

**TABLE 17: IDD MEASUREMENT LOOP**

| | Industrial Range Tc =-40°C to 85°C | Extended or Mil Temperature Range, Tc = -40°C to 85°C or -55°C to 125°C | |
|---|---|---|---|
| **IDD Test** | **IDD6: Self Refresh Current** | **IDD6E/M: Self Refresh Current** | **IDD8: Reset** |
| CKE | LOW | LOW | Mid-level |
| External Clock | Off, CK and CK\ = LOW | Off, CK and CK\ = LOW | Mid-level |
| $^{t}$CK | n\a | n\a | n\a |
| $^{t}$RC | n\a | n\a | n\a |
| $^{t}$RAS | n\a | n\a | n\a |
| $^{t}$RCD | n\a | n\a | n\a |
| $^{t}$RRD | n\a | n\a | n\a |
| $^{t}$RC | n\a | n\a | n\a |
| CL | n\a | n\a | n\a |
| AL | n\a | n\a | n\a |
| CS\ | Mid-level | Mid-level | Mid-level |
| Command Inputs | Mid-level | Mid-level | Mid-level |
| ROW/COLMUN addresses | Mid-level | Mid-level | Mid-level |
| BANK addresses | Mid-level | Mid-level | Mid-level |
| Data I/O | Mid-level | Mid-level | Mid-level |
| Output buffer DQ, DQS | Enabled | Enabled | Mid-level |
| ODT | Enabled, Mid-level | Enabled, Mid-level | Mid-level |
| Burst Length | n\a | n\a | n\a |
| Active BANKS | n\a | n\a | None |
| IDLE BANKS | n\a | n\a | All |
| SRT | Disabled (normal) | Enabled (extended) | n\a |
| ASR | Disabled | Disabled | n\a |

## TABLE 18: $I_{CC}7$ MEASUREMENT LOOP

| Sub-Loop | Cycle Number | Command | CS\ | RAS\ | CAS\ | WE\ | ODT | BA [2:0] | A [15:11] | A [10] | A [9:7] | A [6:3] | A [2:0] | Data | CK, CK\ | CKE |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 0 | 0 | ACT | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | Toggling | Static HIGH |
| | 1 | RDA | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 00000000 | | |
| | 2 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | - | | |
| 1 | 3 | Repeat cycle 2 until *n*RRD - 1 | | | | | | | | | | | | | | |
| | *n*RRD | ACT | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | F | 0 | - | | |
| | *n*RRD + 1 | RDA | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | F | 0 | 00110011 | | |
| | *n*RRD + 2 | D | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | F | 0 | - | | |
| 2 | *n*RRD + 3 | Repeat cycle *n*RRD + 2 until 2 x *n*RRD - 1 | | | | | | | | | | | | | | |
| | 2 x *n*RRD | Repeat sub-loop 0, use BA[2:0] = 2 | | | | | | | | | | | | | | |
| 3 | 3x *n*RRD | Repeat sub-loop 0, use BA[2:0] = 3 | | | | | | | | | | | | | | |
| 4 | 4 x *n*RRD | D | 1 | 0 | 0 | 0 | 0 | 3 | 0 | 0 | 0 | F | 0 | - | | |
| | 4 x *n*RRD + 1 | Repeat cycle 4 x *n*RRD until *n*FAW - 1, if needed | | | | | | | | | | | | | | |
| 5 | *n*FAW | Repeat sub-loop 0, use BA[2:0] = 4 | | | | | | | | | | | | | | |
| 6 | *n*FAW + *n*RRD | Repeat sub-loop 1, use BA[2:0] = 5 | | | | | | | | | | | | | | |
| 7 | *n*FAW + 2x*n*RRD | Repeat sub-loop 0, use BA[2:0] = 6 | | | | | | | | | | | | | | |
| 8 | *n*FAW + 3x*n*RRD | Repeat sub-loop 1, use BA[2:0] = 7 | | | | | | | | | | | | | | |
| 9 | *n*FAW + 4x*n*RRD | D | 1 | 0 | 0 | 0 | 0 | 7 | 0 | 0 | 0 | F | 0 | - | | |
| | *n*FAW + 4x*n*RRD+1 | Repeat cycle *n*FAW + 4 x *n*RRD until 2 x *n*FAW - 1, if needed | | | | | | | | | | | | | | |
| 10 | 2 x *n*FAW | ACT | 0 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | F | 0 | - | | |
| | 2 x *n*FAW + 1 | RDA | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 1 | 0 | F | 0 | 00110011 | | |
| | 2 x *n*FAW + 2 | D | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | F | 0 | - | | |
| | 2 x *n*FAW + 3 | Repeat cycle 2 x *n*FAW + 2 until 2 x *n*FAW + *n*RRD - 1 | | | | | | | | | | | | | | |
| 11 | 2 x *n*FAW + *n*RRD | ACT | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | - | | |
| | 2 x *n*FAW + *n*RRD+1 | RDA | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 00000000 | | |
| | 2 x *n*FAW + *n*RRD+2 | D | 1 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 | 0 | 0 | - | | |
| | 2 x *n*FAW + *n*RRD+3 | Repeat cycle 2 x *n*FAW + *n*RRD + 2 until 2 x *n*FAW + 2 x *n*RRD - 1 | | | | | | | | | | | | | | |
| 12 | 2 x *n*FAW + 2x *n*RRD | Repeat sub-loop 10, use BA[2:0] = 2 | | | | | | | | | | | | | | |
| 13 | 2 x *n*FAW + 3x *n*RRD | Repeat sub-loop 11, use BA[2:0] = 3 | | | | | | | | | | | | | | |
| 14 | 2 x *n*FAW + 4x *n*RRD | D | 1 | 0 | 0 | 0 | 0 | 3 | 0 | 0 | 0 | F | 0 | - | | |
| | 2 x *n*FAW+4x *n*RRD+1 | Repeat cycle 2 x *n*FAW + 4 x *n*RRD until 3 x *n*FAW - 1, if needed | | | | | | | | | | | | | | |
| 15 | 3 x nFAW | Repeat sub-loop 10, use BA[2:0] = 4 | | | | | | | | | | | | | | |
| 16 | 3 x nFAW + nRRD | Repeat sub-loop 11, use BA[2:0] = 5 | | | | | | | | | | | | | | |
| 17 | 3 x nFAW + 2x nRRD | Repeat sub-loop 10, use BA[2:0] = 6 | | | | | | | | | | | | | | |
| 18 | 3 x nFAW + 3x nRRD | Repeat sub-loop 11, use BA[2:0] = 7 | | | | | | | | | | | | | | |
| 19 | 3 x nFAW + 4x nRRD | D | 1 | 0 | 0 | 0 | 0 | 7 | 0 | 0 | 0 | F | 0 | - | | |
| | 3 x nFAW + 4x nRRD +1 | Repeat cycle 3 x *n*FAW + 4 x *n*RRD until 4 x *n*FAW - 1, if needed | | | | | | | | | | | | | | |

## TABLE 19: ICC MAXIMUM LIMITS

| Icc | | Speed Bin DDR3-800 | DDR3-1066 | DDR3-1333 | UNITS | Notes |
|---|---|---|---|---|---|---|
| Icc0 | IND | 437 | 488 | 544 | mA | 1 |
| | EXT | 456 | 508 | | mA | 2 |
| | MIL-TEMP | 475 | | | mA | 3 |
| Icc1 | IND | 544 | 637 | 731 | mA | 1 |
| | EXT | 578 | 663 | | mA | 2 |
| | MIL-TEMP | 603 | | | mA | 3 |
| Icc2P0 | IND | 59 | 59 | 59 | mA | 1 |
| | EXT | 76 | 76 | | mA | 2 |
| | MIL-TEMP | 220 | | | mA | 3 |
| Icc2P1 | IND | 148 | 171 | 196 | mA | 1 |
| | EXT | 191 | 223 | | mA | 2 |
| | MIL-TEMP | 220 | | | mA | 3 |
| Icc2Q | IND | 230 | 265 | 300 | mA | 1 |
| | EXT | 299 | 344 | | mA | 2 |
| | MIL-TEMP | 343 | | | mA | 3 |
| Icc2N | IND | 244 | 268 | 318 | mA | 1 |
| | EXT | 316 | 349 | | mA | 2 |
| | MIL-TEMP | 362 | | | mA | 3 |
| Icc2NT | IND | 393 | 465 | 515 | mA | 1 |
| | EXT | 506 | 605 | | mA | 2 |
| | MIL-TEMP | 581 | | | mA | 3 |
| Icc3P | IND | 148 | 173 | 196 | mA | 1 |
| | EXT | 154 | 181 | | mA | 2 |
| | MIL-TEMP | 163 | | | mA | 3 |
| Icc3N | IND | 245 | 268 | 294 | mA | 1 |
| | EXT | 250 | 273 | | mA | 2 |
| | MIL-TEMP | 269 | | | mA | 3 |
| Icc4R | IND | 1128 | 1275 | 1421 | mA | 1 |
| | EXT | 1150 | 1300 | | mA | 2 |
| | MIL-TEMP | 1175 | | | mA | 3 |
| Icc4W | IND | 1176 | 1421 | 1740 | mA | 1 |
| | EXT | 1200 | 1450 | | mA | 2 |
| | MIL-TEMP | 1125 | | | mA | 3 |
| Icc5B | IND | 980 | 1077 | 1176 | mA | 1 |
| | EXT | 1000 | 1100 | | mA | 2 |
| | MIL-TEMP | 1020 | | | mA | 3 |
| Icc6 | IND | 30 | 30 | 30 | mA | 1 |
| | EXT | 54 | 54 | | mA | 2 |
| | MIL-TEMP | 95 | | | mA | 3 |
| Icc7 | IND | 1700 | 1860 | 2055 | mA | 1 |
| | EXT | 1844 | 2000 | | mA | 2 |
| | MIL-TEMP | 1988 | | | mA | 3 |
| Icc8 | IND | Icc2P + 2mA | Icc2P + 2mA | Icc2P + 2mA | mA | 1 |
| | EXT | Icc2P + 2.1mA | Icc2P + 2.1mA | | mA | 2 |
| | MIL-TEMP | Icc2P + 2.4mA | | | mA | 3 |

NOTES:

1. Tc = 0°C to ≤ 85°C; SRT and ASR are disabled, enabling ASR could increase ICCx by up to an additional 2mA.
2. Tc = -40°C to ≤ 105°C; SRT and ASR are disabled, enabling ASR could increase ICCx by up to an additional 2mA.
3. Tc = -55°C to ≤ 125°C; SRT and ASR are disabled, enabling ASR could increase ICCx by up to an additional 2mA.

## TABLE 20: DC ELECTRICAL CHARACTERISTICS AND OPERATING CONDITIONS

All Voltages are referenced to Vss

| Parameter/Condition | Symbol | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **Supply Voltage** | $V_{CC}$ | 1.425 | 1.5 | 1.575 | V | 1,2 |
| **I/O Supply Voltage** | $V_{CC}Q$ | 1.425 | 1.5 | 1.575 | V | 1,2 |
| **Input Leakage Current:** Any input $0V \le V_{IN} \le V_{CC}$, $V_{REF}$ pin $0V \le V_{IN} \le 1.1V$ All other pins not under test = 0V | $I_I$ | -2 | - | 2 | µA | |
| **VREF Supply Leakage Current:** $V_{REFDQ}$ = Vcc/2 or $V_{REFCA}$ = Vcc/2 All other pins not under test = 0V | $I_{VREF}$ | -1 | - | 1 | µA | 3,4 |

NOTES:

1. Vcc and VccQ must track one another, VccQ must be less than or equal to Vcc, Vss = VssQ.
2. Vcc and VccQ may include AC noise of ± 50mV (250 kHz to 20MHz) in addition to the DC (0Hz to 250kHz) specifications, Vcc and VccQ must be at the same level for valid AC timing parameters.
3. $V_{REF}$ (see Table 22).
4. The minimum limit requirement is for testing purposes. The leakage current on the $V_{REF}$ pin should be minimal.

## TABLE 21: DC ELECTRICAL CHARACTERISTICS AND INPUT CONDITIONS

All Voltages are referenced to Vss

| Parameter/Condition | Symbol | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| **VIN low; DC/commands/address busses** | $V_{IL}$ | $V_{SS}$ | n/a | See Table 20 | V | |
| **VIN high; DC/commands/address busses** | $V_{IH}$ | See Table 20 | n/a | $V_{CC}$ | V | |
| **Input reference voltage command/address bus** | $V_{REFCA}$(DC) | 0.49 x $V_{CC}$ | 0.5 x $V_{CC}$ | 0.51 x $V_{CC}$ | V | 1,2 |
| **I/O reference voltage DQ bus** | $V_{REFDQ}$(DC) | 0.49 x $V_{CC}$ | 0.5 x $V_{CC}$ | 0.51 x $V_{CC}$ | V | 2,3 |
| **I/O reference voltage DQ bus in SELF REFRESH** | $V_{REFDQ}$(SR) | $V_{SS}$ | 0.5 x $V_{CC}$ | $V_{CC}$ | V | 4 |
| **Command/address termination voltage** (system level, not direct DRAM input) | $V_{TT}$ | - | 0.5 x $V_{CC}Q$ | - | V | 5 |

NOTES:

1. $V_{REFCA}$(DC) is expected to be approximately 0.5 x Vcc and to track variations in the DC level. Externally generated peak noise (noncommon mode) on $V_{REFCA}$ may not exceed ± 1% x Vcc around the $V_{REFCA}$(DC) value. Peak-to-peak AC noise on $V_{REFCA}$ should not exceed ± 2% of $V_{REFCA}$(DC).
2. DC values are determined to be less than 20MHz in frequency. DRAM must meet specifications if the DRAM induces additional AC noise greater than 20MHz in frequency.
3. $V_{REFDQ}$(DC) is expected to be approximately 0.5 x Vcc and to track variations in the DC level. Externally generated peak noise (noncommon mode) on VREFDQ may not exceed ± 1% x Vcc around the VREFDQ(DC) value. Peak-to-peak AC noise on VREFDQ should not exceed ± 2% of VREFDQ(DC).
4. $V_{REFDQ}$(DC) may transition to $V_{REFDQ}$(SR) and back to $V_{REFDQ}$(DC) when in SELF zREFRESH, within restrictions outlined in the SELF REFRESH section.
5. $V_{TT}$ is not applied directly to the device. $V_{TT}$ is a system supply for signal termination resistors. MIN and MAX values are system-dependent.

**TABLE 22: INPUT SWITCHING CONDITIONS**

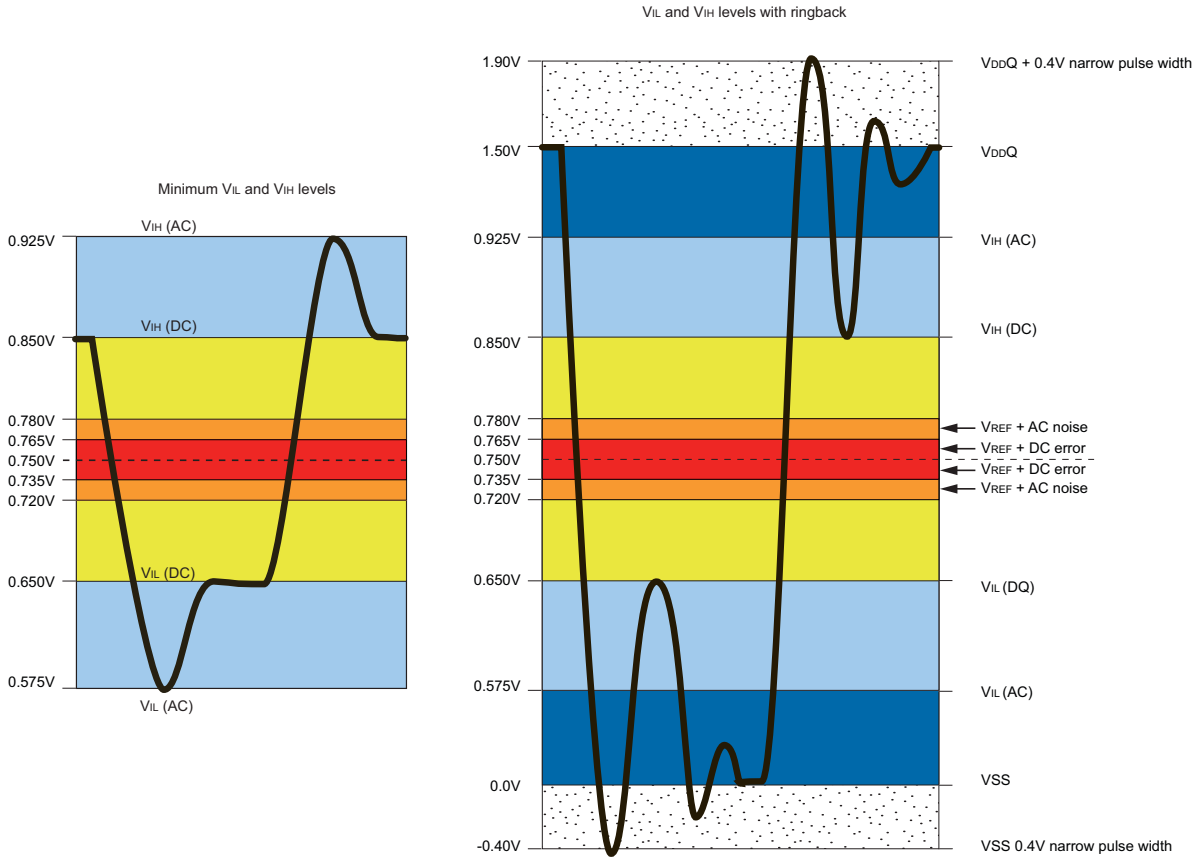
| Parameter/Condition | Symbol | DDR3-1066 DDR3-900 | DDR1333 | UNITS |
|---|---|---|---|---|
| Command and Address | | | | |
| **Input high AC voltage: Logic 1** | $V_{IH}$ (AC175) MIN | +175 | +175 | mV |
| **Input high AC voltage: Logic 1** | $V_{IH}$ (AC150) MIN | +150 | +150 | mV |
| **Input high DC voltage: Logic 1** | $V_{IH}$ (DC100) MIN | +100 | +100 | mV |
| **Input high DC voltage: Logic 0** | $V_{IL}$ (DC100) MAX | -100 | -100 | mV |
| **Input high AC voltage: Logic 0** | $V_{IL}$ (AC150) MAX | -150 | -150 | mV |
| **Input high AC voltage: Logic 0** | $V_{IL}$ (AC175) MAX | -175 | -175 | mV |
| DQ and DM | | | | |
| **Input high AC voltage: Logic 1** | $V_{IH}$ (AC175) MIN | +175 | - | mV |
| **Input high AC voltage: Logic 1** | $V_{IH}$ (AC150) MIN | +150 | +150 | mV |
| **Input high DC voltage: Logic 1** | $V_{IH}$ (DC100) MIN | +100 | +100 | mV |
| **Input high DC voltage: Logic 0** | $V_{IL}$ (DC100) MAX | -100 | -100 | mV |
| **Input high AC voltage: Logic 0** | $V_{IL}$ (AC150) MAX | -150 | -150 | mV |
| **Input high AC voltage: Logic 0** | $V_{IL}$ (AC175) MAX | -175 | - | mV |

NOTES:

1. All voltages are referenced to $V_{REF}$, $V_{REF}$ is $V_{REFCA}$ for control, command, and address. All slew rates and setup/hold times are specified at the DRAM ball. $V_{REF}$ is $V_{REFDQ}$ for DQ and DM inputs.
2. Input setup timing parameters ($^{t}IS$ and $^{t}DS$) are referenced at $V_{IL}(AC)$/$V_{IH}(AC)$, not $V_{REF}(DC)$.
3. Input hold timing parameters ($^{t}IH$ and $^{t}DH$) are referenced at $V_{IL}(DC)$/$V_{IH}(DC)$, not $V_{REF}(AC)$.
4. Single-ended input slew rate = 1V/ns; maximum input voltage swing under test is 900mV (peak-to-peak).

## OPERATING CONDITIONS

### FIGURE 6 - INPUT SIGNAL




Notes: 1. Numbers in diagrams reflect nominal values.

## AC OVERSHOOT/UNDERSHOOT SPECIFICATION

### Table 23: Control and Address Pins

| Parameter | DDR3-800 | DDR3-1066 | DDR3-1333 |
|---|---|---|---|
| **Maximum peak amplitude allowed for overshoot area** (see Figure 16 on page 38) | 0.4V | 0.4V | 0.4V |
| **Maximum peak amplitude allowed for overshoot area** (see Figure 17 on page 39) | 0.4V | 0.4V | 0.4V |
| **Maximum overshoot area above $V_{CC}$** (see Figure 16 on page 38) | 0.67Vns | 0.5Vns | 0.4Vns |
| **Maximum undershoot area below $V_{SS}$** (see Figure 17 on page 39) | 0.67Vns | 0.5Vns | 0.4Vns |

### Table 24: Clock, Data, Strobe, and Mask Pins

| Parameter | DDR3-800 | DDR3-1066 | DDR3-1333 |
|---|---|---|---|
| **Maximum peak amplitude allowed for overshoot area** (see Figure 16 on page 38) | 0.4V | 0.4V | 0.4V |
| **Maximum peak amplitude allowed for overshoot area** (see Figure 17 on page 39) | 0.4V | 0.4V | 0.4V |
| **Maximum overshoot area above $V_{CC}$/ $V_{CC}Q$** (see Figure 16 on page 38) | 0.25Vns | 0.19Vns | 0.15Vns |
| **Maximum undershoot area below $V_{SS}$/ $V_{SS}Q$** (see Figure 17 on page 39) | 0.25Vns | 0.19Vns | 0.15Vns |

### Figure 7 & 8: Overshoot/Undershoot Specifications

**Figure 7: Overshoot**

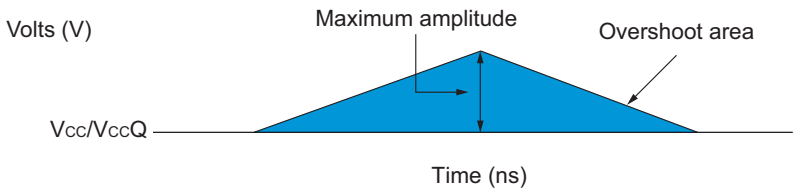
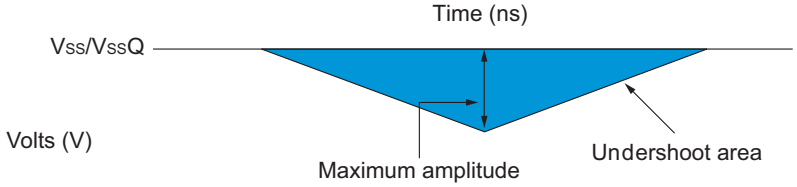



**Figure 8: Undershoot**



## TABLE 25: DIFFERENTIAL INPUT OPERATING CONDITIONS (CKx, CKx\, DQSx, AND DQSx\)

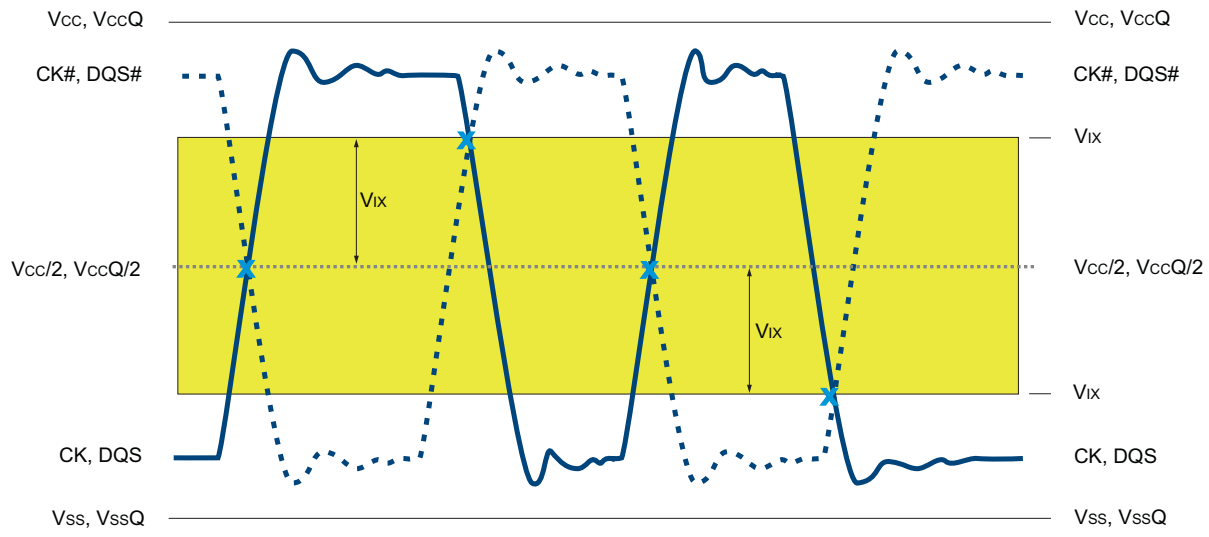
| Parameter/Condition | Symbol | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| **Differential input voltage, logic high - slew** | $V_{IH}$ DIFF(AC)slew | +200 | n/a | mV | 4 |
| **Differential input voltage, logic low - slew** | $V_{IL}$ DIFF(AC)slew | n/a | -200 | mV | 4 |
| **Differential input voltage, logic high** | $V_{IH}$ DIFF(AC) | 2x($V_{IH}$(AC)-$V_{REF}$) | $V_{CC}$/$V_{CC}$Q | mV | 5 |
| **Differential input voltage, logic low** | $V_{IL}$ DIFF(AC) | $V_{SS}$/$V_{SS}$Q | 2x($V_{REF}$-$V_{IL}$(AC)) | mV | 6 |
| **Differential input crossing voltage relative to Vcc/2 for DQS, DQS\, CK, CK** | $V_{IX}$ | $V_{REF}$(DC) - 150 | $V_{REF}$(DC) + 150 | mV | 7 |
| **Differential input crossing voltage relative to Vcc/2 for CK, CK** | $V_{IX(175)}$ | $V_{REF}$(DC) - 175 | $V_{REF}$(DC) + 175 | mV | 7,8 |
| **Single-ended high level for strobes** | $V_{SHE}$ | $V_{CC}$Q/2 + $V_{IH}$(AC) | $V_{CC}$Q | mV | 5 |
| **Single-ended high level for CK, CK** | | $V_{CC}$/2 + $V_{IH}$(AC | $V_{CC}$ | | |
| **Single-ended low level for strobes** | $V_{SEL}$ | $V_{SS}$Q | $V_{CC}$Q/2-$V_{IL}$(AC) | mV | 6 |
| **Single-ended low level for CK, CK** | | $V_{SS}$ | $V_{CC}$/2-$V_{IL}$(AC) | | |

NOTES:

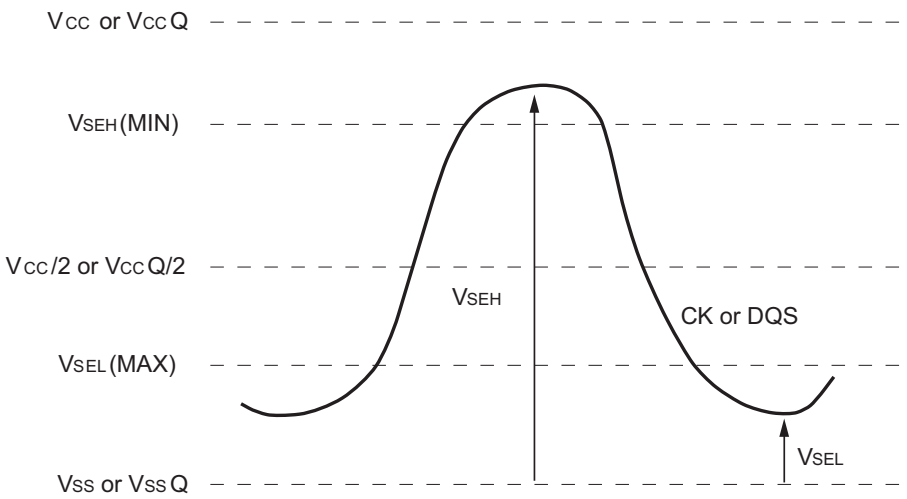
1. Clock is referenced to VccD and Vss. Data strobe is referenced to VccQ and VssQ.
2. Reference is $V_{REFCA}$(DC) for clock and for $V_{REFDQ}$(DC) for strobe.
3. Differential input slew rate = 2V/ms.
4. Defines slew rate reference points relative to input crossing voltages.
5. MAX limit is relative to single-ended signals, the overshoot specifications are applicable.
6. MIN limit is relative to single-ended signals, the undershoot specifications are applicable.
7. The typical value of $V_{IX}$(AC) is expected to be about 0.5 x Vcc of the transmitting device and $V_{IX}$(AC) is expected to track variations in Vcc. $V_{IX}$(AC) indicates the voltage at which differential input signals must cross.
8. The $V_{IX}$ extended range (±175mV) is allowed only for the clock and this $V_{IX}$ extended range is only allowed when the following conditions are met: The single-ended input signals are monotonic, have the single-ended swing $V_{SEL}$, $V_{SEH}$ of at least Vcc/2 ±250mV, and the differential slew rate of CK, CK\ is greater than 3V/ns.

## OVERSHOOT/UNDERSHOOT SPECIFICATIONS

### FIGURE 9 - VIX FOR DIFFERENTIAL SIGNALS

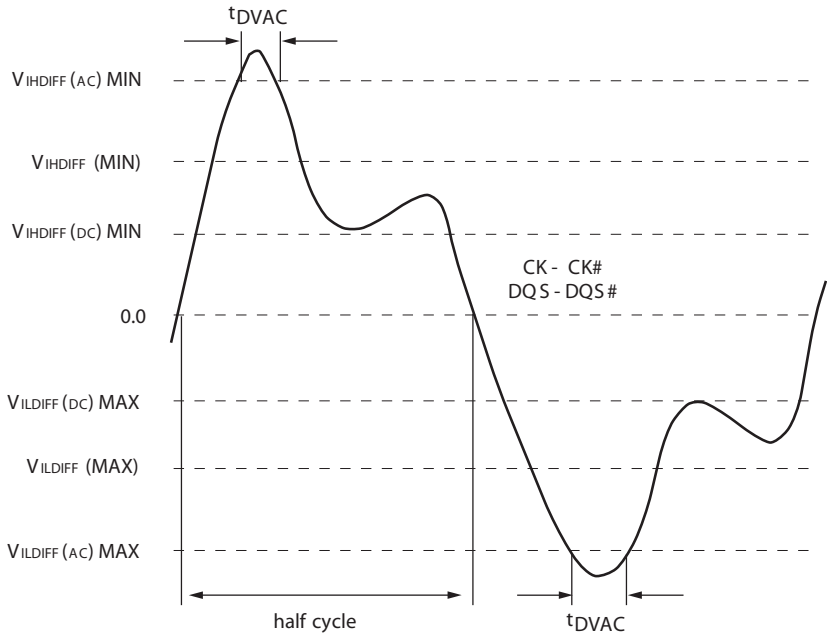



### FIGURE 10 - SINGLE-ENDED REQUIREMENTS FOR DIFFERENTIAL SIGNALS



## OVERSHOOT/UNDERSHOOT SPECIFICATIONS

### FIGURE 11 - DEFINITION OF DIFFERENTIAL AC-SWING AND tDVAC




### TABLE 26: DIFFERENTIAL INPUT OPERATING CONDITIONS (tDVAC) FOR CKx, CKx\, DQSx, AND DQSx\

Below VIL (AC)

| Slew Rate (V/ns) | tDVAC (ps) at [VIHDIFF(AC) to VILDiff(AC)] | |
|---|---|---|
| | 350mV | 300mV |
| -4.0 | 75 | 175 |
| 4.0 | 57 | 170 |
| 3.0 | 50 | 167 |
| 2.0 | 38 | 163 |
| 1.9 | 34 | 162 |
| 1.6 | 29 | 161 |
| 1.4 | 22 | 159 |
| 1.2 | 13 | 155 |
| 1.0 | 0 | 150 |
| <1.0 | 0 | 150 |

## SLEW RATE DEFINITIONS FOR SINGLE-ENDED INPUT SIGNALS

Setup ($^{t}$IS and $^{t}$DS) nominal slew rate for a rising signal is defined as the slew-rate between the last crossing of $V_{REF}$ and the first crossing $V_{IH}$(AC) MIN. Setup ($^{t}$IS and $^{t}$DS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF}$ an the first crossing of $V_{IL}$(AC) MAX.

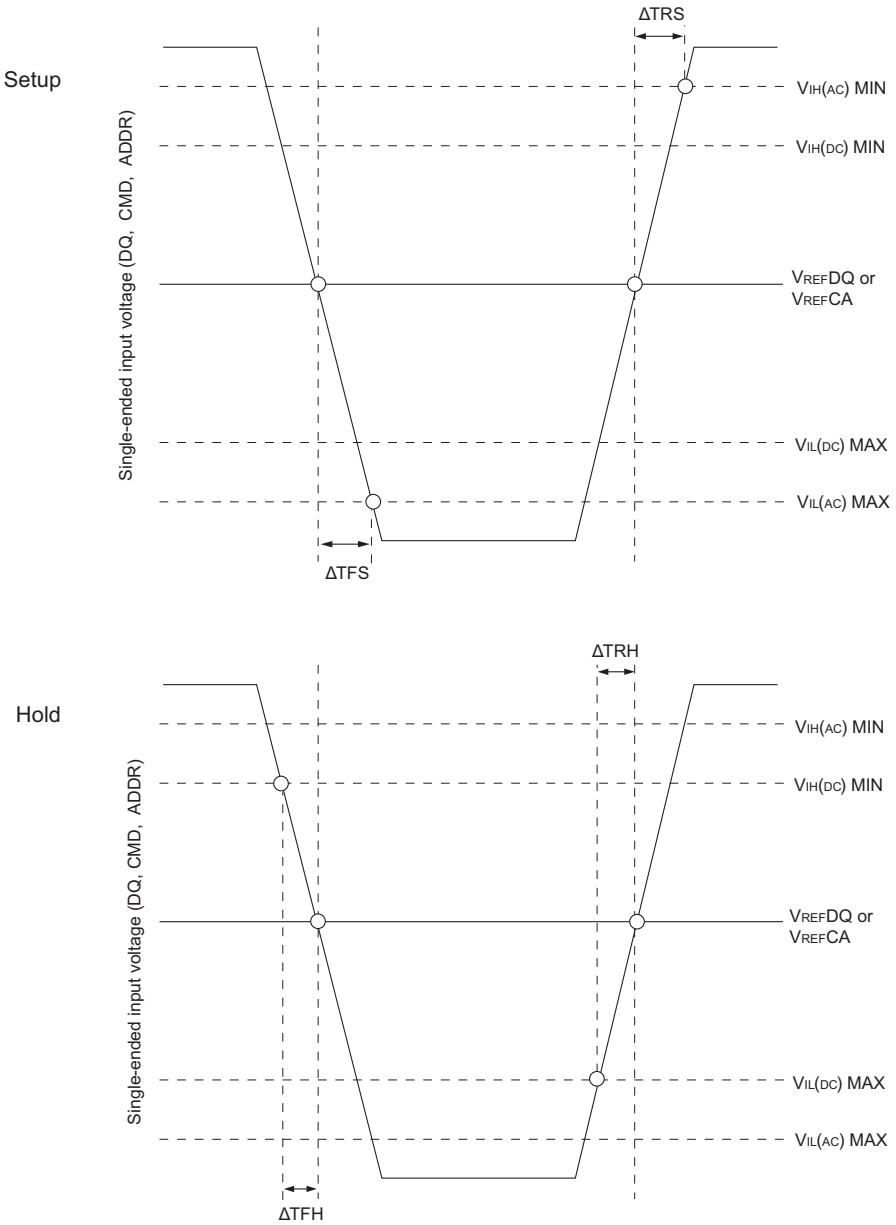
Hold ($^{t}$IH and $^{t}$DH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL}$(DC) MAX and the first crossing of $V_{REF}$. Hold ($^{t}$IH and $^{t}$DH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH}$(DC) MIN and the first crossing of $V_{REF}$.

**TABLE 27: SINGLE-ENDED INPUT SLEW RATE**

| Input Slew Rate (Linear Signals) | | Measured | | |
|---|---|---|---|---|
| **Input** | **Edge** | **From** | **To** | **Calculation** |
| **Setup** | Rising | $V_{REF}$ | $V_{IH}$(AC)MIN | $V_{IH}$(AC) MIN - $V_{REF}$ |
| | Falling | $V_{REF}$ | $V_{IL}$(AC)MAX | $\frac{V_{REF} - V_{IL}(AC)\ MAX}{\Delta TFS}$ |
| **Hold** | Rising | $V_{IL}$(DC)Max | $V_{REF}$ | $\frac{V_{REF} - V_{IL}(DC)\ MAX}{\Delta TFH}$ |
| | Falling | $V_{IH}$(DC)MIN | $V_{REF}$ | $\frac{V_{IH}(DC)\ MIN - V_{REF}}{\Delta TRSH}$ |

## SLEW RATE DEFINITIONS FOR SINGLE-ENDED INPUT SIGNALS

### FIGURE 12 - NOMINAL SLEW RATE DEFINITION FOR SINGLE-ENDED INPUT SIGNALS



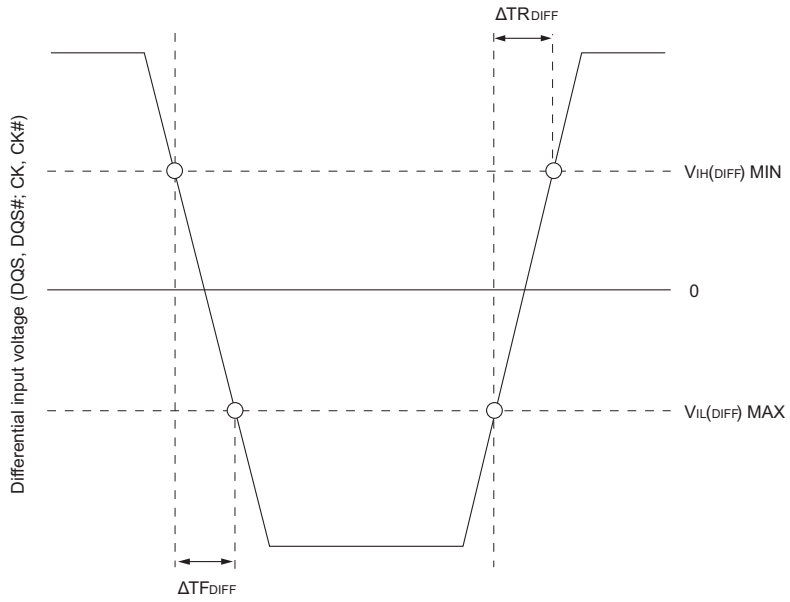
## SLEW RATE DEFINITIONS FOR DIFFERENTIAL INPUT SIGNALS

Input slew rate for differential signals (CKx, CKx\, UDQSx , UDQSx\, LDQSx and LDQSx\) are defined and measured as shown in Table 28. The nominal slew rate for a rising signal is defined as the slew rate between $V_{IL}$(DIFF) MAX and $V_{IH}$(DIFF) MIN. The nominal slew rate for a falling signal is defined as the slew rate between $V_{IH}$(DIFF) MIN and $V_{IL}$(DIFF) MAX.

### TABLE 28: DIFFERENTIAL INPUT SLEW RATE DEFINITION

| Input Slew Rate (Linear Signals) | | Measured | | |
|---|---|---|---|---|
| Input | Edge | From | To | Calculation |
| CK and DQS Reference | Rising | $V_{REF}$ | $V_{IH}$(AC)MIN | $\frac{V_{IH}(DIFF)\ MIN - V_{IL}(DIFF)\ MAX}{\Delta TR(DIFF)}$ |
| | Falling | $V_{REF}$ | $V_{IL}$(AC)MAX | $\frac{V_{IH}(DIFF)\ MIN - V_{IL}(DIFF)\ MAX}{\Delta TF(DIFF)}$ |

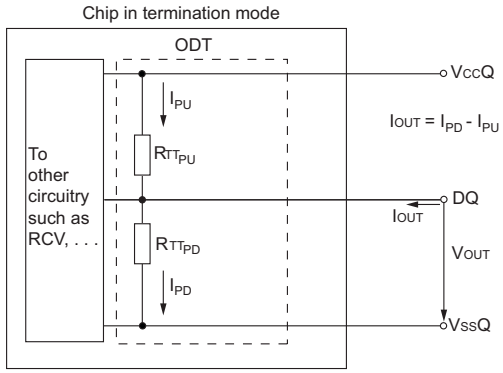
### FIGURE 13 - NOMINAL DIFFERENTIAL INPUT SLEW RATE DEFINITION FOR DQS, DQS# AND CK, CK#



## ODT CHARACTERISTICS

ODT's effective resistance RTT is defined by MR1[9,6 and 2]. ODT is applied to the DQx, UDMx, LDMx, UDQSx, UDQSx\, LDQSx and LDQSx\ balls. The ODT target values are listed in Table 29.

## FIGURE 14 - ODT LEVELS AND I-V CHARACTERISTICS




## TABLE 29: ON-DIE TERMINATION DC ELECTRICAL CHARACTERISTICS

| Parameter/Condition | Symbol | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|
| RTT effective impedance | RTT_EFF | See Table 30 | | | | 1, 2, 4 |
| Deviation of VM with respect to VccQ/2 | ΔVM | -5 | | 5 | % | 1, 2, 3, 4 |

NOTES:

1. Tolerance limits are applicable after a proper ZQ calibration has been performed at a stable temperature and voltage (VccQ=Vcc, VssQ-Vss). Refer to "ODT Sensitivity" on page 37 if either the temperature or voltage changes after calibration.

2. Measurement definition for RTT: Apply VIH(AC) to a pin under test and measure the current I[VIH(AC)], then apply VIL(AC) to pin under test and measure current I[VIL(AC)]:

$$RTT = \frac{VIL(AC) - VIL(AC)}{I[VIH(AC))-I(VIL(AC))]}$$

3. Measure voltage (VM) at the tested pin with no load:

$$\Delta VM = \left[\frac{2 \times VM}{VccQ} - 1\right] \times 100$$

4. For extended MIL-temp devices, the minimum values are derated by 6% when the device is between -40°C and 0°C (Tc).

## Table 30: RTT Effective Impedances

| MR1 [9,6,2] | RTT | Resistor | VOUT | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| 0, 1, 0 | 120Ω | RTT120PD240 | 0.2 x VccQ | 0.6 | 1.0 | 1.1 | RZQ/1 |
| | | | 0.5 x VccQ | 0.9 | 1.0 | 1.1 | RZQ/1 |
| | | | 0.8 x VccQ | 0.9 | 1.0 | 1.4 | RZQ/1 |
| | | RTT120PU240 | 0.2 x VccQ | 0.9 | 1.0 | 1.4 | RZQ/1 |
| | | | 0.5 x VccQ | 0.9 | 1.0 | 1.1 | RZQ/1 |
| | | | 0.8 x VccQ | 0.9 | 1.0 | 1.1 | RZQ/1 |
| | 120Ω | | VIL(AC) to VIH(AC) | 0.9 | 1.0 | 1.6 | RZQ/2 |
| 0, 0, 1 | 60Ω | RTT60PD120 | 0.2 x VccQ | 0.6 | 1.0 | 1.1 | RZQ/2 |
| | | | 0.5 x VccQ | 0.9 | 1.0 | 1.1 | RZQ/2 |
| | | | 0.8 x VccQ | 0.9 | 1.0 | 1.4 | RZQ/2 |
| | | RTT60PU240 | 0.2 x VccQ | 0.9 | 1.0 | 1.4 | RZQ/2 |
| | | | 0.5 x VccQ | 0.9 | 1.0 | 1.1 | RZQ/2 |
| | | | 0.8 x VccQ | 0.9 | 1.0 | 1.1 | RZQ/2 |
| | 60Ω | | VIL(AC) to VIH(AC) | 0.9 | 1.0 | 1.6 | RZQ/4 |
| 0, 1, 1 | 40Ω | RTT40PD80 | 0.2 x VccQ | 0.6 | 1.0 | 1.1 | RZQ/3 |
| | | | 0.5 x VccQ | 0.9 | 1.0 | 1.1 | RZQ/3 |
| | | | 0.8 x VccQ | 0.9 | 1.0 | 1.4 | RZQ/3 |
| | | RTT40PU80 | 0.2 x VccQ | 0.9 | 1.0 | 1.4 | RZQ/3 |
| | | | 0.5 x VccQ | 0.9 | 1.0 | 1.1 | RZQ/3 |
| | | | 0.8 x VccQ | 0.9 | 1.0 | 1.1 | RZQ/3 |
| | 40Ω | | VIL(AC) to VIH(AC) | 0.9 | 1.0 | 1.6 | RZQ/6 |
| 1, 0, 1 | 30Ω | RTT30PD60 | 0.2 x VccQ | 0.6 | 1.0 | 1.1 | RZQ/4 |
| | | | 0.5 x VccQ | 0.9 | 1.0 | 1.1 | RZQ/4 |
| | | | 0.8 x VccQ | 0.9 | 1.0 | 1.4 | RZQ/4 |
| | | RTT30PU60 | 0.2 x VccQ | 0.9 | 1.0 | 1.4 | RZQ/4 |
| | | | 0.5 x VccQ | 0.9 | 1.0 | 1.1 | RZQ/4 |
| | | | 0.8 x VccQ | 0.9 | 1.0 | 1.1 | RZQ/4 |
| | 30Ω | | VIL(AC) to VIH(AC) | 0.9 | 1.0 | 1.6 | RZQ/8 |
| 1, 0, 0 | 20Ω | RTT20PD40 | 0.2 x VccQ | 0.6 | 1.0 | 1.1 | RZQ/6 |
| | | | 0.5 x VccQ | 0.9 | 1.0 | 1.1 | RZQ/6 |
| | | | 0.8 x VccQ | 0.9 | 1.0 | 1.4 | RZQ/6 |
| | | RTT20PU40 | 0.2 x VccQ | 0.9 | 1.0 | 1.4 | RZQ/6 |
| | | | 0.5 x VccQ | 0.9 | 1.0 | 1.1 | RZQ/6 |
| | | | 0.8 x VccQ | 0.9 | 1.0 | 1.1 | RZQ/6 |
| | 20Ω | | VIL(AC) to VIH(AC) | 0.9 | 1.0 | 1.6 | RZQ/12 |

## ODT SENSITIVITY

If either the temperature or voltage changes after I/O calibration, the tolerance limits listed in Table 29 can be expected to widen according to Tables 31 and 32.

**TABLE 31: ODT SENSITIVITY DEFINITION**

| Symbol | MIN | MAX | UNITS |
|---|---|---|---|
| RTT | 0.9 - dRTTdT x dRTTdV x [DV] | 1.6 + dRTTdT x [DT] + dRTTdV x [DV] | RZQ/(2, 4, 6, 8, 12) |

**TABLE 32 - ODT TEMPERATURE & VOLTAGE SENSITIVITY**

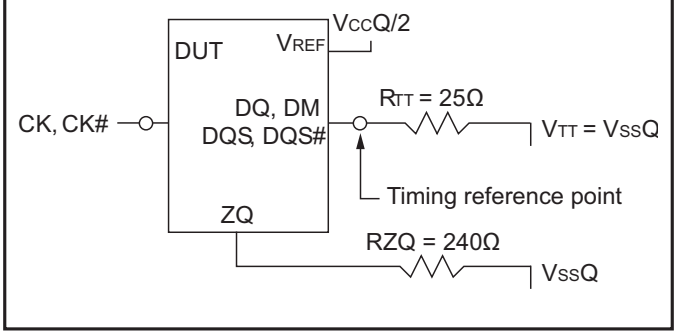
| Change | MIN | MAX | UNITS |
|---|---|---|---|
| dRTTdT | 0 | 1.5 | 0 |
| dRTTdV | 0 | 0.15 | 0 |

## ODT TIMING DEFINITIONS

ODT loading differs from that used in AC timing measurements. Two parameters define when ODT turns on or off synchronously, two define when ODT turns on or off Asynchronously and, another defines when ODT turns on or off dynamically. Table 33 outlines and provides definition and measurement reference settings for each parameter.

ODT turn-on time begins when the output leaves HIGH-Z and ODT resistance begins to turn on. ODT turn-off time begins when the output leaves LOW-Z and ODT resistance begins to turn-off.

**FIGURE 15 - ODT TIMING REFERENCE LOAD**



## ODT TIMING DEFINITIONS

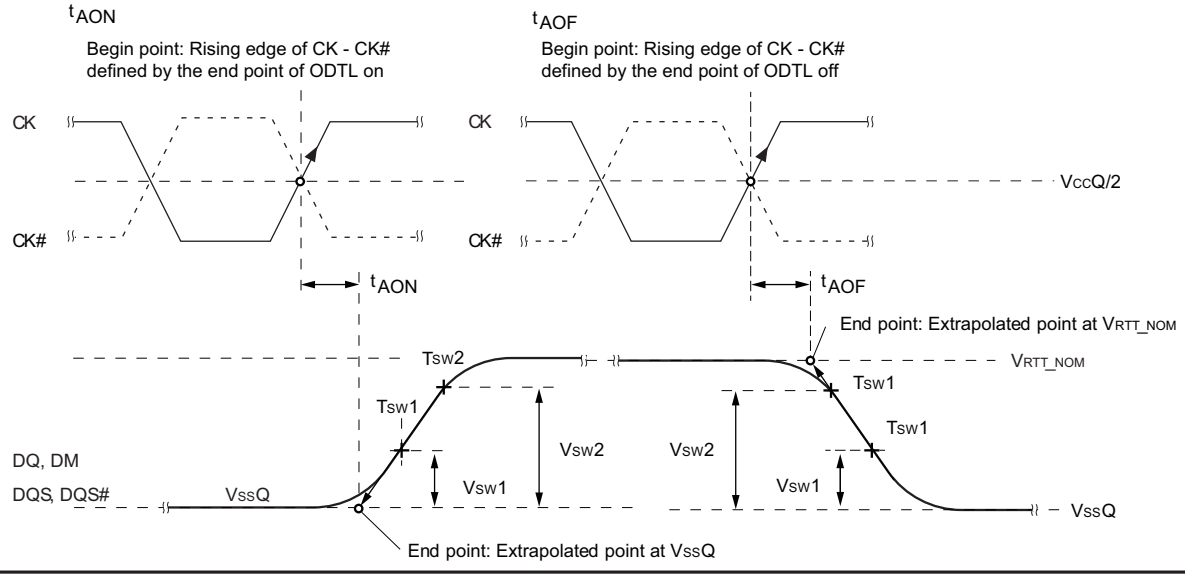
### TABLE 33: ODT TIMING DEFINITIONS

| Symbol | Begin Point Definition | End Point Definition | Figure |
|---|---|---|---|
| $t_{AON}$ | Rising edge of CK-CK\ defined by the end point of ODTL on | Extrapolated point at VssQ | Figure 25 on page 60 |
| $t_{AOF}$ | Rising edge of CK-CK\ defined by the end point of ODTL off | Extrapolated point at VRTT_NORM | Figure 25 on page 60 |
| $t_{AONPD}$ | Rising edge of CK-CK\ with ODT first being registered HIGH | Extrapolated point at VssQ | Figure 26 on page 61 |
| $t_{AOFPD}$ | Rising edge of CK-CK\ with ODT first being registered LOW | Extrapolated point at VRTT_NOM | Figure 26 on page 61 |
| $t_{ADC}$ | Rising edge of CK-CK\ defined by the end point of ODTLCNW, ODTLCWN4, or ODTLCWN8 | Extrapolated points at VRTT_WR and VRTT_NOM | Figure 27 on page 62 |

### TABLE 34: REFERENCE SETTINGS FOR ODT TIMING MEASUREMENTS

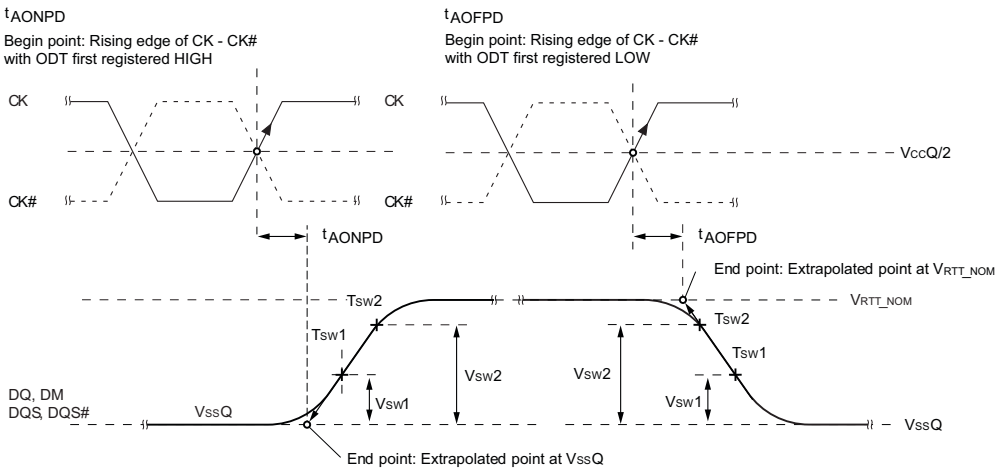
| Measured Parameter | RTT_NORM Setting | RTT_WR_Setting | VSW1 | VSW2 |
|---|---|---|---|---|
| $t_{AON}$ | RZQ/4 (60Ω) | n/a | 50mV | 100mV |
| | RZQ/12 (20Ω) | n/a | 100mV | 200mV |
| $t_{AOF}$ | RZQ/4 (60Ω) | n/a | 50mV | 100mV |
| | RZQ/12 (20Ω) | n/a | 100mV | 200mV |
| $t_{AONPD}$ | RZQ/4 (60Ω) | n/a | 50mV | 100mV |
| | RZQ/12 (20Ω) | n/a | 100mV | 200mV |
| $t_{AOFPD}$ | RZQ/4 (60Ω) | n/a | 50mV | 100mV |
| | RZQ/12 (20Ω) | n/a | 100mV | 200mV |
| $t_{ADC}$ | RZQ/12 (20Ω) | RZQ/2 (120Ω) | 200mV | 300mV |

### FIGURE 16 - $t_{AON}$ AND $t_{AOF}$ DEFINITIONS

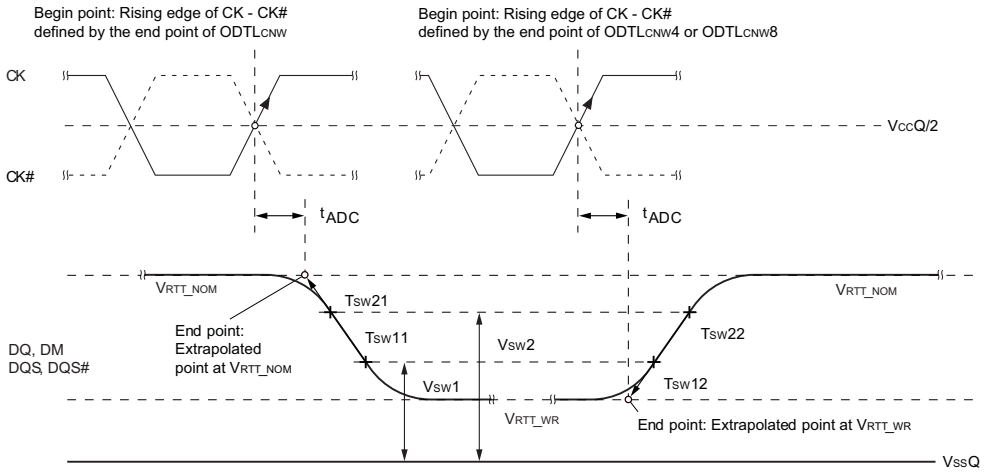


## ODT CHARACTERISTICS

### FIGURE 17 - $^{t}$AONPD AND $^{t}$AOFPD DEFINITION

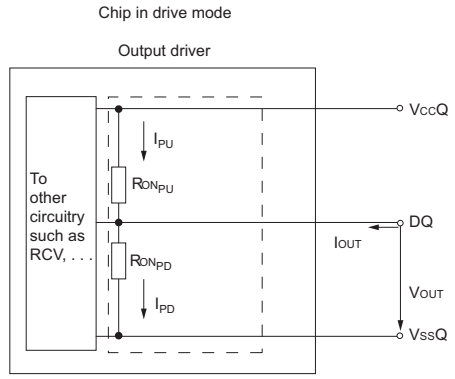



### FIGURE 18 - $^{t}$ADC DEFINITION



## OUTPUT DRIVER IMPEDANCE

### FIGURE 19 - OUTPUT DRIVER




### 34 OHM OUTPUT DRIVER IMPEDANCE

The 34Ω driver (MR1[5,1]=01) is the default driver. Unless otherwise stated, all timings and specifications listed herein apply to the 34Ω driver only. Its impedance RON is defined by the value of the external reference resistor RZQ as follows: RON34=RZQ/7 (with nominal RZQ=240Ω±1%) and is actually 34.3Ω±1%. The 34Ω output driver impedance characteristics are listed in Table 35.

### TABLE 35: 34Ω DRIVER IMPEDANCE CHARACTERISTICS

| MR1[5,1] | RON | RESISTOR | VOUT | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|
| 0, 1 | 34.3Ω | RON34PD | 0.2/VccQ | 0.6 | 1.0 | 1.1 | RZQ/7 | 1 |
| | | | 0.5/VccQ | 0.9 | 1.0 | 1.1 | RZQ/7 | 1 |
| | | | 0.8/VccQ | 0.9 | 1.0 | 1.4 | RZQ/7 | 1 |
| | | RON34PU | 0.2/VccQ | 0.9 | 1.0 | 1.4 | RZQ/7 | 1 |
| | | | 0.5/VccQ | 0.9 | 1.0 | 1.1 | RZQ/7 | 1 |
| | | | 0.8/VccQ | 0.6 | 1.0 | 1.1 | RZQ/7 | 1 |
| Pull-Up/Pull-Down mismatch (MMPUPD) | | | 0.5/VccQ | -10 | n/a | 10 | % | 1, 2 |

NOTES:

1. Tolerance limits assume RZQ of 240Ω (±1%) and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage (VccQ = Vcc, VssQ = Vss). Refer to “34 Ohm drive sensitivity” if either the temperature or the voltage changes after calibration

2. Measurement definition for mismatch between pull-up and pull-down (MMPUPD). Mearure both RONPU and RONPD at 0.5 x VccQ:

$$MMPUD = \frac{RONPU - RONPD}{RONNOM}$$

# 34 Ohm OUTPUT DRIVER IMPEDANCE

## 34 Ohm Driver

The 34Ω driver's current range has been calculated and summarized in Table 37 for Vcc=1.5V, Table 38 for Vcc=1.575V and Table 39 for Vcc=1.425V. The individual pull-up and pull-down resistors (RON34PD and RON34PU) are defined as follows with the Impedance Calculations listed in Table 36.

- RON34PD=(VOUT)/[IOUT]: RON34PU is turned off
- RON34PU=(VccQ-VOUT)/[IOUT]: RON34PD is turned off

### Table 36: 34Ω Driver Pull-Up and Pull-Down Impedance Calculations

| RON | | | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| RZQ = 240Ω±1% | | | | 237.6 | 240 | 242.4 | Ω |
| RZQ = (240Ω±1%)/7 | | | | 33.9 | 34.3 | 34.6 | Ω |
| **MR1[5,1]** | **RON** | **RESISTOR** | **VOUT** | **MIN** | **TYP** | **MAX** | **UNITS** |
| 0, 1 | 34.3Ω | RON34PD | 0.2/VccQ | 2.04 | 34.3 | 38.1 | Ω |
| | | | 0.5/VccQ | 30.5 | 34.3 | 38.1 | Ω |
| | | | 0.8/VccQ | 30.5 | 34.3 | 48.5 | Ω |
| | | RON34PU | 0.2/VccQ | 30.5 | 34.3 | 48.5 | Ω |
| | | | 0.5/VccQ | 30.5 | 34.3 | 38.1 | Ω |
| | | | 0.8/VccQ | 20.4 | 34.3 | 38.1 | Ω |

### Table 37: 34Ω Driver IOH/IOL Characteristics: Vcc = VccQ = 1.5V

| MR1[5,1] | RON | RESISTOR | VOUT | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| 0, 1 | 34.3Ω | RON34PD | IOL @ 0.2 x VccQ | 14.7 | 8.8 | 7.9 | mA |
| | | | IOL @ 0.5 x VccQ | 24.6 | 21.9 | 19.7 | mA |
| | | | IOL @ 0.8 x VccQ | 39.3 | 35 | 24.8 | mA |
| | | RON34PU | IOL @ 0.2 x VccQ | 39.3 | 35 | 24.8 | mA |
| | | | IOL @ 0.5 x VccQ | 24.6 | 21.9 | 19.7 | mA |
| | | | IOL @ 0.8 x VccQ | 14.7 | 8.8 | 7.9 | mA |

### Table 38: 34Ω Driver IOH/IOL Characteristics: Vcc=VccQ=1.575V

| MR1[5,1] | RON | RESISTOR | VOUT | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| 0, 1 | 34.3Ω | RON34PD | IOL @ 0.2 x VccQ | 15.5 | 9.2 | 8.3 | mA |
| | | | IOL @ 0.5 x VccQ | 25.8 | 23 | 20.7 | mA |
| | | | IOL @ 0.8 x VccQ | 41.2 | 36.8 | 26 | mA |
| | | RON34PU | IOL @ 0.2 x VccQ | 41.2 | 36.8 | 26 | mA |
| | | | IOL @ 0.5 x VccQ | 25.8 | 23 | 20.7 | mA |
| | | | IOL @ 0.8 x VccQ | 15.5 | 9.2 | 8.3 | mA |

## 34 Ohm OUTPUT DRIVER IMPEDANCE

### Table 39: 34Ω Driver IOH/IOL Characteristics: VCC=VCCQ=1.425V

| MR1[5,1] | RON | RESISTOR | VOUT | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| 0, 1 | 34.3Ω | RON34PD | IOL @ 0.2 x VccQ | 14 | 8.3 | 7.5 | mA |
| | | | IOL @ 0.5 x VccQ | 23.3 | 20.8 | 18.7 | mA |
| | | | IOL @ 0.8 x VccQ | 37.3 | 33.3 | 23.5 | mA |
| | | RON34PU | IOL @ 0.2 x VccQ | 37.3 | 33.3 | 23.5 | mA |
| | | | IOL @ 0.5 x VccQ | 23.3 | 20.8 | 18.7 | mA |
| | | | IOL @ 0.8 x VccQ | 14 | 8.3 | 7.5 | mA |

## 34Ω OUTPUT DRIVER SENSITIVITY

If either the temperature or voltage changes after ZQ calibration, the tolerance limits listed in Table 35 can be expected to widen according to Table 40 and 41.

### Table 40: 34Ω Output Driver Sensitivity Definition

| Symbol | MIN | MAX | UNITS |
|---|---|---|---|
| RON @ 0.8 x VccQ | 0.9 - dRONdTH x [ΔT] + dRONdVH x [ΔV] | 1.1 - dRONdTH x [ΔT] + dRONdVH x [ΔV] | RZQ/7 |
| RON @ 0.5 x VccQ | 0.9 - dRONdTM x [ΔT] + dRONdVM x [ΔV] | 1.1 - dRONdTM x [ΔT] + dRONdVM x [ΔV] | RZQ/7 |
| RON @ 0.2 x VccQ | 0.9 - dRONdTL x [ΔT] + dRONdVL x [ΔV] | 1.1 - dRONdTL x [ΔT] + dRONdVL x [ΔV] | RZQ/7 |

### Table 41: 34Ω Output Driver Voltage and Temperature Sensitivity

| Change | MIN | MAX | UNITS |
|---|---|---|---|
| dRONdTM | 0 | 1.5 | %/°C |
| dRONdVM | 0 | 0.13 | %/mV |
| dRONdTL | 0 | 1.5 | %/°C |
| dRONdVL | 0 | 0.13 | %/mV |
| dRONdTH | 0 | 1.5 | %/°C |
| dRONdVH | 0 | 0.13 | %/mV |

## ALTERNATIVE 40 OHM DRIVER

**TABLE 42 - 40Ω DRIVER IMPEDANCE CHARACTERISTICS**

| MR1[5,1] | RON | RESISTOR | VOUT | MIN | TYP | MAX | UNITS | NOTES |
|---|---|---|---|---|---|---|---|---|
| 0, 1 | 40.0Ω | RON40PD | 0.2/VccQ | 0.6 | 1.0 | 1.1 | RZQ/6 | 1 |
| | | | 0.5/VccQ | 0.9 | 1.0 | 1.1 | RZQ/6 | 1 |
| | | | 0.8/VccQ | 0.9 | 1.0 | 1.4 | RZQ/6 | 1 |
| | | RON40PU | 0.2/VccQ | 0.9 | 1.0 | 1.4 | RZQ/6 | 1 |
| | | | 0.5/VccQ | 0.9 | 1.0 | 1.1 | RZQ/6 | 1 |
| | | | 0.8/VccQ | 0.6 | 1.0 | 1.1 | RZQ/6 | 1 |
| Pull-Up/Pull-Down mismatch (MMPUPD) | | | 0.5/VccQ | -10 | n/a | 10 | % | 1, 2 |

NOTES:

1. Tolerance limits assume RZQ of 240Ω (±1%) and are applicable after proper ZQ calibration has been performed at a stable temperature and voltage (VccQ = Vcc, VssQ = Vss). Refer to "40 Ohm drive sensitivity" if either the temperature or the voltage changes after calibration

2. Measurement definition for mismatch between pull-up and pull-down (MMPUPD). Mearure both RONPU and RONPD at 0.5 x VccQ:

$$MM_{PUPD} = \frac{R_{ONPU} - R_{ONPD}}{R_{ONNOM}} \times 100$$

## 40Ω OUTPUT DRIVER SENSITIVITY

If either the temperature or voltage changes after I/O calibration, the tolerance limits listed in Table 42 can be expected to widen according to Table 43 and 44.

**TABLE 43: 40Ω OUTPUT DRIVER SENSITIVITY DEFINITION**

| Symbol | MIN | MAX | UNITS |
|---|---|---|---|
| RON @ 0.8 x VccQ | 0.9 - dRONdTH x [ΔT] + dRONdVH x [ΔV] | 1.1 - dRONdTH x [ΔT] + dRONdVH x [ΔV] | RZQ/6 |
| RON @ 0.5 x VccQ | 0.9 - dRONdTM x [ΔT] + dRONdVM x [ΔV] | 1.1 - dRONdTM x [ΔT] + dRONdVM x [ΔV] | RZQ/6 |
| RON @ 0.2 x VccQ | 0.9 - dRONdTL x [ΔT] + dRONdVL x [ΔV] | 1.1 - dRONdTL x [ΔT] + dRONdVL x [ΔV] | RZQ/6 |

## ALTERNATIVE 40 OHM DRIVER

### TABLE 44: 40Ω OUTPUT DRIVER VOLTAGE AND TEMPERATURE SENSITIVITY

| Change | MIN | MAX | UNITS |
|---|---|---|---|
| dRONdTM | 0 | 1.5 | %/°C |
| dRONdVM | 0 | 0.15 | %/mV |
| dRONdTL | 0 | 1.5 | %/°C |
| dRONdVL | 0 | 0.15 | %/mV |
| dRONdTH | 0 | 1.5 | %/°C |
| dRONdVH | 0 | 0.15 | %/mV |

## OUTPUT CHARACTERISTICS AND OPERATING CONDITIONS

The SDRAM uses both single-ended and differential output drivers. The single-ended output driver is summarized in Table 45 while the differential output driver is summarized in Table 46.

### TABLE 45: SINGLE-ENDED OUTPUT DRIVER CHARACTERISTICS

| Parameter/Condition | Symbol | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| **Output leakage current:** DQ are disabled; 0V ≤ VOUT ≤ VccQ; ODT is disabled; ODT is HIGH | IOZ | -5 | 5 | uA | 1 |
| **Output slew rate:** Single-ended; for rising and falling edges, measure between VOL(AC) = VREF - 0.1 x VccQ and VOH (AC) = VREF + 0.1 x VccQ | SRQSE | 2.5 | 6 | V/ns | 1, 2, 3, 4 |
| **Single-ended DC high-level output voltage** | VOH(DC) | 0.8 x VccQ | | V | 1, 2, 5 |
| **Single-ended DC mid-point level output voltage** | VOM(DC) | 0.5 x VccQ | | V | 1, 2, 5 |
| **Single-ended DC low-point level output voltage** | VOL(DC) | 0.2 x VccQ | | V | 1, 2, 5 |
| **Single-ended DC high-point level output voltage** | VOH(AC) | VTT + 0.1 x VccQ | | V | 1, 2, 3, 6 |
| **Single-ended DC low-point level output voltage** | VOL(AC) | VTT - 0.1 x VccQ | | V | 1, 2, 3, 6 |
| **Delta RON between pull-up and pull-down for DQ/DQS** | MMPUPD | -10 | 10 | % | 1, 7 |
| **Test load for AC timing and output slew rates** | Output to VTT (VccQ/2) via 25Ω resistor | | | | 3 |

NOTES:

1. RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (VccQ = Vcc, VssQ = Vss).
2. VTT = VccQ/2
3. See Figure 31 on page 68 for the test load configuration.
4. The 6V/ns maximum is applicable for a single DQ signal when it is switching from either HIGH to LOW or LOW to HIGH while the remaining DQ signals in the same byte lane are combinations, the maximum limit of 6V/ns maximum is reduced to 5V/ns.
5. See Table 35 on page 40 IV curve linearity. Do not use AC Test load.
6. See Table 47 on page 47 for output slew rate.
7. See Table 35 on page 40 for additional information.
8. See Figure 29 on page 66 for an example of a single-ended output signal.

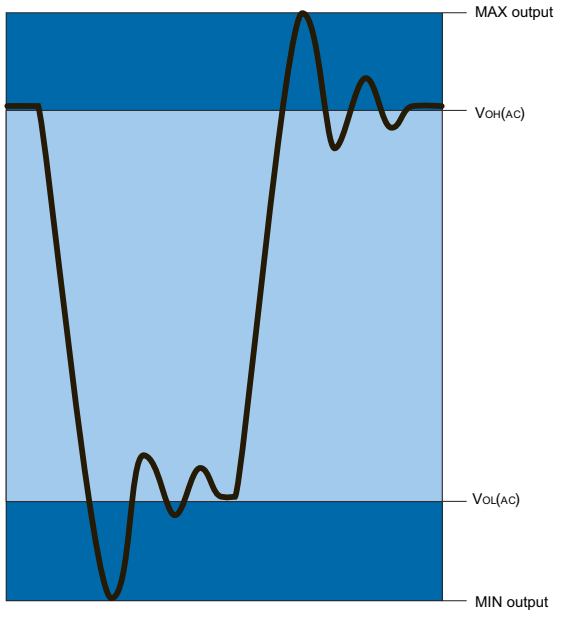
## TABLE 46: DIFFERENTIAL OUTPUT DRIVER CHARACTERISTICS

| Parameter/Condition | Symbol | MIN | MAX | UNITS | NOTES |
|---|---|---|---|---|---|
| **Output leakage current:** DQ are disabled; 0V ≤ VOUT ≤ VccQ; ODT is HIGH | IOZ | -5 | 5 | uA | 1 |
| **Output slew rate:** Differential; for rising and falling edges, measure between VOLDIFF(AC) = - 0.2 x VccQ and VOH (AC) = + 0.2 x VccQ | SRQDIFF | 5 | 12 | V/ns | 1 |
| **Output differential cross-point voltage** | VOX(AC) | VREF-150 | VREF+150 | mV | 1, 2, 3 |
| **Differential high-level output voltage** | VOHDIFF(AC) | + 0.2 x VccQ | | V | 1, 4 |
| **Differential low-level output voltage** | VOLDIFF(AC) | - 0.2 x VccQ | | V | 1, 4 |
| **Delta RON between pull-up and pull-down for DQ/DQS** | MMPUPD | -10 | 10 | % | 1, 5 |
| **Test load for AC timing and output slew rates** | Output to VTT (VccQ/2) via 25Ω resistor | | | | 3 |

NOTES:

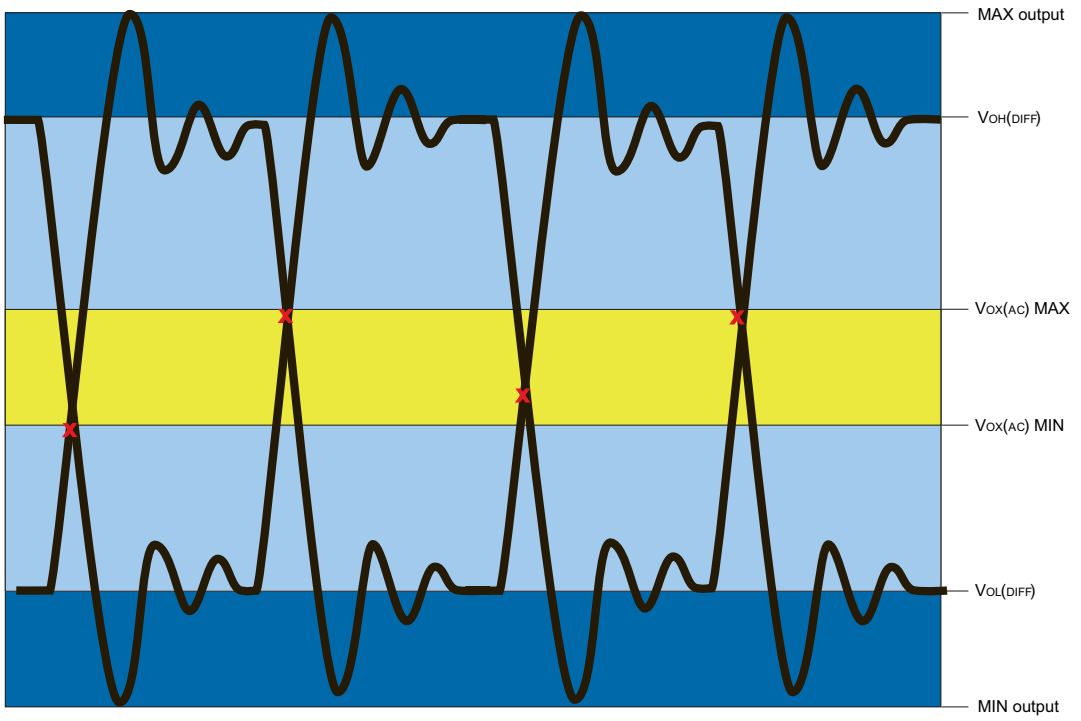
1. RZQ of 240Ω (±1%) with RZQ/7 enabled (default 34Ω driver) and is applicable after proper ZQ calibration has been performed at a stable temperature and voltage (VccQ = Vcc, VssQ = Vss).
2. VREF = VccQ/2
3. See Figure 31 on page 68 for the test load configuration.
4. See Table 48 on page 65 for the output slew rate.
5. See Table 35 on page 58 for additional information.
6. See Figure 30 on page 67 for an example of a differential output signal.

## FIGURE 20 - DQ OUTPUT SIGNAL



## OUTPUT CHARACTERISTICS AND OPERATING CONDITIONS

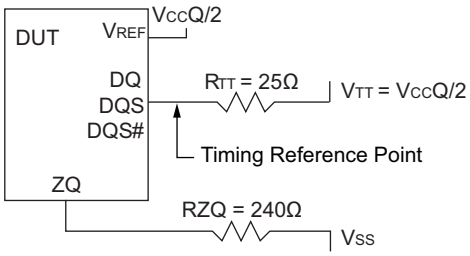
### FIGURE 21 - DIFFERENTIAL OUTPUT SIGNAL




## REFERENCE OUTPUT LOAD

Figure 22 represents the effective reference load of 25Ω used in defining the relevant device AC timing parameters (except ODT reference timing) as well as the output slew rate measurements. It is not intended to be a precise representation of a particular system environment or a depiction of the actual load presented by any specific Industry test system/apparatus. System designers should use IBIS or other simulation tools to correlate the timing reference load presented or exhibited on the system or system environment.

### FIGURE 22 - REFERENCE OUTPUT LOAD FOR AC TIMING AND OUTPUT SLEW RATE



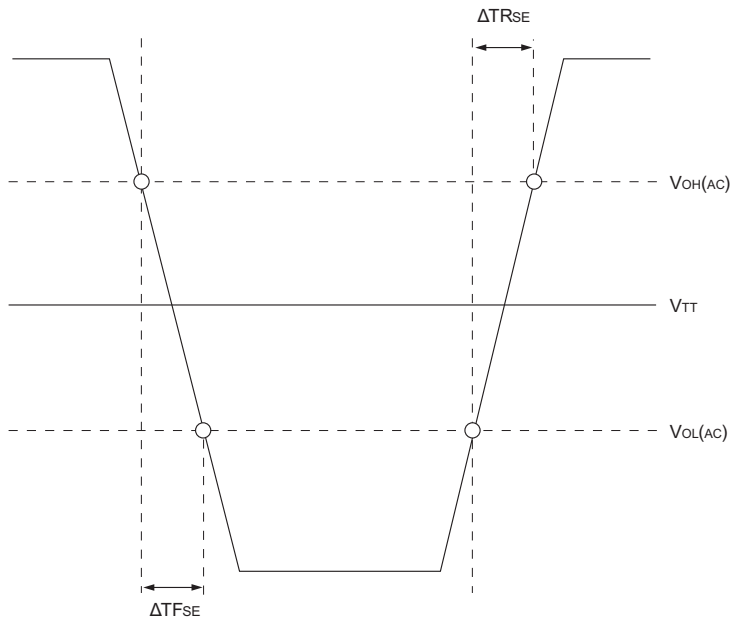
## SLEW RATE DEFINITIONS FOR SINGLE-ENDED OUTPUT SIGNALS

The single-ended output driver is summarized in Table 45. With the reference load for timing measurements, the output slew-rate for falling and rising edges is defined and measured between $V_{OL}(AC)$ and $V_{OH}(AC)$ for single-ended signals as indicated in Table 47 and Figure 23.

### TABLE 47: SINGLE-ENDED OUTPUT SLEW RATE

| Output Slew Rate (Linear Signals) | | Measured | | |
|---|---|---|---|---|
| Output | Edge | From | To | Calculation |
| DQ | Rising | $V_{OL}(AC)$ | $V_{OH}(AC)$ | $\frac{V_{OH}(AC) - V_{OL}(AC)}{\Delta TRSE}$ |
| | Falling | $V_{OH}(AC)$ | $V_{OL}(AC)$ | $\frac{V_{OH}(AC) - V_{OL}(AC)}{\Delta TFSE}$ |

### FIGURE 23 - NOMINAL SLEW RATE DEFINITION FOR SINGLE-ENDED OUTPUT SIGNALS



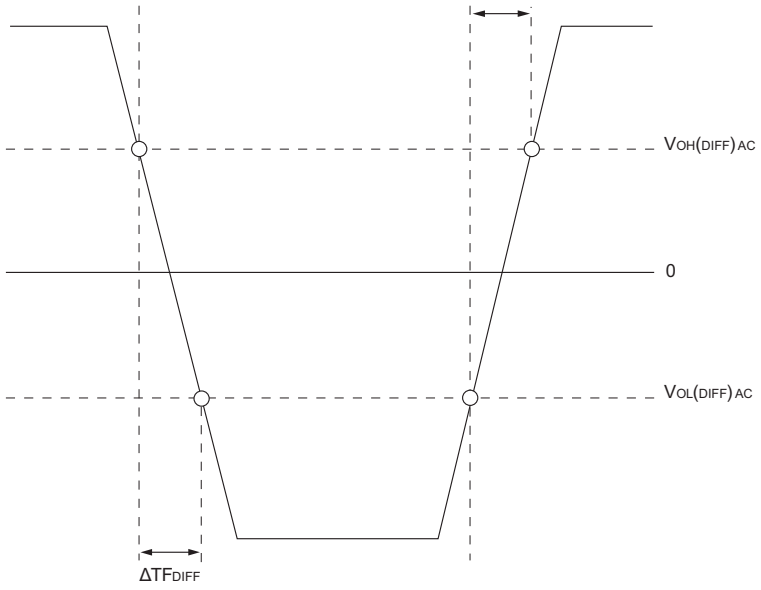
## SLEW RATE DEFINITIONS FOR DIFFERENTIAL OUTPUT SIGNALS

The differential output driver is summarized in Table 46. With the reference load for timing measurements, the output slew rate for falling and rising edges is defined and measured between $V_{OL}$(AC) and $V_{OH}$(AC) for differential signals, as shown in Table 48 and Figure 33.

### TABLE 48: DIFFERENTIAL OUTPUT SLEW RATE DEFINITION

| Output Slew Rate (Linear Signals) | | Measured | | |
|---|---|---|---|---|
| Output | Edge | From | To | Calculation |
| DQS, DQS\ | Rising | $V_{OL}$DIFF(AC) | $V_{OH}$DIFF(AC) | $\frac{V_{OH}DIFF(AC) - V_{OL}DIFF(AC)}{\Delta TRDIFF}$ |
| | Falling | $V_{OH}$DIFF(AC) | $V_{OL}$DIFF(AC) | $\frac{V_{OH}DIFF(AC) - V_{OL}DIFF(AC)}{\Delta TFDIFF}$ |

### FIGURE 24 - NOMINAL DIFFERENTIAL OUTPUT SLEW RATE DEFINITION FOR DQS, DQS#



## TABLE 49: SPEED BINS

| | | | -25 (DDR3-800) [CWL=2.5; 6-6-6] | | -19 (DDR3-1066) [CWL=1.875; 8-8-8] | | -15 (DDR3-1333) [CWL=1.5; 10-10-10] | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| **Parameter** | | **Symbol** | **MIN** | **MAX** | **MIN** | **MAX** | **MIN** | **MAX** | **UNITS** | **NOTES** |
| ACTIVATE to internal READ or WRITE delay time | | $^{t}$RCD | 15 | - | 15 | - | 15 | - | ns | |
| PRECHARGE command period | | $^{t}$RP | 15 | - | 15 | - | 15 | - | ns | |
| ACTIVATE-to-ACTIVATE or REFRESH command period | | $^{t}$RC | 52.5 | - | 52.5 | - | 51 | - | ns | |
| ACTIVATE-to-PRECHARGE command period | | $^{t}$RAS | 37.5 | 60ms | 37.5 | 60ms | 36 | 60ms | ns | 1 |
| CL=5 | CWL=5 | $^{t}$CK (AVG) | 3 | 3.3 | 3 | 3.3 | 3 | 3.3 | ns | 2 |
| | CWL=6 | $^{t}$CK (AVG) | | | | | | | ns | 3 |
| | CWL=7 | $^{t}$CK (AVG) | | | | | | | ns | 3 |
| CL=6 | CWL=5 | $^{t}$CK (AVG) | 2.5 | 3.3 | 2.5 | 3.3 | 2.5 | 3.3 | ns | 2 |
| | CWL=6 | $^{t}$CK (AVG) | | | | | | | ns | 3 |
| | CWL=7 | $^{t}$CK (AVG) | | | | | | | ns | 3 |
| CL=8 | CWL=5 | $^{t}$CK (AVG) | | | | | | | ns | 3 |
| | CWL=6 | $^{t}$CK (AVG) | | | 1.875 | <2.5 | 1.875 | <2 | ns | 2,3 |
| | CWL=7 | $^{t}$CK (AVG) | | | | | | | ns | 3 |
| CL=10 | CWL=5 | $^{t}$CK (AVG) | | | | | | | ns | 3 |
| | CWL=6 | $^{t}$CK (AVG) | | | | | | | ns | 3 |
| | CWL=7 | $^{t}$CK (AVG) | | | | | 1.5 | <1.875 | ns | 2,3 |
| Supported CL Settings | | | 5,6 | | 5, 6, 8 | | 5, 6, 8, 10 | | CK | |
| Supported CWL Settings | | | 5 | | 5, 6 | | 5, 6, 7 | | CK | |

NOTES:

1. $^{t}$REFI depends on $^{t}$OPER
2. The CL and CWL setting result in $^{t}$CK requirements. When making a selection of $^{t}$CK, both CL and CWL requirement settings need to be fulfilled.
3. Reserved (filled blocks) settings are not allowed.

## TABLE 50 (SHEET 1 OF 6) - ELECTRICAL CHARACTERISTICS AND AC OPERATING CONDITIONS

| Parameter | | Symbol | -25 (DDR3-800) [CWL=2.5; 6-6-6] | | -19 (DDR3-1066) [CWL=1.875; 8-8-8] | | -15 (DDR3-1333) [CWL=1.5; 10-10-10] | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| **Clock period average: DLL disable mode** | TC = 0°C to <85°C | $^{t}$CKDLL_DIS | 8 | 7800 | 8 | 7800 | 8 | 7800 | ns | 9,42 |
| | TC = 85°C to 105°C | | 8 | 3900 | 8 | 3900 | 8 | 3900 | | 9,42 |
| | TC = >105°C to ≤125°C | | 8 | 2900 | 8 | 2900 | 8 | 2900 | | 9,42 |
| **Clock period average: DLL enable mode** | | $^{t}$CK (AVG) | See SPEED BIN TABLE (#49) for tCK range allowed | | | | | | ns | 10,11 |
| **HIGH pulse width average** | | $^{t}$CH (AVG) | 0.47 | 0.53 | 0.47 | 0.53 | 0.47 | 0.53 | CK | 12 |
| **LOW pulse width average** | | $^{t}$CL (AVG) | 0.47 | 0.53 | 0.47 | 0.53 | 0.47 | 0.53 | CK | 12 |
| **Clock period JITTER** | DLL LOCKED | $^{t}$JITPER | -100 | 100 | -90 | 90 | -80 | 80 | ps | 13 |
| | DLL LOCKING | $^{t}$JITPER, LCK | -90 | 90 | -80 | 80 | -70 | 70 | ps | 13 |
| **Clock absolute period** | | $^{t}$CLK (ABS) | MIN=$^{t}$CK (AVG) MIN+$^{t}$JITPER MIN; MAX=$^{t}$CK (AVG)MAX+$^{t}$JITPER MAX | | | | | | ps | |
| **Clock absolute HIGH pusle width** | | $^{t}$CH (ABS) | 0.43 | - | 0.43 | - | 0.43 | - | $^{t}$CK (AVG) | 14 |
| **Clock absolute LOW pulse width** | | $^{t}$CL (ABS) | 0.43 | - | 0.43 | - | 0.43 | - | $^{t}$CK (AVG) | 15 |
| **Cycle-to-Cycle JITTER** | DLL LOCKED | $^{t}$JITCC | 200 | | 180 | | 160 | | ps | 16 |
| | DLL LOCKING | $^{t}$JITCC, LCK | 180 | | 160 | | 140 | | ps | 16 |
| **Cumulative error across** | 2 Cycles | $^{t}$ERR2PER | -147 | 147 | -132 | 132 | -118 | 118 | ps | 17 |
| | 3 Cycles | $^{t}$ERR3PER | -175 | 175 | -157 | 157 | -140 | 140 | ps | 17 |
| | 4 Cycles | $^{t}$ERR4PER | -194 | 194 | -175 | 175 | -155 | 155 | ps | 17 |
| | 5 Cycles | $^{t}$ERR5PER | -209 | 209 | -188 | 188 | -168 | 168 | ps | 17 |
| | 6 Cycles | $^{t}$ERR6PER | -222 | 222 | -200 | 200 | -177 | 177 | ps | 17 |
| | 7 Cycles | $^{t}$ERR7PER | -232 | 232 | -209 | 209 | -186 | 186 | ps | 17 |
| | 8 Cycles | $^{t}$ERR8PER | -241 | 241 | -217 | 217 | -193 | 193 | ps | 17 |
| | 9 Cycles | $^{t}$ERR9PER | -249 | 249 | -224 | 224 | -200 | 200 | ps | 17 |
| | 10 Cycles | $^{t}$ERR10PER | -257 | 257 | -231 | 231 | -205 | 205 | ps | 17 |
| | 11 Cycles | $^{t}$ERR11PER | -263 | 263 | -237 | 237 | -210 | 210 | ps | 17 |
| | 12 Cycles | $^{t}$ERR12PER | -269 | 269 | -242 | 242 | -215 | 215 | ps | 17 |
| | n = 13, 14 ... 49, 50 Cycles | $^{t}$ERRnPER | $^{t}$ERRnPER MIN = (1+0.68ln[n]) x $^{t}$JITPER MIN<br>$^{t}$ERRnPER MAX = (1+0.68ln[n]) x $^{t}$JITPER MAX | | | | | | ps | 17 |

## TABLE 50 (SHEET 2 OF 6) - ELECTRICAL CHARACTERISTICS AND AC OPERATING CONDITIONS

| Parameter | | Symbol | -25 (DDR3-800) [CWL=2.5; 6-6-6] | | -19 (DDR3-1066) [CWL=1.875; 8-8-8] | | -15 (DDR3-1333) [CWL=1.5; 10-10-10] | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| **DQ Input Timing** | | | | | | | | | | |
| Data SETUP time to DQS, DQS\ | Base (specification) | $t_{DS}$ AC175 | 75 | - | 25 | - | - | - | ps | 18,19 |
| | VREF @ 1V/ns | | 250 | - | 200 | - | - | - | ps | 19,20 |
| Data SETUP time to DQS, DQS\ | Base (specification) | $t_{DS}$ AC150 | 125 | - | 75 | - | 30 | - | ps | 18,19 |
| | VREF @ 1V/ns | | 275 | - | 250 | - | 180 | - | ps | 19,20 |
| Data HOLD time from DQS, DQS\ | Base (specification) | $t_{DH}$ AC100 | 150 | - | 100 | - | 65 | - | ps | 18,19 |
| | VREF @ 1V/ns | | 250 | - | 200 | - | 165 | - | ps | 19,20 |
| Minimum Data Pulse Width | | $t_{DIPW}$ | 600 | - | 490 | - | 400 | - | ps | 41 |
| **DQ Ouput Timing** | | | | | | | | | | |
| DQS, DQS\ to DQ SKEW, per access | | $t_{DQSQ}$ | - | 200 | - | 150 | - | 125 | ps | |
| DQ Output HOLD time from DQS, DQS\ | | $t_{QH}$ | 0.38 | - | 0.38 | - | 0.38 | - | tCK (AVG) | 21 |
| DQ LOW-Z time from CK, CK\ | | $t_{LZ}$ (DQ) | -800 | 400 | -600 | 300 | -500 | 250 | ps | 22,23 |
| DQ HIGH-A time from CK, CK\ | | $t_{HZ}$ (DQ) | - | 400 | - | 300 | - | 250 | ps | 22,23 |
| **DQ Strobe Input Timing** | | | | | | | | | | |
| DQS,DQS\ RISING to CK, CK\ RISING | | $t_{DQSS}$ | -0.25 | 0.25 | -0.25 | 0.25 | -0.25 | 0.25 | CK | 25 |
| DQS, DQS\ DIFFERENTIAL Input Low pulse width | | $t_{DQSL}$ | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | CK | |
| DQS, DQS\ DIFFERENTIAL Input HIGH pulse width | | $t_{DQSH}$ | 0.45 | 0.55 | 0.45 | 0.55 | 0.45 | 0.55 | CK | |
| DQS, DQS\ FALLING Setup to CK, CK\ RISING | | $t_{DSS}$ | 0.2 | - | 0.2 | - | 0.2 | - | CK | 25 |
| DQS, DQS\ FALLING Hold from CK, CK\ RISING | | $t_{DSH}$ | 0.2 | - | 0.2 | - | 0.2 | - | CK | 25 |
| DQS, DQS\ DIFFERENTIAL WRITE preamble | | $t_{WPRE}$ | 0.9 | - | 0.9 | - | 0.9 | - | CK | |
| DQS, DQS\ DIFFERENTIAL WRITE postamble | | $t_{WPST}$ | 0.3 | - | 0.3 | - | 0.3 | - | CK | |
| **DQ Strobe Output Timing** | | | | | | | | | | |
| DQS, DQS\ RISING to/from RISING CK, CK\ | | $t_{DQSCK}$ | -400 | 400 | -300 | 300 | -255 | 255 | ps | 23 |
| DQS, DQS\ RISING to/from RISING CK, CK\ when DLL is disabled | | $t_{DQSK}$ DLL_DIS | 1 | 10 | 1 | 10 | 1 | 10 | ns | 26 |
| DQS, DQS\ DIFFERENTIAL Output HIGH time | | $t_{QSH}$ | 0.38 | - | 0.38 | - | 0.4 | - | CK | 21 |
| DQS, DQS\ DIFFERENTIAL Output LOW time | | $t_{QSL}$ | 0.38 | - | 0.38 | - | 0.4 | - | CK | 21 |
| DQS, DQS\ LOW-Z time (RL-1) | | $t_{LZ}$ (DQS) | -800 | 400 | -600 | 300 | -500 | 250 | ps | 22,23 |
| DQS, DQS\ HIGH-Z time (RL+BL/2) | | $t_{HZ}$ (DQS) | - | 400 | - | 300 | - | 250 | ps | 22,23 |
| DQS, DQS\ DIFFERENTIAL READ preamble | | $t_{RPRE}$ | 0.9 | Note 24 | 0.9 | Note 24 | 0.9 | Note 24 | CK | 23,24 |
| DQS, DQS\ DIFFERENTIAL READ postamble | | $t_{RPST}$ | 0.3 | Note 27 | 0.3 | Note 27 | 0.3 | Note 27 | CK | 23,27 |

## TABLE 50 (SHEET 3 OF 6) - ELECTRICAL CHARACTERISTICS AND AC OPERATING CONDITIONS

| Parameter | | | Symbol | -25 (DDR3-800) [CWL=2.5; 6-6-6] | | -19 (DDR3-1066) [CWL=1.875; 8-8-8] | | -15 (DDR3-1333) [CWL=1.5; 10-10-10] | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| **Command and Address Timing** | | | | | | | | | | | |
| **DLL Locking time** | | | tDLLK | 512 | - | 512 | - | 512 | - | CK | 28 |
| **CTRL, CMD, ADDR setup to CK, CK** | | Base (specification) | tIS AC175 | 200 | - | 125 | - | 65 | - | ps | 29,30 |
| | | VREF @ 1V/ns | | 375 | - | 300 | - | 240 | - | ps | 20,30 |
| **CTRL, CMD, ADDR setup to CK, CK** | | Base (specification) | tIS AC150 | 350 | - | 275 | - | 190 | - | ps | 29,30 |
| | | VREF @ 1V/ns | | 500 | - | 425 | - | 340 | - | ps | 20,30 |
| **CTRL, CMD, ADDR hold to CK, CK** | | Base (specification) | tIH DC100 | 275 | - | 200 | - | 140 | - | ps | 29,30 |
| | | VREF @ 1V/ns | | 375 | - | 300 | - | 240 | - | ps | 20,30 |
| **Minimum CTRL, CMD, ADDR pulse width** | | | tPW | 900 | - | 780 | - | 620 | - | ps | 41 |
| **ACTIVATE to Internal READ or WRITE delay** | | | tRCD | See "Speed Bin Table (#49) for tRCD | | | | | | ns | 31 |
| **PRECHARGE command period** | | | tRP | See "Speed Bin Table (#49) for tRP | | | | | | ns | 31 |
| **ACTIVATE-to-PRECHARGE command period** | | | tRAS | See "Speed Bin Table (#49) for tRAS | | | | | | ns | 31,32 |
| **ACTIVATE-to-ACTIVATE command period** | | | tRCD | See "Speed Bin Table (#49) for tRC | | | | | | ns | 31 |
| **ACTIVATE-to-ACTIVATE minimum command period** | 1KB page size | | tRRD | MIN=greater of 4CK or 10ns | | MIN=greater of 4CK or 7.5ns | | MIN=greater of 4CK or 6ns | | CK | 31 |
| | 2KB page size | | | MIN=greater of 4CK or 10ns | | | | MIN=greater of 4CK or 6ns | | CK | 31 |
| **Four ACTIVATE windows for 1KB page size** | | | tFAW | 40 | - | 37.5 | - | 30 | - | ns | 31 |
| **Four ACTIVATE windows for 2KB page size** | | | | 50 | - | 50 | - | 45 | - | ns | 31 |
| **WRITE recovery time** | | | tWR | MIN = 15ns; MAX = n/a | | | | | | CK | 31,32,33 |
| **Delay from start of internal WRITE transaction to internal READ command** | | | tWTR | MIN = greater of 4CK or 7.5ns; MAX = n/a | | | | | | CK | 31,34 |
| **READ-to-PRECHARE time** | | | tRTP | MIN = greater of 4CK or 7.5ns; MAX = n/a | | | | | | CK | |
| **CAS\-to-CAS\ command delay** | | | tCCD | MIN = 4CK; MAX = n/a | | | | | | CK | |
| **Auto precharge WRITE recovery + PRECHARGE time** | | | tDAL | MIN = WR + tRP/tCK (AVG); MAX = n/a | | | | | | CK | |
| **MODE REGISTER SET command cycle time** | | | tMRD | MIN = 4CK; MAX = n/a | | | | | | CK | |
| **MODE REGISTER SET command update delay** | | | tMOD | MIN = greater of 12CK or 15ns; MAX = n/a | | | | | | CK | |
| **MULTIPURPOSE REGISTER READ burst end to mode register set for multipurpose register exit** | | | tMPRR | MIN = 1CK; MAX = n/a | | | | | | CK | |

## TABLE 50 (SHEET 4 OF 6) - ELECTRICAL CHARACTERISTICS AND AC OPERATING CONDITIONS

| Parameter | | Symbol | -25 (DDR3-800) [CWL=2.5; 6-6-6] | | -19 (DDR3-1066) [CWL=1.875; 8-8-8] | | -15 (DDR3-1333) [CWL=1.5; 10-10-10] | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| **Calibration Timing** | | | | | | | | | | |
| **ZQCL command: Long Calibration time** | POWER-UP and RESET operation | $^{t}$ZQINIT | 512 | - | 512 | - | 512 | - | CK | |
| | Normal operation | $^{t}$ZQOPER | 256 | - | 256 | - | 256 | - | CK | |
| **ZQCS command: Short Calibration Time** | | $^{t}$ZQCS | 64 | - | 64 | - | 64 | - | CK | |
| **Initialization and RESET Timing** | | | | | | | | | | |
| **Exit RESET from CKE HIGH to a valid command** | | $^{t}$XPR | MIN = greater of 5CK or tRFC + 10ns; MAX = n/a | | | | | | CK | |
| **Begin power supply ramp to power supplies stable** | | $^{t}$VDDPR | MIN = n/a; MAX = 200 | | | | | | ms | |
| **RESET\ LOW to power supplies stable** | | $^{t}$RPS | MIN = 0; MAX = 200 | | | | | | ms | |
| **RESET\ LOW to I/O and RTT HIGH-Z** | | $^{t}$IOZ | MIN = n/a; MAX = 200 | | | | | | ns | 35 |
| **REFRESH Timing** | | | | | | | | | | |
| **REFRESH-to-ACTIVATE or REFRESH command period** | | $^{t}$RFC | MIN = 110; MAX = 9 x $^{t}$REFI | | | | | | ns | |
| **Maximum REFRESH period** | TC ≤ 85°C | - | 64 | | | | | | ms | 36 |
| | TC >85°C ≤ 105°C | | 32 | | | | | | ms | 36 |
| | TC >105°C ≤ 125°C | | 24 | | | | | | ms | 36 |
| **Maximum REFRESH period/interval** | TC ≤ 85°C | $^{t}$REFI | 7.8 | | | | | | µs | 36 |
| | TC >85°C ≤ 105°C | | 3.9 | | | | | | µs | 36 |
| | TC >105°C ≤ 125°C | | 2.9 | | | | | | µs | 36 |
| **SELF REFRESH Timing** | | | | | | | | | | |
| **Exit SELF REFRESH TO commands not requiring a locked DLL** | | $^{t}$XS | MIN = greater of 5CK or $^{t}$RFC + 10ns; MAX = n/a | | | | | | CK | |
| **EXIT SELF REFRESH TO commands requiring a locked DLL** | | $^{t}$XSDLL | MIN = $^{t}$DLLK (MIN); MAX = n/a | | | | | | CK | 28 |
| **MINIMUM CKE LOW pulse width for SELF REFRESH entry to SELF REFRESH exit timing** | | $^{t}$CKESR | MIN = $^{t}$CKE (MIN) + CK; MAX = n/a | | | | | | CK | |
| **Valid clocks after SELF REFRESH entry or POWER-DOWN entry** | | $^{t}$CKSRE | MIN = greater of 5CK or 10ns; MAX = n/a | | | | | | CK | |
| **Valid clocks before SELF REFRESH exit, POWER-DOWN exit, or RESET exit** | | $^{t}$CKSRX | MIN = greater of 5CK or 10ns; MAX = n/a | | | | | | CK | |

## TABLE 50 (SHEET 5 OF 6) - ELECTRICAL CHARACTERISTICS AND AC OPERATING CONDITIONS

| Parameter | | Symbol | -25 (DDR3-800) [CWL=2.5; 6-6-6] | | -19 (DDR3-1066) [CWL=1.875; 8-8-8] | | -15 (DDR3-1333) [CWL=1.5; 10-10-10] | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| **POWER-DOWN Timing** | | | | | | | | | | |
| CKE MIN pulse width | | tCKE (MIN) | Greater of 3CK or 7.5ns | | Greater of 3CK or 5.625ns | | Greater of 3CK or 5.625ns | | CK | |
| Command pass disable delay | | tCPDED | MIN = 1; MAX = n/a | | | | | | CK | |
| POWER-DOWN entry to POWER-DOWN exit timing | | tPD | MIN = tCKE (MIN); MAX = 60ms | | | | | | CK | |
| Begin POWER-DOWN period prior to CKE registered HIGH | | tANPD | WL - 1CK | | | | | | CK | |
| POWER-DOWN entry period: ODT either synchronous or asynchronous | | PDE | Greater of tANPD or tRFC - REFRESH command to CKE LOW time | | | | | | CK | |
| POWER-DOWN exit period: ODT either synchronous or asynchronous | | PDX | tANPD + tXPDLL | | | | | | CK | |
| **POWER-DOWN Entry MINIMUM Timing** | | | | | | | | | | |
| ACTIVATE command to POWER-DOWN entry | | tACTPDEN | MIN = 1 | | | | | | CK | |
| PRECHARGE/PRECHARGE ALL command to POWER-DOWN entry | | tPRPDEN | MIN = 1 | | | | | | CK | |
| REFRESH command to POWER-DOWN entry | | tREFPDEN | MIN = 1 | | | | | | CK | 37 |
| MRS command to POWER-DOWN entry | | tMRSPDEN | MIN = tMOD (MIN) | | | | | | CK | |
| READ/READ with AUTO PRECHARGE command to POWER-DOWN entry | | tRDPDEN | MIN = RL + 4 + 1 | | | | | | CK | |
| WRITE Command to POWER-DOWN entry | BL8 (OTF, MRS) BC4OTF | tWRPDEN | MIN = WL + 4 + tWR/tCK (AVG) | | | | | | CK | |
| | BC4MRS | tWRPDEN | MIN = WL + 2 + tWR/tCK (AVG) | | | | | | CK | |
| WRITE with AUTO PRECHARGE command to POWER-DOWN entry | BL8 (OTF, MRS) BC4OTF | tWRAPDEN | MIN = WL + 4 + WR + 1 | | | | | | CK | |
| | BC4MRS | tWRAPDEN | MIN = WL + 2 + WR + 1 | | | | | | CK | |
| **POWER-DOWN Exit Timing** | | | | | | | | | | |
| DLL on, any valid command, or DLL off to commands not requiring DLL locked | | tXP | MIN = Greater of 3CK or 7.5ns; MAX = n/a | | | | | MIN = Greater of 3CK or 6ns; MAX = n/a | CK | |
| PRECHARGE POWER-DOWN with DLL off to command requiring DLL locked | | tXPDLL | MIN = Greater of 10CK or 24ns; MAX = n/a | | | | | | CK | 28 |

## TABLE 50 (SHEET 6 OF 6) - ELECTRICAL CHARACTERISTICS AND AC OPERATING CONDITIONS

| Parameter | Symbol | -25 (DDR3-800) [CWL=2.5; 6-6-6] | | -19 (DDR3-1066) [CWL=1.875; 8-8-8] | | -15 (DDR3-1333) [CWL=1.5; 10-10-10] | | Units | Notes |
|---|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | | |
| **ODT Timing** | | | | | | | | | |
| RTT synchronous TURN-ON delay | ODTL on | | | | | | | CK | 38 |
| RTT synchronous TURN-OFF delay | ODTL off | | | | | | | CK | 40 |
| RTT TURN-ON from ODTL ON reference | $^{t}$AON | -400 | 400 | -300 | 300 | -250 | 250 | ps | 23,38 |
| RTT TURN-OFF from ODTL OFF reference | $^{t}$AOF | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | CK | 39,40 |
| Asynchronous RTT TURN-ON delay (POWER-DOWN with DLL OFF) | $^{t}$AONPD | MIN = 2; MAX = 8.5 | | | | | | ns | 38 |
| Asynchronous RTT TURN-OFF delay (POWER-DOWN with DLL OFF) | $^{t}$AOFPD | MIN = 2; MAX = 8.5 | | | | | | ns | 40 |
| ODT HIGH time without WRITE command or with WRITE command and BC8 | $ODT_{H8}$ | MIN = 6; MAX = n/a | | | | | | CK | |
| ODT HIGH time without WRITE command or with WRITE command and BC4 | $ODT_{H4}$ | MIN = 4; MAX = n/a | | | | | | CK | |
| **Dynamic ODT Timing** | | | | | | | | | |
| RTT_NOM-to=RTT_WR change skew | $ODTL_{CNW}$ | WL - 2CK | | | | | | CK | |
| RTT_WR-to-RTT_NOM change skew - BC4 | $ODTL_{CNW4}$ | 4CK + ODTL OFF | | | | | | CK | |
| RTT_WR-to-RTT_NOM change skew - BC8 | $ODTL_{CNW8}$ | 6CK + ODTL OFF | | | | | | CK | |
| RTT dynamic change skew | $^{t}$ADC | 0.3 | 0.7 | 0.3 | 0.7 | 0.3 | 0.7 | CK | 39 |
| **WRITE Leveling Timing** | | | | | | | | | |
| First DQS, DQS\ RISING edge | $^{t}$WLMRD | 40 | - | 40 | - | 40 | - | CK | |
| DQS; DQS\ delay | $^{t}$WLDQSEN | 25 | - | 25 | - | 25 | - | CK | |
| WRITE Leveling SETUP from rising CK, CK\ crossing to rising DQS, DQS\ crossing | $^{t}$WLS | 325 | - | 245 | - | 195 | - | ps | |
| WRITE Leveling HOLD from rising DQS, DQS\ crossing to rising CK, CK\ crossing | $^{t}$WLH | 325 | - | 245 | - | 195 | - | ps | |
| WRITE Leveling output delay | $^{t}$WLO | 0 | 9 | 0 | 9 | 0 | 9 | ns | |
| WRITE Leveling output error | $^{t}$WLOE | 0 | 2 | 0 | 2 | 0 | 2 | ns | |

## NOTES

1. Parameters are applicable with 0˚C ≤ Tc ≤ +95˚C and Vcc/VccQ = + 1.5V ± 0.075V.
2. All voltages are referenced to Vss.
3. Output timings are only valid for RON34 output buffer selection.
4. Unit $^{t}$CK (AVG) represents the actual $^{t}$CK (AVG) of the input clock under operation. Unit CK represents one clock cycle of the input clock, counting the actual clock edges.
5. AC timing and ICC tests may use a VIL-to-VIH swing of up to 900mV I the test environment, but input timing is still referenced to VREF (except $^{t}$IS, $^{t}$IH, $^{t}$DS, and $^{t}$DH use the AC/DC trip points and CK, CK\ and DQS, DQS\ use their crossing points). The minimum slew rate for the input signals used to test the device is 1V/ns for single-ended inputs and 2V/ ns for differential inputs in the range between VIL (AC) and VIH (AC).
6. All timings that use time-based values (ns, µs, ms) should use $^{t}$CK (AVG) to determine the correct number of clocks (Table 50 uses CK or CK (AVG) interchangeably). In the case of non-interger results, all minimum limits are to be rounded up to the nearest whole integer.
7. The use of STROBE or DQSDIFF refers to the DQS and DQS\ differential crossing point when DQS is the rising edge. The use of CLOCK or CK refers to the CK and CK\ differential crossing point when CK is the rising edge.
8. This output load is used for all AC timing (except ODT reference timing) and slew rates. The actual test load may be different. The output signal voltage reference point is VccQ/2 for single-ended signals and the crossing point for differential signals.
9. When operating in DLL disable mode, LOGIC Devices, Inc. (LDI) does not warrant compliance with normal mode timings or functionality.
10. The clock's $^{t}$CK (AVG) is the average clock over any 200 consecutive clocks and $^{t}$CK (AVG) MIN is the smallest clock rate allowed, with the exception of a deviation due to clock jitter. Input clock jitter is allowed provided it does not exceed values specified and must be of a random Gaussian distribution in nature.
11. Spread spectrum is not included in the jitter specification values. However, the input clock can accommodate spread-spectrum at a sweep rate in the range of 20-60kHz with and additional 1% of $^{t}$CK (AVG) as a long-term jitter component; however, the spread-spectrum may not use a clock rate below $^{t}$CK (AVG) MIN.
12. The clock's $^{t}$CH (AVG) and $^{t}$CL (AVG) are the average half clock period over any 200 consecutive clocks and is the smallest clock half period allowed, with the exception of values specified and must of a random Gaussian distribution in nature.
13. The period jitter ($^{t}$JITPER) is the maximum deviation in the clock period from the average or nominal clock. It is allowed in either the positive or negative direction.
14. $^{t}$CH (ABS) is the absolute instantaneous clock high pulse width as measured from one rising edge to the following falling edge.
15. $^{t}$CL (ABS) is the absolute instantaneous clock low pulse width as measured from one falling edge to the following rising edge.
16. The cycle-to-cycle jitter ($^{t}$JITCC) is the amount the clock period can deviate from one cycle to the next. It is important to keep cycle-to-cycle jitter at a minimum during the DLL locking time.
17. The cumulative jitter error ($^{t}$ERRnPER), where n is the number of clocks between 2 and 50, is the amount of clock time allowed to accumulate consecutively away from the average clock over n number of clock cycles.
18. $^{t}$DS (base) and $^{t}$DH (base) values are for a single-ended 1V/ns DQ slew rate and 2V/ns for differential DQS, DQS\ slew rate.
19. These parameters are measured from a data signal (DM, DQ0, DQ1 … DQn and so forth) transition edge to its respective data strobe signal (DQS, DQS\) crossing.
20. The setup and hold times are listed converting the base specification values (to which derating tables apply) to VREF when the slew rate is 1V/ns. These values, with a slew rate of 1V/ns are for reference only.
21. When the device is operated with input clock jitter, this parameter needs to be derated by the actual $^{t}$JITPER (larger of $^{t}$JITPER (MIN) or $^{t}$JITPER (MAX) of the input clock (output deratings are relative to the SDRAM input clock).
22. Single-ended signal parameter.
23. The SDRAM output timing is aligned to the nominal or average clock. Most output parameters must be derated by the actual jitter error when input clock jitter is present, even when within specification. This results in each parameter becoming larger. The following parameters are required to be derated by subtracting $^{t}$ERR10PER (MAX); $^{t}$DQSCK (MIN), $^{t}$LZ (DQS) MAX, $^{t}$LZ (DQ) MAX, and $^{t}$AON (MAX). The parameter $^{t}$RPRE (MIN) is derated by subtracting $^{t}$JITPER (MAX), while $^{t}$RPRE (MAX) is derated by $^{t}$JITPER (MIN).
24. The maximum preamble is bound by $^{t}$LZDQS (MAX).
25. These parameters are measured from a data strobe signal (DQS, DQS\) crossing to its respective clock signal (CK, CK\) crossing. The specification values are not affected by the amount of clock jitter applied, as these are relative to the clock signal crossing. These parameters should be met whether clock jitter is present or not.
26. The $^{t}$DQSCK DLL_DIS parameter begins CL + AL - 1 cycles after the READ command.
27. The maximum postamble is bound by $^{t}$HZDQS (MAX).
28. Commands requiring a locked DLL are: READ (and RDAP) and synchronous ODT commands. In addition, after any change of latency $^{t}$XPDLL, timing must be met.
29. $^{t}$IS (base) and $^{t}$IH (base) values are for a single-ended 1 V/ns control/command/ address slew rate and 2 V/ns CK, CK# differential slew rate.
30. These parameters are measured from a command/address signal transition edge to its respective clock (CK, CK\) signal crossing. The specification values are not affected by the amount of clock jitter applied as the setup and hold times are relative to the clock signal crossing that latches the command/address. These parameters should be met whether clock jitter is present or not.
31. For these parameters, the DDR3 SDRAM device supports tnPARAM (nCK) = RU ($^{t}$PARAM [ns]/ $^{t}$CK[AVG][ns]), assuming all input clock

## NOTES CONTINUED

jitter specifications are satisfied. For example, the device will support $^{t}$nRP (nCK) = RU ($^{t}$RP)/$^{t}$CK[AVG]) if all input clock jitter specifications are met. This means for DDR2-800; 6-6-6, of which $^{t}$RP = 15ns, the device will support $^{t}$nRP = RU ($^{t}$RP/$^{t}$CK [AVG]) = 6 as long as the input clock jitter specifications are met. That is, the PRECHARGE command at T0 and the ACTIVATE command at T0+6 are valid even if six clocks are less than 15ns due to input clock jitter.

32. During READs and WRITEs with AUTO PRECHARGE, the DDR3 SDRAM will hold off the internal PRECHARGE command until $^{t}$RAS (MIN) has been satisfied.

33. When operating in DLL disable mode, the greater of 4CK or 15ns is satisfied for $^{t}$WR.

34. The start of the write recovery time is defined as follows:

    - For BL8 (fixed by MRS and OTF): Rising clock edge four clock cycles after WL.
    - For BC4 (OTF): Rising clock edge four clock cycles after WL.
    - For BC4 (fixed by MRS): Rising clock edge two clock cycles after WL.

35. RESET\ should be LOW as soon as power starts to ramp to ensure the outputs are in HIGH-Z Until RESET\ is LOW, the outputs are at risk of driving the bus and could result in excessive current, depending on the bus activity.

36. The refresh period is 64ms when Tc is less than or equal to 85˚C. This equates to an average refresh rate of 7.8124µs. However, nine REFRESH commands should be asserted at least once every 70.3µs. When Tc is greater than 85˚C, the refresh period is 32ms and when Tc is greater than 105˚C, the refresh period is 24ms.

37. Although CKE is allowed to be registered LOW after a REFRESH command when $^{t}$REFPDEN (MIN) is satisfied, there are cases where additional time such as $^{t}$XPDLL (MIN) is required.

38. ODT turn-on time MIN is when the device leaves HIGH-Z and ODT resistance begins to turn on. ODT turn-on time maximum is when the ODT resistance is fully on. The ODT reference load is shown in Figure 23.

39. Half-clock output parameters must derated by the actual $^{t}$ERR10PER and $^{t}$JITDTY when input clock jitter is present. This results in each parameter becoming larger. The parameters $^{t}$ADC (MIN) and $^{t}$AOF(MIN) are each required to be derated by subtracting both tERR10PER (MAX) and $^{t}$JITDTY (MAX). The parameters $^{t}$ADC (MAX) and $^{t}$AOF (MAX) are required to be derated by subtracting both $^{t}$ERR10PER (MAX) and $^{t}$JITDTY (MAX).

40. ODT turn-off time minimum is when the device starts to turn off ODT resistance. ODT turn-off time maximum is when the SDRAM buffer is in HIGH-Z. The ODT reference load is shown in Figure 24. This output load is used for ODT timings (see Figure 31).

41. Pulse width of an input signal is defined as the width between the first crossing of VREF (DC) and the consecutive crossing of VREF(DC).

42. Should the clock rate be larger than $^{t}$RFC(MIN), an AUTO REFRESH command should have at least one NOP command between it and another AUTO REFRESH command. Additionally, if the clock rate is slower than 40ns (25MHz) all REFRESH commands should be followed by a PRECHARGE ALL command.

## COMMAND AND ADDRESS SETUP, HOLD, AND DERATING

The total $^{t}$IS (setup time) and $^{t}$IH (hold time) required is calculated by adding the data sheet $^{t}$IS(base) and $^{t}$IH (base) values (Tables 51) to the $\Delta^{t}$IS and $\Delta^{t}$IH derating values (Table 52), respectively.

Although the total setup time for slow slew rates might be negative, a valid input signal is still required to complete the transition and to reach VIH(AC)/VIL(AC) (see Figure 14 for input signal requirements). For slew rates which fall between the values listed in Table 52 and Table 53, the derating values may be obtained by linear interpolation.

Setup ($^{t}$IS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIH(AC) MIN. Setup ($^{t}$IS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VREF(DC) and the first crossing of VIL(AC) MAX. If the actual signal is always earlier than the nominal slew rate line between the shaded "VREF(DC)-to-AC region", use the nominal slew rate for derating value (see Figure 25). If the actual signal is later than the nominal slew rate line anywhere between the shaded "VREF(DC)-to-AC region", the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for the derating value (see Figure 27).

Hold ($^{t}$IH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of VIL(DC) MAX and the first crossing of VREF(DC). Hold ($^{t}$IH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of VIH(DC) MIN and the first crossing of VREF(DC). If the actual signal is always later than the nominal slew rate line between the shaded "DC-to-VREF(DC) region", use the nominal slew rate for derating value (see Figure 26). If the actual signal is earlier than the nominal slew rate line anywhere between the shaded "DC-to-VREF(DC) region", the slew rate of a tangent line to the actual signal from the DC level to the VREF(DC) level is used for the derating value (see Figure 28).

**TABLE 51: COMMAND AND ADDRESS SETUP AND HOLD VALUES REFERENCED AT 1V/NS – AC/DC BASED**

| Symbol | DDR3-800 | DDR3-1066 | DDR3-1333 | UNITS | REFERENCE |
|---|---|---|---|---|---|
| $^{t}$IS(base)AC175 | 200 | 125 | 65 | ps | VIH(AC)/VIL(AC) |
| $^{t}$IS(base)AC150 | 350 | 275 | 190 | ps | VIH(AC)/VIL(AC) |
| $^{t}$IH(base)DC100 | 275 | 200 | 140 | ps | VIH(AC)/VIL(AC) |

**TABLE 52: DERATING VALUES FOR $^{t}$IS/$^{t}$IH – AC175/DC100-BASED**

*Shaded cells indicate slew-rate combinations not supported*

**$\Delta^{t}$IS, $\Delta^{t}$IH Derating (ps) - AC/DC-Based, AC175 Threshold; VIH(AC) = VREF(DC) + 175mV, VIL(AC) = VREF(DC) - 175mV**

| CMD/ADDR Slew Rate V/ns | CK, CK\ Differential Slew Rate | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 4.0V/ns | | 3.0V/ns | | 2.0V/ns | | 1.8V/ns | | 1.6V/ns | | 1.4V/ns | | 1.2V/ns | | 1.0V/ns | |
| | $\Delta^{t}$IS | $\Delta^{t}$IH | $\Delta^{t}$IS | $\Delta^{t}$IH | $\Delta^{t}$IS | $\Delta^{t}$IH | $\Delta^{t}$IS | $\Delta^{t}$IH | $\Delta^{t}$IS | $\Delta^{t}$IH | $\Delta^{t}$IS | $\Delta^{t}$IH | $\Delta^{t}$IS | $\Delta^{t}$IH | $\Delta^{t}$IS | $\Delta^{t}$IH |
| 2.0 | 88 | 50 | 88 | 50 | 88 | 50 | 96 | 58 | 96 | 66 | 112 | 74 | 120 | 84 | 128 | 100 |
| 1.5 | 59 | 34 | 50 | 34 | 59 | 34 | 67 | 42 | 67 | 50 | 83 | 58 | 91 | 68 | 99 | 84 |
| 1.0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 8 | 16 | 24 | 24 | 32 | 34 | 40 | 50 |
| 0.9 | -2 | -4 | -2 | -4 | -2 | -4 | 6 | 4 | 6 | 12 | 22 | 20 | 30 | 30 | 38 | 46 |
| 0.8 | -6 | -10 | -6 | -10 | -6 | -10 | 2 | -2 | 2 | 6 | 18 | 14 | 26 | 24 | 34 | 40 |
| 0.7 | -11 | -16 | -11 | -16 | -11 | -16 | -3 | -8 | -3 | 0 | 13 | 8 | 21 | 18 | 29 | 34 |
| 0.6 | -17 | -26 | -17 | -26 | -17 | -26 | -9 | -18 | -9 | -10 | 7 | -2 | 15 | 8 | 23 | 24 |
| 0.5 | -35 | -40 | -35 | -40 | -35 | -40 | -27 | -32 | -27 | -24 | -11 | -16 | -2 | -6 | 5 | 10 |
| 0.4 | -62 | -60 | -62 | -60 | -62 | -60 | -54 | -52 | -54 | -44 | -38 | -36 | -30 | -26 | -22 | -10 |

## Table 53: Derating Values for tIS/tIH – AC150/DC100-Based

*Shaded cells indicate slew-rate combinations not supported*

**ΔtIS, ΔtIH Derating (ps) - AC/DC-Based, AC150 Threshold; VIH(AC) = VREF(DC) + 150mV, VIL(AC) = VREF(DC) - 150mV**

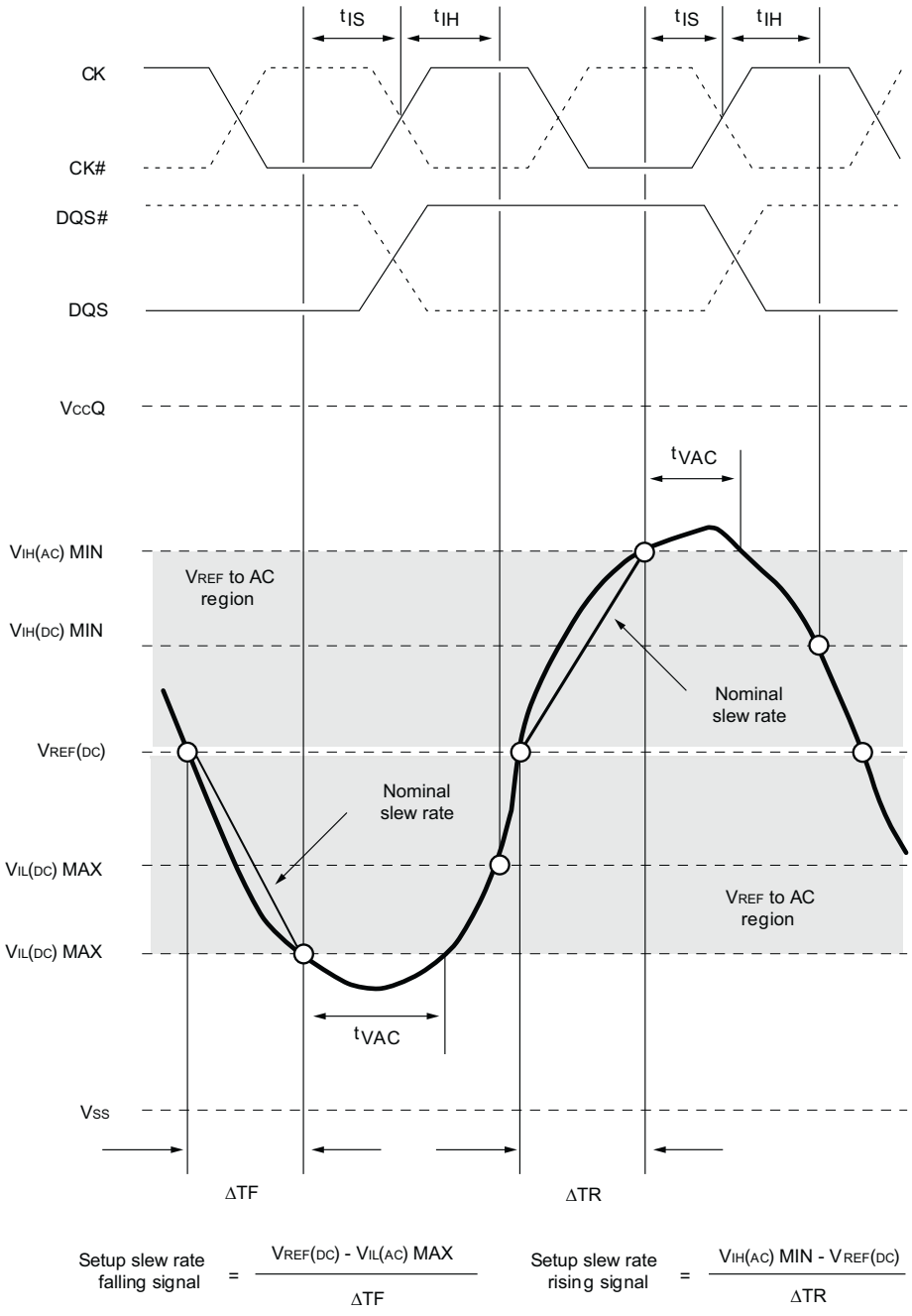
| CMD/ADDR Slew Rate V/ns | CK, CK\ Differential Slew Rate | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 4.0V/ns | | 3.0V/ns | | 2.0V/ns | | 1.8V/ns | | 1.6V/ns | | 1.4V/ns | | 1.2V/ns | | 1.0V/ns | |
| | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH | ΔtIS | ΔtIH |
| 2.0 | 75 | 50 | 75 | 50 | 75 | 50 | 83 | 58 | 91 | 66 | 99 | 74 | 107 | 84 | 115 | 100 |
| 1.5 | 50 | 34 | 50 | 34 | 50 | 34 | 58 | 42 | 66 | 50 | 74 | 58 | 82 | 68 | 90 | 84 |
| 1.0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 16 | 16 | 24 | 24 | 32 | 34 | 40 | 50 |
| 0.9 | 0 | -4 | 0 | -4 | 0 | -4 | 8 | 4 | 16 | 12 | 24 | 20 | 32 | 30 | 40 | 46 |
| 0.8 | 0 | -10 | 0 | -10 | 0 | -10 | 8 | -2 | 16 | 6 | 24 | 14 | 32 | 24 | 40 | 40 |
| 0.7 | 0 | -16 | 0 | -16 | 0 | -16 | 8 | -8 | 16 | 0 | 24 | 8 | 32 | 18 | 40 | 34 |
| 0.6 | -1 | -26 | -1 | -26 | -1 | -26 | 7 | -18 | 15 | -10 | 23 | -2 | 31 | 8 | 39 | 24 |
| 0.5 | -10 | -40 | -10 | -40 | -10 | -40 | -2 | -32 | 6 | -24 | 14 | -16 | 22 | -6 | 30 | 10 |
| 0.4 | -25 | -60 | -25 | -60 | -25 | -60 | -17 | -52 | -9 | -44 | -1 | -36 | 7 | -26 | 15 | -10 |

## Table 54: Minimum Required Time tVAC above VIH(AC) for a Valid Transition

*Below VIL(AC)*

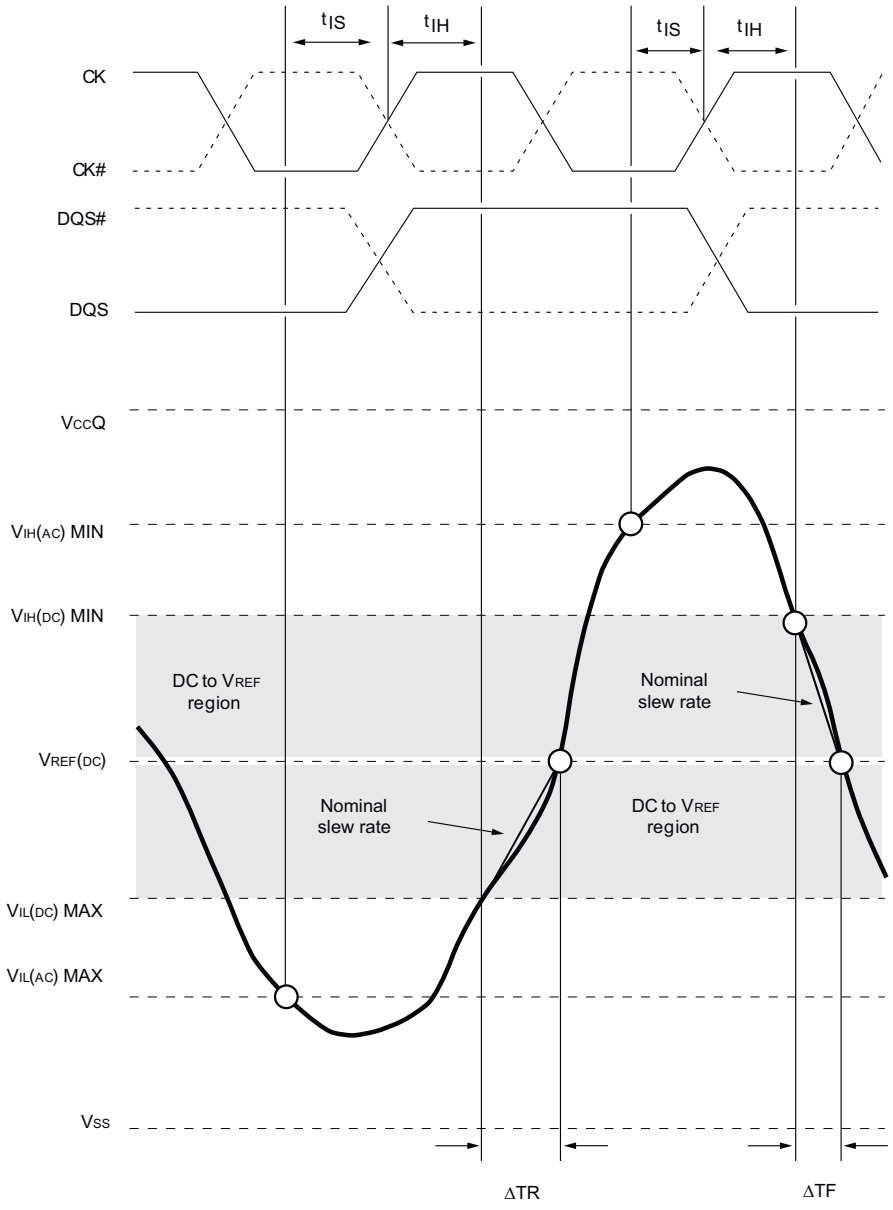
| Slew Rate (V/ns) | tVAC at 175mV(ps) | tVAC at 150mV(ps) |
|---|---|---|
| >2.0 | 75 | 175 |
| 2.0 | 57 | 170 |
| 1.5 | 50 | 167 |
| 1.0 | 38 | 163 |
| 0.9 | 34 | 162 |
| 0.8 | 29 | 161 |
| 0.7 | 22 | 159 |
| 0.6 | 13 | 155 |
| 0.5 | 0 | 150 |
| <0.5 | 0 | 150 |

## FIGURE 25 - NOMINAL SLEW RATE AND tVAC FOR tIS (COMMAND AND ADDRESS – CLOCK)




Notes: 1. Both the clock and the strobe are drawn on different time scales.

## Figure 26 - Nominal Slew Rate for tIH (Command and Address – Clock)

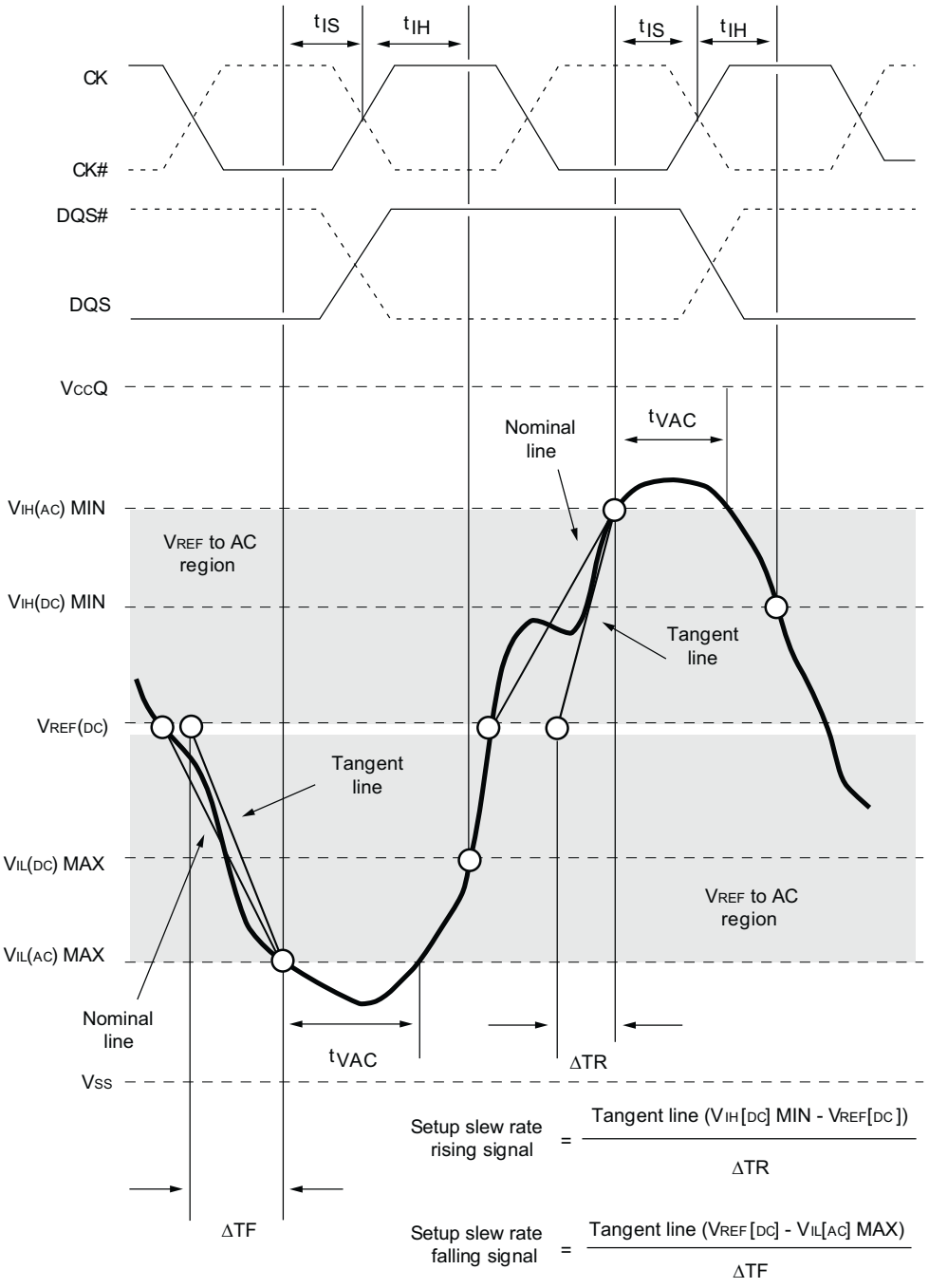



$$\text{Hold slew rate rising signal} = \frac{V_{REF(DC)} - V_{IL(DC)}\ MAX}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{V_{IH(DC)}\ MIN - V_{REF(DC)}}{\Delta TF}$$

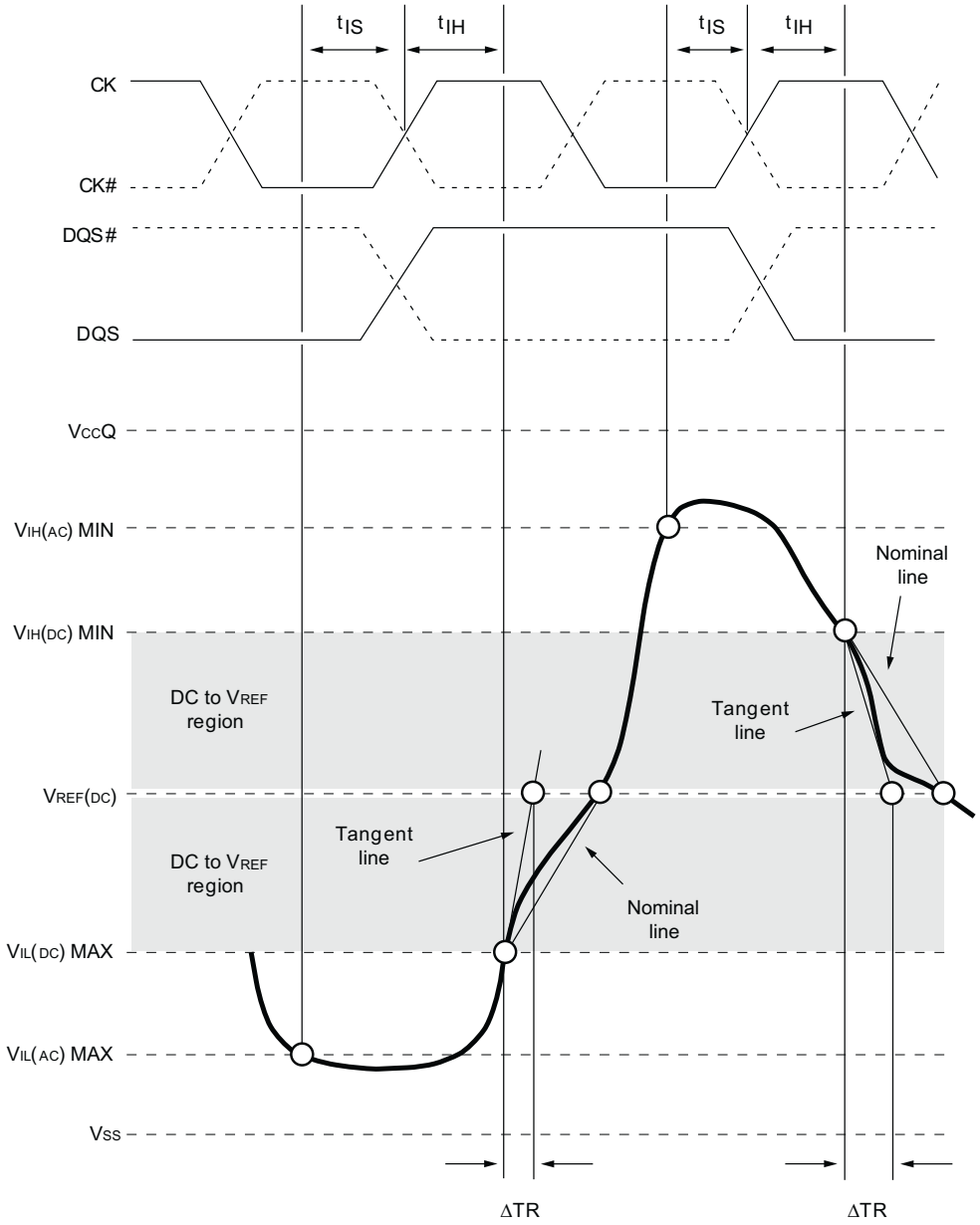
Notes: 1. Both the clock and the strobe are drawn on different time scales.

## FIGURE 27 - TANGENT LINE FOR tIS (COMMAND AND ADDRESS – CLOCK)




Notes: 1. Both the clock and the strobe are drawn on different time scales.

## Figure 28 - Tangent Line for tIH (Command and Address – Clock)




$$\text{Hold slew rate rising signal} = \frac{\text{Tangent line } (V_{REF}[DC] - V_{IL}[DC] \text{ MAX})}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{\text{Tangent line } (V_{IH}[DC] \text{ MIN} - V_{REF}[DC])}{\Delta TF}$$

Notes: 1. Both the clock and the strobe are drawn on different time scales.

## DATA SETUP, HOLD AND DERATING

The total $^{t}$DS (setup time) and $^{t}$DH (hold time) required is calculated by adding the data sheet $^{t}$DS (base) and $^{t}$DH (base) values (see Table 55) to the $\Delta^{t}$DS and $\Delta^{t}$DH derating values (see Table 56), respectively.

Although the total setup time for slow slew rates might be negative, a valid input signal is still required to complete the transition and to reach $V_{IH}/V_{IL}$(AC). For slew rates which fall between the values listed in Table 57, the derating values may be obtained by linear interpolation.

Setup ($^{t}$DS) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{REF}$(DC) and the first crossing of $V_{IH}$(AC) MIN. Setup ($^{t}$DS) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{REF}$(DC) and the first crossing of $V_{IL}$(AC) MAX. If the actual signal is always earlier than the nominal slew rate line between the shaded "$V_{REF}$(DC)-to-AC region", use the nominal slew rate derating value (see Figure 29). If the actual signal is later than the nominal slew rate line anywhere between the shaded "$V_{REF}$(DC)-to-AC region", the slew rate of a tangent line to the actual signal from the AC level to the DC level is used for the derating value (see Figure 31).

Hold ($^{t}$DH) nominal slew rate for a rising signal is defined as the slew rate between the last crossing of $V_{IL}$(DC) MAX and the first crossing of $V_{REF}$(DC). Hold ($^{t}$DH) nominal slew rate for a falling signal is defined as the slew rate between the last crossing of $V_{IH}$(DC) MIN and the first crossing of $V_{REF}$(DC). If the actual signal is always later than the nominal slew rate line between the shaded "DC-to-$V_{REF}$(DC) region", use the nominal slew rate for derating value (see Figure 30). If the actual signal is earlier than the nominal slew rate line anywhere between the shaded "DC-to-$V_{REF}$(DC) region", the slew rate of a tangent line to the actual signal from the "DC-to-$V_{REF}$(DC) region", is used for the derating value (see Figure 32).

### TABLE 55: DATA SETUP AND HOLD VALUES AT 1V/NS (DQSx, DQSx\ AT 2V/NS) – AC/DC BASED

| Symbol | DDR3-800 | DDR3-1066 | DDR3-1333 | UNITS | REFERENCE |
|---|---|---|---|---|---|
| $^{t}$DS(base)AC175 | 75 | 25 | - | ps | $V_{IH}$(AC)/$V_{IL}$(AC) |
| $^{t}$DS(base)AC150 | 125 | 75 | 30 | ps | $V_{IH}$(AC)/$V_{IL}$(AC) |
| $^{t}$DS(base)DC100 | 150 | 100 | 65 | ps | $V_{IH}$(AC)/$V_{IL}$(AC) |

### TABLE 56: DERATING VALUE FOR $^{t}$DS/$^{t}$DH – AC175/DC100 - BASED

*Shaded cells indicate slew-rate combinations not supported*

**$\Delta^{t}$DS, $\Delta^{t}$DH Derating (ps) – AC175/D100-Based**

| DQ Slew Rate V/ns | DQS, DQS# Differential Slew Rate | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 4.0V/ns | | 3.0V/ns | | 2.0V/ns | | 1.8V/ns | | 1.6V/ns | | 1.4V/ns | | 1.2V/ns | | 1.0V/ns | |
| | $\Delta^{t}$DS | $\Delta^{t}$DH | $\Delta^{t}$DS | $\Delta^{t}$DH | $\Delta^{t}$DS | $\Delta^{t}$DH | $\Delta^{t}$DS | $\Delta^{t}$DH | $\Delta^{t}$DS | $\Delta^{t}$DH | $\Delta^{t}$DS | $\Delta^{t}$DH | $\Delta^{t}$DS | $\Delta^{t}$DH | $\Delta^{t}$DS | $\Delta^{t}$DH |
| 2.0 | 88 | 50 | 88 | 50 | 88 | 50 | | | | | | | | | | |
| 1.5 | 59 | 34 | 59 | 34 | 59 | 34 | 67 | 42 | | | | | | | | |
| 1.0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 16 | 16 | | | | | | |
| 0.9 | | | -2 | -4 | -2 | -4 | 6 | 4 | 14 | 12 | 22 | 20 | | | | |
| 0.8 | | | | | -6 | -10 | 2 | -2 | 10 | 6 | 18 | 14 | 26 | 24 | | |
| 0.7 | | | | | | | -3 | -8 | 5 | 0 | 13 | 8 | 21 | 18 | 29 | 34 |
| 0.6 | | | | | | | | | -1 | -10 | 7 | -2 | 15 | 8 | 23 | 24 |
| 0.5 | | | | | | | | | | | -11 | -16 | -2 | -6 | 5 | 10 |
| 0.4 | | | | | | | | | | | | | -30 | -26 | -22 | -10 |

## Table 57: Derating Value for tDS/tDH – AC150/DC100 - Based

*Shaded cells indicate slew-rate combinations not supported*

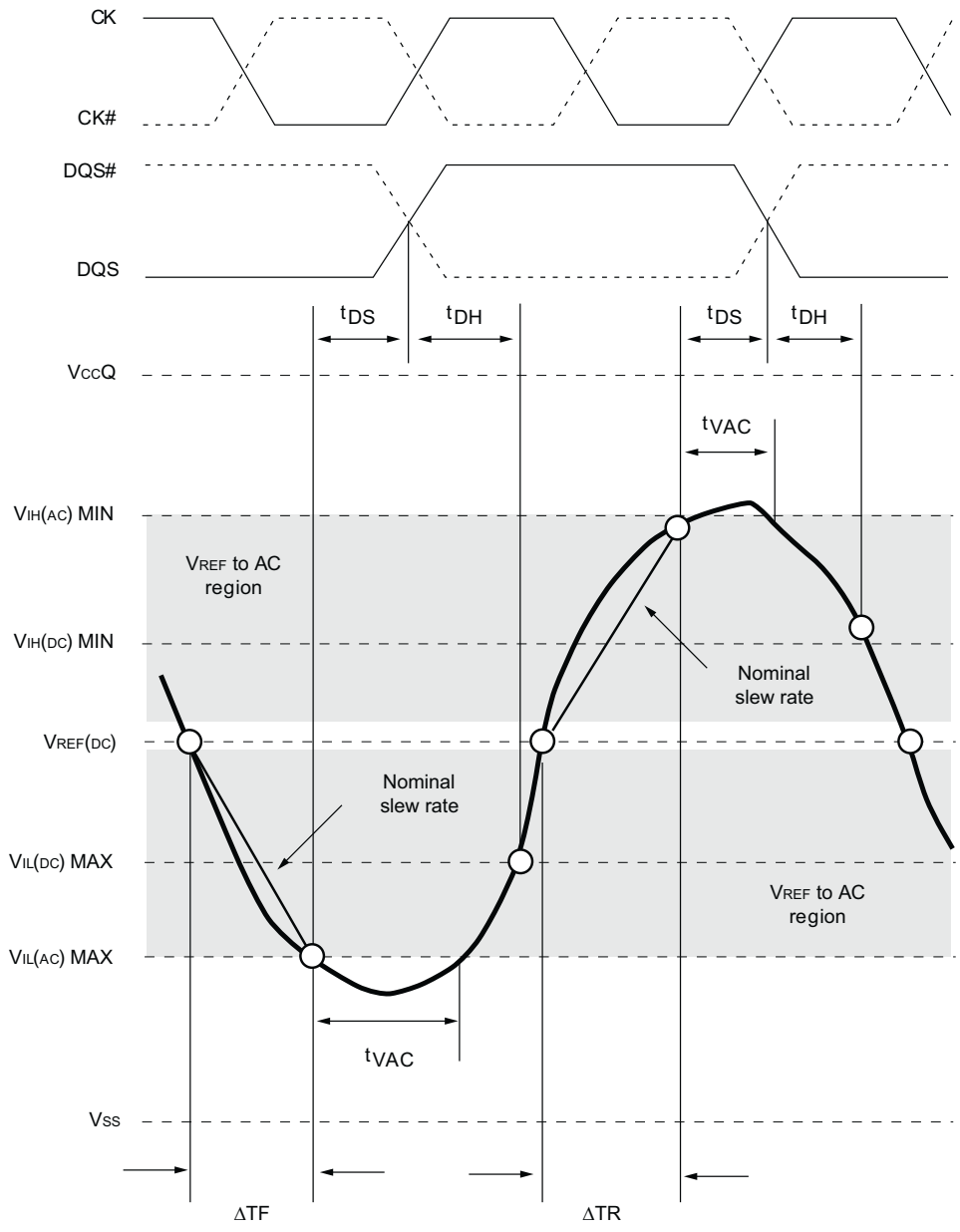
**ΔtDS, ΔtDH Derating (ps) – AC150/DC100-Based**

| DQ Slew Rate V/ns | DQS, DQS# Differential Slew Rate | | | | | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | 4.0V/ns | | 3.0V/ns | | 2.0V/ns | | 1.8V/ns | | 1.6V/ns | | 1.4V/ns | | 1.2V/ns | | 1.0V/ns | |
| | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH | ΔtDS | ΔtDH |
| 2.0 | 75 | 50 | 75 | 50 | 75 | 50 | | | | | | | | | | |
| 1.5 | 50 | 34 | 50 | 34 | 50 | 34 | 58 | 42 | | | | | | | | |
| 1.0 | 0 | 0 | 0 | 0 | 0 | 0 | 8 | 8 | 16 | 16 | | | | | | |
| 0.9 | | | 0 | -4 | 0 | -4 | 8 | 4 | 16 | 12 | 24 | 20 | | | | |
| 0.8 | | | | | 0 | -10 | 8 | -2 | 16 | 6 | 24 | 14 | 32 | 24 | | |
| 0.7 | | | | | | | 8 | -8 | 16 | 0 | 24 | 8 | 32 | 18 | 40 | 34 |
| 0.6 | | | | | | | | | 15 | -10 | 23 | -2 | 31 | 8 | 39 | 24 |
| 0.5 | | | | | | | | | | | 14 | -16 | 22 | -6 | 30 | 10 |
| 0.4 | | | | | | | | | | | | | 7 | -26 | 15 | -10 |

## Table 58: Required Time tVAC Above VIH(AC) (Below VIL[AC]) for a Valid Transition

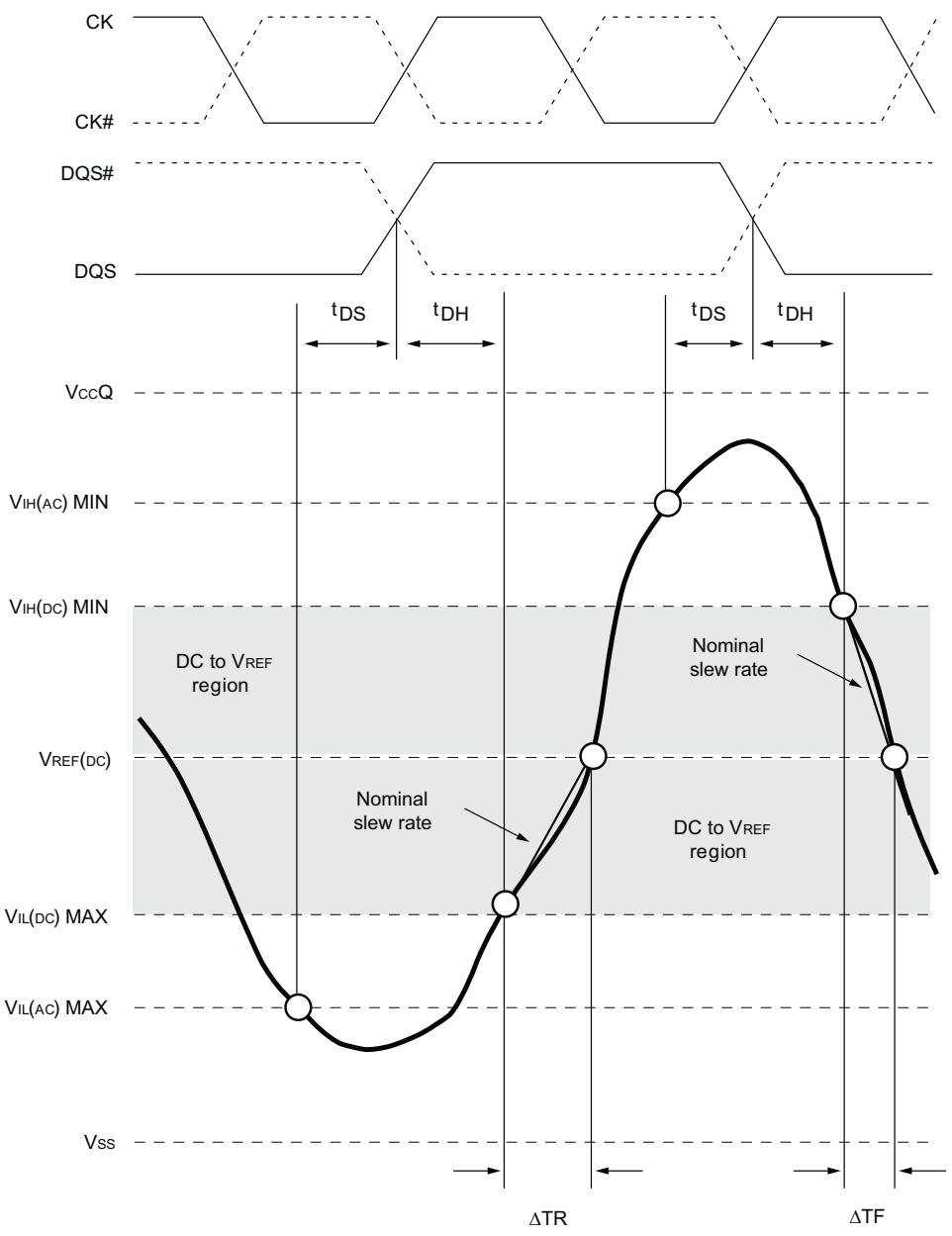
| Slew Rate (V/ns) | tVAC at 175mV(ps) [MIN] | tVAC at 150mV(ps) [MIN] |
|---|---|---|
| >2.0 | 75 | 175 |
| 2.0 | 57 | 170 |
| 1.5 | 50 | 167 |
| 1.0 | 38 | 163 |
| 0.9 | 34 | 162 |
| 0.8 | 29 | 161 |
| 0.7 | 22 | 159 |
| 0.6 | 13 | 155 |
| 0.5 | 0 | 150 |
| <0.5 | 0 | 150 |

## FIGURE 29 - NOMINAL SLEW RATE AND tVAC FOR tDS (DQ – STROBE)




Notes: 1. Both the clock and the strobe are drawn on different time scales.

## FIGURE 30 - NOMINAL SLEW RATE FOR tDH (DQ – STROBE)

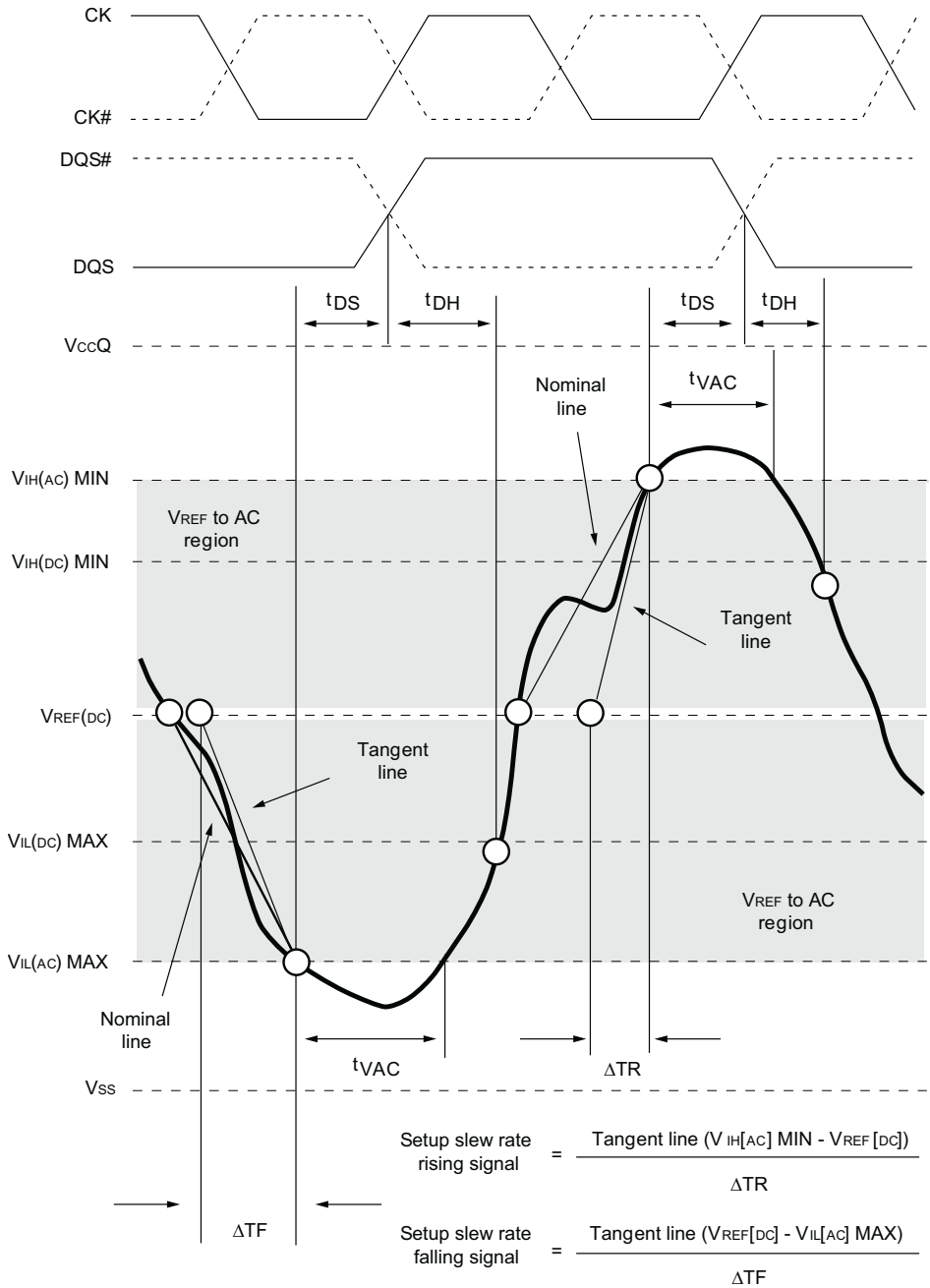



$$\text{Hold slew rate rising signal} = \frac{V_{REF(DC)} - V_{IL(DC)}\ MAX}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{V_{IH(DC)}\ MIN - V_{REF(DC)}}{\Delta TF}$$

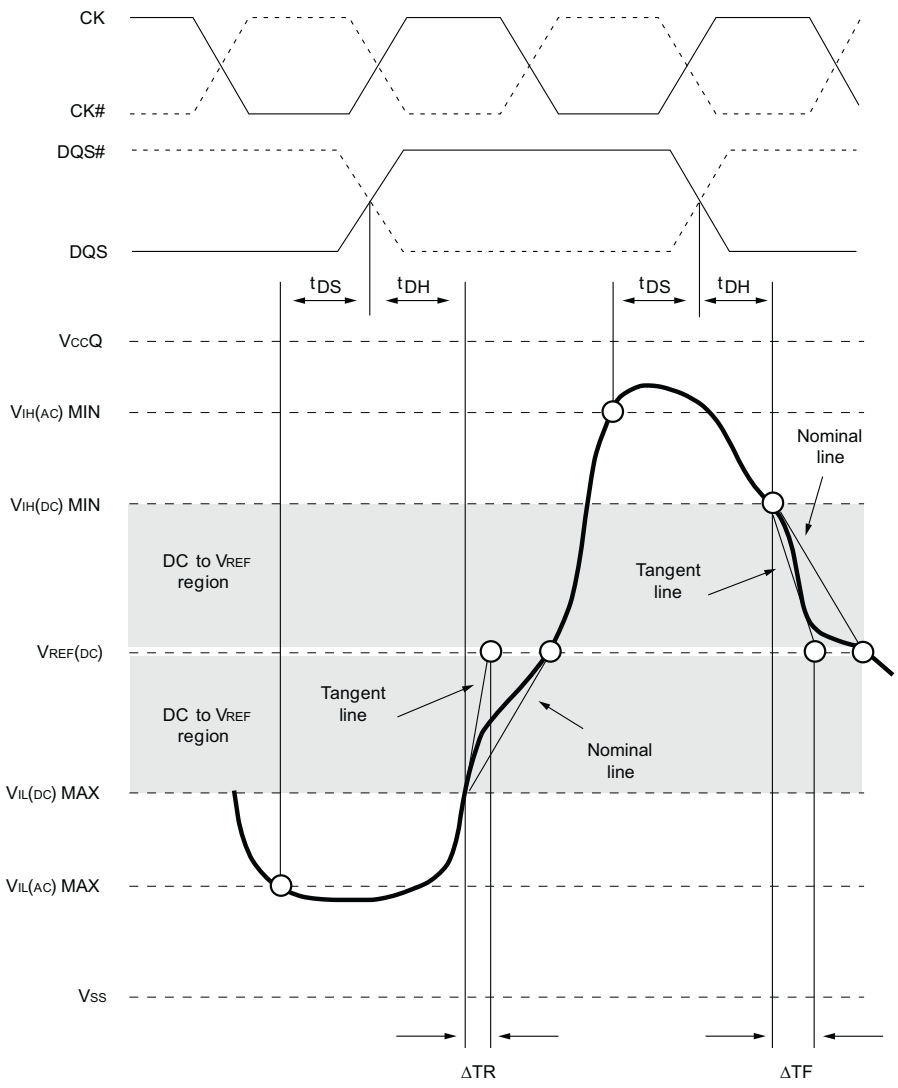
Notes: 1. Both the clock and the strobe are drawn on different time scales.

## FIGURE 31 - NOMINAL SLEW RATE AND tVAC FOR tDS (DQ – STROBE)




Notes: 1. Both the clock and the strobe are drawn on different time scales.

## FIGURE 32 - NOMINAL SLEW RATE FOR tDH (DQ – STROBE)




$$\text{Hold slew rate falling signal} = \frac{\text{Tangent line } (V_{REF[DC]} - V_{IL[DC]} \text{ MAX})}{\Delta TR}$$

$$\text{Hold slew rate falling signal} = \frac{\text{Tangent line } (V_{IH[DC]} \text{ MIN} - V_{REF[DC]})}{\Delta TF}$$

Notes: 1. Both the clock and the strobe are drawn on different time scales.

## COMMANDS TRUTH TABLE

### TABLE 59: TRUTH TABLE - COMMAND

| | | | CKE | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Function | | Symbol | Prev Cycle | Next Cycle | CS\ | RAS\ | CAS\ | WE\ | BA[2:0] | An | A12 | A10 | A[11,0:0] | Notes |
| Mode Register Set | | MRS | H | H | L | L | L | L | BA | | | | | |
| REFRESH | | REF | H | H | L | L | L | H | V | V | V | V | V | |
| SELF REFRESH entry | | SRE | H | L | L | L | L | H | V | V | V | V | V | 6 |
| SELF REFRESH exit | | SRX | L | H | H<br>L | V<br>H | V<br>H | V<br>H | V | V | V | V | V | 6,7 |
| Single-Bank PRECHARGE | | PRE | H | H | L | L | L | L | VBA | V | V | L | V | |
| PRECHARGE all banks | | PREA | H | H | L | L | L | L | V | V | V | H | V | |
| Bank ACTIVATE | | ACT | H | H | L | L | L | H | BA | | | | CA | |
| WRITE | BL8MRS BC4MRS | WR | H | H | L | H | H | L | BA | RFU | V | L | CA | 8 |
| | BC4OTF | WRS4 | H | H | L | H | H | L | BA | RFU | L | L | CA | 8 |
| | BL8OTF | WRS8 | H | H | L | H | H | L | BA | RFU | H | L | CA | 8 |
| WRITE with AUTO PRECHARGE | BL8MRS BC4MRS | WRAP | H | H | L | H | H | L | BA | RFU | V | H | CA | 8 |
| | BC4OTF | WRAPS4 | H | H | L | H | H | L | BA | RFU | L | H | CA | 8 |
| | BL8OTF | WRAPS8 | H | H | L | H | H | L | BA | RFU | H | H | CA | 8 |
| READ | BL8MRS BC4MRS | RD | H | H | L | H | H | H | BA | RFU | V | L | CA | 8 |
| | BC4OTF | RDS4 | H | H | L | H | H | H | BA | RFU | L | L | CA | 8 |
| | BL8OTF | RDS8 | H | H | L | H | H | H | BA | RFU | H | L | CA | 8 |
| READ with AUTO PRECHARGE | BL8MRS BC4MRS | RDAP | H | H | L | H | H | H | BA | RFU | V | H | CA | 8 |
| | BC4OTF | RDAPS4 | H | H | L | H | H | H | BA | RFU | L | H | CA | 8 |
| | BL8OTF | RDAPS8 | H | H | L | H | H | H | BA | RFU | H | H | CA | 8 |
| NO OPERATION | | NOP | H | H | L | H | H | H | V | V | V | V | V | 9 |
| Device DESELECTED | | DES | H | H | H | X | X | X | X | X | X | X | X | 10 |
| POWER-DOWN entry | | PDE | H | L | L<br>H | H<br>V | H<br>V | H<br>V | V | V | V | V | V | 6 |
| POWER-DOWN exit | | PDX | L | H | L<br>H | H<br>V | H<br>V | H<br>V | V | V | V | V | V | 6,11 |
| ZQ CALIBRATION LONG | | ZQCL | H | H | L | H | H | L | X | X | X | H | X | 12 |
| ZQ CALIBRATION SHORT | | ZQCS | H | H | L | H | H | L | X | X | X | L | X | |

NOTES:

1. Commands are defined by states of CS\, RAS\, CAS\, WE\, and CKE at the rising edge of the clock. The MSB of BA, RA, and CA are device-density and configuration-dependent.
2. RESET\ is LOW enabled and used only for asynchronous RESET. Thus, RESET\ must be held HIGH during any normal operation.
3. The state of ODT does not affect the states described in this table.
4. Operations apply to the bank defined by the bank address. For MRS, BA selects one of four mode registers.
5. "V" means "H" or "L" (a defined logic level), and "X" means "Don't Care".
6. See Table 59 for additional information on CKE transition.
7. SELF REFRESH exit is asynchronous.
8. Burst READs or WRITEs cannot be terminated or interrupted, MRS (fixed) and OTF BL/BC are defined in MR0.
9. The purpose of the NOP command is to prevent the SDRAM from registering any unwanted commands. A NOP will not terminate and operation that is in execution.
10. The DES and NOP commands perform similarly.
11. The POWER-DOWN mode does not perform any REFRESH operations.
12. ZQ CALIBRATION LONG is used for either ZQINT (first ZQCL command during initialization) or ZQOPER (ZQCL command after initialization).

**TABLE 60: TRUTH TABLE - CKE**

| Current State [3] | CKE (n-1) Previous Cycle [4] | CKE (n) Present Cycle [4] | (RAS\, CAS\, WE\, CS\) Command [5] | Action [5] | Notes |
|---|---|---|---|---|---|
| POWER-DOWN | L | L | "Don't Care" | Maintain POWER-DOWN | 1,2 |
| | L | H | DES or NOP | POWER-DOWN exit | 1,2 |
| SELF REFRESH | L | L | "Don't Care" | Maintain SELF REFRESH | 1,2 |
| Bank(s) ACTIVE | H | H | DES or NOP | SELF REFRESH exit | 1,2 |
| READING | H | L | DES or NOP | Active POWER-DOWN entry | 1,2 |
| WRITING | H | L | DES or NOP | POWER-DOWN entry | 1,2 |
| PRECHARGING | H | L | DES or NOP | POWER-DOWN entry | 1,2 |
| REFRESHING | H | L | DES or NOP | PRECHARGE POWER-DOWN entry | 1,2 |
| All Banks IDLE | H | L | DES or NOP | PRECHARGE POWER-DOWN entry | 1,2,6 |
| | H | L | REFRESH | SELF REFRESH | |

NOTES:

1. All states and sequences not shown are illegal or reserved unless explicitly described elsewhere in this document.
2. $^{t}$CKE(MIN) means CKE must be registered at multiple consecutive positive clock edges. CKE must remain at the valid input level the entire time it takes to achieve the required number of registration clocks. Thus, after any CKE transition, CKE may not transition from its valid level during the time period of $^{t}$IS + $^{t}$CKE(MIN) + $^{t}$IH.
3. Current state = The state of the SDRAM immediately prior to clock edge n.
4. CKE (n) is the logic state of CKE at clock edge n, CKE (n-1) was the state of CKE at the previous clock edge.
5. COMMAND is the command registered at the clock edge (must be a legal command as defined in Table 58). Action is a result of COMMAND. ODT does not affect the states described in this table and is not listed.
6. Idle state = all banks are closed, no data bursts are in progress, CKE is HIGH and all timings from previous operations are satisfied. All SELF REFRESH exit and POWER-DOWN exit parameters are also satisfied.

## DESELECT (DES)

The DES command (CS\ HIGH) prevents new commands from being executed by the SDRAM. Operations already in progress are not affected.

## NO OPERATION (NOP)

The NOP command (CS\ LOW) prevents unwanted commands from being registered during idle or wait states. Operations already in progress are not affected.

## ZQ CALIBRATION

### ZQ Calibration LONG (ZQCL)

The ZQCL command is used to perform the initial calibration during a power-up initialization and reset sequence. This command may be issued at any time by the controller depending on the system environment. The ZQCL command triggers the calibration engine inside the SDRAM. After calibration is achieved, the calibrated values are transferred from the calibration engine to the SDRAM I/O, which are reflected as updated RON and ODT values.

The SDRAM is allowed a timing window defined by either $^{t}$ZQINIT or $^{t}$ZQOPER to perform the full calibration and transfer of values. When ZQCL is issued during the initialization sequence, the timing parameter tZQINIT must be satisfied. When initialization is complete, subsequent ZQCL commands require the timing parameter $^{t}$ZQOPER to be satisfied.

### ZQ Calibration SHORT (ZQCS)

The ZQCS command is used to perform periodic calibrations to account for small voltage and temperature variations. The shorter timing window is provided to perform the reduced calibration and transfer of values as defined by timing parameter $^{t}$ZQCS. A ZQCS command can effectively correct a minimum of 0.5% RON and RTT impedance errors within 64 clock cycles, assuming the maximum sensitivities specified in Table 40 and Table 41.

## ACTIVATE

The ACTIVATE command is used to open (or ACTIVATE) a row in a particular bank for a subsequent access. The value on the BA [2:0] inputs selects the bank, and the address provided on inputs A[n:0] selects the row. This row remains open (or ACTIVE) for accesses until a PRECHARGE command is issued to that bank.

A PRECHARGE command must be issued before opening a different row in the same bank.

## READ

The READ command is used to initiate a burst READ access to an ACTIVE row. The address provided on inputs A[2:0] selects the starting column address depending on the burst length and burst type selected (see table 65). The value on input A10 determines whether or not auto precharge is used. If auto precharge is selected, the row being accessed will be PRECHARGED at the end of the READ burst. If AUTO PRECHARGE is not selected, the row will remain open for subsequent accesses. The value on input A12 (if enabled in the MODE REGISTER) when the READ command is issued, determines whether BC4 (chop) or BL8 is used. After a READ command is issued, the READ burst may not be interrupted. A summary of READ commands is shown in Table 61.

### TABLE 61: READ COMMAND SUMMARY

| | | | CKE | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Function | | Symbol | Prev Cycle | Next Cycle | CS\ | RAS\ | CAS\ | WE\ | $BA_{[2:0]}$ | $A_n$ | $A_{12}$ | $A_{10}$ | $A_{[11,0:0]}$ | Notes |
| READ | BL8MRS BC4MRS | RD | H | | L | H | L | H | BA | RFU | V | L | CA | |
| | BC4OTF | RDS4 | H | | L | H | L | H | BA | RFU | L | L | CA | |
| | BL8OTF | RDS8 | H | | L | H | L | H | BA | RFU | H | L | CA | |
| READ with AUTO PRECHARGE | BL8MRS BC4MRS | RDAP | H | | L | H | L | H | BA | RFU | V | H | CA | |
| | BC4OTF | RDAPS4 | H | | L | H | L | H | BA | RFU | L | H | CA | |
| | BL8OTF | RDAPS8 | H | | L | H | L | H | BA | RFU | H | H | CA | |

## WRITE

The WRITE command is used to initiate a burst WRITE access to an ACTIVE row. The value on the BA[2:0] inputs selects the bank. The value on input A10 determines whether or not AUTO PRECHARGE is used. The value on input A12 (if enabled in the MODE REGISTER [MR]) when the WRITE command is issued, determines whether BC4 (chop) or BL8 is used. The WRITE command summary is shown in Table 62.

### TABLE 62: WRITE COMMAND SUMMARY

| | | | CKE | | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Function | | Symbol | Prev Cycle | Next Cycle | CS\ | RAS\ | CAS\ | WE\ | $BA_{[2:0]}$ | $A_n$ | $A_{12}$ | $A_{10}$ | $A_{[11,0:0]}$ | Notes |
| WRITE | BL8MRS BC4MRS | WR | H | | L | H | L | L | BA | RFU | V | L | CA | |
| | BC4OTF | WRS4 | H | | L | H | L | L | BA | RFU | L | L | CA | |
| | BL8OTF | WRS8 | H | | L | H | L | L | BA | RFU | H | L | CA | |
| WRITE with AUTO PRECHARGE | BL8MRS BC4MRS | WRAP | H | | L | H | L | L | BA | RFU | V | H | CA | |
| | BC4OTF | WRAPS4 | H | | L | H | L | L | BA | RFU | L | H | CA | |
| | BL8OTF | WRAPS8 | H | | L | H | L | L | BA | RFU | H | H | CA | |

## PRECHARGE

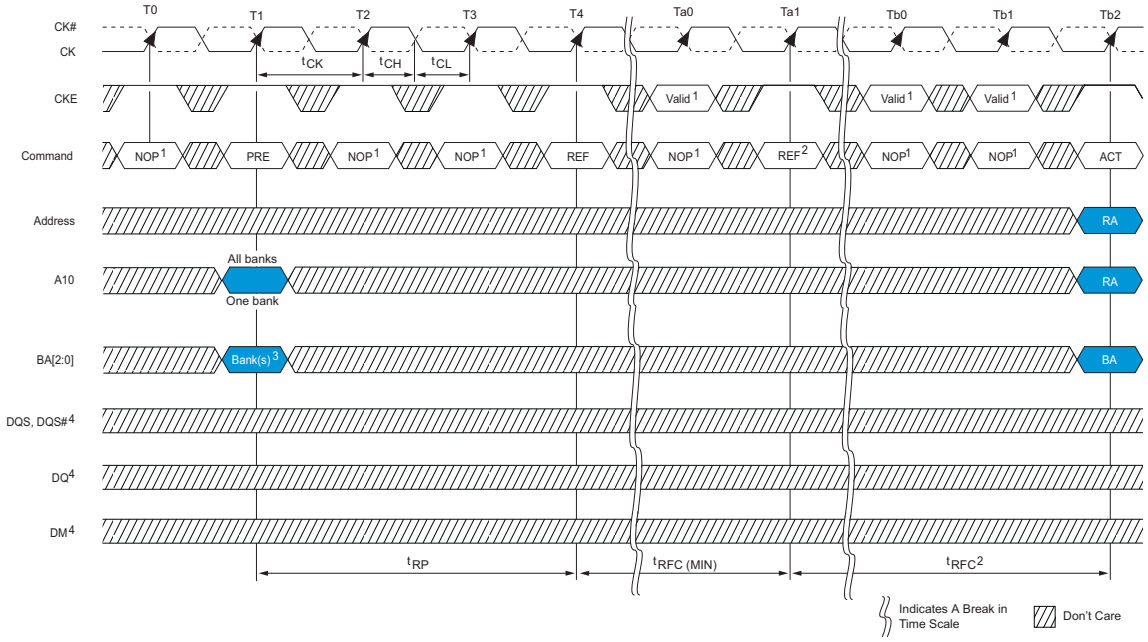
The PRECHARGE command is used to DEACTIVATE the open row in a particular bank or in all banks. The bank(s) are available for a subsequent row access at a specified time ($^{t}$RP) after the PRECHARGE command is issued, except in the case of concurrent AUTO PRECHARGE. A READ or WRITE command to a different bank is allowed during concurrent AUTO PRECHARGE as long as it does not interrupt the data transfer in the current bank and does not violate any other timing parameters. Input A10 determines whether one or all banks are precharged. In the case where only one bank is recharged. Inputs BA[2:0] select the bank; otherwise, BA[2:0] are treated as “Don’t Care”. After a bank is PRECHARGED, it is in the idle state and must be activated prior to any READ or WRITE commands being issued to that bank. A PRECHARGE command is treated as a NOP if there is no open row in that bank (idle state) or if the previously open row is already in the process of precharging. However, the PRECHARGE period is determined by the last PRECHARGE command issued to the bank.

## REFRESH

REFRESH is used during normal operation of the SDRAM and is analogous to CAS\-before RAS\ (CBR) refresh or AUTO REFRESH. This command is non-persistent, so it must be issued each time a REFRESH is required. The addressing is generated by the internal REFRESH command. The SDRAM requires REFRESH cycles at an average interval of 7.8µs (maximum when Tc≤85˚C or 3.9µs MAX when Tc≤95˚C). The REFRESH period begins when the REFRESH command is registered and ends $^{t}$RFC (MIN) later.

To allow for improved efficiency in scheduling and switching between tasks, some flexibility in the absolute REFRESH interval is provided. A maximum of eight REFRESH commands can be posted to any given SDRAM, meaning that the maximum absolute interval between any REFRESH command and the next REFRESH command is nine times the maximum average interval refresh rate. SELF REFRESH may be entered with up to eight REFRESH commands being posted. After exiting SELF REFRESH (when entered with posted REFRESH commands) additional posting of REFRESH commands is allowed to the extent the maximum number of cumulative posted REFRESH commands (both pre and post SELF REFRESH) does not exceed eight REFRESH commands.

## FIGURE 33 - REFRESH MODE




Notes: 1. NOP commands are shown for ease of illustration; other valid commands may be possible at these times. CKE must be active during the PRECHARGE, ACTIVATE, and REFRESH commands, but may be inactive at other times (see “Power-Down Mode” on page 153).

## SELF REFRESH

The SELF REFRESH command is used to retain data in the SDRAM, even if the rest of the system is powered down. When in the SELF REFRESH mode, the SDRAM retains data without external clocking. The SELF REFRESH mode is also a convenient method used to enable/disable the DLL as well as to change the clock frequency within the allowed synchronous operating range. All power supply inputs (including $V_{REFCA}$ and $V_{REFDQ}$) must be maintained at valid levels upon entry/exit and during SELF REFRESH mode operation. All power supply inputs (including $V_{REFCA}$ and $V_{REFDQ}$) must be maintained at valid levels upon entry/exit and during SELF REFRESH mode under certain conditions:

- Vss< $V_{REFDQ}$< Vcc is maintained
- $V_{REFDQ}$ is valid and stable prior to CKE going back HIGH
- The first WRITE operation may not occur earlier than 512 clocks after $V_{REFDQ}$ is valid
- All other SELF REFRESH mode exit time requirements are met.

## DLL DISABLE MODE

If the DLL is disabled by the MODE REGISTER (MR1[0] can be switched during initialization or later), the SDRAM is targeted, but not guaranteed to operate similarly to the NORMAL mode with a few notable exceptions:

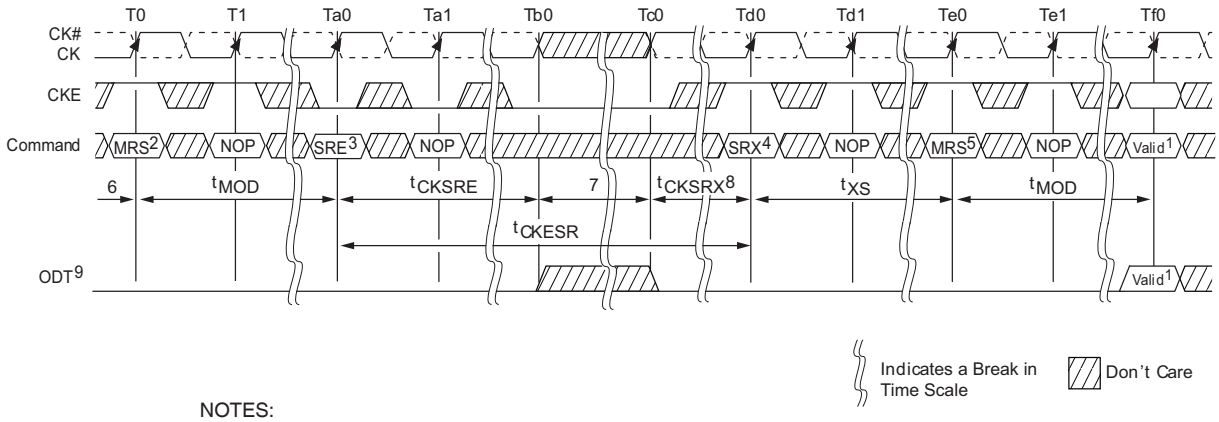
- The SDRAM supports only one value of CAS latency (CL=6) and one value of CAS WRITE latency (CWL=6).
- DLL DISABLE mode affects the READ data clock-to-data strobe relationship ($^{t}$DQSCK), but not the READ data-to-data strobe relationship ($^{t}$DQSQ, $^{t}$QH). Special attention is needed to line the READ data up with the controller time domain when the DLL is disabled.
- In NORMAL operation (DLL on), $^{t}$DQSCK starts from the rising clock edge AL + CL cycles after the READ command. In DLL DISABLE mode, $^{t}$DQSCK starts AL = CL – 1 cycles after the READ command. Additionally, with the DLL disabled, the value of $^{t}$DQSCK could be larger than $^{t}$CK.

The ODT feature is not supported during DLL DISABLE mode (including dynamic ODT). The ODT resistors must be disabled by continuously registering the ODT ball LOW by programming $R_{TT}$_NORM MR1[9,6,2] and $R_{TT}$_WR MR2[10,9] to “0” while in DLL DISABLE mode.

Specific steps must be followed to switch between the DLL enable and DLL DISABLE modes due to a gap in the allowed clock rates between the two modes ($^{t}$CK[AVG]MAX and $^{t}$CK[DLL DISABLE] MIN, respectively). The only time the clock is allowed to cross this clock rate gap is during SELF REFRESH mode. Thus, the required procedure for switching from the DLL ENABLE to DLL DISABLE mode is to change frequency curing self refresh (see Figure 34):

1. Starting from the IDLE state (all banks are PRECHARGED, all timings are fulfilled, ODT is turned off, and $R_{TT}$_NOM and $R_{TT}$_WR are HIGH-Z), set MR1[0] to “1” to DISABLE the DLL.
2. Enter SELF REFRESH mode after $^{t}$MOD has been satisfied.
3. After $^{t}$CKSRE is satisfied, change the frequency to the desired clock rate.
4. SELF REFRESH may be exited when the clock is stabled with the new frequency for $^{t}$CKSRX.
5. The SDRAM will be ready for its next command in the DLL DISABLE mode after the greater of $^{t}$MRD or $^{t}$MOD has been satisfied. A ZQCL command should be issued with appropriate timing met as well.

## FIGURE 34 - DLL ENABLE MODE TO DLL DISABLE MODE




NOTES:

1. Any valid command.
2. Disable DLL by setting MR1[0] to "1."
3. Wait tXS, then set MR1[0] to "0" to enable DLL.
4. Wait tMRD, then set MR0[8] to "1" to begin DLL RESET.
5. Wait tMRD, update registers (CL, CWL, and write recovery may be necessary).
6. Wait tMOD, any valid command.
7. Starting with the idle state.
8. Change frequency.
9. Clock must be stable at least tCKSRX.
10. Static LOW in case RTT_NOM or RTT_WR is enabled; otherwise, static LOW or HIGH.

A similar procedure is required for switching from the DLL disable mode back to the DLL enable mode. This also requires changing the frequency during self refresh mode (see Figure 44 on page 100).

1. Starting from the idle state (all banks are precharged, all timings are fulfilled, ODT is turned off, and RTT_NOM and RTT_WR are High-Z), enter self refresh mode.

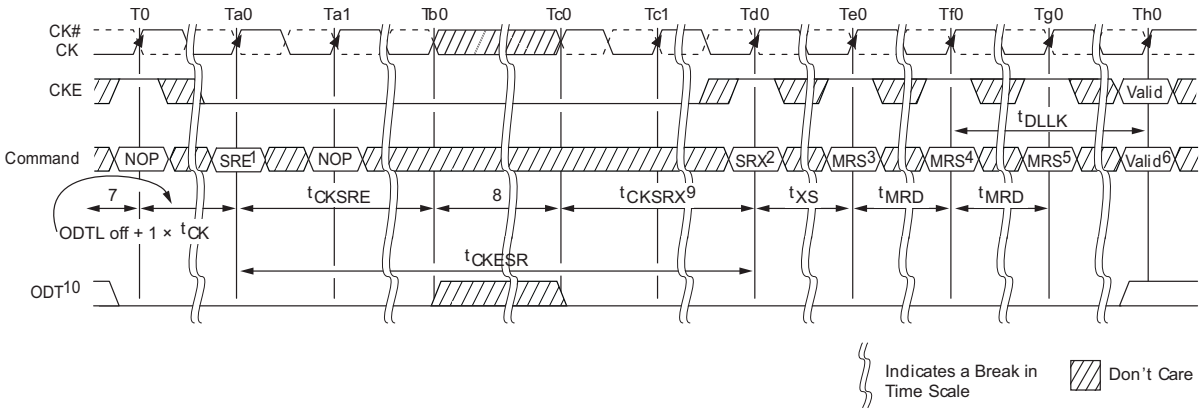
2. After tCKSRE is satisfied, change the frequency to the new clock rate.

3. Self refresh may be exited when the clock is stable with the new frequency for tCKSRX. After tXS is satisfied, update the mode registers with the appropriate values. At a minimum, set MR1[0] to "0" to enable the DLL. Wait tMRD, then set MR0[8] to "1" to enable DLL RESET.

4. After another tMRD delay is satisfied, then update the remaining mode registers with the appropriate values.

5. The DRAM will be ready for its next command in the DLL enable mode after the greater of tMRD or tMOD has been satisfied. However, before applying any command or function requiring a locked DLL, a delay of tDLLK after DLL RESET must be satisfied. A ZQCL command should be issued with the appropriate timings met as well.

## FIGURE 35- DLL DISABLE MODE TO DLL ENABLE MODE




NOTES:

1. Enter SELF REFRESH.
2. Exit SELF REFRESH.
3. Wait $^{t}$XS, then set MR1[0] to "0" to enable DLL.
4. Wait $^{t}$MRD, then set MR0[8] to "1" to begin DLL RESET.
5. Wait $^{t}$MRD, update registers (CL, CWL, and write recovery may be necessary).
6. Wait $^{t}$MOD, any valid command.
7. Starting with the idle state.
8. Change frequency.
9. Clock must be stable at least $^{t}$CKSRX.
10. Static LOW in case RTT_NOM or RTT_WR is enabled; otherwise, static LOW or HIGH.

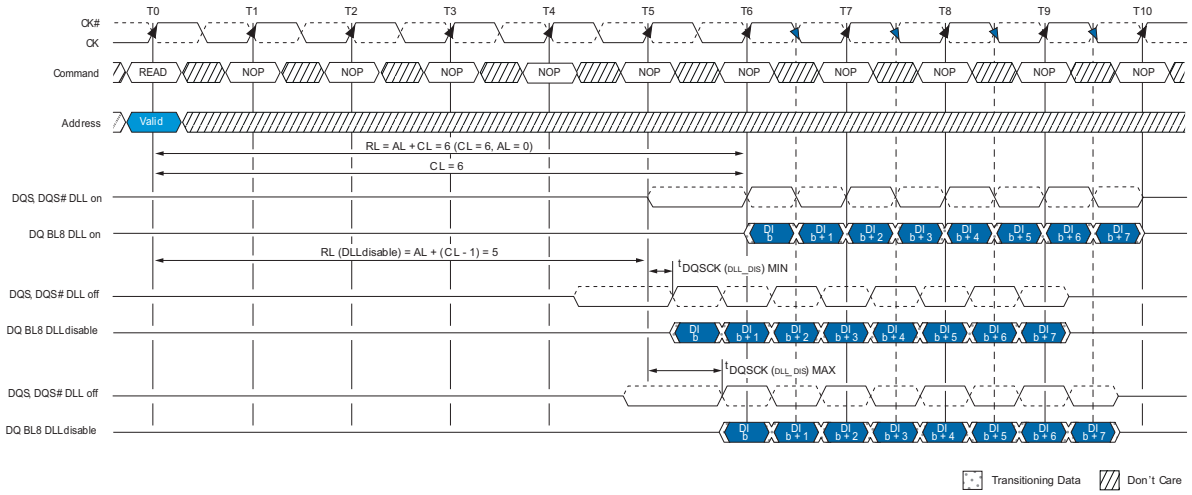
The clock frequency range for the DLL disable mode is specified by the parameter $^{t}$CKDLL_DIS. Due to latency counter and timing restrictions, only CL = 6 and CWL = 6 are supported.

DLL disable mode will affect the read data clock to data strobe relationship ($^{t}$DQSCK) but not the data strobe to data relationship ($^{t}$DQSQ, $^{t}$QH). Special attention is needed to the controller time domain.

Compared to the DLL on mode where $^{t}$DQSCK starts from the rising clock edge AL + CL cycles after the READ command, the DLL disable mode $^{t}$DQSCK starts AL + CL - 1 cycles after the READ command (see Figure 45 on page 101).

WRITE operations function similarly between the DLL enable and DLL disable modes; however, ODT functionality is not allowed with DLL disable mode.

## FIGURE 36 - DLL DISABLE tDQSCK TIMING



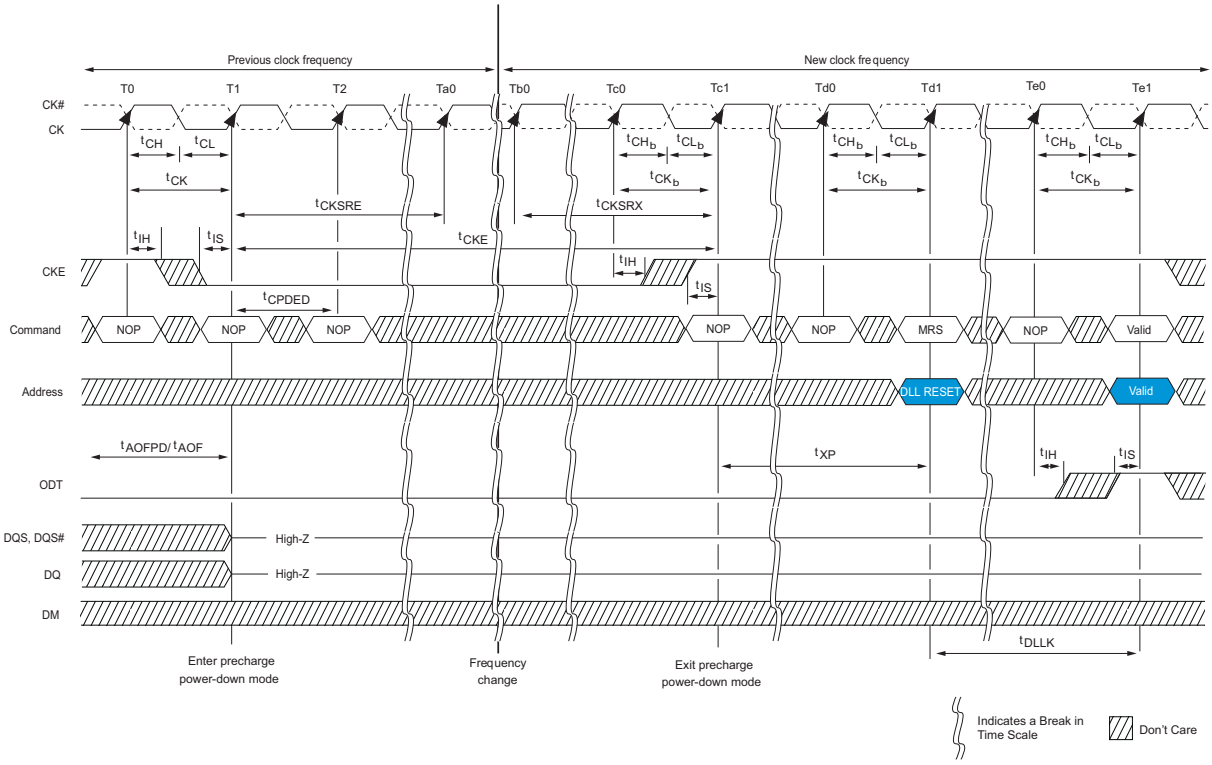

## INPUT CLOCK FREQUENCY CHANGE

When the DDR3 SDRAM is initialized, it requires the clock to be stable during most NORMAL states of operation. This means that after the clock frequency has been set to the stable state, the clock period is not allowed to deviate except what is allowed for by the clock jitter and spread spectrum clocking (SSC) specifications.

The input clock frequency can be changed from one stable clock rate to another under two conditions: SELF REFRESH mode and PRECHARGE power-down mode. Outside of these two modes, it is illegal to change the clock frequency. For the SELF REFRESH mode condition, when the DDR3 SDRAM has been successfully placed into SELF REFRESH mode and $^{t}$CKSRE has been satisfied, the state of the clock becomes a "Don't Care". When the clock becomes a "Don't Care", changing the clock frequency is permissible, provided the new clock frequency is stable prior to $^{t}$CKSRX. When entering and exiting self refresh mode for the sole purpose of changing the clock frequency, the SELF REFRESH entry and exit specifications must still be met.

The PRECHARGE power-down mode condition is when the DDR3 SDRAM is in PRECHARGE power-down mode (either fast exit mode or slow exit mode). Either ODT must be at a logic LOW or RTT_NOM and RTT_WR must be disabled via MR1 and MR2. This ensures RTT_NOM and RTT_WR are in an off state prior to entering PRECHARGE power-down mode while maintaining CKE at a logic LOW. A minimum of $^{t}$CKSRE must occur after CKE goes LOW before the clock frequency can change. The DDR3 SDRAM input clock frequency is allowed to change only within the minimum and maximum operating frequency specified for the particular speed/temperature grade ($^{t}$CK [AVG] MIN to $^{t}$CK [AVG] MAX) device. During the input clock frequency change, CKE must be held at a stable LOW level. When the input clock frequency is changed, a stable clock must be provided to the SDRAM, $^{t}$CKSRX before PRECHARGE power-down may be exited. After PRECHARGE power-down is exited and $^{t}$XP has been satisfied, the DLL must be reset via the MRS. Depending on the new clock frequency, additional MRS commands may need to be issued. During the DLL lock time, RTT_NOM and RTT_WR must remain in an off state. After the DLL lock time, the SDRAM is ready to operate with a new clock frequency (period). This process is depicted in Figure 37.

## FIGURE 37- CHANGE FREQUENCY DURING PRECHARGE POWER-DOWN




NOTES:

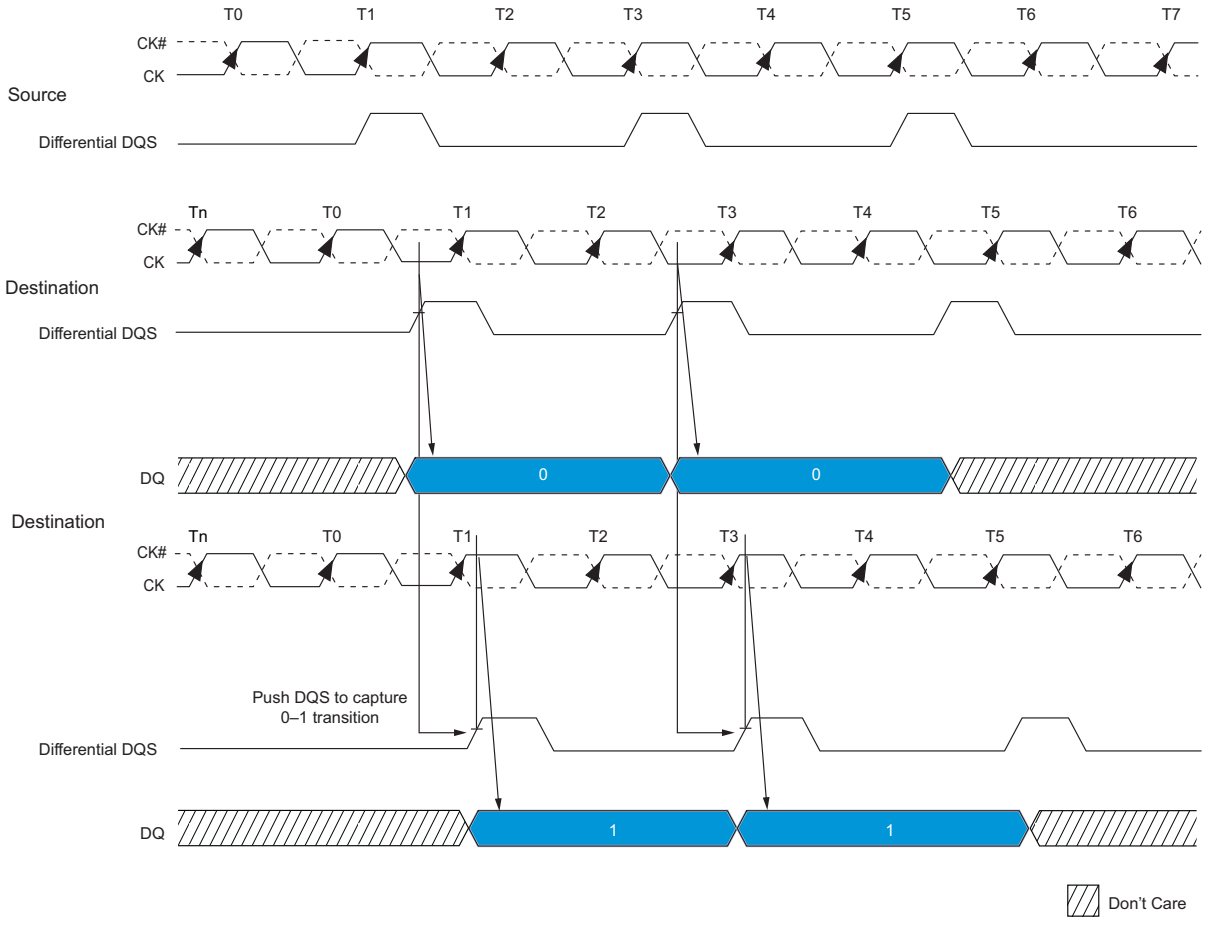
1. Applicable for both slow-exit and fast-exit precharge power-down modes.
2. tAOFPD and tAOF must be satisfied and outputs High-Z prior to T1 (see "On-Die Termination (ODT)" on page 161 for exact requirements).
3. If the RTT_NOM feature was enabled in the mode register prior to entering precharge power-down mode, the ODT signal must be continuously registered LOW ensuring RTT is in an off state. If the RTT_NOM feature was disabled in the mode register prior to entering precharge power-down mode, RTT will remain in the off state. The ODT signal can be registered either LOW or HIGH in this case.

## WRITE LEVELING

For better signal integrity, DDR3 SDRAM memory sub-system designs have adopted use of fly-by topology for the commands, addresses, control signals and clocks. WRITE leveling is a scheme for the memory controller to de-skew the DQSx strobe (DQSx, DQSx\) to CK relationship at the SDRAM with a simple feedback feature provided it by the DDR3 SDRAM itself. WRITE leveling is generally used as part of the initialization process, if required. For NORMAL SDRAM operation, this feature must be disabled. This is the only SDRAM operation where the DQS functions as an input (to capture the incoming clock) and the DQs function as outputs (to report the stat of the clock). Note that nonstandard ODT schemes are required.

The memory controller using the WRITE leveling procedure must have adjustable delay setting on its DQS strobe to align the rising edge of DQS to the clock at the SDRAM pins. This is accomplished when the SDRAM asynchronously feeds back the CK status via the DQ bus and samples with the rising edge of DQS. The controller repeatedly delays the DQS strobe until a CK transition from “0” to “1” is detected. The DQS delay established through this procedure helps ensure $^{t}$DQSS, $^{t}$DSS, and $^{t}$DSH specifications in systems that use fly by topology by de-skewing the trace length mismatch. A conceptual timing of this procedure is shown in Figure 38.

### FIGURE 38- WRITE LEVELING CONCEPT



## WRITE LEVELING

When WRITE leveling is enabled, the rising edge of DQS samples CK and the rime DQ outputs the sampled CK's status. The prime DQ for each of the (4) words contained in the iMOD is DQ0 for the low byte, DQ8 for the high byte. It outputs the status of CK sampled by LDQSx and UDQSx. All other DQs (DQ[7:1], DQ[15:9] for the low word, DQ[23:17],DQ[31:25] for the next word, DQ[39:33], DQ[47:41] for the next and DQ[55:49], DQ[63:57] for the HIGH word DQ[71:64] for the ECC Byte) continue to drive LOW. Two prime DQ on each of the (4) words contained in the LDI iMOD allow each byte lane to be leveled independently.

## WRITE LEVELING PROCEDURE

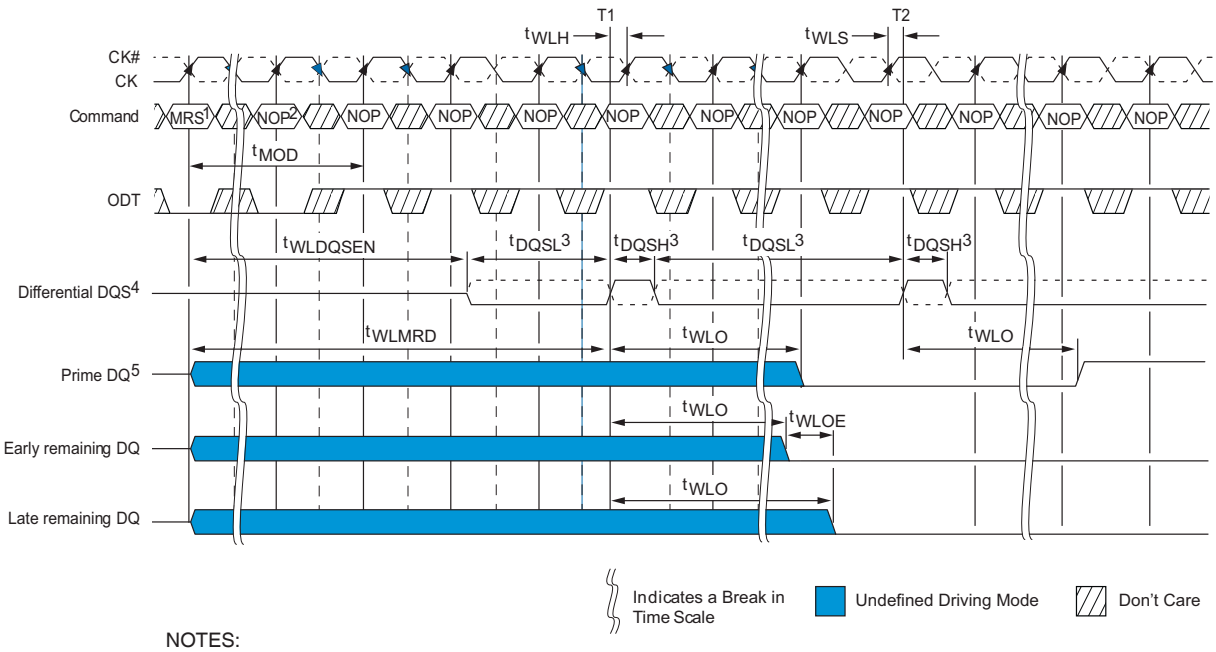
A memory controller initiates the SDRAM WRITE Leveling mode by setting the MR1[7] to a "1", assuming the other programmable features (MR0, MR1, MR2, and MR3) are first set and the DLL is fully reset and locked. The DQ balls enter the WRITE Leveling mode going from a "HIGH-Z" state to an undefined driving state so the DQ bus should not be driven. During WRITE Leveling mode, only the NOP and DES commands are allowed. The memory controller should attempt to level only one rank at a time; thus, the outputs of other ranks should be disabled by setting MR1[12] to a "1". The memory controller may assert ODT after a $^{t}$MOD delay as the SDRAM will be ready to process the ODTL on delay (WL-2$^{t}$CK), provided it does not violate the aforementioned $^{t}$MOD delay requirement.

The memory controller may drive LDQSx, UDQSx LOW and LDQSx\, UDQSx\ HIGH after $^{t}$WLDQSEN has been satisfied. The controller may begin to toggle LDQSx, UDQSx after $^{t}$WLMRD (one L[U]DQSs toggle is DQSs transitioning from a LOW state to a HIGH state with L[U]DQSx\ transitioning from a HIGH state to a LOW state, then both transition back to their original states). At a minimum, ODTL on and $^{t}$AON must be satisfied at least one clock prior to DQS toggling.

After $^{t}$WLMRD and DQS LOW preamble ($^{t}$WPRE) have been satisfied, the memory controller may provide either a single DQSx toggle or multiple DQSx toggles to sample CK for a given DQSx to CK skew. Each DQS toggle must not violate $^{t}$DQSL (MIN) and $^{t}$DQSH (MIN) specifications. $^{t}$DQSL (MAX) and $^{t}$DQSH (MAX) specifications are not applicable during WRITE leveling mode. The DQSx must be able to distinguish the CK's rising edge within $^{t}$WLS and $^{t}$WLH. The prime DQ will output the CK's status asynchronously from the associated DQSx rising edge CK capture within $^{t}$WLO. The remaining DQs that always drive LOW when DQS is toggling must be LOW within $^{t}$WLOE after the first $^{t}$WLO is satisfied (the prime DQs going LOW). As previously noted, DQSx is an input and not an output during this process. Figure 39 depicts the basic timing parameters for the overall write leveling procedure.

The memory controller will likely sample each applicable prime DQ state and determine whether to increment or decrement it DQS delay setting. After the memory controller performs enough DQSx toggles to detect the CK's "0-1" transition, the memory controller should lock the DQS delay setting for the SDRAM iMOD device. After locking the DQS setting, leveling for the rank will have been achieved, and the WRITE leveling mode for the rank should be disabled or reprogrammed (if WRITE leveling of another rank follows).

## FIGURE 39- WRITE LEVELING SEQUENCE




NOTES:

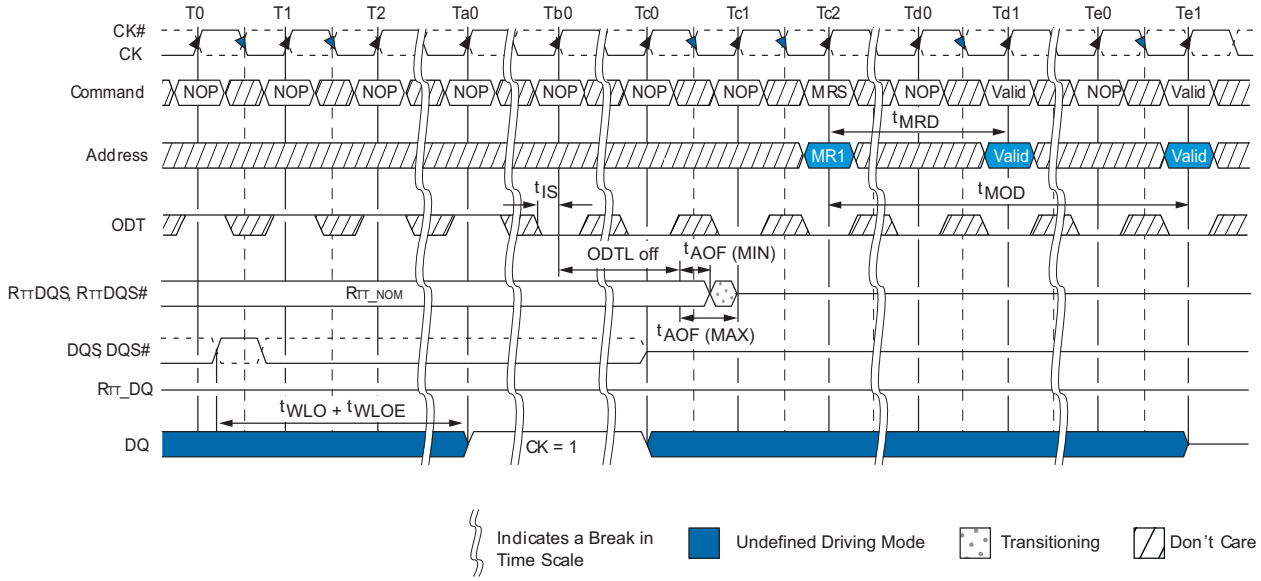
1. MRS: Load MR1 to enter write leveling mode.
2. NOP: NOP or DES.
3. DQS, DQS# needs to fulfill minimum pulse width requirements tDQSH (MIN) and tDQSL (MIN) as defined for regular writes. The maximum pulse width is system-dependent.
4. Differential DQS is the differential data strobe (DQS, DQS#). Timing reference points are the zero crossings. The solid line represents DQS; the dotted line represents DQS#.
5. DRAM drives leveling feedback on a prime DQ (DQ0 for x4 and x8). The remaining DQ are driven LOW and remain in this state throughout the leveling procedure.

## WRITE LEVELING EXIT MODE

After the DDR3 SDRAM iMOD has been WRITE leveled, the controller must exit from WRITE Leveling mode before the NORMAL mode can be used. Figure 40 depicts a general procedure in exiting WRITE Leveling. After the last rising DQS (capturing a "1" at T0), the memory controller should stop driving the DQS signals after tWLO (MAX) delay plus enough delay to enable the memory controller to capture the applicable prime DQ state (at – Tb0). The DQ balls become undefined when DQS no longer remains LOW and they remain undefined until tMOD after the MRS command (at Te1).

The ODT input should be deasserted LOW such that ODTL off (MIN) expires after the DQSx is no longer driving LOW. When ODT LOW satisfies tIS, ODT must be kept LOW (at –Tb0) until the SDRAM is ready for either another rank to be leveled or until the NORMAL mode can be used. After DQS termination is switched off, WRITE level mode should be disabled via the MRS command (at Tc2). After tMOD is satisfied (at Te1), any valid command may be registered by the SDRAM. Some MRS commands may be issued after tMRD (at Td1).

## FIGURE 40- EXIT WRITE LEVELING




Notes: 1. The DQ result, "= 1," between Ta0 and Tc0, is a result of the DQS, DQS# signals capturing CK HIGH just after the T0 state.

# OPERATIONS

## Initialization

The following sequence is required for power up and initialization, as shown in Figure 41.

1. Apply power. RESET\ is recommended to be below 0.2 x VccQ during power ramp to ensure the outputs remain disabled (HIGH-Z) and ODT off ($R_{TT}$ is also HIGH-Z). All other inputs, including ODT may be undefined.

   During power up, either of the following conditions may exist and must be met:

   **• Condition A:**

   - Vcc and VccQ are driven from a single power source and are ramped with a maximum delta voltage between them of $\Delta V \leq 300mV$. Slope reversal of any power supply signal is allowed. The voltage levels on all balls other than Vcc, VccQ, Vss and VssQ must be less than or equal to VccQ and Vcc on one side and must be greater than or equal to VssQ and Vss on the other side.
   - Both Vcc and VccQ power supplies ramp to Vcc (MIN) and VccQ (MIN) within $^{t}$VccPR=200ms.
   - Both Vcc and VccQ power supplies ramp to Vcc (MIN) and VccQ (MIN) within $^{t}$VccPR=200ms.
   - $V_{REFDQ}$ tracks Vcc x 0.5, $V_{REFCA}$ tracks Vcc x 0.5.
   - $V_{TT}$ is limited to 0.95V when the power ramp is complete and is not applied directly to the device; however, $^{t}$VTD should be greater than or equal to zero to avoid device latchup.

   **• Condition B:**

   - Vcc may be applied before or at the same time as VccQ.
   - VccQ may be applied before or at the same time as $V_{TT}$, $V_{REFDQ}$ and $V_{REFCA}$.
   - No slope reversals are allowed in the power supply ramp for this condition.

2. Until stable power, maintain RESET\ LOW to ensure the outputs remain disabled (HIGH-Z). After the power is stable, RESET\ must be LOW for at least 200µs to begin the initialization process. ODT will remain in the HIGH-Z state while RESET\ is LOW and until CKE is registered HIGH.

3. CKE must be LOW 10ns prior to RESET\ transitioning HIGH.

4. After RESET\ transitions HIGH, wait 500µs (minus one clock) with CKE LOW.

5. After this CKE LOW time, CKE may be brought HIGH (synchronously) and only NOP or DES commands may be issued. The clock must be present and valid for at least 10ns (and a minimum of five clocks) and ODT must be driven LOW at least tIS prior to CKE being registered HIGH. When CKE is registered HIGH, it must be continuously registered HIGH until the full initialization process is complete.

6. After CKE is registered HIGH and after $^{t}$XPR has been satisfied, MRS commands may be issued. Issue an MRS (LOAD MODE) command to MR2 with the applicable settings (provide LOW to BA2 and BA0 and HIGH to BA1).

7. Issue an MRS command to MR3 with the applicable settings.

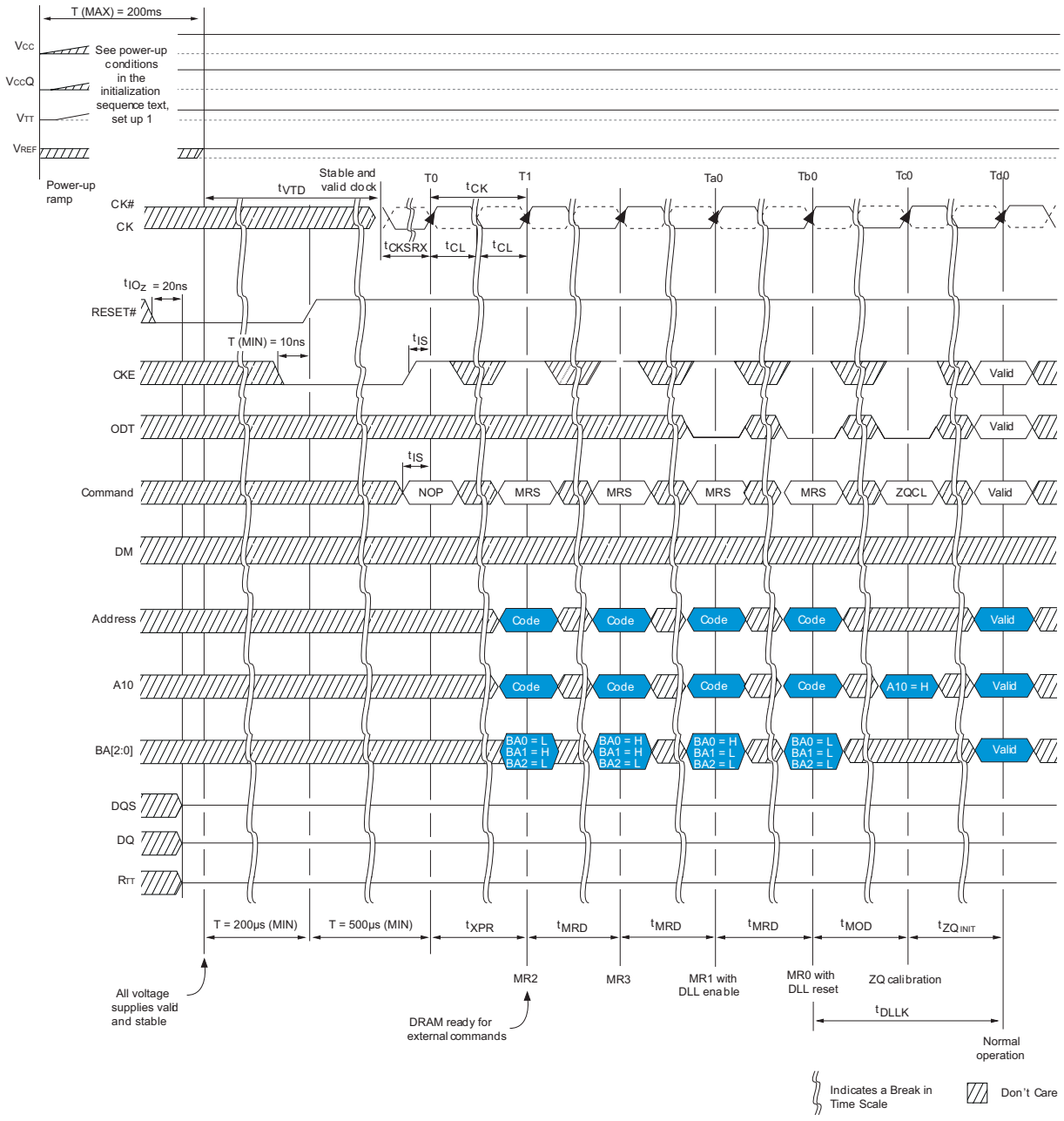
8. Issue an MRS command to MR1 with the applicable settings, including enabling the DLL and configuring ODT.

9. Issue and MRS command to MR0 with the applicable settings, including a DLL RESET command. $^{t}$DLLK (512) cycles of clock input are required to lock the DLL.

10. Issue a ZQCL command to calibrate $R_{TT}$ and RON values for the process voltage temperature (PVT). Prior to NORMAL operation. $^{t}$ZQINIT must be satisfied.

11. When $^{t}$DLLK and $^{t}$ZQINIT have been satisfied, the DDR3 SDRAM will be ready for normal operation.

## FIGURE 41- INITIALIZATION SEQUENCE



## MODE REGISTERS

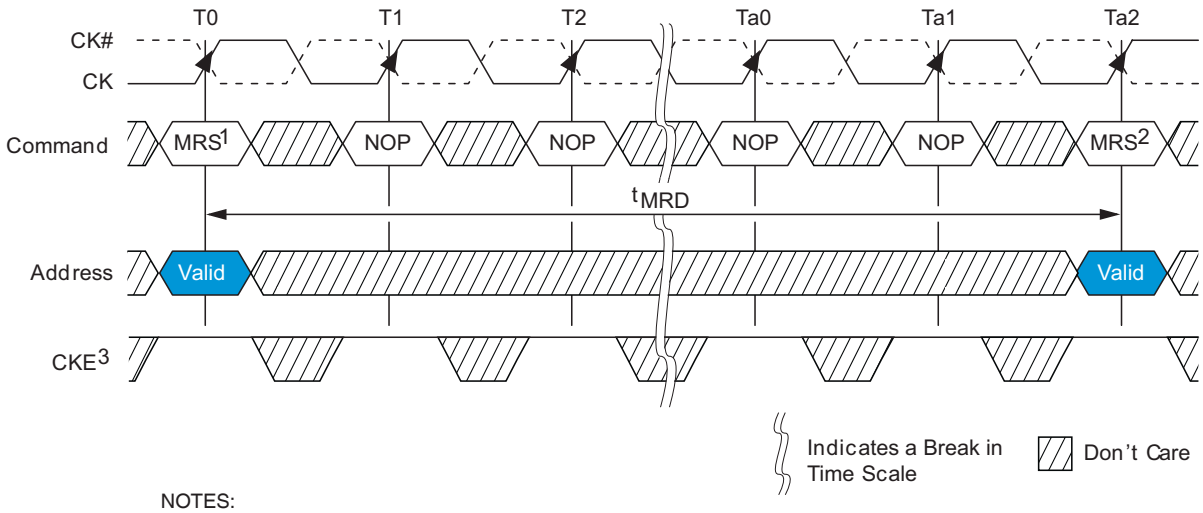
Mode registers (MR0-MR3) are used to define various modes of programmable operation of the DDR3 SDRAM iMOD. A mode register is programmed via the MODE REGISTER SET (MRS) command during initialization and it retains the stored information (except for MR0[8] which is self-clearing) until it is either reprogrammed, RESET\ goes LOW, or until the device loses power.

Contents of a mode register can be altered by re-executing the MRS command. If the user chooses to modify only a subset of the mode register's variables, all variables must be programmed when the MRS command is issued. Reprogramming the mode register will not alter the contents of the memory array, provided it is performed correctly.

The MRS command can only be issued (or re-issued) when all banks are idle and in the PRECHARGED state ($^{t}$RP is satisfied and no data bursts are in progress). After an MRS command has been issued, two parameters must be satisfied: $^{t}$MRD and $^{t}$MOD.

The controller must wait $^{t}$MRD before initiating any subsequent MRS commands (see Figure 42).

### FIGURE 42- MRS-TO-MRS COMMAND TIMING ($^{t}$MRD)

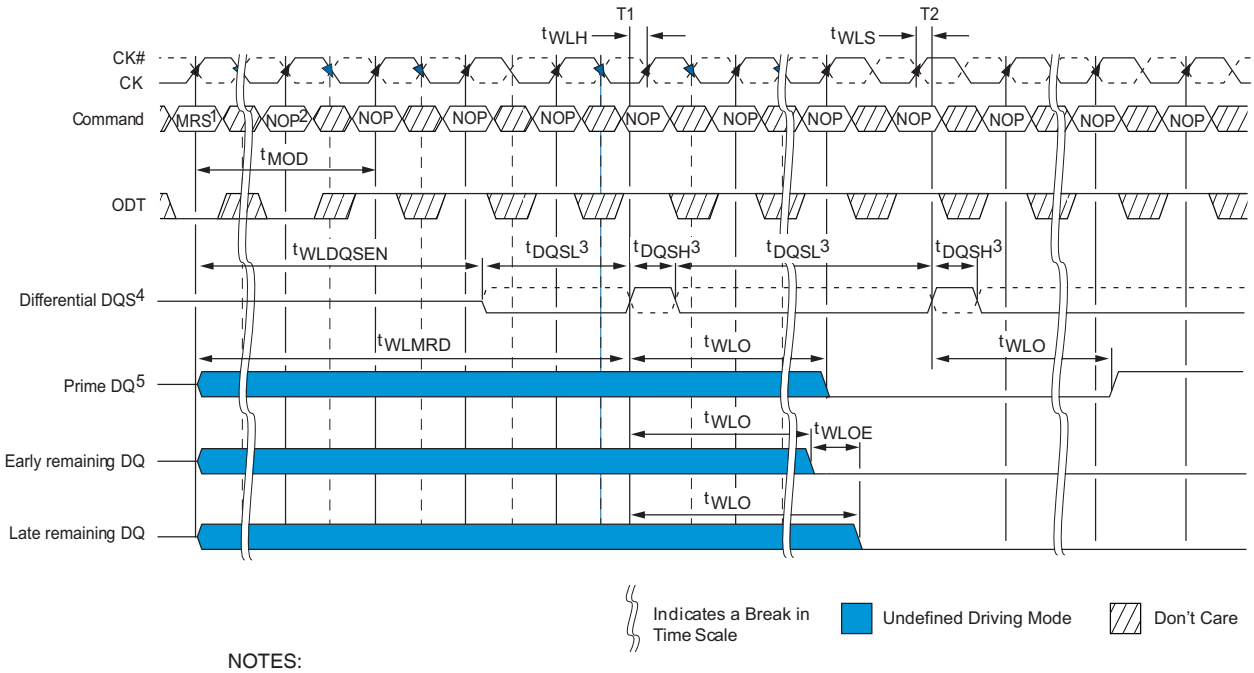



NOTES:

1. Prior to issuing the MRS command, all banks must be idle and precharged, $^{t}$RP (MIN) must be satisfied, and no data bursts can be in progress.the leveling procedure.
2. $^{t}$MRD specifies the MRS-to-MRS command minimum cycle time.
3. CKE must be registered HIGH from the MRS command until $^{t}$MRSPDEN (MIN) (see "Power-Down Mode" on page 153).
4. For a CAS latency change, $^{t}$XPDLL timing must be met before any nonMRS command.

The controller must also wait $^{t}$MOD before initiating any nonMRS commands (excluding NOP and DES), as shown in Figure 52 on page 111. The DRAM requires $^{t}$MOD in order to update the requested features, with the exception of DLL RESET, which requires additional time. Until $^{t}$MOD has been satisfied, the updated features are to be assumed unavailable.

## FIGURE 43- MRS-TO-NONMRS COMMAND TIMING ($t_{MOD}$)




NOTES:

1. Prior to issuing the MRS command, all banks must be idle (they must be precharged, tRP must be satisfied, and no data bursts can be in progress).
2. Prior to Ta2 when tMOD (MIN) is being satisfied, no commands (except NOP/DES) may be issued.
3. If RTT was previously enabled, ODT must be registered LOW at T0 so that ODTL is satisfied prior to Ta1. ODT must also be registered LOW at each rising CK edge from T0 until tMOD (MIN) is satisfied at Ta2.
4. CKE must be registered HIGH from the MRS command until tMRSPDEN (MIN), at which time power-down may occur (see "Power-Down Mode" on page 133).

## MODE REGISTER 0 (MR0)

The base register, MR0 is used to define various DDR3 iMOD modes of operation. These definitions include the selection of a burst length, burst type, CAS latency, operating mode, DLL RESET, WRITE recovery and PRECHARGE power-down mode, as shown in Figure 44.

# MODE REGISTER 0 (MR0)

## BURST TYPE

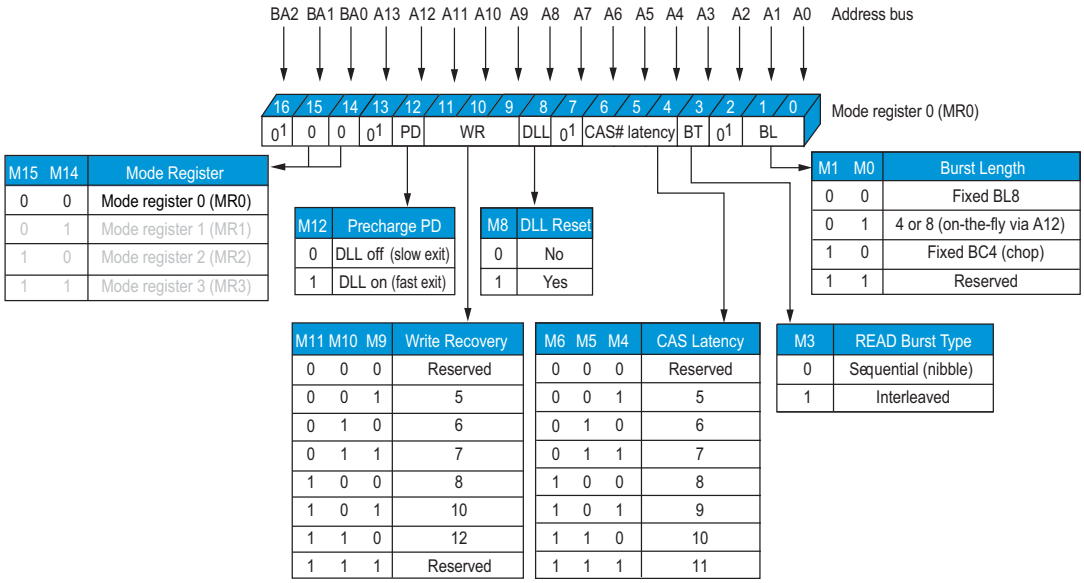
Accesses within a given burst may be programmed to either a sequential or an interleaved order. The burst type is selected via MR0[3], as shown in Figure 44. The ordering of accesses within a burst is determined by the burst length, the burst type and the starting column address, as shown in Table 65. DDR3 only supports 4-bit burst chop and 8-bit burst access modes. Full interleaved address ordering is supported for READs, while WRITEs are restricted to nibble (BC4) or word (BL8) boundaries.

## BURST LENGTH

Burst length is defined by MR0[1:0] (see Figure 44). READ and WRITE accesses to the DDR3 SDRAM iMOD are burst-oriented, with the burst length being programmable to “4” (chop mode). “8” (fixed burst), or selectable using A12 during a READ/WRITE command (on the fly). The burst length determines the maximum number of column locations that can be accessed for a given READ or WRITE command. When MR0[1:0] is set to “01” during a READ/WRITE command, if A12=0, then BC4 (chop) mode is selected. If A12=1, then BL8 mode is selected. Specific timing diagrams, and turnaround between READ/WRITE are shown in the READ/WRITE sections of this document.

When a READ or WRITE command is issued, a block of columns equal to the burst length is effectively selected. All accesses for that burst take place within this block, meaning that the burst will wrap within the block if a boundary is reached. The block is uniquely selected by A[i:2] when the burst length is set to “4” and by A[i:3] when the burst length is set to “8” (where Ai is the most significant column address bit for a given starting location within the block. The programmed burst length applies to both READ and WRITE bursts.

## FIGURE 44- MODE REGISTER 0 (MR0) DEFINITIONS




| M15 | M14 | Mode Register |
|---|---|---|
| 0 | 0 | Mode register 0 (MR0) |
| 0 | 1 | Mode register 1 (MR1) |
| 1 | 0 | Mode register 2 (MR2) |
| 1 | 1 | Mode register 3 (MR3) |

| M12 | Precharge PD |
|---|---|
| 0 | DLL off (slow exit) |
| 1 | DLL on (fast exit) |

| M8 | DLL Reset |
|---|---|
| 0 | No |
| 1 | Yes |

| M1 | M0 | Burst Length |
|---|---|---|
| 0 | 0 | Fixed BL8 |
| 0 | 1 | 4 or 8 (on-the-fly via A12) |
| 1 | 0 | Fixed BC4 (chop) |
| 1 | 1 | Reserved |

| M11 | M10 | M9 | Write Recovery |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | 5 |
| 0 | 1 | 0 | 6 |
| 0 | 1 | 1 | 7 |
| 1 | 0 | 0 | 8 |
| 1 | 0 | 1 | 10 |
| 1 | 1 | 0 | 12 |
| 1 | 1 | 1 | Reserved |

| M6 | M5 | M4 | CAS Latency |
|---|---|---|---|
| 0 | 0 | 0 | Reserved |
| 0 | 0 | 1 | 5 |
| 0 | 1 | 0 | 6 |
| 0 | 1 | 1 | 7 |
| 1 | 0 | 0 | 8 |
| 1 | 0 | 1 | 9 |
| 1 | 1 | 0 | 10 |
| 1 | 1 | 1 | 11 |

| M3 | READ Burst Type |
|---|---|
| 0 | Sequential (nibble) |
| 1 | Interleaved |

Notes: 1. MR0[16, 13, 7, 2] are reserved for future use and must be programmed to “0.”

**TABLE 65: BURST ORDER**

| Burst Length | Read/Write | Starting Column Address (A[2,1,0]) | Burst Type (Decimal) | | Notes |
|---|---|---|---|---|---|
| | | | Type = Sequential | Type = Interleaved | |
| 4 CHOP | READ | 0 0 0 | 0,1,2,3,Z,Z,Z,Z | 0,1,2,3,Z,Z,Z,Z | 1,2 |
| | | 0 0 1 | 1,2,3,0,Z,Z,Z,Z | 1,0,3,2,Z,Z,Z,Z | 1,2 |
| | | 0 1 0 | 2,3,0,1,Z,Z,Z,Z | 2,3,0,1,Z,Z,Z,Z | 1,2 |
| | | 0 1 1 | 3,0,1,2,Z,Z,Z,Z | 3,2,1,0,Z,Z,Z,Z | 1,2 |
| | | 1 0 0 | 4,5,6,7,Z,Z,Z,Z | 4,5,6,7,Z,Z,Z,Z | 1,2 |
| | | 1 0 1 | 5,6,7,4,Z,Z,Z,Z | 5,4,7,6,Z,Z,Z,Z | 1,2 |
| | | 1 1 0 | 6,7,4,5,Z,Z,Z,Z | 6,7,4,5,Z,Z,Z,Z | 1,2 |
| | | 1 1 1 | 7,4,5,6,Z,Z,Z,Z | 7,6,5,4,Z,Z,Z,Z | 1,2 |
| | WRITE | 0 V V | 0,1,2,3,X,X,X,X | 0,1,2,3,X,X,X,X | 1,3,4 |
| | | 1 V V | 4,5,6,7,X,X,X,X | 4,5,6,7,X,X,X,X | 1,3,4 |
| 8 | READ | 0 0 0 | 0,1,2,3,4,5,6,7 | 0,1,2,3,4,5,6,7 | 1 |
| | | 0 0 1 | 1,2.3,0,5,6,7,4 | 1,0,3,2,5,4,7,6 | 1 |
| | | 0 1 0 | 2,3,0,1,6,7,4,5 | 2,3,0,1,6,7,4,5 | 1 |
| | | 0 1 1 | 3,0,1,2,7,4,5,6 | 3,2,1,0,7,6,5,4 | 1 |
| | | 1 0 0 | 4,5,6,7,0,1,2,3 | 4,5,6,7,0,1,2,3 | 1 |
| | | 1 0 1 | 5,6,7,4,1,2,3,0 | 5,4,7,6,1,0,3,2 | 1 |
| | | 1 1 0 | 6,7,4,5,2,3,0,1 | 6,7,4,5,2,3,0,1 | 1 |
| | | 1 1 1 | 7,4,5,6,3,0,1,2 | 7,6,5,4,3,2,1,0 | 1 |
| | WRITE | V V V | 0,1,2,3,4,5,6,7 | 0,1,2,3,4,5,6,7 | 1,3 |

NOTES:
1. Internal READ and WRITE operations start at the same point in time for BC4 as they do for BL8.
2. Z = Data and Strobe output drivers in tri-state.
3. X="Don't Care"

## DLL RESET

DLL RESET is defined by MR0[8] (see Figure 44). Programming MR0[8] to "1" activates the DLL RESET function. MR0[8] is self-clearing, meaning it returns to a value of "0" after the DLL RESET function has been initiated.

Anytime the DLL RESET function has been initiated, CKE must be HIGH and the clock held stable for 512 ($^{t}$DLLK) clock cycles before a READ command can be issued. This is to allow time for the internal clock to be synchronized with the external clock. Failing to wait for synchronization to occur may result in invalid output timing specifications such as $^{t}$DQSCK timings.

## WRITE RECOVERY

WRITE RECOVERY time is defined by MR0[11:9] (see Figure 44). WRITE RECOVERY values of 5,6,7,8,10 or 12 may be used by programming MR0[11:9]. The user is required to program the correct value of WRITE RECOVERY and is calculated by dividing $^{t}$WR (ns) by $^{t}$CK (ns) and rounding up a non-integer value to the next integer: WR (cycles)=roundup ($^{t}$WR[ns]/$^{t}$CK [ns]).

## PRECHARGE POWER-DOWN (PRECHARGE PD)

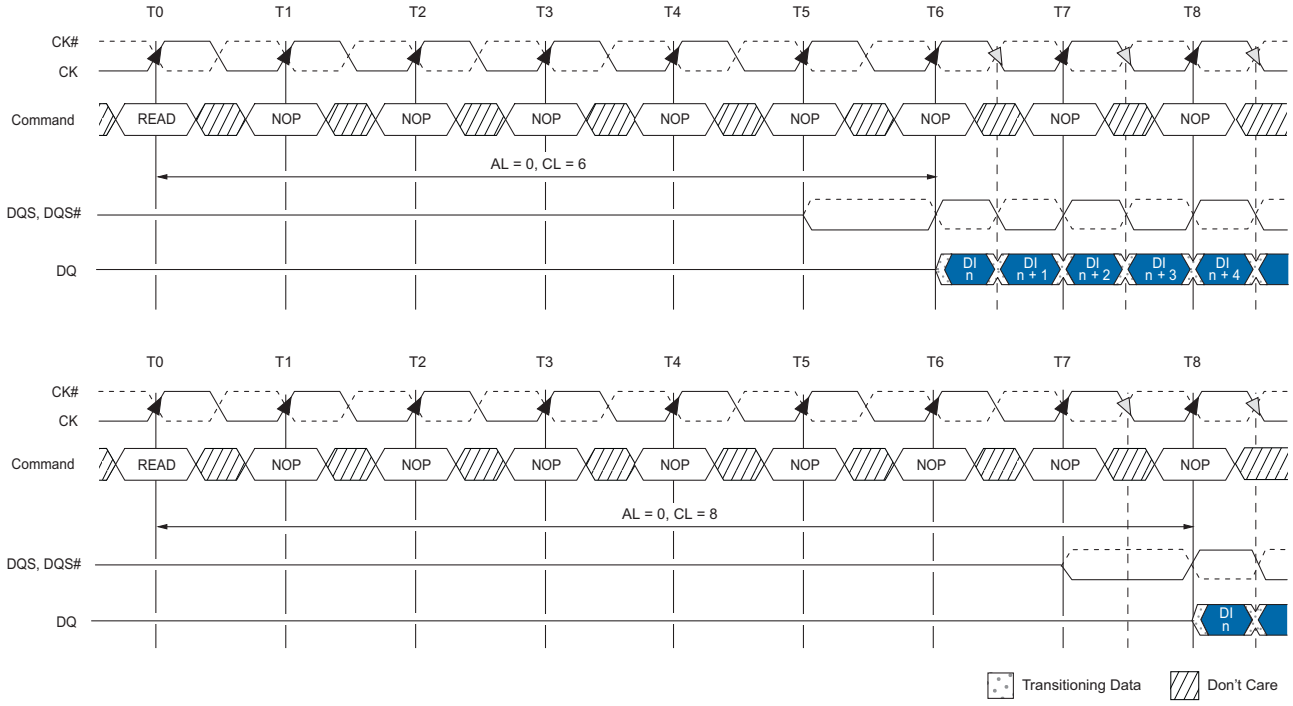
The PRECHARGE PD bit applies only when PRECHARGE power-down mode is being used. When MR0[12] is set to "0", the DLL is off during PRECHARGE power-down providing a lower standby current mode; however, $^{t}$XPDLL must be satisfied when exiting. When MR0[12] is set to "1", the DLL continues to run during PRECHARGE power-down mode to enable a faster exit of PRECHARGE power-down mode; however, $^{t}$XP must be satisfied when exiting (see Power-Down mode on Page 133).

## CAS Latency (CL)

The CL is defined by MR0[6:4], as shown in Figure 44. CAS latency is the delay, as measured in clock cycles, between the internal READ command and the availability of the first bit of valid output data. The CL can be set to 5,6, 8, or 10. DDR3 SDRAM iMODs do not support half-clock latencies.

Examples of CL=6 and CL=8 are shown in Figure 45 (below). If an internal READ command is registered at clock edge n, and the CAS latency is m clocks, the data will be available nominally coincident with clock edge n+m. Table 49 indicates the CLs supported at available operating frequencies.

## FIGURE 45- READ LATENCY




NOTES:

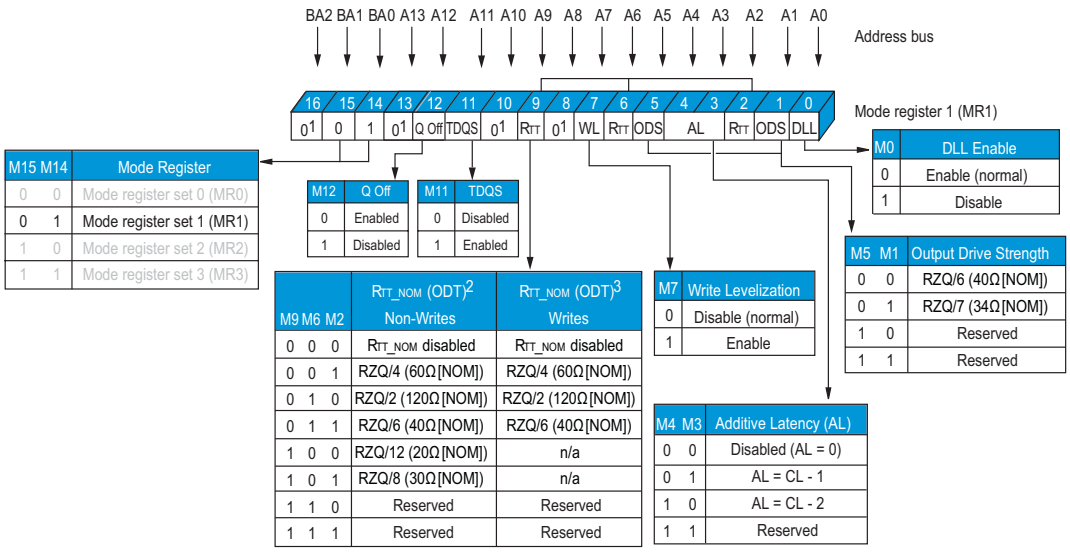
1. For illustration purposes, only CL = 6 and CL = 8 are shown. Other CL values are possible.
2. Shown with nominal $^{t}$DQSCK and nominal $^{t}$DSDQ.

## MODE REGISTER 1 (MR1)

The MODE REGISTER 1 (MR1) controls additional functions and features not available in the other mode registers; Q OFF (OUTPUT DISABLE), DLL ENABLE/DLL DISABLE, RTT_NOM value (ODT), WRITE LEVELING, POSTED CAS ADDITIVE latency, and OUTPUT DRIVE STRENGTH. These functions are controlled via the bits shown in Figure 46 below. The MR1 register is programmed via the MR5 command and retains the stored information until it is reprogrammed, until RESET\ goes LOW (true), or until the device loses power. Reprogramming the MR1 register will not alter the contents of the memory array, provided the operation is performed correctly.

The MR1 register must be loaded when all banks are idle and no bursts are in progress. The controller must satisfy the specified timing parameters $^{t}$MRD and $^{t}$MOD before initiating a subsequent operation.

### FIGURE 46- MODE REGISTER 1 (MR1) DEFINITION




| M15 M14 | Mode Register |
|---|---|
| 0 0 | Mode register set 0 (MR0) |
| 0 1 | Mode register set 1 (MR1) |
| 1 0 | Mode register set 2 (MR2) |
| 1 1 | Mode register set 3 (MR3) |

| M12 | Q Off |
|---|---|
| 0 | Enabled |
| 1 | Disabled |

| M11 | TDQS |
|---|---|
| 0 | Disabled |
| 1 | Enabled |

| M9 M6 M2 | RTT_NOM (ODT)[2] Non-Writes | RTT_NOM (ODT)[3] Writes |
|---|---|---|
| 0 0 0 | RTT_NOM disabled | RTT_NOM disabled |
| 0 0 1 | RZQ/4 (60Ω[NOM]) | RZQ/4 (60Ω[NOM]) |
| 0 1 0 | RZQ/2 (120Ω[NOM]) | RZQ/2 (120Ω[NOM]) |
| 0 1 1 | RZQ/6 (40Ω[NOM]) | RZQ/6 (40Ω[NOM]) |
| 1 0 0 | RZQ/12 (20Ω[NOM]) | n/a |
| 1 0 1 | RZQ/8 (30Ω[NOM]) | n/a |
| 1 1 0 | Reserved | Reserved |
| 1 1 1 | Reserved | Reserved |

| M7 | Write Levelization |
|---|---|
| 0 | Disable (normal) |
| 1 | Enable |

| M4 M3 | Additive Latency (AL) |
|---|---|
| 0 0 | Disabled (AL = 0) |
| 0 1 | AL = CL - 1 |
| 1 0 | AL = CL - 2 |
| 1 1 | Reserved |

| M0 | DLL Enable |
|---|---|
| 0 | Enable (normal) |
| 1 | Disable |

| M5 M1 | Output Drive Strength |
|---|---|
| 0 0 | RZQ/6 (40Ω[NOM]) |
| 0 1 | RZQ/7 (34Ω[NOM]) |
| 1 0 | Reserved |
| 1 1 | Reserved |

NOTES:

1. MR1[16, 13, 10, 8] are reserved for future use and must be programmed to “0.”
2. During write leveling, if MR1[7] and MR1[12] are “1” then all RTT_NOM values are available for use.
3. During write leveling, if MR1[7] is a “1,” but MR1[12] is a “0,” then only RTT_NOM write values are available for use.

## DLL ENABLE/DLL DISABLE

The DLL may be enabled or disabled by programming MR1[0] during the LOAD MODE command, as shown in Figure 46 (previous page). The DLL must be enabled for NORMAL operation. DLL ENABLE is required during power-up initialization and upon returning to NORMAL operation after having DISABLED the DLL for the purpose of debugging or evaluation. ENABLING the DLL should always be followed by resetting the DLL using the appropriate LOAD MODE command.

If the DLL is enabled prior to entering SELF REFRESH mode, the DLL is automatically DISABLED when entering SELF REFRESH operation and is automatically RE-ENABLED and RESET upon exit of SELF REFRESH. If the DLL is DISABLED prior to entering SELF REFRESH, the DLL remains DISABLED even upon exit of the SELF REFRESH operation until it has been RE-ENABLED and RESET.

The SDRAM is not tested, nor does LDI warrant compliance with NORMAL mode timings or functionality when the DLL is disabled. An attempt has been made for the SDRAM to operate in the NORMAL mode whenever possible when the DLL is disabled; however, by industry standards, the following exceptions have been observed, defined and listed:

1. ODT is NOT ALLOWED to be used
2. The OUTPUT DATA is no longer edge-aligned to the clock
3. CL and CWL can only be six clocks

When the DLL is DISABLED, timing and functionality can vary from the NORMAL operational specifications when the DLL is enabled. DISABLING the DLL also implies the need to change the clock frequency.

## OUTPUT DRIVE STRENGTH

The DDR3 SDRAM iMOD uses a programmable impedance output buffer. The drive strength mode register setting is defined by MR1[5:1], RZQ/7 (34Ω [NOM]) is the primary output driver impedance setting for the device. To calibrate the output driver impedance, and external precision resistor (RZQ) is connected between the ZQ ball and VssQ. The value of the resistor is 240Ω±1%.

The output impedance is set during initialization. Additional impedance calibration updates do not affect device operation and all data sheet timings and current specifications are met during an update.

To meet the 34Ω specification, the output drive strength must be set to 34Ω during initialization. To obtain a calibrated output driver impedance after power-up, the DDR3 iMOD SDRAM needs a calibration command that is part of the initialization and reset procedure.

## OUTPUT ENABLE/DISABLE

The OUTPUT ENABLE function is defined by MR1[12], as shown in Figure 46. When enabled (MR1[12]=0), all outputs (DQx, DQSx, DQSx\) are tri-stated. The output DISABLE feature is intended to be used during Icc characterization of the READ current and during $^{t}$DQSS margining (WRITE LEVELING) only.

## ON-DIE TERMINATION (ODT)

ODT resistance RTT_NOM is defined by MR1[9,6,2] (see Figure 46). The RTT termination value applies to the DQx, LDMx, UDMx, L[U]DQSx and L[U]DQSx\. The DDR3 device architecture supports multiple RTT termination values based on RZQ/n where n can be 3,4,6,8 or 12 and RZQ is 240Ω.

Unlike DDR2, DDR3 ODT must be turned off prior to READING data out and must remain off during READ burst. RTT_NOM termination is allowed any time after the DRAM is initialized, calibrated, and not performing READ accesses, or in SELF REFRESH mode. Additionally, WRITE accesses with dynamic ODT enabled (RTT_WR) temporarily replaces RTT_NOM with RTT_WR.

The actual effective termination, RTT_EFF, may be different from the RTT targeted value due to non-linearity of the termination. For RTT_EFF values and calculations, see the ON-DIE TERMINATION (ODT) description later in this DS.

The ODT feature is designed to improve signal integrity of the memory device by enabling the DDR3 SDRAM controller to independently turn ON/OFF ODT for any or all devices in the end designs array. The ODT input control pin is used to determine when RTT is turned on (ODTLon) and off (ODTLoff), assuming ODT has been ENABLED via MR1[9,6,2].

Timings for ODT are detailed in the “ON-DIE Termination (ODT)” description later in this DS.

## WRITE LEVELING

The WRITE LEVELING function is enabled by MR1[7], as shown in Figure 46, WRITE LEVELING is used (during initialization) to de-skew the DQSx strobe to clock offset as a result of fly-by topology designs. For better signal integrity, some end use designs of DDR3 devices adopted fly-by topology for the commands, addresses, control signals and clocks.

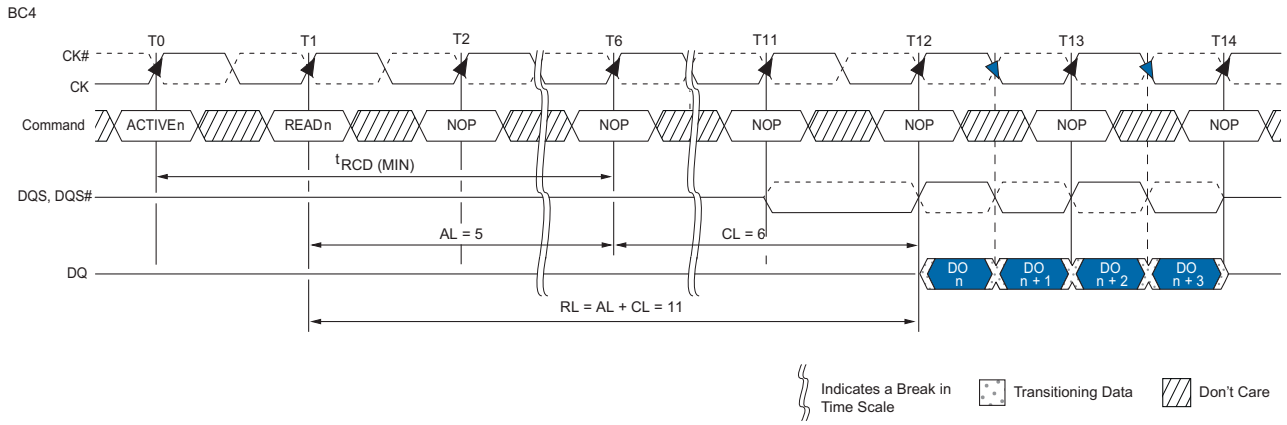
The fly-by topology benefits from a reduced number of stubs and their lengths, however, fly-by topology induces flight time skew between the clock and DQSx strobe (and DQx) at each SDRAM in the array. Controllers will have a difficult time maintaining $^{t}$DQSS, $^{t}$DSS and $^{t}$DSH specifications without supporting WRITE LEVELING in systems which use fly-by topology based designs. WRITE LEVELING timing and detailed operation information is provided in “WRITE LEVELING.

## POSTED CAS ADDITIVE LATENCY (AL)

AL is supported to make the command and data bus efficient for sustainable bandwidths in DDR3 SRAMs. MR1[4,3] define the value of AL (see Figure 46). MR1[4,3] enables the user to program the DDR3 SDRAM with an AL=0, CL-1, or CL-2.

With this feature, the DDR3 SDRAM enables a READ or WRITE command to be issued after the ACTIVATE command for that bank prior to $^{t}$RCD(MIN). The only restriction is ACTIVATE to READ or WRITE + AL ≥ $^{t}$RCD(MIN) must be satisfied. Assuming $^{t}$RCD(MIN) = CL, a typical application using this feature, sets AL=CL – 1$^{t}$CK = $^{t}$RCD(MIN-1$^{t}$CK. The READ or WRITE command is held for the time of the AL before it is released internally to the DDR3 SDRAM iMOD device. READ latency (RL) is controlled by the sum of the AL and CAS latency (CL), RL=AL+CL, WRITE latency (WL) is the sum of CAS WRITE latency and AL, WL=AL + CWL (see “MODE REGISTER 2 (MR2))”. Examples of READ and WRITE latencies are shown in Figure 47 and Figure 49.

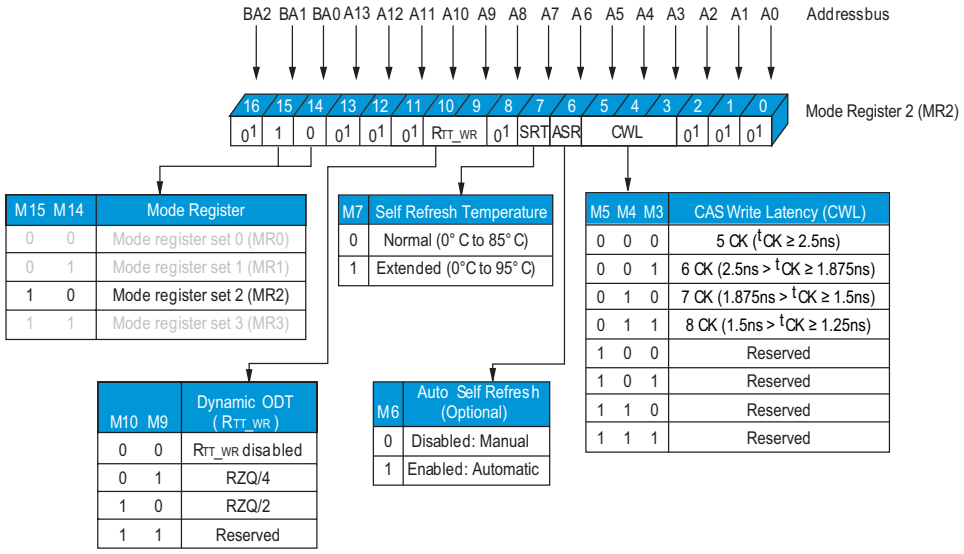
### FIGURE 47- READ LATENCY (AL = 5, CL = 6)



## MODE REGISTER 2 (MR2)

The MODE REGISTER 2 (MR2) controls additional functions and features not available in the other mode registers. These additional functions are CAS WRITE latency (CWL), AUTO SELF REFRESH (ASR), SELF REFRESH TEMPERATURE (SRT) and DYNAMIC ODT ($R_{TT\_WR}$). These functions are controlled via the bits shown in Figure 48. The MR2 is programmed via the MRS command and will retain the stored information until it is programmed again or until the device loses power. Reprogramming the MR2 register will not alter the contents of the memory array, provided that the operation has been performed correctly. The MR2 register must be loaded when all banks are idle and no data bursts are in progress and the memory controller must wait for the specified time $^{t}$MRD and $^{t}$MOD before initiating a subsequent operation.

### FIGURE 48- MODE REGISTER 2 (MR2) DEFINITION




| M15 | M14 | Mode Register |
|---|---|---|
| 0 | 0 | Mode register set 0 (MR0) |
| 0 | 1 | Mode register set 1 (MR1) |
| 1 | 0 | Mode register set 2 (MR2) |
| 1 | 1 | Mode register set 3 (MR3) |

| M7 | Self Refresh Temperature |
|---|---|
| 0 | Normal (0° C to 85° C) |
| 1 | Extended (0°C to 95° C) |

| M5 | M4 | M3 | CAS Write Latency (CWL) |
|---|---|---|---|
| 0 | 0 | 0 | 5 CK ($^{t}$CK ≥ 2.5ns) |
| 0 | 0 | 1 | 6 CK (2.5ns > $^{t}$CK ≥ 1.875ns) |
| 0 | 1 | 0 | 7 CK (1.875ns > $^{t}$CK ≥ 1.5ns) |
| 0 | 1 | 1 | 8 CK (1.5ns > $^{t}$CK ≥ 1.25ns) |
| 1 | 0 | 0 | Reserved |
| 1 | 0 | 1 | Reserved |
| 1 | 1 | 0 | Reserved |
| 1 | 1 | 1 | Reserved |

| M10 | M9 | Dynamic ODT ($R_{TT\_WR}$) |
|---|---|---|
| 0 | 0 | $R_{TT\_WR}$ disabled |
| 0 | 1 | RZQ/4 |
| 1 | 0 | RZQ/2 |
| 1 | 1 | Reserved |

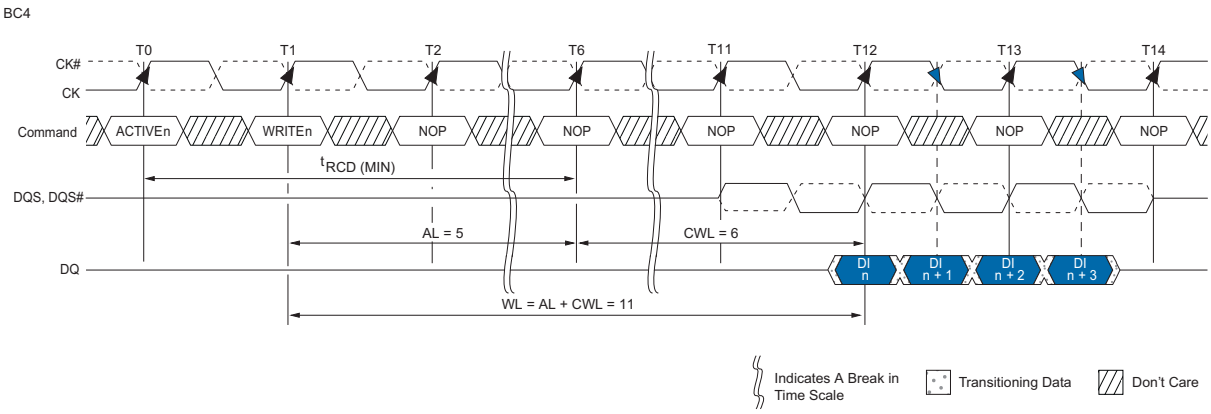
| M6 | Auto Self Refresh (Optional) |
|---|---|
| 0 | Disabled: Manual |
| 1 | Enabled: Automatic |

Notes: 1. MR2[16, 13:11, 8, and 2:0] are reserved for future use and must all be programmed to “0.”

## CAS WRITE LATENCY (CWL)

CWL is defined by MR2[5:3] and is the delay, in clock cycles, from the releasing of the internal WRITE to the latching of the first data in. CWL must be correctly set to the corresponding operating clock frequency (see Figure 48). The overall WRITE LATENCY (WL) is equal to CWL + AL (see Figure 46).

### FIGURE 49- CAS WRITE LATENCY




## AUTO SELF REFRESH (ASR)

Mode register MR2[6] is used to DISABLE/ENABLE the ASR function.

When ASR is DISABLED, the SELF REFRESH mode's REFRESH rate is assumed to be at the normal 85˚C limit (commonly referred to as the 1X REFRESH rate). In the DISABLED mode, ASR requires the user to ensure the SDRAM never exceeds a Tc of 85˚C while in SELF REFRESH unless the user enables the SRT feature listed below, supporting an elevated temp up to +95˚C while in SELF REFRESH.

The standard SELF REFRESH current test specifies test conditions to normal case temperature (85˚C) only, meaning if ASR is enabled, the standard SELF REFRESH current specification does not apply (see the "EXTENDED TEMPERATURE USAGE" description later in this DS).

## SELF REFRESH TEMPERATURE (SRT)

Mode register MR2[7] is used to DISABLE/ENABLE the SRT function. When SRT is Disabled, the SELF REFRESH mode's refresh rate is assumed to be at the normal 85˚C limit. In the DISABLED mode, SRT requires the user to ensure the SDRAM never exceeds the Tc limit of 85˚C while in SELF REFRESH mode unless the user enables ASR.

When SRT is enabled, the SDRAM SELF REFRESH is changed internally from 1X to 2X, regardless of the case temperature (Tc). This enables the user to operate the SDRAM beyond the standard 85˚C limit up to the optional extended temperature range of +95˚C while in SELF REFRESH mode. The standard SELF REFRESH current test specifies test conditions to normal case temperature (85˚C) only, meaning if SRT is enabled, the standard SELF REFRESH current specifications do not apply.

## SRT vs. ASR

If the normal case temperature limit of 85˚C is not exceeded, then neither SRT nor ASR is required, and both can be DISABLED throughout operation. If the extended temperature option is used, the user is required to provide a 2X refresh rate during (manual) refresh for Extended temp devices or 3X refresh rate for Mil-temp devices. SRT and ASR should be enabled for automatic REFRESH services on all devices used in temperature environments ≤95˚C

SRT forces the SDRAM to switch the internal SELF REFRESH rate from 1X to 2X. SELF REFRESH is performed at 2X regardless of Tc.

ASR automatically switches the SDRAM's internal SELF REFRESH rate from 1X to 2X, however, while in SELF REFRESH mode, ASR enables the REFRESH rate automatically adjust between 1X and 2X REFRESH rate over the supported temperature range. One other disadvantage with ASR is the SDRAM cannot always switch from a 1X to a 2X refresh rate at an exact case Temperature of 85˚C. Although the SDRAM will support data integrity when it switches from a 1X to 2X rate, it may switch at a lower temperature than 85˚C.

Since only one mode is necessary at one instant in time, SRT and ASR cannot be simultaneously enabled.

## DYNAMIC ODT

The dynamic ODT (RTT_WR) feature is defined by MR2[10,9]. Dynamic ODT is enabled when a value is selected. This new DDR3 feature enables the ODT termination value to change without issuing an MRS command, essentially changing the ODT termination "on-the-fly".

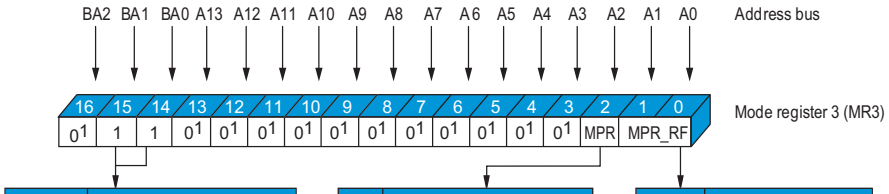
With dynamic ODT (RTT_WR) when beginning a WRITE burst and subsequently switches back to ODT (RTT_WR) is enabled: ODTLCNW, ODTLCNW4, ODTLCNW* ODTH4, ODTH8 and tADC.

Dynamic ODT is only applicable during WRITE cycles, If ODT (RTT_NOM) is disabled, dynamic ODT (RTT_WR) is still permitted. RTT_NOM and RTT_WR can be used independent of one another. Dynamic ODT is not available during WRITE LEVELING mode, regardless of the state of ODT (RTT_NOM). For details on ODT operation, refer to the "On-Die-Termination (ODT)" section.

## MODE REGISTER (MR3)

The mode register 3 (MR3) controls additional functions and features not available via MR0, MR1 or MR2. Currently defined as the MULTIPURPOSE REGISTER (MPR). This function is controlled via the bits shown in Figure 50. The MR3 is programmed via the LOAD MODE command and retains the stored information until it is programmed again or until the device loses power. Reprogramming the MR3 register will not alter the contents of the memory array, provided the programming of the MR3 has been performed correctly. The MR3 register must be loaded when all banks are idle and no data bursts are in progress and the memory controller must wait the specified time tMRD and tMOD before initiating a subsequent operation.

### FIGURE 50 - MODE REGISTER 3 (MR3) DEFINITION




| M15 M14 | Mode Register |
|---|---|
| 0 0 | Mode register set (MR0) |
| 0 1 | Mode register set 1 (MR1) |
| 1 0 | Mode register set 2 (MR2) |
| 1 1 | Mode register set 3 (MR3) |

| M2 | MPR Enable |
|---|---|
| 0 | Normal DRAM operations [2] |
| 1 | Dataflow from MPR |

| M1 M0 | MPR READ Function |
|---|---|
| 0 0 | Predefined pattern [3] |
| 0 1 | Reserved |
| 1 0 | Reserved |
| 1 1 | Reserved |

NOTES:

1. MR3[16 and 13:4] are reserved for future use and must all be programmed to "0."
2. When MPR control is set for normal DRAM operation, MR3[1, 0] will be ignored.
3. Intended to be used for READ synchronization.

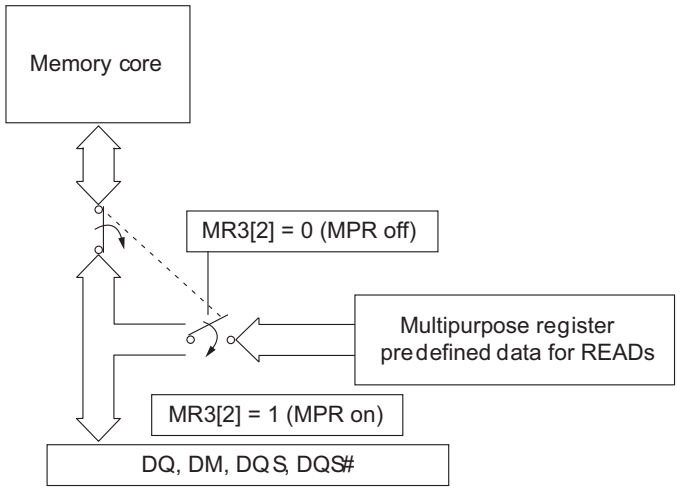
## MULTIPURPOSE REGISTER (MPR)

The MULTIPURPOSE REGISTER function is used to output a predefined system timing calibration bit sequence. Bit 2 is the master bit that enables or disables access to the MPR register and bits 1 and 0 determine which mode the MPR is placed in. The basic concept of the multipurpose register is shown in Figure 51.

If MR3[2] is a "0", then the MPR access is disabled and the SDRAM operates in normal mode. However, if MR3[2] is a "1", then SDRAM no longer outputs normal read data but outputs MPR data as defined by MR3[0,1]. If MR3[0,1] is equal to "00", then a predefined read pattern for system calibration is selected.

To enable the MPR, the MRS command is issued to MR3 and MR3[2]=1 (see Table 66). Prior to issuing the MRS command, all banks must be in the idle state (all banks are precharged, and $^{t}$RP is met). When the MPR is enabled, any subsequent READ or RDAP commands are redirected to the multipurpose register. The resulting operation when either a READ or a RDAP command is issued is defined by MR3[1:0]when MPR is enabled (see Table 67). When the MPR is enabled, only READ or RDAP commands are allowed until a subsequent MRS command is issued with the MPR disabled (MR3[2]=0). POWER-DOWN, SELF REFRESH and any other NON READ or RDAP command is not allowed. The RESET function is supported during MPR enable mode.

### FIGURE 51 - MULTIPURPOSE REGISTER (MPR) BLOCK DIAGRAM




NOTES:

1. A predefined data pattern can be read out of the MPR with an external READ command.
2. MR3[2] defines whether the data flow comes from the memory core or the MPR. When the data flow is defined, the MPR contents can be read out continuously with a regular READ or RDAP command.

**TABLE 66: BURST ORDER**

| MR3[2] MPR | MR3[1:0] MPR READ Function | Function |
|---|---|---|
| 0 | "Don't Care" | Normal Operation, no MPR transaction. All subsequent READs come from the SDRAM memory array. All subsequent WRITEs go to the SDRAM memory array. |
| 1 | A[1:0] (See Table 66) | Enable MPR mode, subsequent READ/RDAP commands defined by bits 1 and 2. |

## MPR FUNCTIONAL DESCRIPTION

The MPR JEDEC definition allows for either a prime DQ0 for lower byte and DQ8 for the upper byte of each of the (4) words contained in the LDI iMOD, to output the MPR data with the remaining DQs driven LOW, or for all DQs to output the MPR data. The MPR readout supports fixed READ burst and READ burst chop (MRS and OTF via A12/BC#) with regular READ latencies and AC timings applicable. This providing the DLL is locked as required.

MPR addressing for a valid MPR READ is as follows:

- A[1:0] must be set to "00" as the burst order is fixed per nibble
- A2 selects the burst order
  - BL8, A2 is set to "0", and the burst order is fixed to 0,1,2,3,4,5,6,7
- For burst chop 4 cases, the burst order is switched on the nibble base and:
  - A2=0: burst order =0,1,2,3
  - A2=1: burst order =4,5,6,7
- Burst order bit 0 (the first bit) is assigned to LSB, and burst order bit 7 (the last bit) is assigned to MSB
- A[9:3] are a "Don't Care"
- A10 is a "Don't Care"
- A11 is a "Don't Care"
- A12: Selects burst chop mode on-the-fly, if enabled within MR0
- A13 is a "Don't Care"
- BA[2:0] are a "Don't Care"

## MPR REGISTER ADDRESS DEFINITIONS and BURSTING ORDER

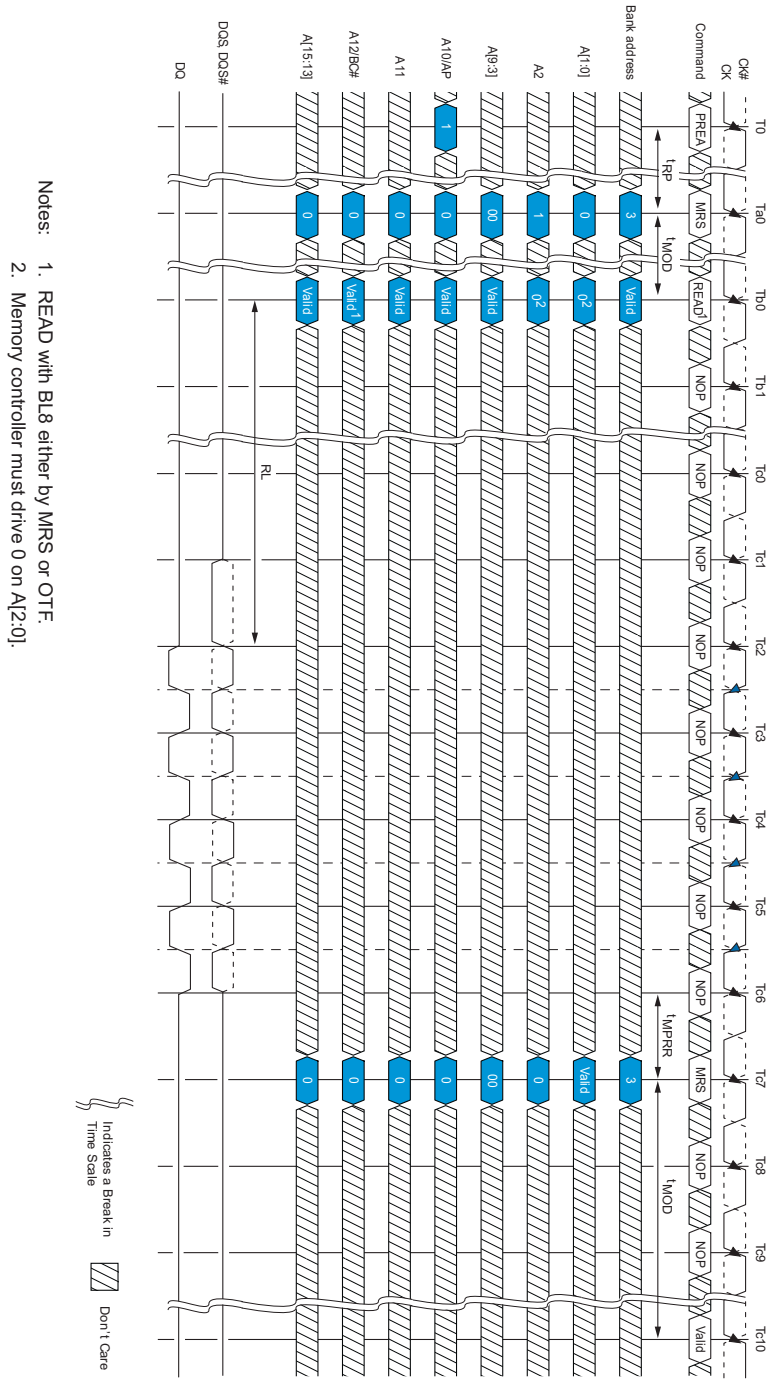
The MPR currently supports a single data format. This data format is a predefined READ pattern for system calibration. The predefined pattern is always a repeating 0-1 bit pattern.

Examples of the different type of predefined READ pattern bursts are shown in Figures 52, 53, and 54.

### TABLE 67: BURST ORDER

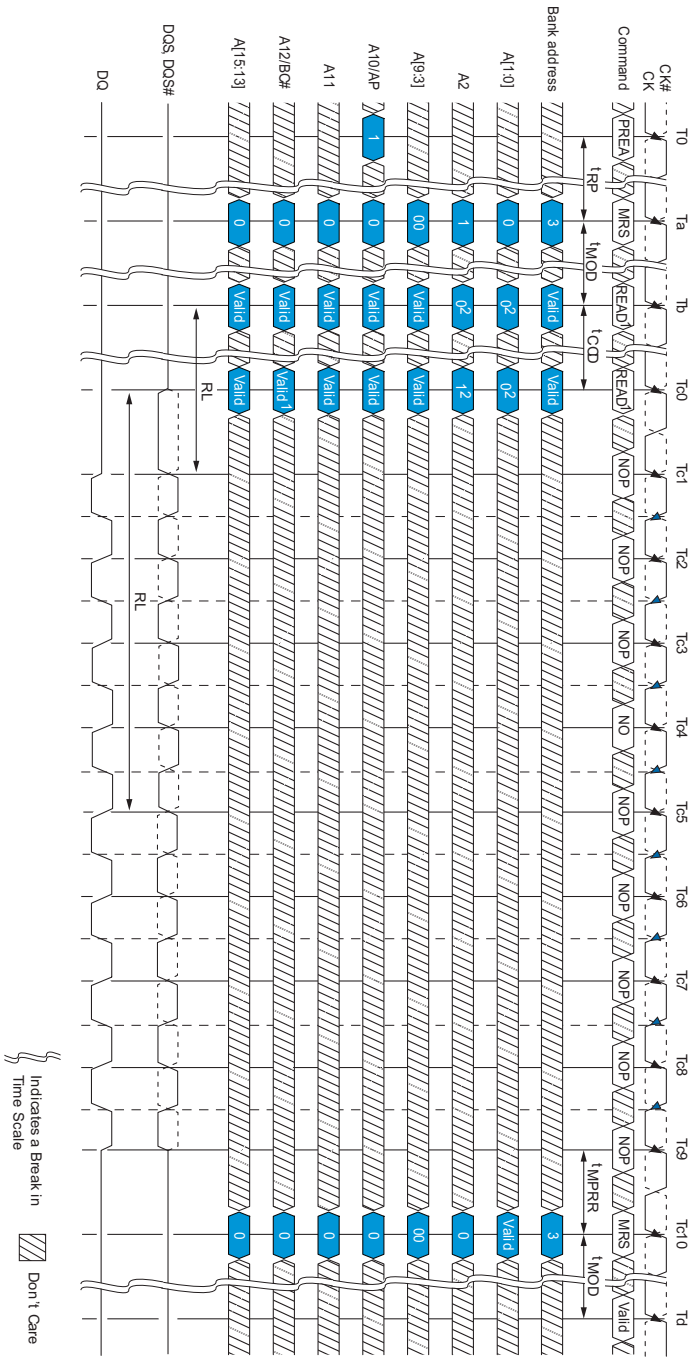
| MR3[2] | MR3[1:0] | Function | Burst Length | Read A[2:0] | Burst Order and Data Pattern |
|---|---|---|---|---|---|
| 1 | 00 | READ predefined pattern for system calibration | BL8 | 000 | Burst Order: 0,1,2,3,4,5,6,7<br>Predefined pattern: 0,1,0,1,0,1,0,1 |
| | | | BC4 | 000 | Burst Order: 0,1,2,3<br>Predefined pattern: 0,1,0,1 |
| | | | BC4 | 100 | Burst Order: 4,5,6,7<br>Predefined pattern: 0,1,0,1 |
| 1 | 01 | RFU | n/a<br>n/a<br>n/a | n/a<br>n/a<br>n/a | n/a<br>n/a<br>n/a |
| 1 | 10 | RFU | n/a<br>n/a<br>n/a | n/a<br>n/a<br>n/a | n/a<br>n/a<br>n/a |
| 1 | 11 | RFU | n/a<br>n/a<br>n/a | n/a<br>n/a<br>n/a | n/a<br>n/a<br>n/a |

## Figure 52 - MPR System Read Calibration with BL8: Fixed Burst Order Single Readout



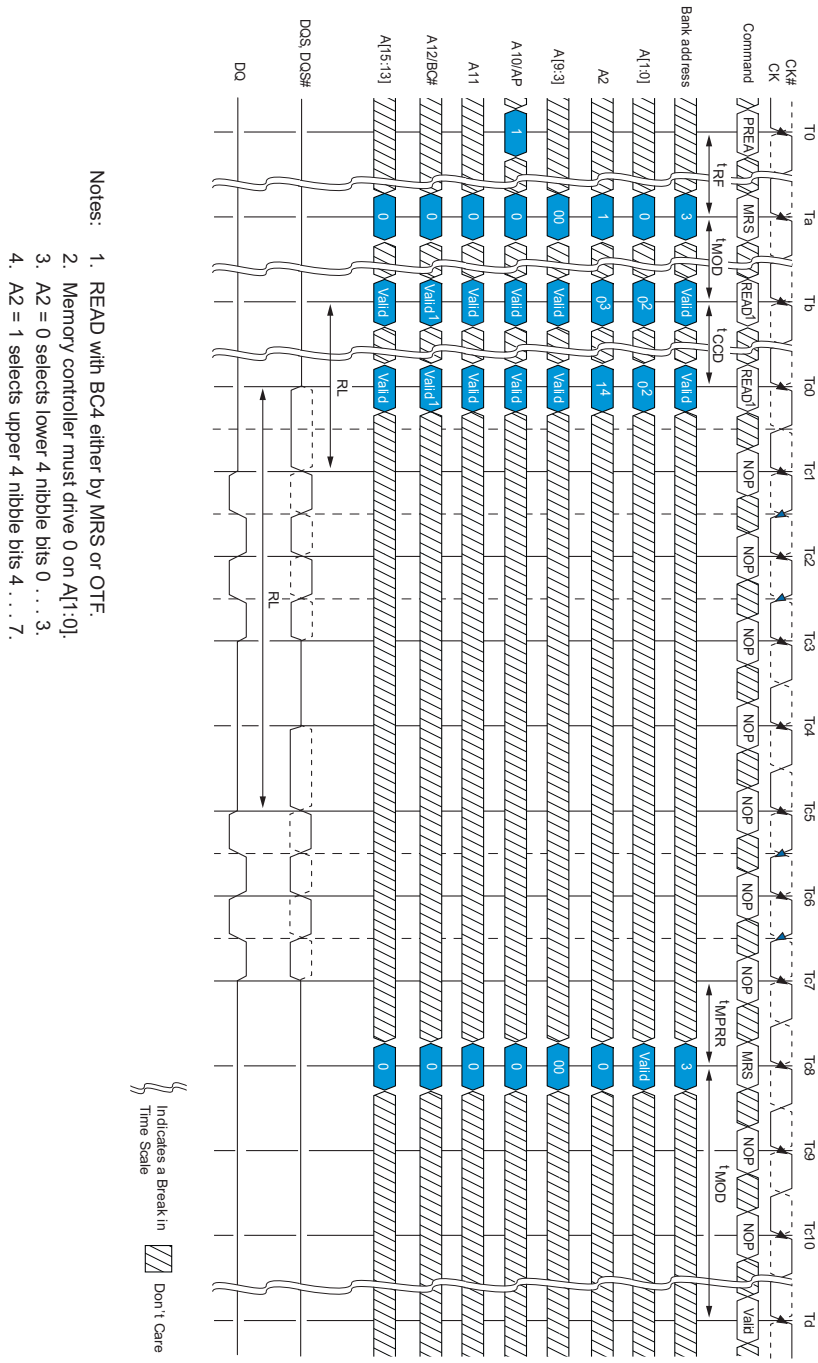

Notes:
1. READ with BL8 either by MRS or OTF.
2. Memory controller must drive 0 on A[2:0].

## Figure 53 - MPR System Read Calibration with BL8: Fixed Burst Order, Back-to-Back Readout



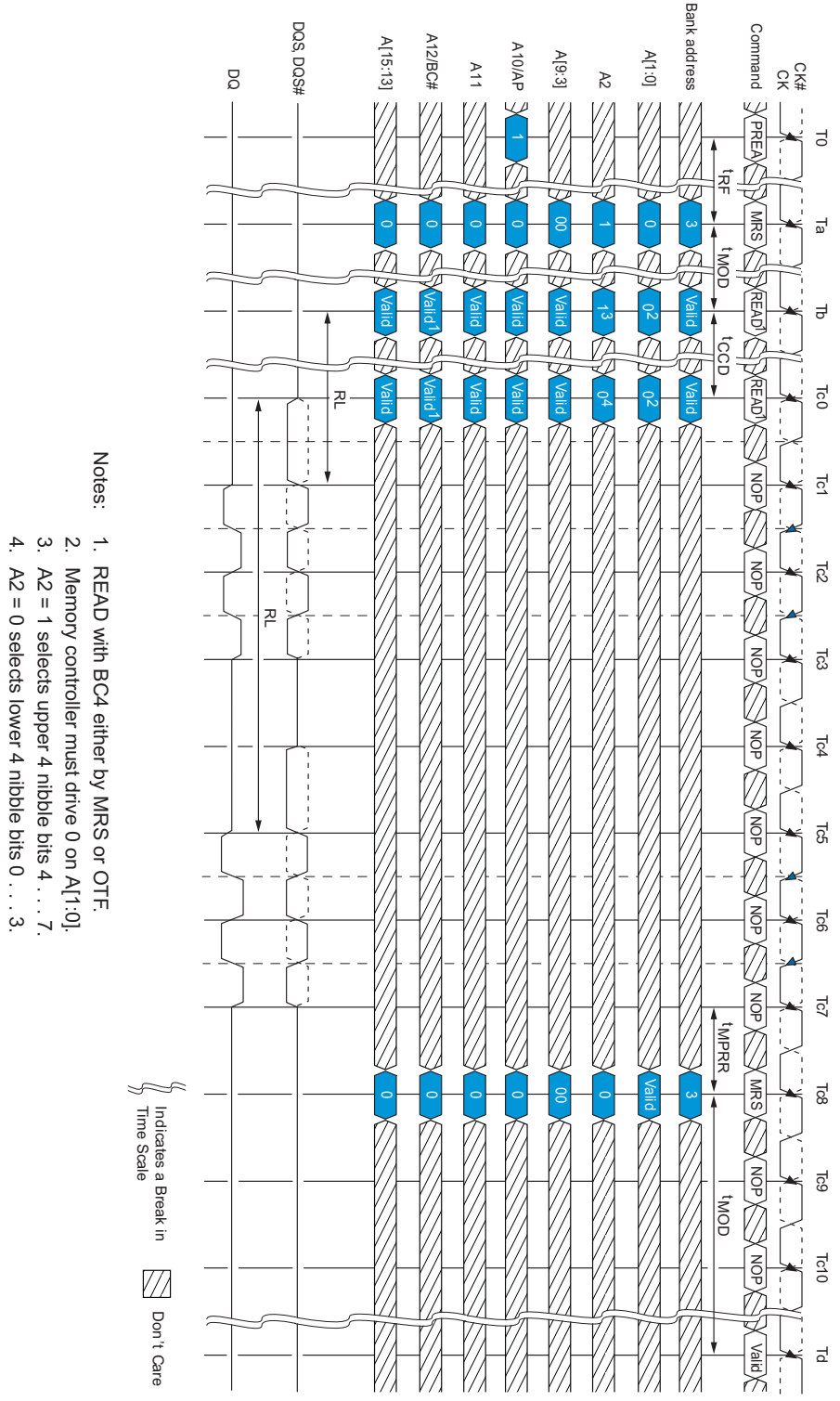

Notes:
1. READ with BL8 either by MRS or OTF.
2. Memory controller must drive 0 on A[2:0].

## Figure 54 - MPR System Read Calibration with BC4: Lower Nibble, Then Upper Nibble




Notes:
1. READ with BC4 either by MRS or OTF.
2. Memory controller must drive 0 on A[1:0].
3. A2 = 0 selects lower 4 nibble bits 0 . . . 3.
4. A2 = 1 selects upper 4 nibble bits 4 . . . 7.

## Figure 55 - MPR System Read Calibration with BC4: Upper Nibble, Then Lower Nibble




Notes:
1. READ with BC4 either by MRS or OTF.
2. Memory controller must drive 0 on A[1:0].
3. A2 = 1 selects upper 4 nibble bits 4 . . . 7.
4. A2 = 0 selects lower 4 nibble bits 0 . . . 3.

## MPR READ PREDEFINED PATTERN

The predetermined READ calibration pattern is a fixed pattern of 0,1,0,1,0,1,0,1. The following is an example of using the READ out predetermined READ calibration pattern. The example is to perform multiple READS from the MULTIPURPOSE REGISTER (MPR) in order to do system level READ timing calibration based on the predetermined and standardized pattern.

The following protocol outlines the steps used to perform the READ calibration:

- Precharge all banks
- After $^{t}$RP is satisfied, set MRS, MR3[2] = 1 and MR3[1:0]=00. This redirects all subsequent READs and Loads the predefined pattern into the MPR. As soon as $^{t}$MRD and $^{t}$MOD are satisfied, the MPR is available.
- Data WRITE operations are not allowed until the MPR returns to the normal SDRAM state
- Issue a READ with burst order information (all other address pins are “Don’t Care”):
  - A[1:0] = 00 (data burst order is fixed starting at nibble)
  - A2 = 0 (for BL8, burst order is fixed as 0,1,2,3,4,5,6,7)
  - A12 = 1 (use BL8)
- After RL = AL + CL, the SDRAM bursts out the predefined READ calibration pattern (0,1,0,1,0,1,0,1)
- The memory controller repeats the calibration READs until READ data capture at the memory controller is optimized
- After the last MPR READ burst and after $^{t}$MPRR has been satisfied, issue MRS, MR3[2] = 0 and MR3[1:0] = “Don’t Care” to the normal SDRAM state. All subsequent READ and WRITE accesses will be regular READS and WRITES from/to the SDRAM array
- When $^{t}$MRD and $^{t}$MOD are satisfied from the last MRS, the regular SDRAM commands (such as ACTIVATE a Memory bank for regular READ or WRITE access) are permitted

## MODE REGISTER SET (MRS)

The mode registers are loaded via inputs BA[2:0], A[13:0]. BA[2:0] determines which mode register is programmed:

- BA2 = 0, BA1 = 0, BA0 = 0 for MR0
- BA2 = 0, BA1 = 0, BA0 = 1 for MR1
- BA2 = 0, BA1 = 1, BA0 = 0 for MR2
- BA2 = 0, BA1 = 1, BA0 = 1 for MR3

The MRS command can only be issued (or reissued) when all banks are idle and in the precharged state ($^{t}$RP is satisfied and no data bursts are in progress). The controller must wait the specified time $^{t}$MRD before initiating a subsequent operation such as an ACTIVATE command. There is also a restriction after issuing an MRS command with regard to when the updated functions become available. This parameter is specified by $^{t}$MOD. Both $^{t}$MRD and $^{t}$MOD parameters are shown in Figure 42 and 43. Violating either of these requirements will result in unspecified operation.

## ZQ CALIBRATION

The ZQ CALIBRATION command is used to calibrate the SDRAM output drivers (RON) and ODT values ($R_{TT}$) over process, voltage, and temperature, provided a dedicated 240Ω (±1%) external resistor is connected from the SDRAM’s ZQ ball to VssQ.

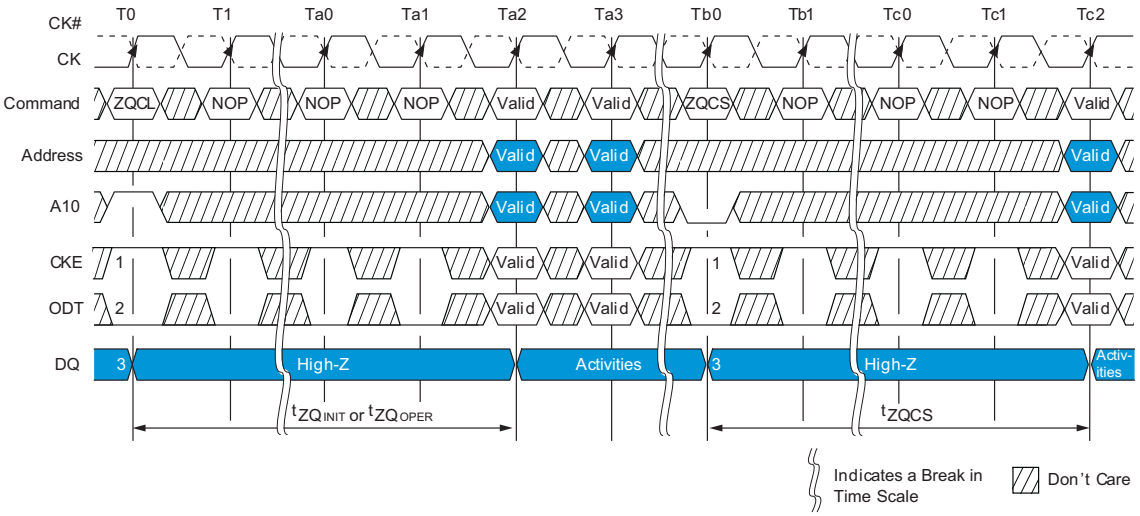
DDR3 SDRAMs need a longer time to calibrate $R_{ON}$ and ODT at power up INITIALIZATION and SELF REFRESH exit and a relatively shorter time to perform periodic calibrations. DDR3 SDRAM defines two ZQ CALIBRATION commands: ZQ CALIBRATION LONG (ZQCL) and ZQ CALIBRATION SHORT (ZQCS). An example of ZQ CALIBRATION timing is shown in Figure 56.

All banks must be PRECHARGED and $^{t}$RP must be met before ZQCL or ZQCS commands can be issued to the SDRAM. No other activities (other than another ZQCL or ZQCS command may be issued to the SDRAM) can be performed on the SDRAM array by the controller for the duration of $^{t}$ZQINIT or $^{t}$ZQOPER. The quiet time on the SDRAM array helps accurately calibrate $R_{ON}$ and ODT. After SDRAM calibration is achieved, the SDRAM should disable the ZQ ball’s current consumption path to reduce overall power usage.

ZQ CALIBRATION commands can be issued in parallel to DLL RESET and locking time. Upon SELF REFRESH exit, an explicit ZQCL is required if ZQ CALIBRATION is desired.

In dual rank system designs that share the ZQ resistor between devices, the controller must not allow overlap of $^{t}$ZQINT, $^{t}$ZQOPER or $^{t}$ZQCS between ranks.

## FIGURE 56 - ZQ CALIBRATION TIMING (ZQCL AND ZQCS)




NOTES:

1. CKE must be continuously registered HIGH during the calibration procedure.
2. ODT must be disabled via the ODT signal or the MRS during the calibration procedure.
3. All devices connected to the DQ bus should be High-Z during calibration.

## ACTIVATE

Before any READ or WRITE commands can be issued to a bank within the SDRAM, a ROW in that bank must be opened (ACTIVATED). This is accomplished via the ACTIVATE command, which selects both the BANK and the ROW to be ACTIVATED.

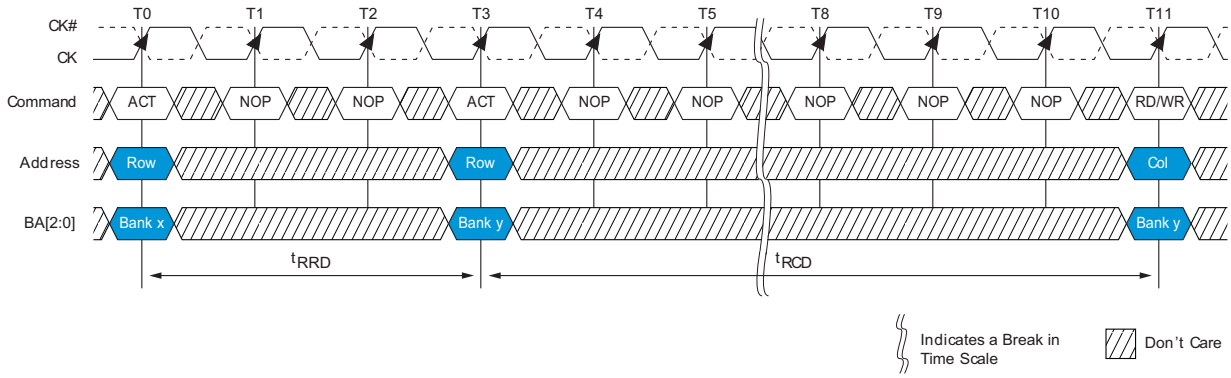
After a ROW is opened with an ACTIVATE command, a READ or WRITE command may be issued to that ROW, subject to the $^{t}$RCD specification. However, if the additive latency is programmed correctly, a READ or WRITE command may be issued prior to $^{t}$RCD (MIN). In this operation, the SDRAM enables a READ or WRITE command to be issued after the ACTIVATE command for that bank, but prior to $^{t}$RCD (MIN) (see "POSTED CAS ADDITIVE LATENCY (AL)). $^{t}$RCD (MIN) should be divided by the clock period and rounded up to the next whole number to determine the earliest clock edge after the ACTIVATE command on which the READ or WRITE command can be entered. The same procedure is used to convert other specification limits from time units to clock cycles.

When at least one bank is open, any READ-to-READ command delay or WRITE-to-WRITE command delay is restricted to $^{t}$CCD (MIN).

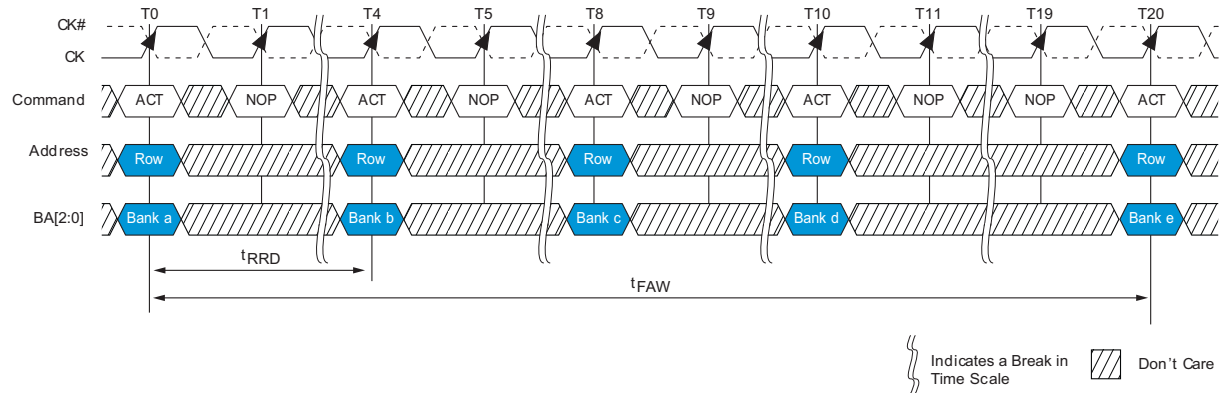
A subsequent ACTIVATE command to a different ROW in the same BANK can only be issued after the previous ACTIVE ROW has been closed (PRE-CHARGED). The minimum time interval between successive ACTIVATE commands to the same BANK is defined by $^{t}$RC.

A subsequent ACTIVATE command to another BANK can be issued while the first BANK is being accessed, which results in a reduction of total ROW-ACCESS overhead. The minimum time interval between successive ACTIVATE commands may be issued in a given $^{t}$FAW (MIN) period, and the $^{t}$RRD (MIN) restriction still applies. The $^{t}$FAW (MIN) parameter applies, regardless of the number of BANKS already opened or closed.

## FIGURE 57 - EXAMPLE: MEETING tRRD (MIN) AND tRCD (MIN)




## FIGURE 58 - EXAMPLE: tFAW

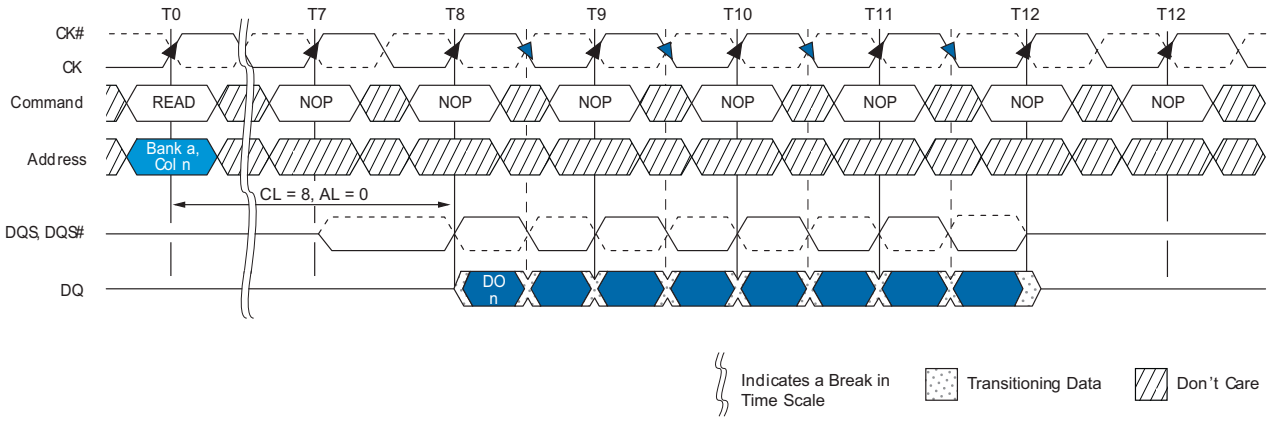


## READ

READ bursts are initiated with a READ command. The starting COLUMN and BANK addresses are provided with the READ command and AUTO PRECHARGE is either enabled or disabled for that burst access. If AUTO PRECHARGE is enabled, the ROW being accessed is automatically PRECHARGED at the completion of the burst sequence. If AUTO PRECHARGE is disabled, the ROW will be left open after the completion of the burst.

During READ bursts, the valid data out element from the starting column address is available at READ LATENCY (RL) clocks later. RL is defined as the sum of POSTED CAS ADDITIVE LATENCY (AL) and CAS LATENCY (CL) (RL = AL + CL). The value of AL and CL is programmable in the mode register via the MRS command. Each subsequent data-out element will be valid nominally at the next positive or negative clock edge (that is, at the next crossing of CK and CK\). Figure 59 shows an example of RL based on a CL setting of 8 as well as AL=0.

### FIGURE 59 - READ LATENCY




Notes: 1. DO n = data-out from column n.
2. Subsequent elements of data-out appear in the programmed order following DO n.

L[U]DQSx, L[U]DQSx\ is driven by the SDRAM along with the output data. The initial LOW state on L[U]DQSx and HIGH state on L[U]DQSx\, is known as the READ preamble ($^{t}$RPRE). The LOW state on DQSx and the HIGH state on L[U]DQSx\, coincident with the last data-out element, is known as the READ postamble ($^{t}$RPST). Upon completion of a burst, assuming no other commands have been initiated, the DQ will go HIGH-Z. A detailed explanation of $^{t}$DQSQ (valid data-out skew), $^{t}$QH (data-out window hold), and the valid data window are depicted in Figure 71. A detailed explanation of $^{t}$DQSCK (DQS transition skew to CK) is also depicted in Figure 71.

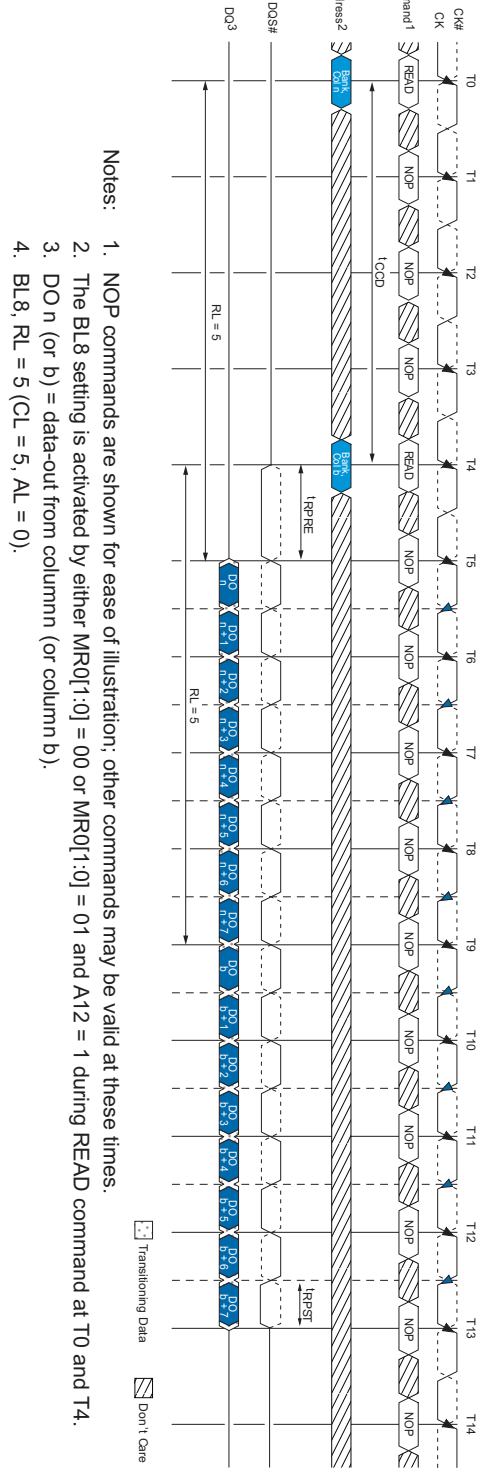
Data from any READ burst may be concatenated with data from a subsequent READ command to provide a continuous flow of data. The first data element from the new burst follows the last element of a completed burst. The new READ command should be issued $^{t}$CCD cycles after the first READ command. This is shown for BL8 in Figure 60. If BC4 is enabled, $^{t}$CCD must still be met which will cause a gap in the data output, as shown in Figure 61. Nonconsecutive READ data is reflected in Figure 62. DDR3 SDRAMs do not allow interrupting or truncating any READ burst.

Data from any READ burst must be completed before a subsequent WRITE burst is allowed. An example of a READ burst followed by a WRITE burst for BL8 is shown in Figure 63. To ensure the READ data is completed before the WRITE data is on the bus, the minimum READ-to-WRITE timing is RL + $^{t}$CCD – WL + 2$^{t}$CK.

A READ burst may be followed by a PRECHARGE command to the same bank provided AUTO PRECHARGE is not ACTIVATED. The minimum READ-to-PRECHARGE command spacing to the same bank is four clocks and must also satisfy a minimum analog time from the READ command. This time is called $^{t}$RTP (READ-to-PRECHARGE). $^{t}$RTP starts AL cycles later than the READ command. Examples for BL8 are shown in Figure 65 and BC4 in Figure 66. Following the PRECHARGE command, a subsequent command to the same bank cannot be issued until $^{t}$RP is met. The PRECHARGE command followed by another PRECHARGE command to the same bank is allowed. However, the precharge period will be determined by the last PRECHARGE command issued to the bank.

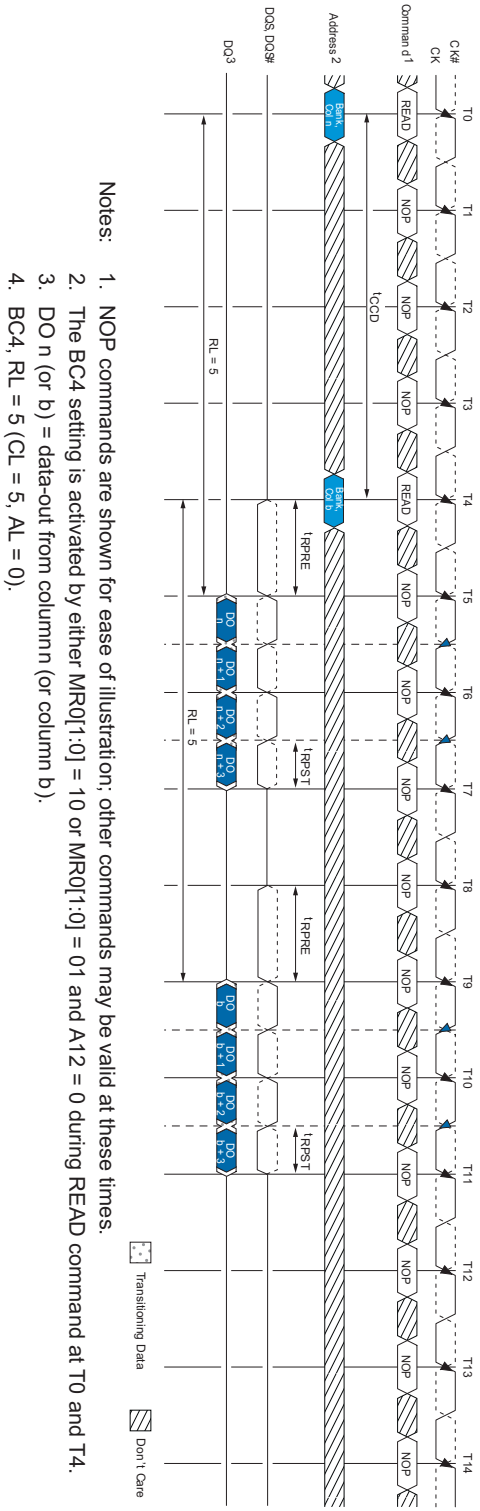
If A10 is HIGH when a READ command is issued, the READ with AUTO PRECHARGE function is engaged. The SDRAM starts an AUTO PRECHARGE operation on the rising edge which is AL + $^{t}$RTP cycles after the READ command. DDR3 SDRAMs support a $^{t}$RAS lockout feature (see Figure 68). If $^{t}$RAS (MIN) is not satisfied at the edge, the starting point of the AUTO PRECHARGE operation will be delayed until $^{t}$RAS (MIN) is satisfied. In case the internal PRECHARGE operation is pushed out by $^{t}$RTP, $^{t}$RP starts at the point at which the internal PRECHARGE happens. The time from READ with AUTO PRECHARGE to the next ACTIVATE command the same bank is AL + ($^{t}$RTP + $^{t}$RP)*, where "*" means rounded up to the next integer. In any event, internal RECHARGE does not start earlier than four clocks after the last 8n-bit prefetch.

## Figure 60 - Consecutive READ Bursts (BL8)



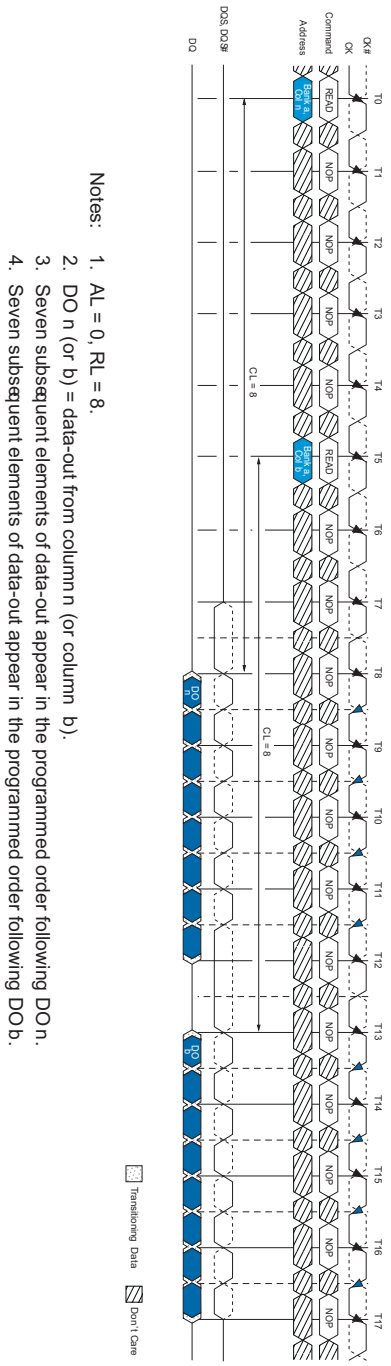

Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during READ command at T0 and T4.
3. DO n (or b) = data-out from columnn (or column b).
4. BL8, RL = 5 (CL = 5, AL = 0).

## Figure 61 - Consecutive READ Bursts (BC4)



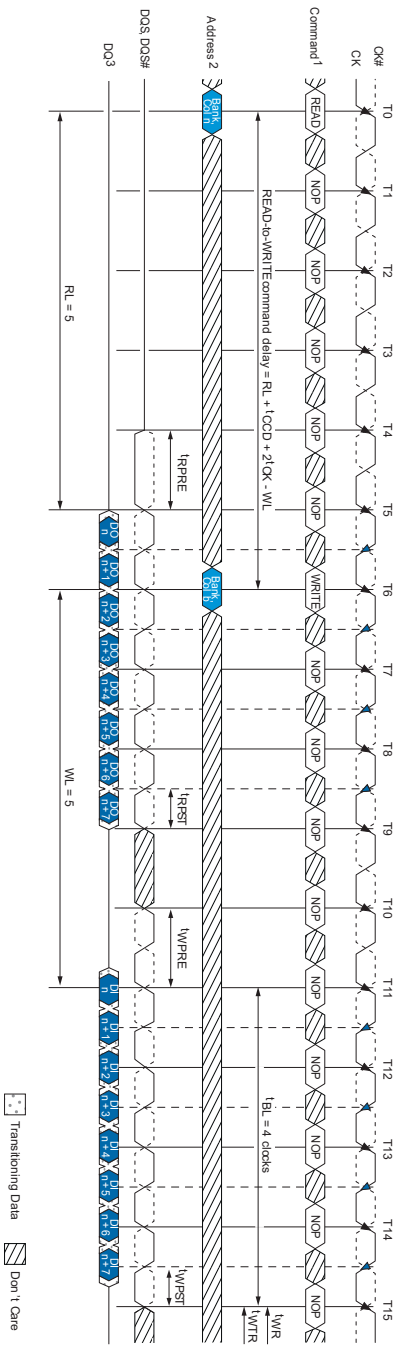

Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BC4 setting is activated by either MR0[1:0] = 10 or MR0[1:0] = 01 and A12 = 0 during READ command at T0 and T4.
3. DO n (or b) = data-out from columnn (or column b).
4. BC4, RL = 5 (CL = 5, AL = 0).

## Figure 62 - Nonconsecutive READ Bursts



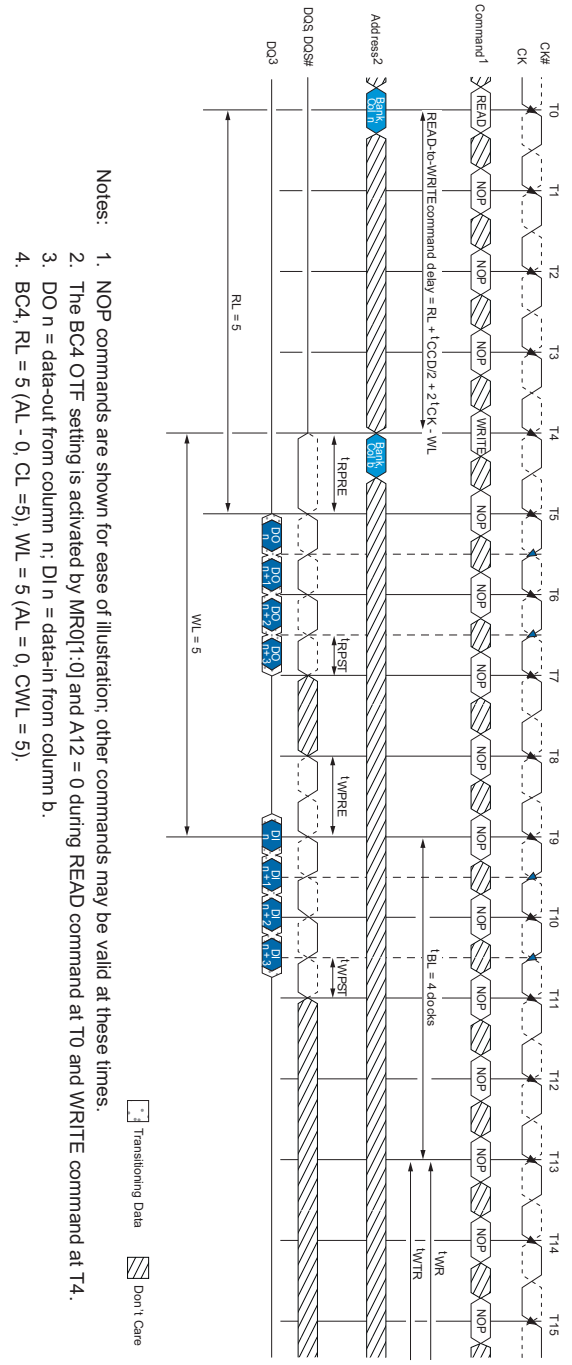

Notes:
1. AL = 0, RL = 8.
2. DO n (or b) = data-out from column n (or column b).
3. Seven subsequent elements of data-out appear in the programmed order following DO n.
4. Seven subsequent elements of data-out appear in the programmed order following DO b.

## Figure 63 - READ (BL8) to WRITE (BL8)



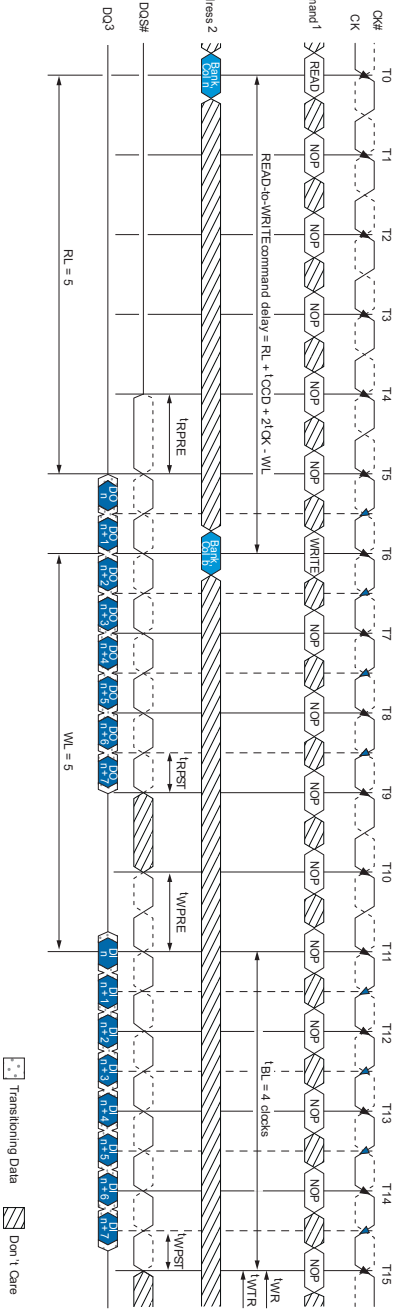

Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during the READ command at T0, and the WRITE command at T6.

## Figure 64 - READ (BC4) to WRITE (BC4) OTF



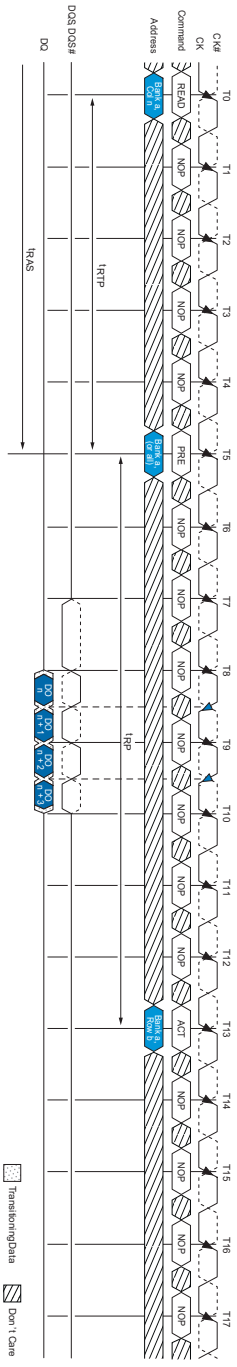

Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BC4 OTF setting is activated by MR0[1:0] and A12 = 0 during READ command at T0 and WRITE command at T4.
3. DO n = data-out from column n; DI n = data-in from column b.
4. BC4, RL = 5 (AL - 0, CL =5), WL = 5 (AL = 0, CWL = 5).

## Figure 65 - READ to PRECHARGE (BL8)

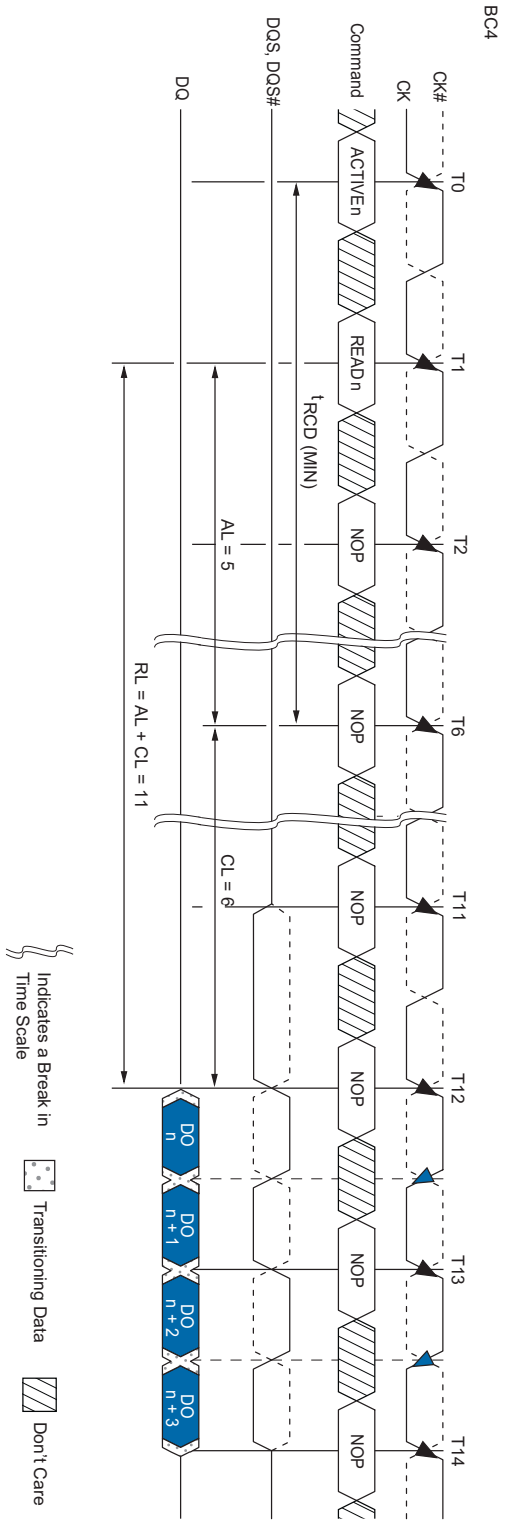



Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during the READ command at T0, and the WRITE command at T6.
3. DO n = data-out from column, DIb = data-in for column b.
4. BL8, RL = 5 (AL = 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

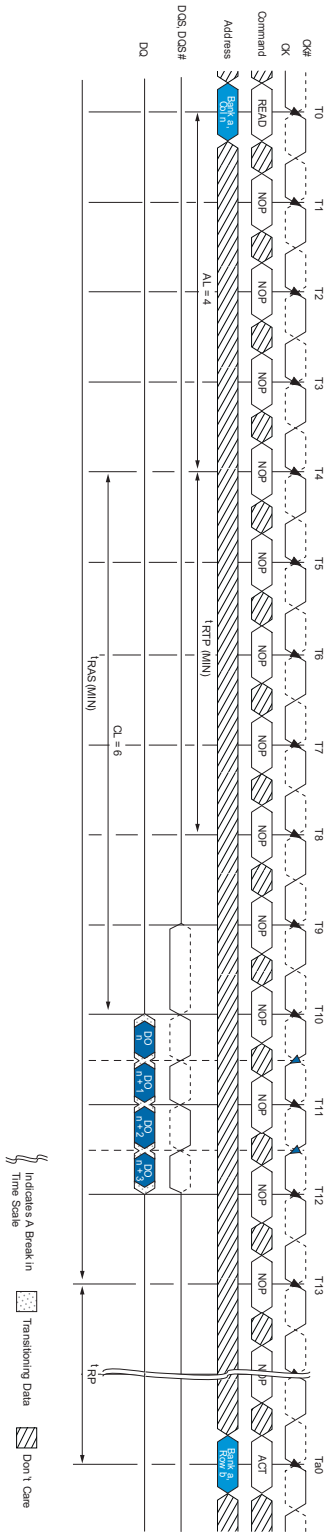
## Figure 66 - READ to PRECHARGE (BC4)



## Figure 67 - READ to PRECHARGE (AL = 5, CL = 6)



## Figure 68 - READ with Auto Precharge (AL = 4, CL = 6)



## READ

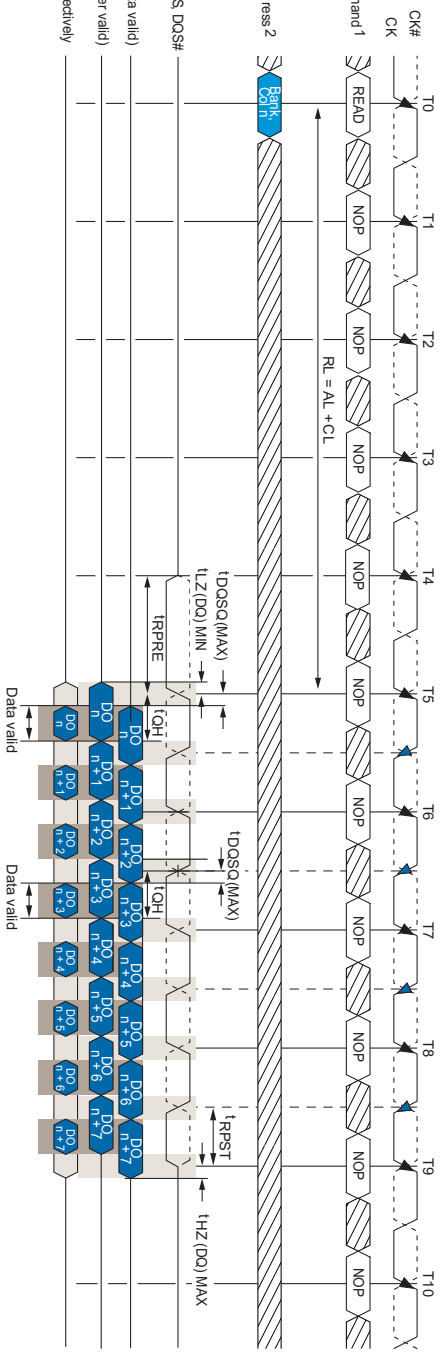
A DQSx to DQ output timing is shown in Figure 69. The DQ transitions between valid data outputs must be within $^{t}$DQSQ of the crossing point of L[U]DQSx, L[U]DQSx\. DQS must also maintain a minimum HIGH and LOW time of $^{t}$QSH and $^{t}$QSL. Prior to the READ preamble, the DQ balls will either be floating or terminated depending on the status of the ODT signal.

Figure 70 shows the strobe-to-clock timing during a READ. The crossing point DQSx, DQSx\ must transition with ± $^{t}$DQSCK of the clock crossing point. The data out has no timing relationship to clock, only to DQS, as shown in Figure 70.

Figure 70 also shows the READ preamble and postamble. Normally, both DQSx and DQSx\ are HIGH-Z to save power (VccQ). Prior to data output from the SDRAM, DQSx is driven LOW and DQSx\ driven HIGH for $^{t}$RPRE. This is known as the READ preamble.

The READ postamble, $^{t}$RPST, is one half clock from the last L[U]DQSx, L[U]DQSx\ transition. During the READ postamble, L[U]DQSx is driven LOW and L[U]DQSx\ driven HIGH. When complete, the DQ will either be disabled or will continue terminating depending on the state of the ODT signal. Figure 75 demonstrates how to measure $^{t}$RPST.

## Figure 69 - Data Output Timing – $^{t}$DQSQ and Data Valid Window



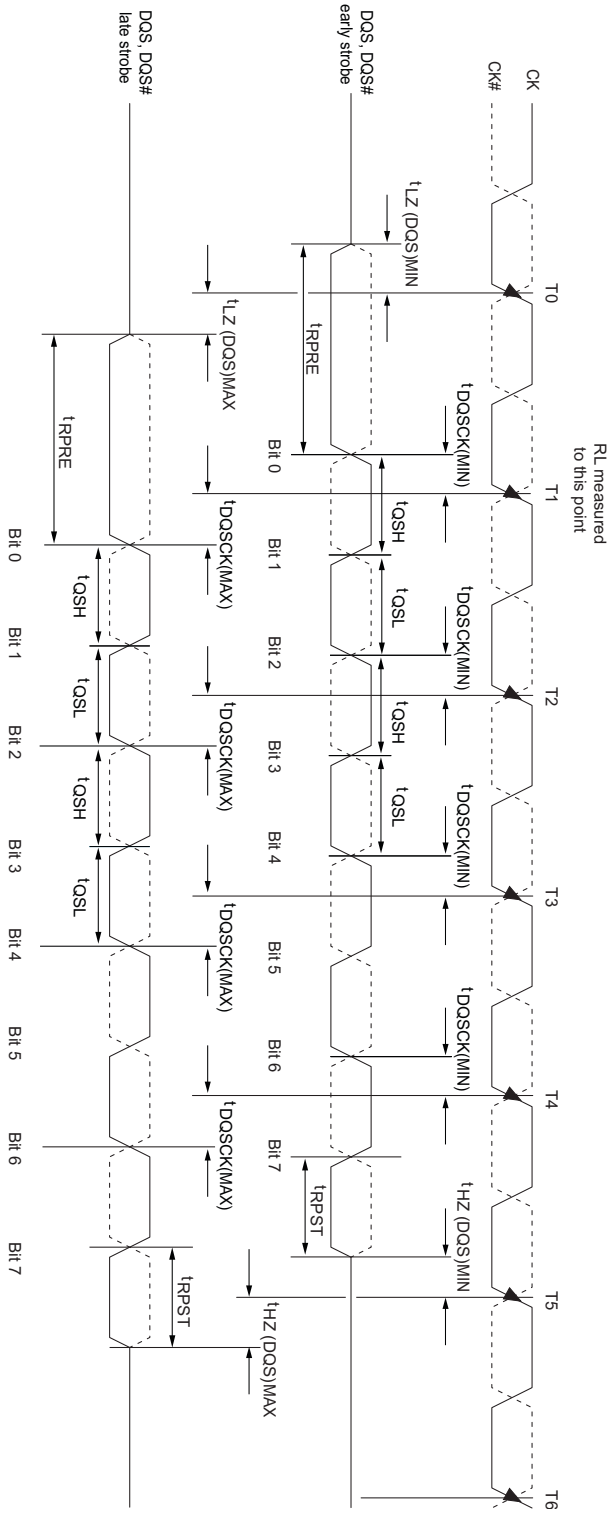

Notes:

1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1, 0] = 0, 0 or MR0[0, 1] = 0, 1 and A12 = 1 during READ command at T0.
3. DO n = data-out from column n.
4. BL8, RL = 5 (AL = 0, CL = 5).
5. Output timings are referenced to $V_{CCQ}$/2 and DLL on and locked.
6. $^{t}$DQSQ defines the skew between DQS, DQS# to data and does not define DQS, DQS# to clock.
7. Early data transitions may not always happen at the same DQ. Data transitions of a DQ can vary (either early or late) within a burst.

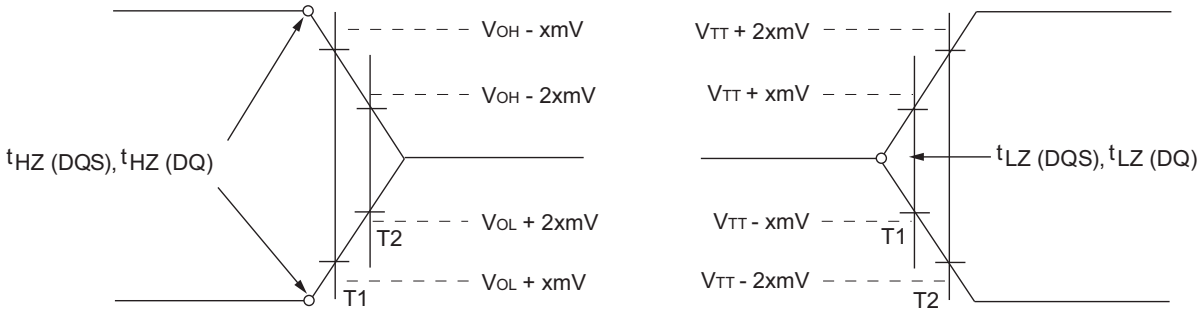
## OUTPUT TIMING

$^{t}$HZ and $^{t}$LZ transitions occur in the same access time as valid data transitions. These parameters are referenced to a specific voltage level which specifies when the device output is no longer driving $^{t}$HZ (DQS) and $^{t}$HZ (DQ) or begins driving $^{t}$LZ (DQS). $^{t}$LZ (DQ), Figure 71 shows a method to calculate the point when the device is not longer driving $^{t}$HZ (DQS) and $^{t}$HZ (DQ) or begins driving $^{t}$LZ (DQS), $^{t}$LZ (DQ) by measuring the signal at two different voltages. The actual voltage measurement points are not critical as long as the calculation is consistent. The parameters $^{t}$LZ (DQS), $^{t}$LZ (DQ), $^{t}$HZ (DQS) and $^{t}$HZ (DQ) are defined as single-ended.

## Figure 70 - Data Strobe Timing – READs



## Figure 71 - Method for Calculating tLZ and tHZ

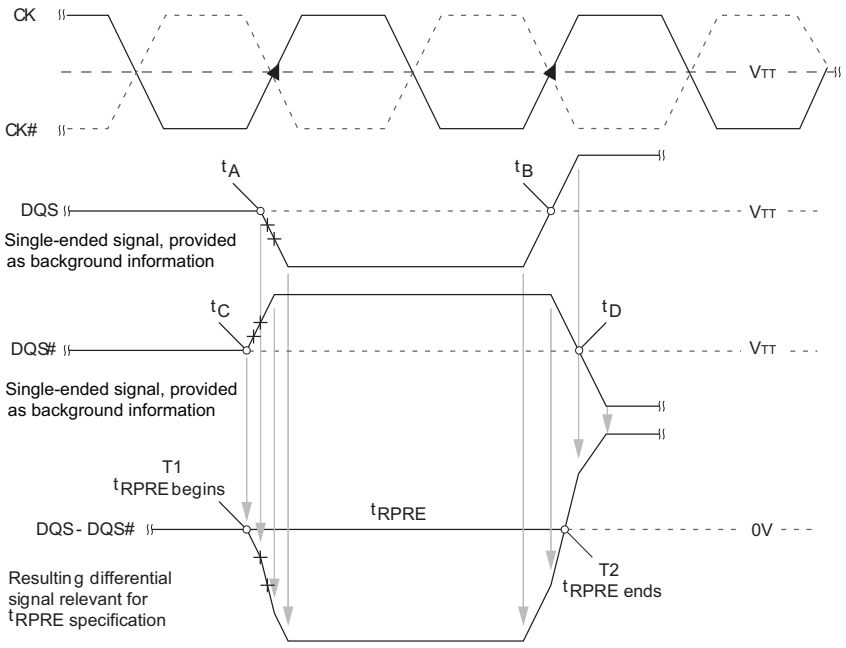



tHZ (DQS), tHZ (DQ) end point = 2 × T1 - T2

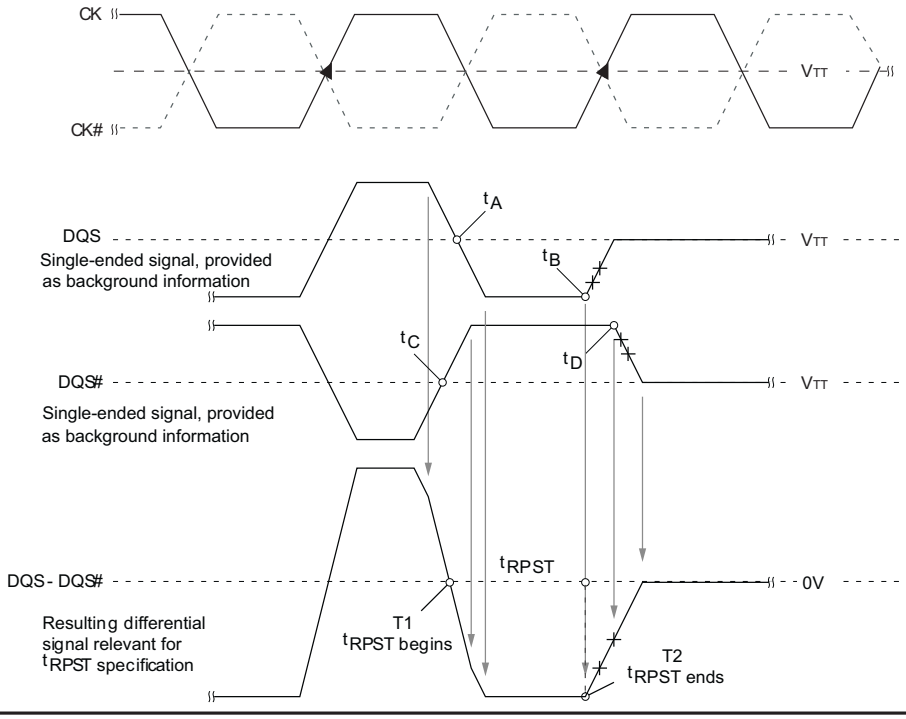
tLZ (DQS), tLZ (DQ) begin point = 2 × T1 - T2

Notes:
1. Within a burst, the rising strobe edge is not necessarily fixed at tDQSCK (MIN) or tDQSCK (MAX). Instead, the rising strobe edge can vary between tDQSCK (MIN) and tDQSCK (MAX).
2. The DQS high pulse width is defined by tQSH, and the DQS low pulse width is defined by tQSL. Likewise, tLZ (DQS) MIN and tHZ (DQS) MIN are not tied to tDQSCK (MIN) (early strobe case) and tLZ (DQS) MAX and tHZ (DQS) MAX are not tied to tDQSCK (MAX) (late strobe case); however, they tend to track one another.
3. The minimum pulse width of the READ preamble is defined by tRPRE (MIN). The minimum pulse width of the READ postamble is defined by tRPST (MIN).

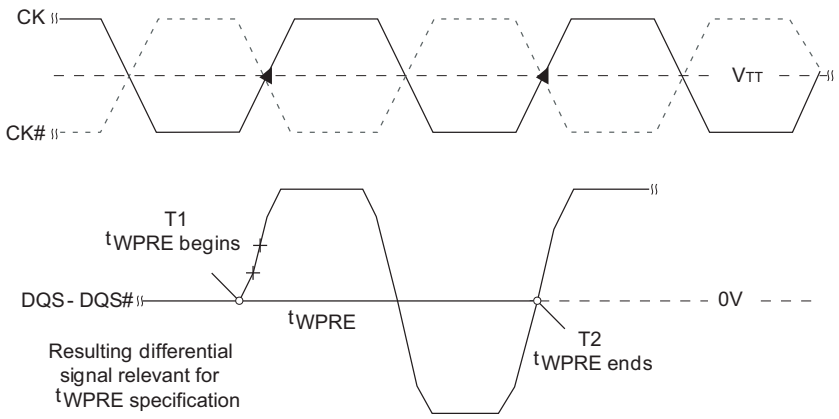
## FIGURE 72 - tRPRE TIMING



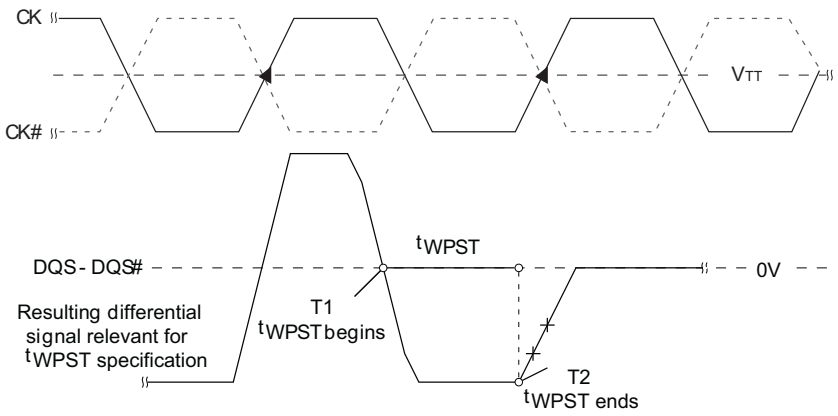

## FIGURE 73 - tRPST TIMING



## FIGURE 74 - $^{t}$WPRE TIMING




## FIGURE 75 - $^{t}$WPST TIMING



## WRITE

WRITE bursts are initiated with a WRITE command. The starting COLUMN and BANK addresses are provided with the WRITE command, and AUTO PRECHARGE is selected, the ROW being accessed will be PRECHARGED at the end of WRITE burst. If AUTO PRECHARGE is not selected, the ROW will remain open for subsequent accesses. After a WRITE command has been issued, the WRITE burst may not be interrupted. For the generic WRITE commands used in Figure 76 though Figure 84, AUTO PRECHARGE is disabled.

During WRITE bursts, the first valid data-in element is registered on a rising edge of DQSx following the WRITE LATENCY (WL) clocks later and subsequent data elements will be registered on successive edges of DQSx. WRITE LATENCY (WL) is defined as the sum of POSTED CAS ADDITIVE LATENCY (AL) and CAS WRITE LATENCY (CWL): WL = AL + CWL. The values of AL and CWL are programmed in the MR- and MR2 registers, respectively. Prior to the first valid DQSx edge, a full cycle is needed (including a dummy crossover of DQSx, DQSx\) and specified as the WRITE preamble shown in Figure 76. The half cycle on DQSx following the last data-in element is known as the WRITE postamble.

The time between the WRITE command and the first valid edge of DQSx is WL clocks ± $^{t}$DQSS. Figure 77 through Figure 84 show the nominal case where $^{t}$DQSS = 0ns; however, Figure 76 includes $^{t}$DQSS (MIN) and $^{t}$DQSS (MAX) cases.

Data may be masked from completing a WRITE using data mask. The mask occurs on the DM ball aligned to the WRITE data. If DM is LOW, the WRITE completes normally. If DM is HIGH, that bit of data is masked.

Upon completion of a burst, assuming no other commands have been initiated, the DQ will remain HIGH-Z and any additional input data will be ignored.

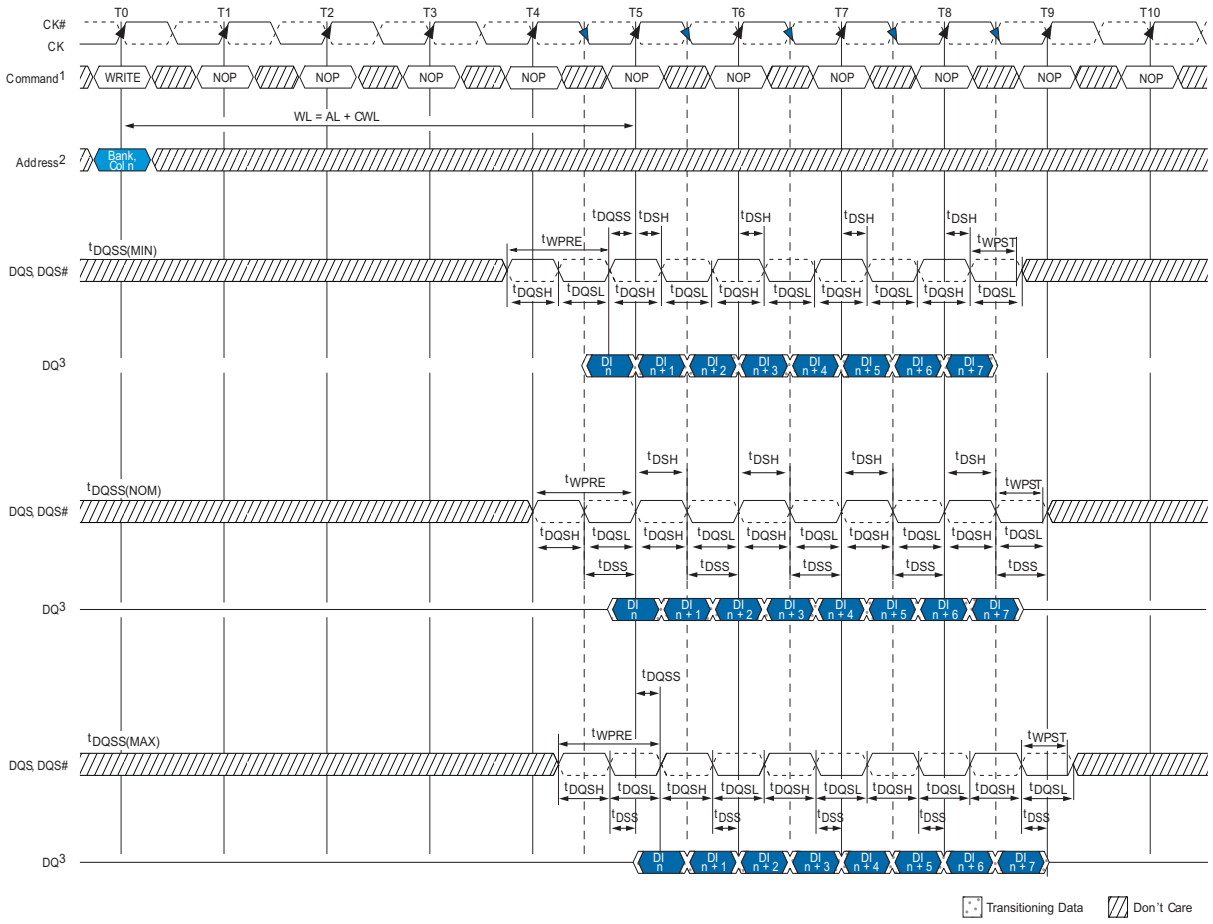
Data for any WRITE burst may be concatenated with a subsequent WRITE command to provide a continuous flow of input data. The new WRITE command can be $^{t}$CCD clocks following the previous WRITE command. The first data element from the new burst is applied after the last element of a completed burst. Figures 77 and 78 show concatenated bursts. An example of nonconsecutive WRITES is shown in Figure 79.

Data for any WRITE burst may be followed by a subsequent READ command after $^{t}$WTR has been met (see Figures 80, 81 and 82).

Data for any WRITE burst may be followed by a subsequent PRECHARGE command providing $^{t}$WR has been met, as shown in Figure 83 and Figure 84.

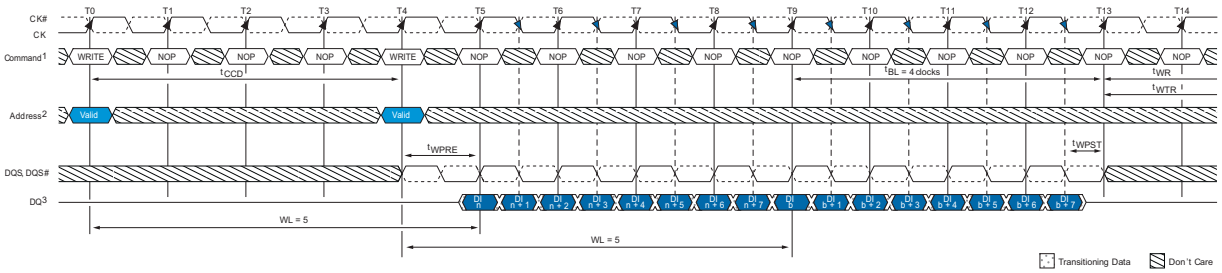
Both $^{t}$WTR and $^{t}$WR starting time may vary depending on the mode register settings (fixed BC4, BL8 vs. OTF).

## FIGURE 76 - WRITE BURST



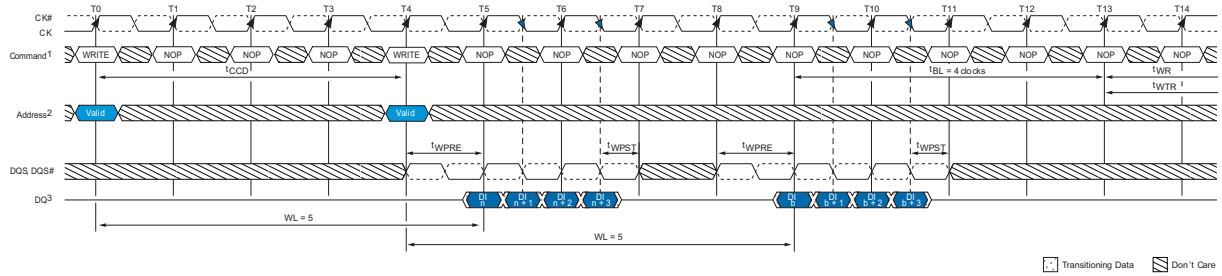

Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during the WRITE command at T0.
3. DI n = data-in for column n.
4. BL8, WL = 5 (AL = 0, CWL = 5).
5. $^{t}$DQSS must be met at each rising clock edge.
6. $^{t}$WPST is usually depicted as ending at the crossing of DQS, DQS#; however, $^{t}$WPST actually ends when DQS no longer drives LOW and DQS# no longer drives HIGH.

## FIGURE 77 - CONSECUTIVE WRITE (BL8) TO WRITE (BL8)



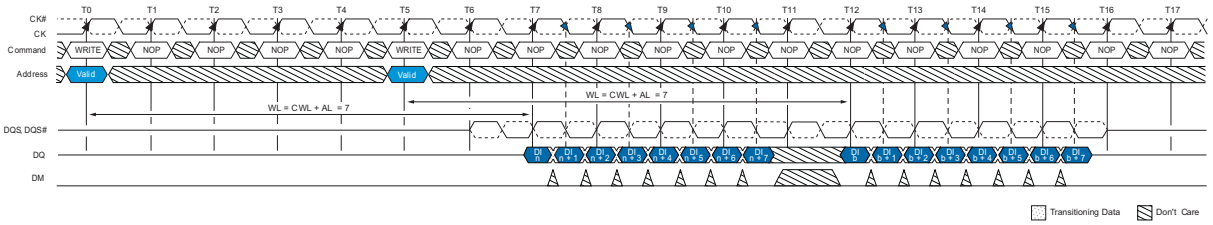

Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and A12 = 1 during the WRITE commands at T0 and T4.
3. DI n (or b) = data-in for column n (or column b).
4. BL8, WL = 5 (AL = 0, CWL = 5).

## FIGURE 78 - CONSECUTIVE WRITE (BC4) TO WRITE (BC4) VIA MRS OR OTF



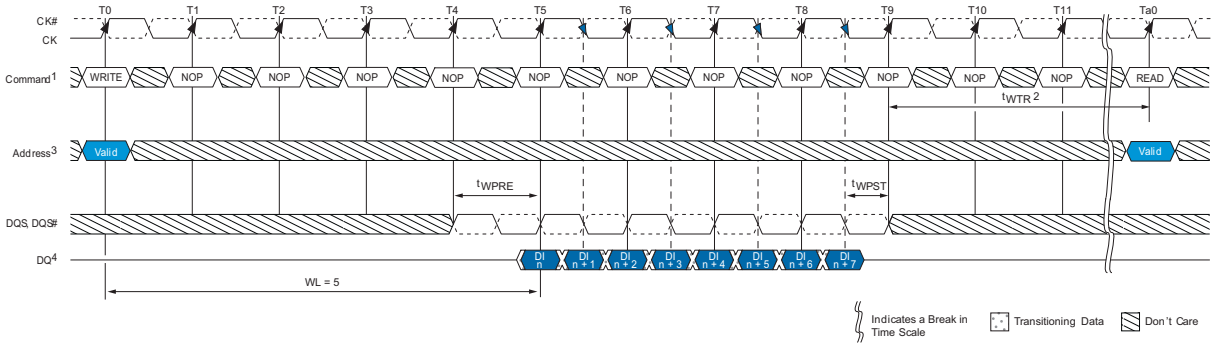

Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. BC4, WL = 5 (AL = 0, CWL = 5).
3. DI n (or b) = data-in for column n (or column b).
4. The BC4 setting is activated by MR0[1:0] = 01 and A12 = 0 during the WRITE command at T0 and T4.

## FIGURE 79 - NONCONSECUTIVE WRITE TO WRITE



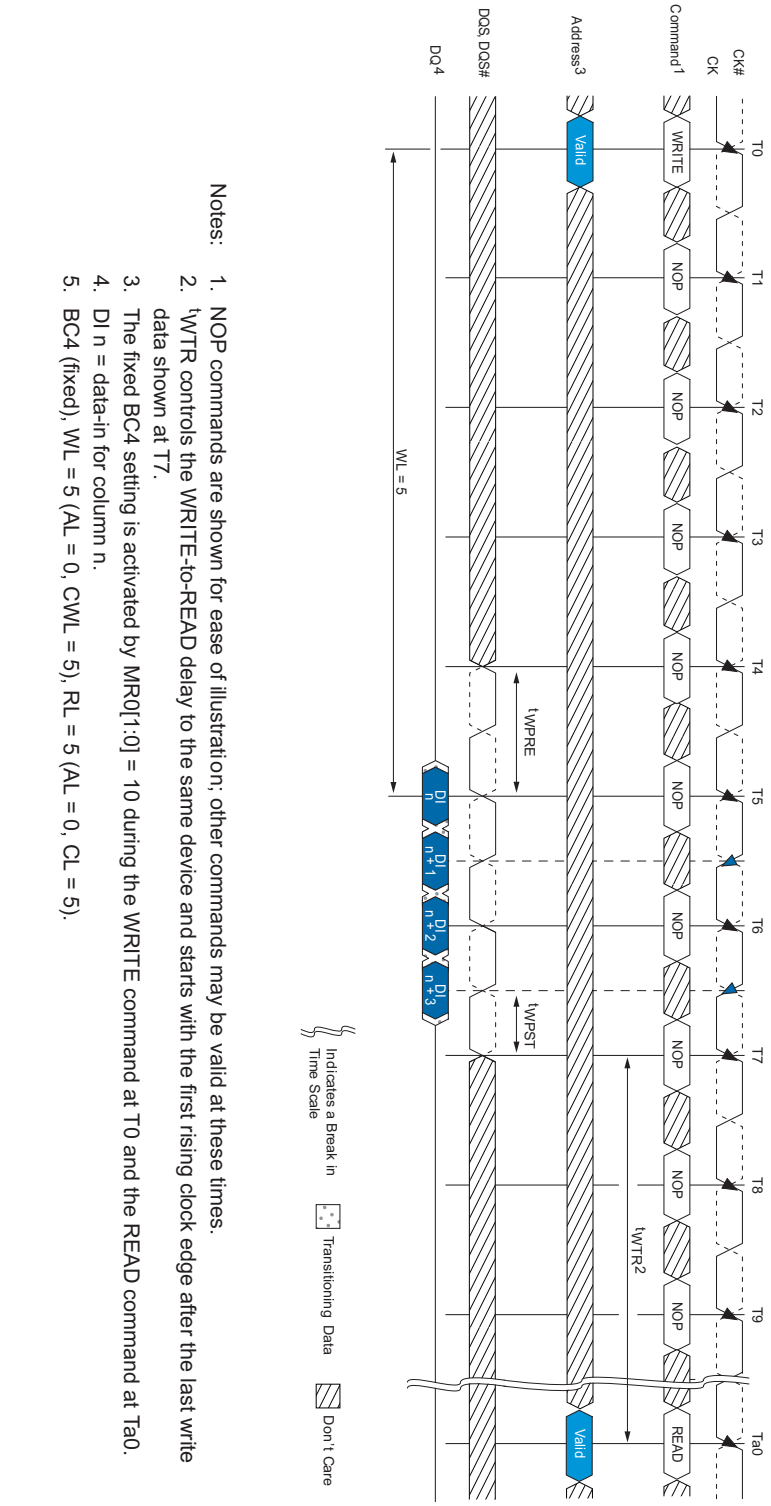

Notes:
1. DI n (or b) = data-in for column n (or column b).
2. Seven subsequent elements of data-in are applied in the programmed order following DOn.
3. Each WRITE command may be to any bank.
4. Shown for WL = 7 (CWL = 7, AL = 0).

## FIGURE 80 - WRITE (BL8) TO READ (BL8)




Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. $^{t}$WTR controls the WRITE-to-READ delay to the same device and starts with the first rising clock edge after the last write data shown at T9.
3. The BL8 setting is activated by either MR0[1:0] = 00 or MR0[1:0] = 01 and MR0[12] = 1 during the WRITE command at T0. The READ command at Ta0 can be either BC4 or BL8, depending on MR0[1:0] and the A12 status at Ta0.
4. DI n = data-in for column n.
5. RL = 5 (AL = 0, CL = 5), WL = 5 (AL = 0, CWL = 5).

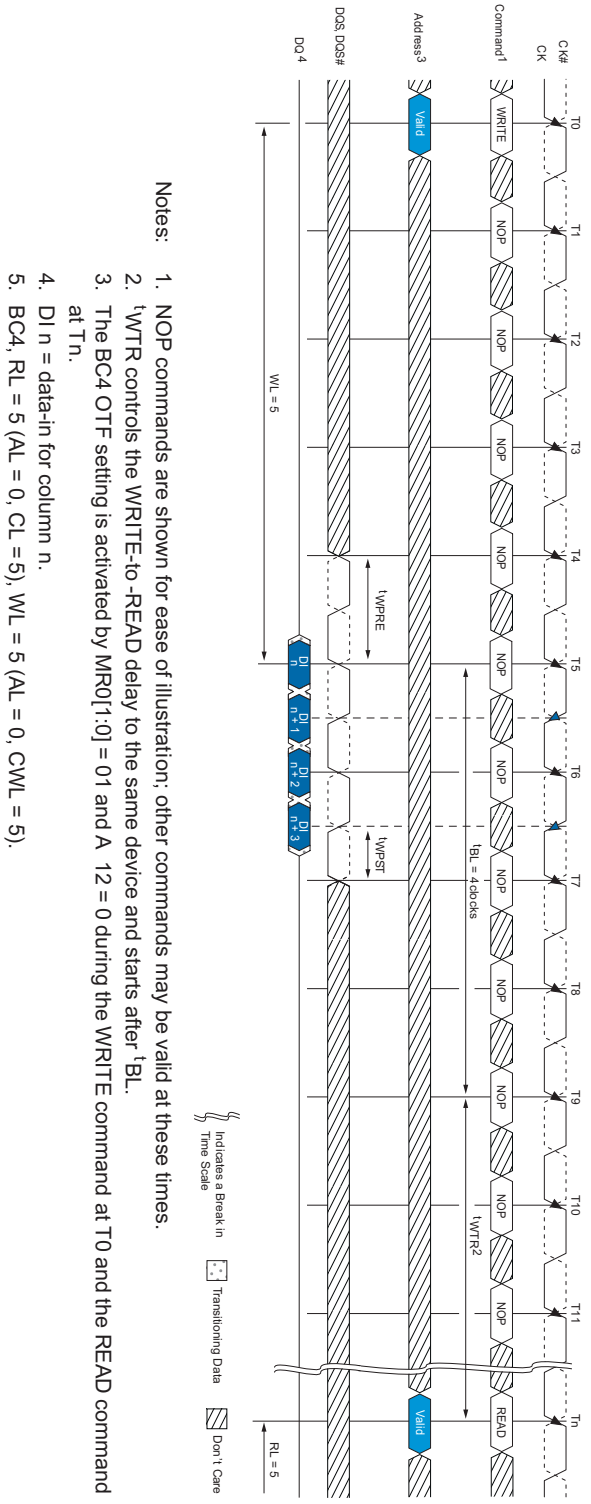
## FIGURE 81 - WRITE TO READ (BC4 MODE REGISTER SETTING)




Notes:

1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. $^{t}$WTR controls the WRITE-to-READ delay to the same device and starts with the first rising clock edge after the last write data shown at T7.
3. The fixed BC4 setting is activated by MR0[1:0] = 10 during the WRITE command at T0 and the READ command at Ta0.
4. DI n = data-in for column n.
5. BC4 (fixed), WL = 5 (AL = 0, CWL = 5), RL = 5 (AL = 0, CL = 5).

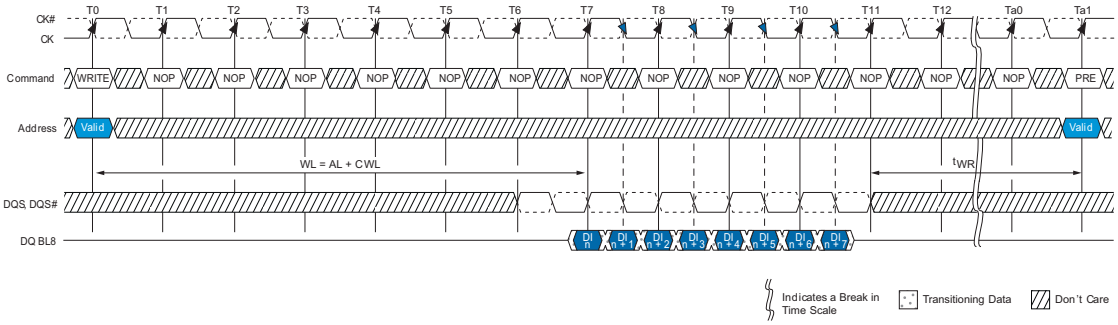
## FIGURE 82 - WRITE (BC4 OTF) TO READ (BC4 OTF)




Notes:

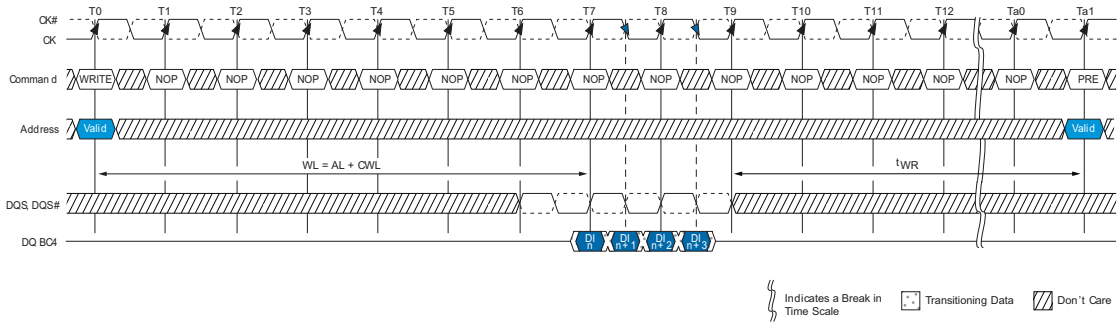
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. $^{t}$WTR controls the WRITE-to -READ delay to the same device and starts after $^{t}$BL.
3. The BC4 OTF setting is activated by MR0[1:0] = 01 and A 12 = 0 during the WRITE command at T0 and the READ command at Tn.
4. DI n = data-in for column n.
5. BC4, RL = 5 (AL = 0, CL =5), WL = 5 (AL = 0, CWL = 5).

## FIGURE 83 - WRITE (BL8) TO PRECHARGE



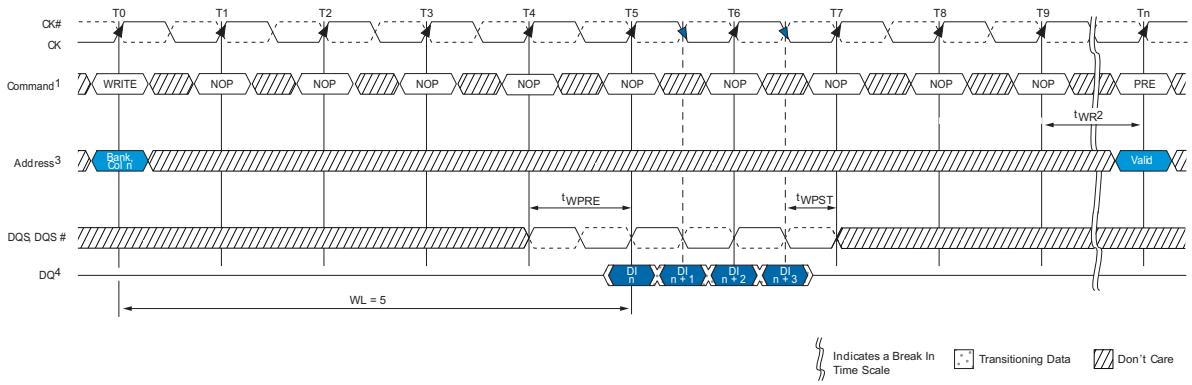

Notes:
1. DI n = data-in from column n.
2. Seven subsequent elements of data-in are applied in the programmed order following DO n.
3. Shown for WL = 7 (AL = 0, CWL = 7).

## FIGURE 84 - WRITE (BC4 MODE REGISTER SETTING) TO PRECHARGE




Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The write recovery time ( $^{t}$WR) is referenced from the first rising clock edge after the last write data is shown at T7. $^{t}$WR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.
3. The fixed BC4 setting is activated by MR0[1:0] = 10 during the WRITE command at T0.
4. DI n = data-in for column n.
5. BC4 (fixed), WL = 5, RL = 5.

## FIGURE 85 - WRITE (BC4 OTF) TO PRECHARGE




Notes:
1. NOP commands are shown for ease of illustration; other commands may be valid at these times.
2. The write recovery time ( $^{t}$WR) is referenced from the rising clock edge at T9. $^{t}$WR specifies the last burst WRITE cycle until the PRECHARGE command can be issued to the same bank.
3. The BC4 setting is activated by MR0[1:0] = 01 and A12 = 0 during the WRITE command at T0.
4. DI n = data-in for column n.
5. BC4 (OTF), WL = 5, RL = 5.

## DQ INPUT TIMING

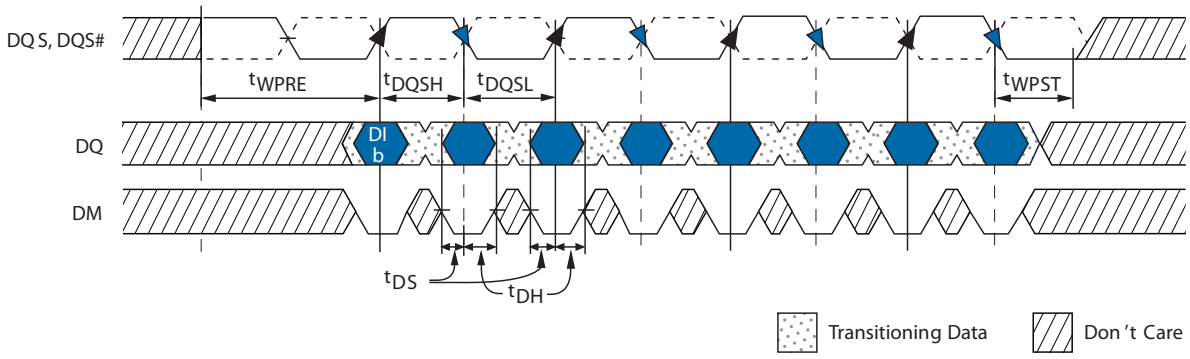
Figure 76 shows the strobe to clock timing during a WRITE. DQSx, DQSx\ must transition within 0.25$^{t}$CK of the clock transitions as limited by $^{t}$DQSS. All data and data mask setup and hold timings are measured relative to the DQSx, DQSx\ crossings, not the clock crossing.

The WRITE preamble and postamble are also shown. One clock prior to data input to the SDRAM, DQSx must be HIGH and DQSx\ must be LOW. Then for a half clock, DQSx is driven LOW (DQSx\ is driven HIGH) during the WRITE preamble. $^{t}$WPRE, likewise, DQSx must be kept LOW by the memory controller after the last data is written to the SDRAM during the WRITE postamble, $^{t}$WPST.

Data setup and hold times are shown in Figure 86. All setup and hold times are measured from the crossing points of DQSx and DQSx\. These setup and hold values pertain to data input and data mask input.

Additionally, the half period of the data input strobe is specified by $^{t}$DQSH and $^{t}$DQSL.

## FIGURE 86 - DATA INPUT TIMING



## PRECHARGE

Input A10 determines whether one bank or all banks are to be PRECHARGED and in the case where only one bank is to be precharged, inputs BA[2:0] select the array BANK.

When all banks are to be PRECHARGED, inputs BA[2:0] are treated as “Don’t Care”. After a bank is PRECHARGED, it is in the IDLE State and must be ACTIVATED prior to any READ or WRITE commands being issued.

## SELF REFRESH

The SELF REFRESH command is initiated like a REFRESH command except CKE is LOW. The DLL is automatically disabled upon entering SELF REFRESH and is automatically enabled and reset upon exiting SELF REFRESH. All power supply inputs (including $V_{REFCA}$ and $V_{REFDQ}$) must be maintained at valid levels upon entry/exit and during SELF REFRESH mode operation. $V_{REFDQ}$ may float or not drive VccQ/2 while in the SELF REFRESH mode under certain conditions:

- Vss<$V_{REFDQ}$<Vcc is maintained
- $V_{REFDQ}$ is valid and stable prior to CKE going back HIGH
- The first WRITE operation may not occur earlier than 512 clocks after $V_{REFDQ}$ is valid
- All other SELF REFRESH mode exit timing requirements are met

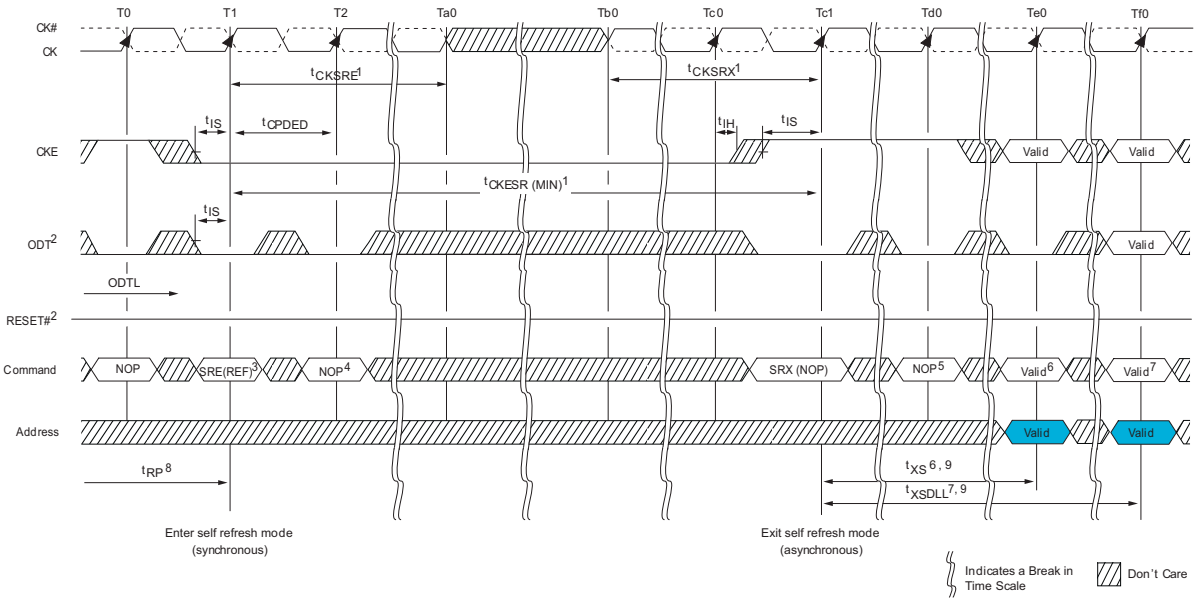
The SDRAM must be idle with all BANKS in the PRECHARGE state ($^{t}RP$ is satisfied and no bursts are in progress) before a SELF REFRESH entry command can be issued. ODT must also be turned off before SELF REFRESH entry by registering the ODT ball LOW prior to the SELF REFRESH entry command (see “On-Die Termination (ODT) for timing requirements). If $R_{TT}$_NOM and $R_{TT}$_WR are disabled in the mode registers, ODT can be a “Don’t Care”. After the SELF REFRESH entry command is registered, CKE must be held LOW to keep the SDRAM in SELF REFRESH mode.

After the SDRAM has entered SELF REFRESH mode, all external control signals, except CKE and RESET\, become “Don’t Care”. The SDRAM initiates a minimum of one REFRESH command internally within the $^{t}CKE$ period when it enters SELF REFRESH mode.

The requirements for entering and exiting SELF REFRESH mode depend on the state of the clock during SELF REFRESH mode. First and foremost, the clock must be stable (meeting $^{t}CK$ specifications) when SELF REFRESH mode is entered. If the clock remains stable and the frequency in not altered while in SELF REFRESH mode, then the SDRAM is allowed to exit SELF REFRESH after $^{t}CKESR$ is satisfied (CKE is allowed to transition HIGH $^{t}CKESR$ later than when CKE was registered LOW). Since the clock remains stable in SELF REFRESH mode (no frequency change), $^{t}CKSRE$ and $^{t}CKSRX$ are not required. However, if the clock is altered during SELF REFRESH mode, then $^{t}CKSRE$ and $^{t}CKSRX$ must be satisfied. When entering SELF REFRESH, $^{t}CKSRE$ must be satisfied prior to altering the clock’s frequency. Prior to exiting SELF REFRESH, $^{t}CKSRX$ must be satisfied prior to registering CKE HIGH.

When CKE is HIGH during SELF REFRESH exit, NOP or DES must be issued for $^{t}XS$ time. $^{t}XS$ is required for the completion of any internal REFRESH that is already in progress and must be satisfied before a valid command not requiring a locked DLL can be issued to the device. $^{t}XS$ is also the earliest time that a SELF REFRESH re-entry may occur (see Figure 87). Before a command requiring a locked DLL can be applied, a ZQCL command must be issued. $^{t}ZQOPER$ timing must be met and $^{t}XSDLL$ must be satisfied. ODT must be off during $^{t}XSDLL$.

## FIGURE 87 - SELF REFRESH ENTRY/EXIT TIMING




Notes:

1. The clock must be valid and stable meeting tCK specifications at least tCKSRE after entering self refresh mode, and at least tCKSRX prior to exiting self refresh mode, if the clock is stopped or altered between states Ta0 and Tb0. If the clock remains valid and unchanged from entry and during self refresh mode, then tCKSRE and tCKSRX do not apply; however, tCKESR must be satisfied prior to exiting at SRX.
2. ODT must be disabled and RTT off prior to entering self refresh at state T1. If both RTT_NOM and RTT_WR are disabled in the mode registers, ODT can be a "Don't Care."
3. Self refresh entry (SRE) is synchronous via a REFRESH command with CKE LOW.
4. A NOP or DES command is required at T2 after the SRE command is issued prior to the inputs becoming "Don't Care."
5. NOP or DES commands are required prior to exiting self refresh mode until state Te0.
6. tXS is required before any commands not requiring a locked DLL.
7. tXSDLL is required before any commands requiring a locked DLL.
8. The device must be in the all banks idle state prior to entering self refresh mode. For example, all banks must be precharged, tRP must be met, and no data bursts can be in progress.
9. Self refresh exit is asynchronous; however, tXS and tXSDLL timings start at the first rising clock edge where CKE HIGH satisfies tISXR at Tc1.tCKSRX timing is also measured so that tISXR is satisfied at Tc1.

## EXTENDED TEMPERATURE USAGE

LOGIC Devices, Inc iMOD DDR3 SDRAM module supports the optional extended temperature range up to ≤95˚C while supporting SELF REFRESH/AUTO REFRESH and support Tc temperatures >95˚C ≤125˚C with MANUAL REFRESH only. When using SELF REFRESH/AUTO REFRESH and the case temperature is >85˚C, SRT and ASR options must be used.

The extended range temperature range SDRAM must be REFRESHED externally at 2X anytime the case temperature is >85˚C. The external REFRESHING requirement is accomplished by reducing the REFRESH PERIOD from 64ms to 32ms. SELF REFRESH mode requires the use of ASR or SRT to support the extended temperature.

**TABLE 68: SELF REFRESH TEMPERATURE AND AUTO SELF REFRESH DESCRIPTION**

| Field | MR2 Bits | Description |
|---|---|---|
| Self Refresh Temperature (SRT) | | |
| **SRT** | 7 | If ASR is disabled (MR2[6]=0), SRT must be programmed to indicate $^{t}$OPER during SELF REFRESH;<br>* MR2[7] = 0: Normal operating temperature range (0˚C to ≤ 85˚C)<br>* MR2[7] = 1: Extended operating temperature range (>85˚C to ≤ 105˚C)<br><br>If ASR is enabled (MR2[7]=1), SRT must be set to 0, even if the extended temperature range is supported.<br>*MR2[7]=0: SRT is disabled. |
| Auto Self Refresh (ASR) | | |
| **ASR** | 6 | When ASR is enabled, the SDRAM automatically provides SELF REFRESH power management functions, (refresh rate for all supported operating temperature values)<br>*MR2[6]=1: ASR is enabled (M7 must = 0)<br><br>When ASR is not enabled, the SRT bit must be programmed to indicate $^{t}$OPER during SELF REFRESH operation.<br>*MR2[6]=0: ASR is disabled, must use manual SELF REFRESH (SRT) |

**TABLE 69: SELF REFRESH MODE SUMMARY**

| MR2[6] (ASR) | MR2[7] (SRT) | SELF REFRESH Operation | Permitted Operating Temperature Range for Self Refresh Mode |
|---|---|---|---|
| **0** | **0** | SELF REFRESH Mode is supported in the normal temperature range. | Normal (0°C to 85°C) |
| **0** | **1** | SELF REFRESH Mode is supported in normal and extended (≤ 95˚C MAX) temperature ranges; When SRT is enabled, it increases self refresh power consumption. | Normal and extended (0°C to 95°C) |
| **1** | **0** | Self refresh mode is supported in normal and extended temperature ranges; Self refresh power consumption may be temperature-dependent. | Normal and extended (0°C to 95°C) |
| **1** | **1** | Illegal. | |

## POWER-DOWN MODE

Power-down is synchronously entered when CKE is registered LOW coincident with a NOP or DES command. CKE is not allowed to go LOW while either an MRS, MPR, ZQCAL, READ or WRITE operation is in progress. CKE is allowed to go LOW while any of the other legal operations are in progress. However, the POWER-DOWN Icc specifications are not applicable until such operations have been completed. Depending on the previous SDRAM state and the command issued prior to CKE going LOW, certain timing constraints must be satisfied (as noted in Table 70). Timing diagrams detailing the different POWER-DOWN mode entry and exits are shown in Figure 88 through Figure 97.

## TABLE 70: COMMAND TO POWER-DOWN ENTRY PARAMETERS

| SDRAM Status | Last Command prior to CKE Low [1] | Parameter (MIN) | Parameter Value | Figure |
|---|---|---|---|---|
| Idle or Active | ACTIVATE | tACTPDEN | 1tCK | Figure 95 |
| Idle or Active | PRECHARGE | tPRPDEN | 1tCK | Figure 96 |
| Active | READ or READAP | tRDPDEN | RL = 4tCK + 1tCK | Figure 91 |
| Active | WRITE: BL8OTF, BL8MRS, BC4OTF | tWRPDEN | WL + 4tCK + tWR/ tCK | Figure 92 |
| Active | WRITE: BC4MRS | | WL + 2tCK + tWR/ tCK | Figure 92 |
| Active | WRITEAP: BL8OTF, BL8MRS, BC4OTF | tWRAPDEN | WL + 4tCK + WR + 1tCK | Figure 93 |
| Active | WRITEAP: BC4MRS | | WL + 2tCK + WR + 1tCK | Figure 93 |
| Idle | REFRESH | tREFPDEN | 1tCK | Figure 94 |
| POWER-DOWN | REFRESH | tXPDLL | Greater of 10tCK or 24ns | Figure 98 |
| Idle | MODE REGISTER SET | tMRSPDEN | tMOD | Figure 97 |

Entering POWER-DOWN mode disables the input and output buffers, excluding CK, CK\, ODT, CKE and RESET\. NOP or DES commands are required until tCPDED has been satisfied, at which time all specified input/output buffers will be disabled. The DLL should be in a locked state when POWER-DOWN is entered for the fastest mode timing. If the DLL is not locked during the POWER-DOWN entry, the DLL must be reset after exiting POWER-DOWN for proper READ operation as well as synchronous ODT operation.

During POWER-DOWN entry, if any bank remains open after all in-progress commands are complete, the SDRAM will be in ACTIVE POWER-DOWN. If all banks are closed after all in-progress commands are complete, the SDRAM will be in PRECHARGE POWER-DOWN mode or fast EXIT mode. When entering PRECHARGE POWER-DOWN, the DLL is turned off in slow exit mode or kept on in fast EXIT mode.

The DLL remains on when entering ACTIVE POWER-DOWN as well. ODT has special timing constraints when slow EXIT mode, PRECHARGE POWER-DOWN is enabled and entered. Refer to “Asynchronous ODT Mode” for detailed ODT usage requirements in slow EXIT mode PRECHARGE POWER-DOWN. A summary of the two POWER-DOWN modes is listed in Table 71.

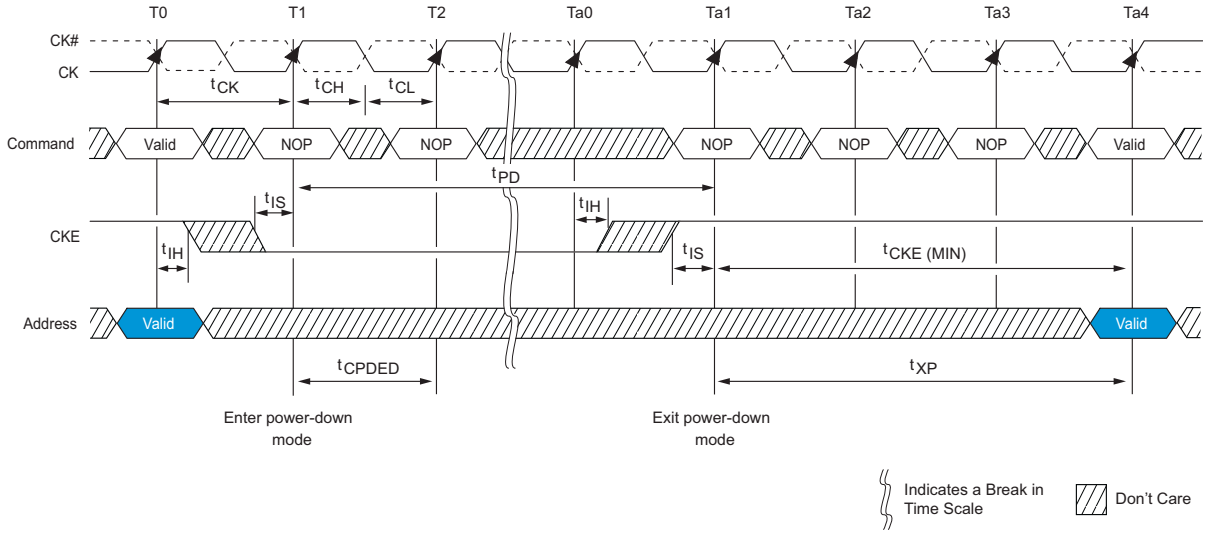
While in either POWER-DOWN state, CKE is held LOW, RESET\ is held HIGH, and a stable clock signal must be maintained. ODT must be in a valid state but all other input signals are a “Don’t Care”. If RESET\ goes LOW during POWER-DOWN, the SDRAM will switch out of POWER-DOWN and go into the RESET state. After CKE is registered LOW, CKE must remain LOW until tPD (MIN) has been satisfied. The maximum time allowed for POWER-DOWN duration is tPD (MAX) (9 x tREFI).

The POWER-DOWN states are synchronously exited when CKE is registered HIGH (with a required NOP or DES command). CKE must be maintained HIGH until tCKE has been satisfied. A valid, executable command may be applied after POWER-DOWN EXIT LATENCY, tXP, tXPDLL have been satisfied. A summary of the POWER-DOWN modes is listed in Table 71.

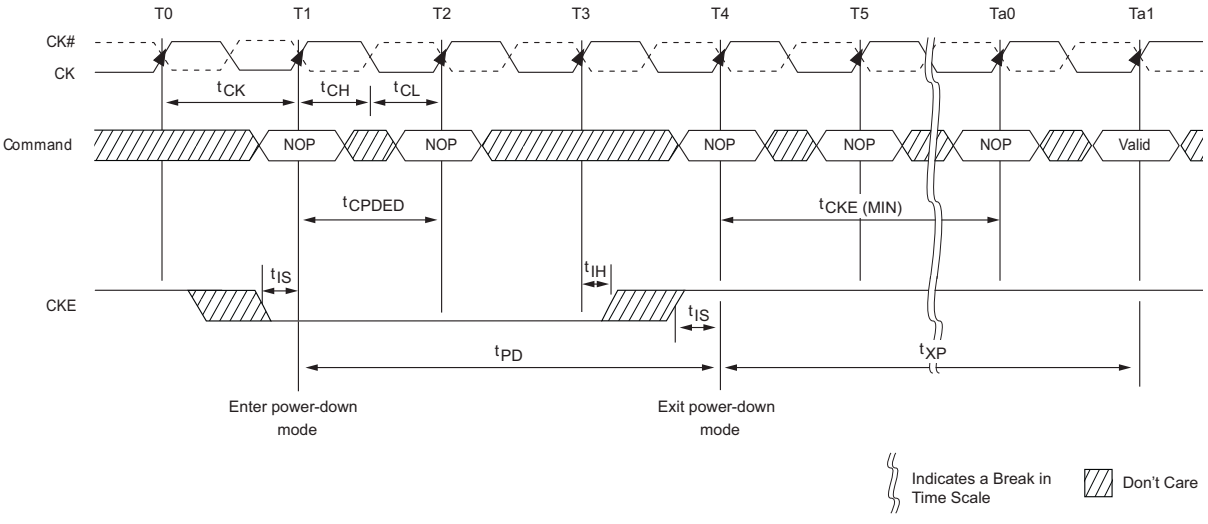
## TABLE 71: POWER-DOWN MODES

| SDRAM State | MR1[12] | DLL State | POWER-DOWN exit | Relevant Parameters |
|---|---|---|---|---|
| ACTIVE (any bank open) | “Don’t Care” | ON | FAST | tXP to any other valid COMMAND |
| PRECHARGE (all banks PRECHARGED) | 1 | ON | FAST | tXP to any other valid COMMAND |
| | 0 | OFF | SLOW | tXDLL to COMMANDS that require the DLL to be locked (READ, RDAP, ODT ON). tXP to any other valid COMMAND. |

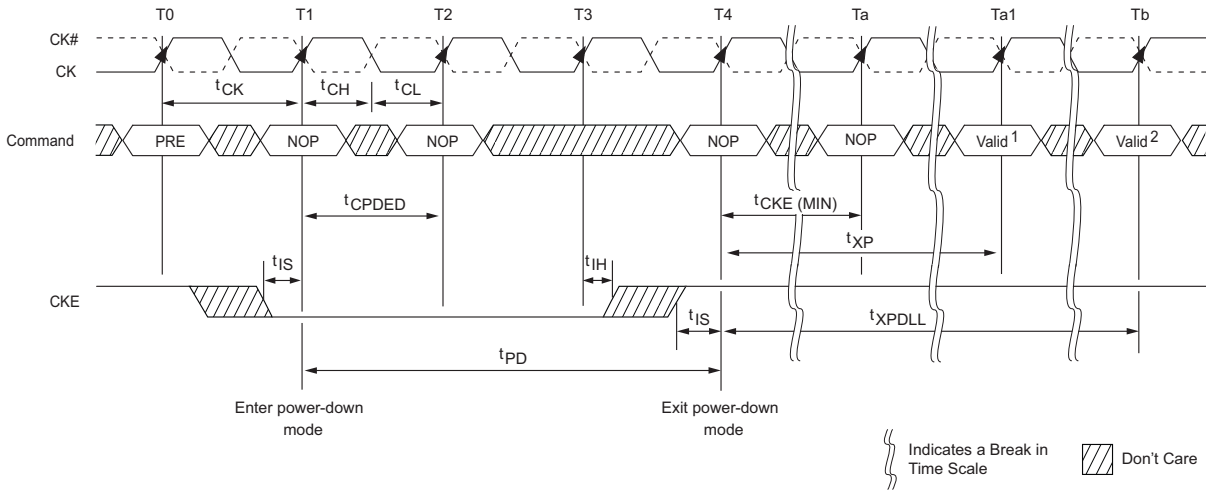
## Figure 88 - Active Power-Down Entry and Exit




## Figure 89 - Precharge Power-Down (Fast-Exit Mode) Entry and Exit

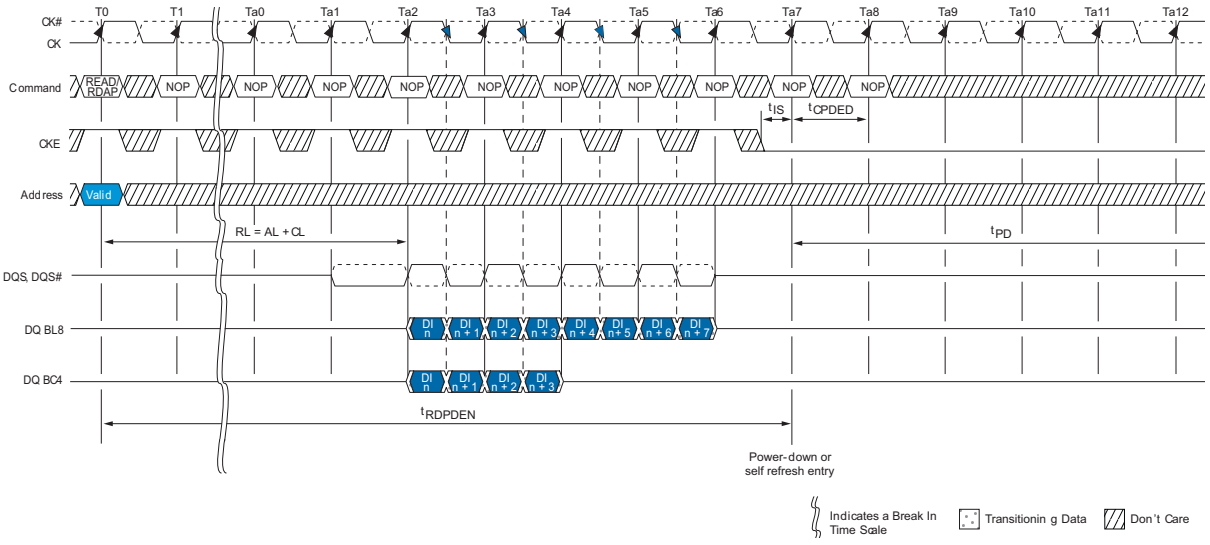


## Figure 90 - Precharge Power-Down (Slow-Exit Mode) Entry and Exit

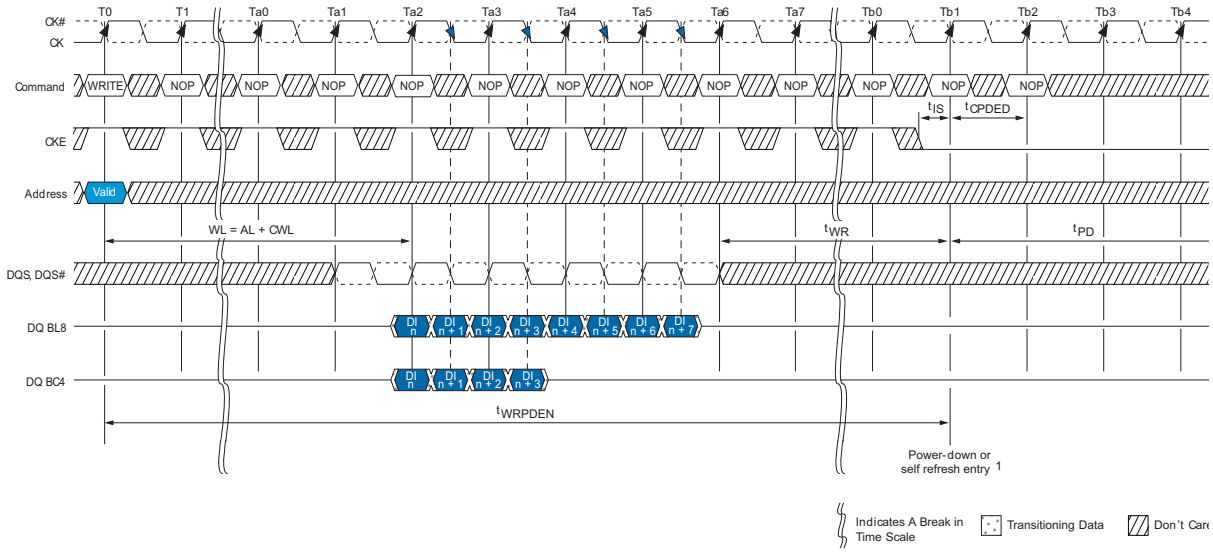



Notes: 1. Any valid command not requiring a locked DLL.
2. Any valid command requiring a locked DLL.

## Figure 91 - Power-Down Entry After READ or READ with Auto Precharge (RDAP)

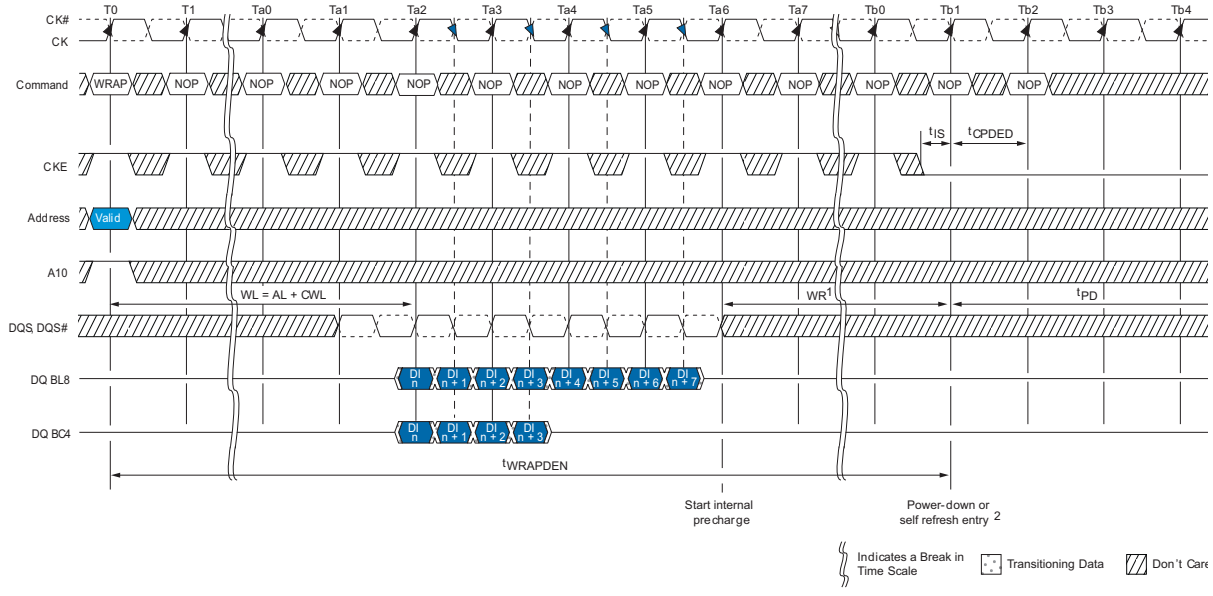


## Figure 92 - Power-Down Entry After WRITE



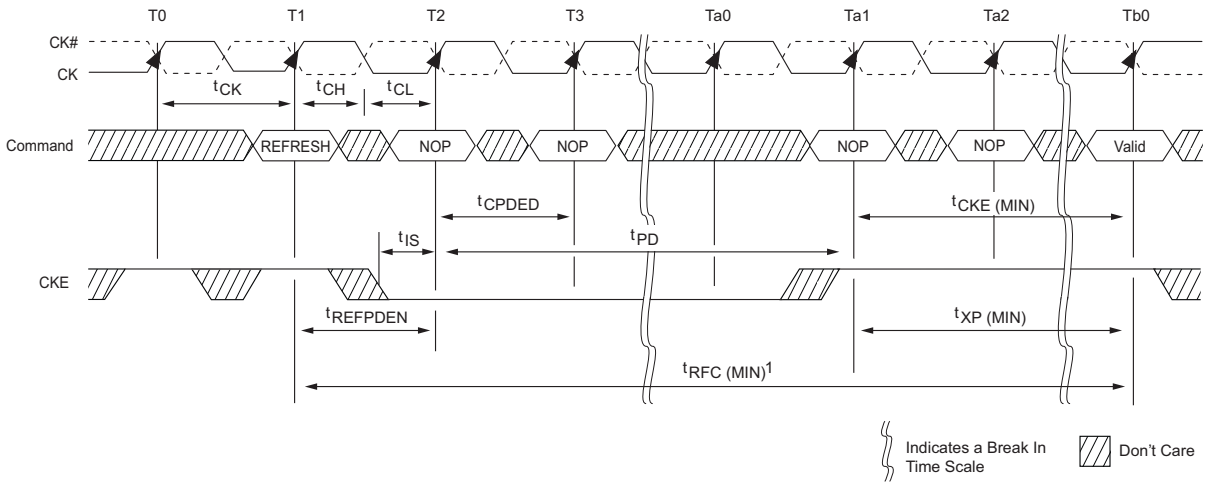

Notes: 1. CKE can go LOW 2tCK earlier if BC4MRS.

## Figure 93 - Power-Down Entry After WRITE with Auto Precharge (WRAP)



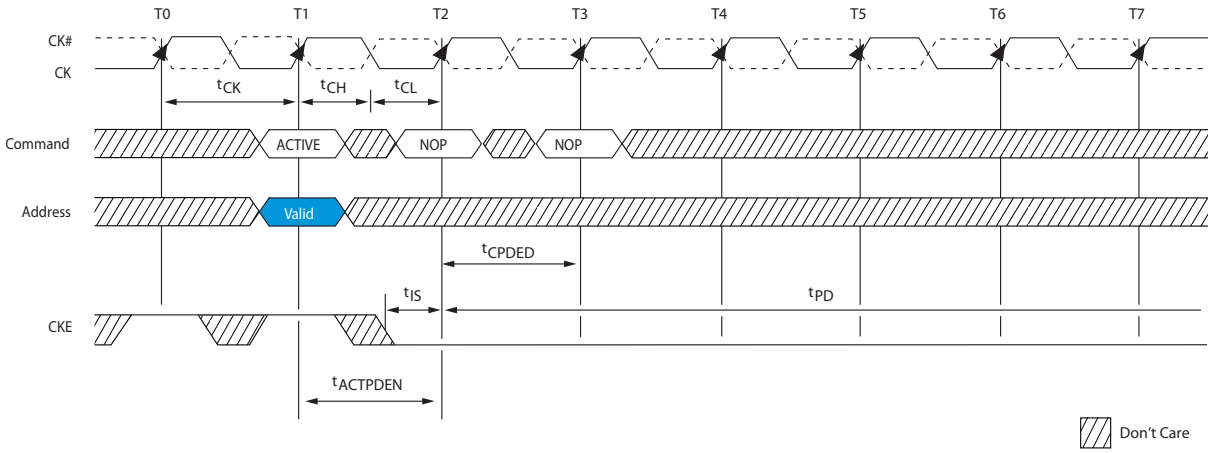

Notes: 1. tWR is programmed through MR0[11:9] and represents tWR (MIN)ns/ tCK rounded up to the next integer tCK.
2. CKE can go LOW 2tCK earlier if BC4MRS.

## FIGURE 94 - REFRESH TO POWER-DOWN ENTRY

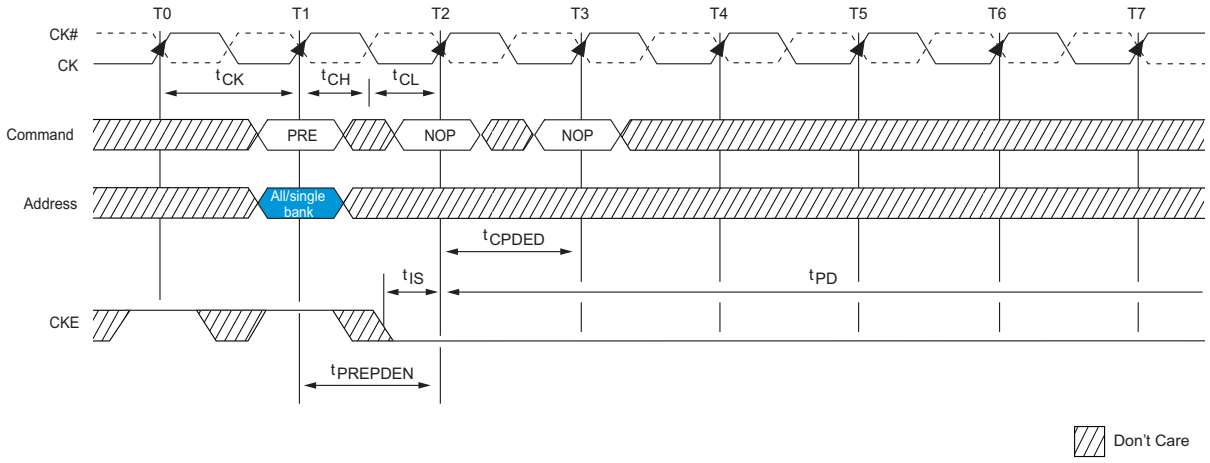



Notes: 1. After CKE goes HIGH during tRFC, CKE must remain HIGH until tRFC is satisfied.

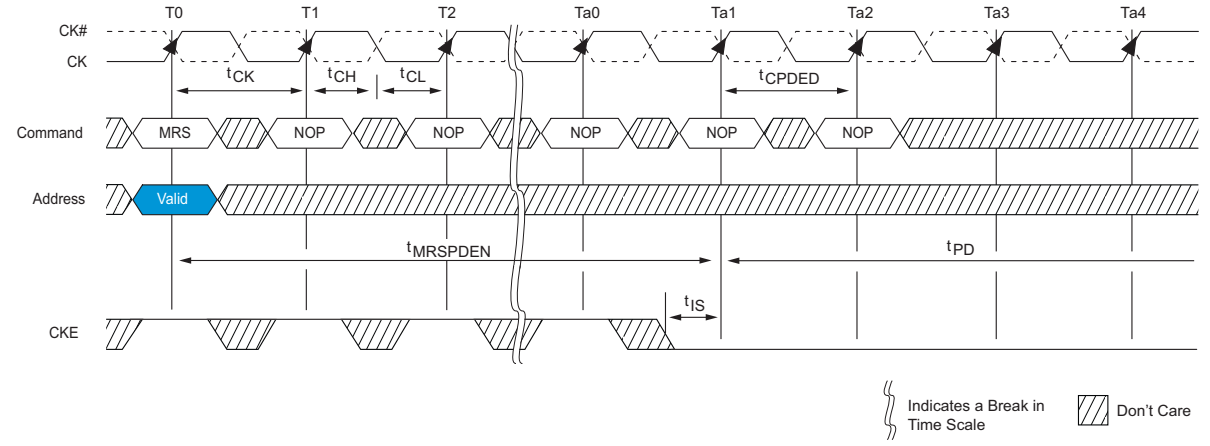
## FIGURE 95 - ACTIVATE TO POWER-DOWN ENTRY



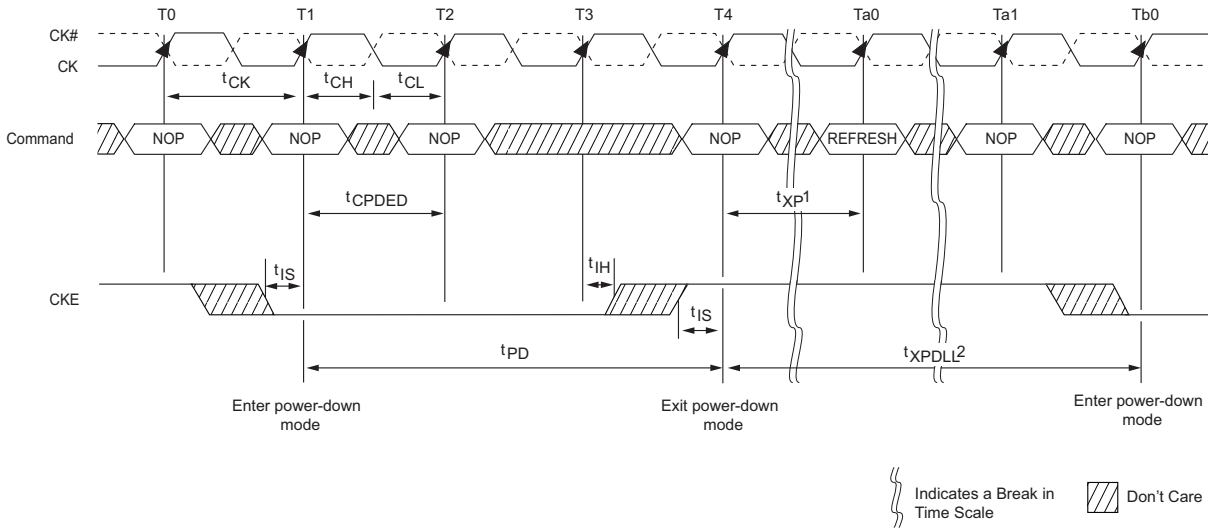
## FIGURE 96 - PRECHARGE TO POWER-DOWN ENTRY




## FIGURE 97 - MRS COMMAND TO POWER-DOWN ENTRY



## FIGURE 98 - POWER-DOWN EXIT TO REFRESH TO POWER-DOWN ENTRY

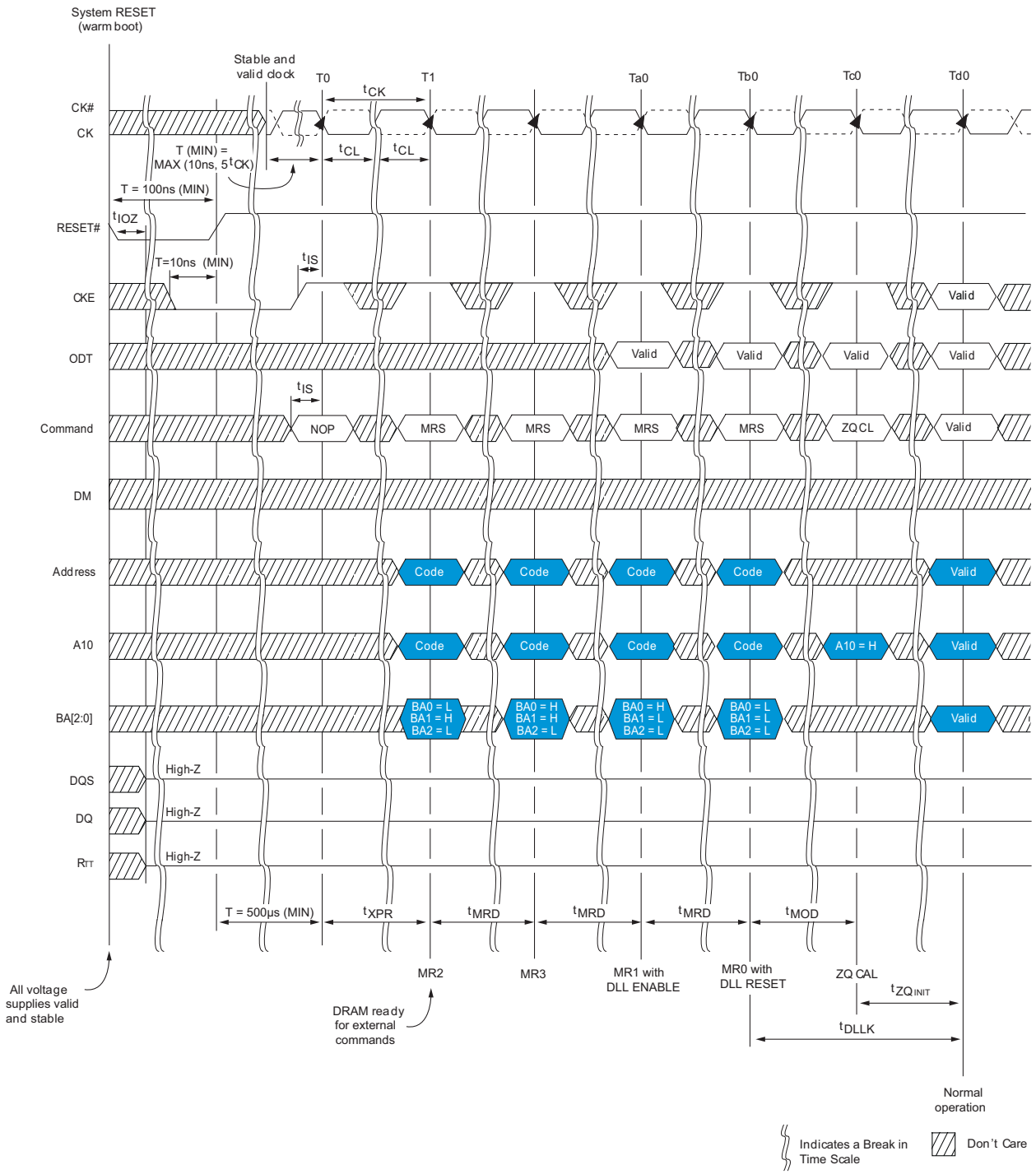



Notes:
1. tXP must be satisfied before issuing the command.
2. tXPDLL must be satisfied (referenced to the registration of power-down exit) before the next power-down can be entered.

## RESET

The RESET signal (RESET\) is an asynchronous signal that triggers any time it drops LOW and there are no restrictions about when it can go LOW. After RESET\ is driven LOW, it must remain LOW for 100ns. During this time, the outputs are disabled, ODT (RTT) turns off (HIGH-Z) and the DDR3 SDRAM resets itself. CKE should be brought LOW prior to RESET\ being driven HIGH. After RESET\ goes HIGH, the SDRAM must be re-initialized as though a normal power up were executed (see Figure 99). All refresh counters on the SDRAM are RESET and data stored in the SDRAM is assumed unknown after RESET\ has been driven LOW.

## FIGURE 99 - RESET SEQUENCE



## ON-DIE TERMINATION (ODT)

ODT is a feature that enables the SDRAM to enable/disable on-die termination resistance for each DQ, LDQSx, LDQSx\ , UDQSx, UDQSx\ LDMx and UDMx for the four words contained in LDI's DDR3 iMOD.

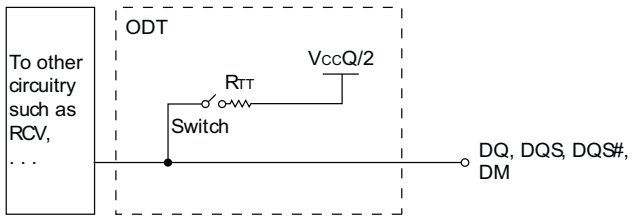
The ODT feature is designed to improve signal integrity of the memory array/sub-system by enabling the DDR3 memory controller to independently turn on or off the SDRAMS internal termination resistance for any grouping of SDRAM devices. The ODT feature is not supported during DLL disable mode. A simple functional representation of the SDRAM ODT feature is shown in Figure 100. The switch is enabled by the internal ODT control logic, which uses the external ODT ball and other control information.

## FUNCTIONAL REPRESENTATION OF ODT

The value of RTT (ODT termination value) is determined by the settings of several mode register bits (see Table 75). The ODT ball is ignored while in SELF REFRESH mode (must be turned off prior to SELF REFRESH entry) or if mode registers MR1 and MR2 are programmed to disable ODT. ODT is comprised of nominal ODT and dynamic ODT modes and either of these can function in synchronous or asynchronous modes (when the DLL is off during PRECHARGE POWER-DOWN or when the DLL is synchronizing). Nominal ODT is the base termination and is used in any allowable ODT state. Dynamic ODT is applied only during WRITEs and provides OTF switching from no RTT or RTT_NOM to RTT_WR.

The actual effective termination, RTT_EFF may be different from the RTT targeted due to nonlinearity of the termination. For RTT_EFF values and calculations, see "ODT Characteristics".

## FIGURE 100 - ON-DIE TERMINATION




## NOMINAL ODT

ODT (NOM) is the base termination resistance for each applicable ball, enabled or disabled via MR1[9,6,2] (see Figure 46), and it is turned on or off via the ODT ball.

## TABLE 72: POWER-DOWN MODES

| MR1[9,6,2] | ODT Pin | SDRAM Termination State | SDRAM State | Notes |
|---|---|---|---|---|
| 000 | 0 | RTT_NOM disabled, ODT OFF | Any valid | 1,2 |
| 000 | 1 | RTT_NOM disabled, ODT ON | Any valid except SELF REFRESH, READ | 1,3 |
| 000-101 | 0 | RTT_NOM enabled, ODT OFF | Any valid | 1,2 |
| 000-101 | 1 | RTT_NOM enabled, ODT ON | Any valid except SELF REFRESH, READ | 1,3 |
| 110 and 111 | X | RTT_NOM reserved, ODT ON or OFF | Illegal | |

NOTES:

1. Assumes dynamic ODT is disabled.
2. ODT is enabled and active during most WRITES for proper termination, but it is not illegal to have it off during WRITES.
3. ODT must be disabled during READs. The RTT_NOM value is restricted during WRITES. Dynamic ODT is applicable if enabled.

## NOMINAL ODT

Nominal ODT resistance RTT_NOM is defined by MR1[9,6,2], as shown in Figure 46. The RTT_NOM termination value applies to the output pins previously mentioned. DDR3 SDRAM iMODs support multiple RTT_NOM values based on RZQ/n where n can be 2,4,6,8 or 12 and RZQ is 240Ω±1%. RTT_NOM termination is allowed any time after the SDRAM is initialized, calibrated and not performing READ accesses or when it is not in SELF REFRESH mode.

WRITE access uses RTT_NOM id dynamic ODT (RTT_WR) is disabled. If RTT_NOM is used during WRITEs, only RZQ/2, RZQ/4 and RZQ/6 are allowed (see Table 71). ODT timings are summarized in Table 73, as well as, listed in Table 50.

Examples of nominal ODT timing are shown in conjunction with the synchronous mode of operation in “Synchronous ODT Mode”.

### TABLE 73: ODT PARAMETER

| Symbol | Description | Begins at | Defined to | Definition for All DDR3 bins | Units |
|---|---|---|---|---|---|
| ODTL ON | ODT synchronous turn on delay | ODT registered HIGH | RTT_ON ± tAON | CWL + AL - 2 | tCK |
| ODTL OFF | ODT synchronous turn off delay | ODT registered HIGH | RTT_ON ± tAOF | CWL + AL - 2 | tCK |
| tAONPD | ODT asynchronous on delay | ODT registered HIGH | RTT_ON | 1-9 | ns |
| tAOFFPD | ODT asynchronous on delay | ODT registered HIGH | RTT_OFF | 1-9 | ns |
| ODTH4 | ODT minimum HIGH time after ODT assertion or WRITE (BC4) | ODT registered HIGH or WRITE registration with ODT HIGH | ODT registered LOW | 4TcK | tCK |
| ODTH8 | ODT minimum HIGH time after WRITE (BL8) | WRITE registration with ODT HIGH | ODT registered LOW | 6TcK | tCK |
| tAON | ODT turn-on relative to ODTL on completion | Completion of ODTL on | RTT_ON | See Table 50 | ps |
| tAOF | ODT turn-off relative to ODTL off completion | Completion of ODTL off | RTT_OFF | 0.5TcK ± 0.2TcK | tCK |

## DYNAMIC ODT

In certain applications, to further enhance signal integrity on the data bus, it is desirable that the termination strength, be changed without issuing an MRS command, essentially changing the ODT termination resistance on-the-fly. With dynamic ODT (RTT_WR) enabled, the SDRAM switches from nominal ODT (RTT_NOM) to dynamic ODT when beginning a WRITE burst and subsequently switches back to nominal ODT at the completion of the WRITE burst sequence. This requirement and the supporting DYNAMIC ODT feature of the DDR3 SDRAM makes it feasible and is described in further detail below:

## DYNAMIC ODT FUNCTIONAL DESCRIPTION:

The dynamic ODT mode is enabled if either MR2[9] or mR2[10] is set to “1”. Dynamic ODT is not supported during DLL disable mode, so RTT_WR must be disabled. The dynamic ODT function is described, as follows:

- Two RTT values are available – RTT_NOM and RTT_WR:
  - The value of RTT_NOM is preselected via MR1[9,6,2]
  - The value for RTT_WR is preselected via MR2[10,9]
- During SDRAM operations without READ or WRITE commands, the termination is controlled as follows:
  - Termination ON/OFF timing is controlled via the ODT ball and LATENCIES ODTl on and ODTL off
  - Nominal termination strength RTT_NOM is used
- When a WRITE command (WR, WRAP, WRS4, WRS8, WRAPS4, WRAPS8) is registered and if dynamic ODT is enabled, the ODT termination is controlled as follows:
  - A latency of ODTLCNW after the WRITE command: termination strength RTT_NOM switches to RTT_WR
  - A Latency of ODTLCWN8 (for BL8, fixed or OTF) or ODTLCWN4 (for BC4, fixed or OTF) after the WRITE command: termination strength RTT_WR switches back to RTT_NOM
  - ON/OFF termination timing is controlled via the ODT ball and determined by ODTL on, ODTL off, ODTH4 and ODTH8.
  - During the tADC transition window, the value of RTT is undefined

ODT is constrained during WRITEs and when dynamic ODT is enabled (see Table 74).

## TABLE 74: DYNAMIC ODT SPECIFIC PARAMETERS

| Symbol | Description | Begins at | Defined to | Definition for All DDR3 bins | Units |
|---|---|---|---|---|---|
| $ODTL_{CNW}$ | Change from RTT_NOM to RTT_WR | WRITE registration | RTT switched from RTT_NOM to RTT_WR | WL - 2 | $^{t}CK$ |
| $ODTL_{CWN4}$ | Change from RTT_WR to RTT_NOM (BC4) | WRITE registration | RTT switched from RTT_WR to RTT_NOM | $4^{t}CK$ + ODTL OFF | $^{t}CK$ |
| $ODTL_{CWN8}$ | Change from RTT_WR to RTT_NOM (BL8) | WRITE registration | RTT switched from RTT_WR to RTT_NOM | $6^{t}CK$ + ODTL OFF | $^{t}CK$ |
| $^{t}ADC$ | RTT change skew | $ODTL_{CNW}$ | RTT trans complete | $0.5^{t}CK \pm 0.2^{t}CK$ | $^{t}CK$ |

## TABLE 75: MODE REGISTERS FOR RTT_NOM

| MR1(RTT_NOM) | | | RTT_NOM (RZQ) | RTT_NOM(Ohms) | RTT_NOM Mode Restriction |
|---|---|---|---|---|---|
| M9 | M6 | M2 | | | |
| 0 | 0 | 0 | Off | Off | n/a |
| 0 | 0 | 1 | RZQ/4 | 60 | SELF REFRESH |
| 0 | 1 | 0 | RZQ/2 | 120 | |
| 0 | 1 | 1 | RZQ/6 | 40 | |
| 1 | 0 | 0 | RZQ/12 | 20 | SELF REFRESH, WRITE |
| 1 | 0 | 1 | RZQ/8 | 30 | |
| 1 | 1 | 0 | Reserved | Reserved | n/a |
| 1 | 1 | 1 | Reserved | Reserved | n/a |

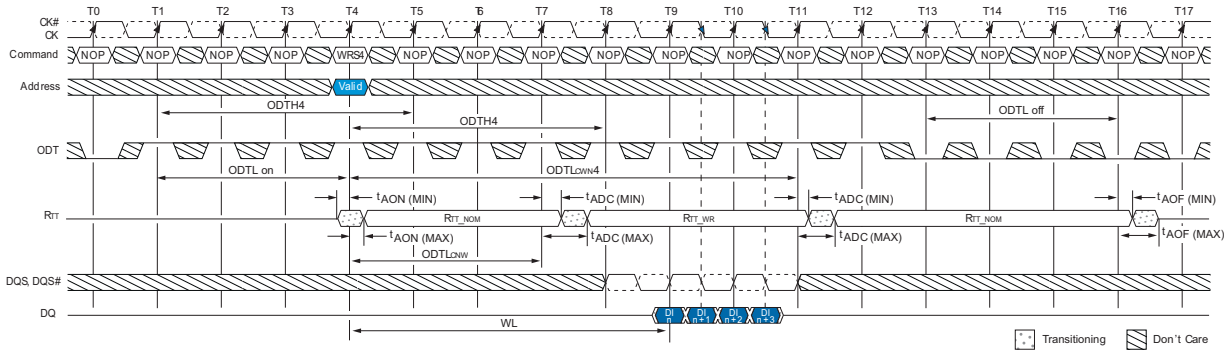
## TABLE 76: MODE REGISTERS FOR RTT_WR

| MR1(RTT_NOM) | | RTT_NOM (RZQ) | RTT_NOM(Ohms) |
|---|---|---|---|
| M10 | M2 | | |
| 0 | 0 | **Dynamic ODT OFF: WRITE does not affect RTT_NOM** | |
| 0 | 1 | RZQ/4 | 60 |
| 1 | 0 | RZQ/2 | 120 |
| 1 | 1 | Reserved | Reserved |
| n/a | n/a | n/a | n/a |
| n/a | n/a | n/a | n/a |
| n/a | n/a | n/a | n/a |
| n/a | n/a | n/a | n/a |

## TABLE 77: TIMING DIAGRAMS FOR DYNAMIC ODT

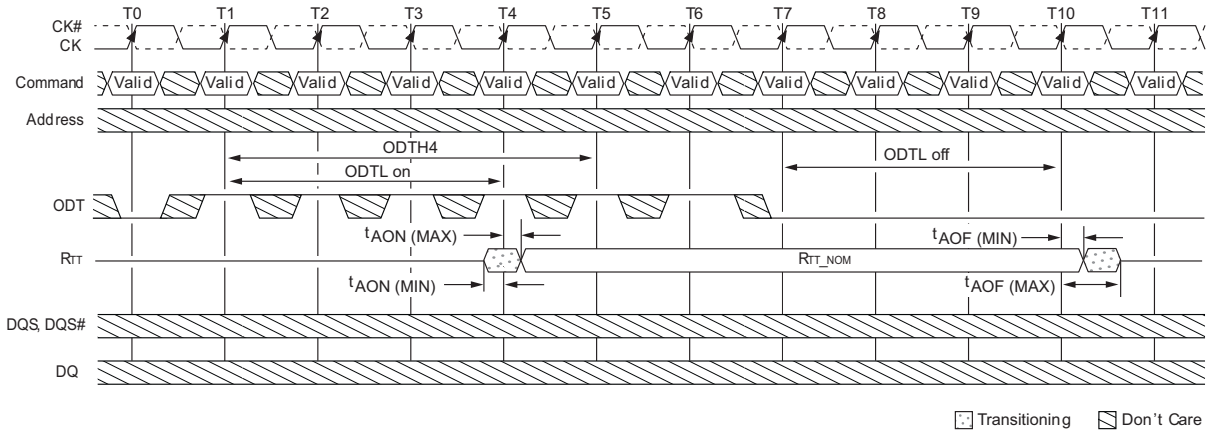
| Figure | Title |
|---|---|
| Figure 101 | Dynamic ODT: ODT asserted before and after the WRITE, BC4 |
| Figure 102 | Dynamic ODT: Without WRITE command |
| Figure 103 | Dynamic ODT: ODT pin asserted together with WRITE command for 6 CK cycles, BL8 |
| Figure 104 | Dynamic ODT: ODT pin asserted with WRITE command for 6 CK cycles, BC4 |
| Figure 105 | Dynamic ODT: ODT pin asserted with WRITE command for 4 CK cycles, BC4 |

## Figure 101 - Dynamic ODT: ODT Asserted Before and After the WRITE, BC4



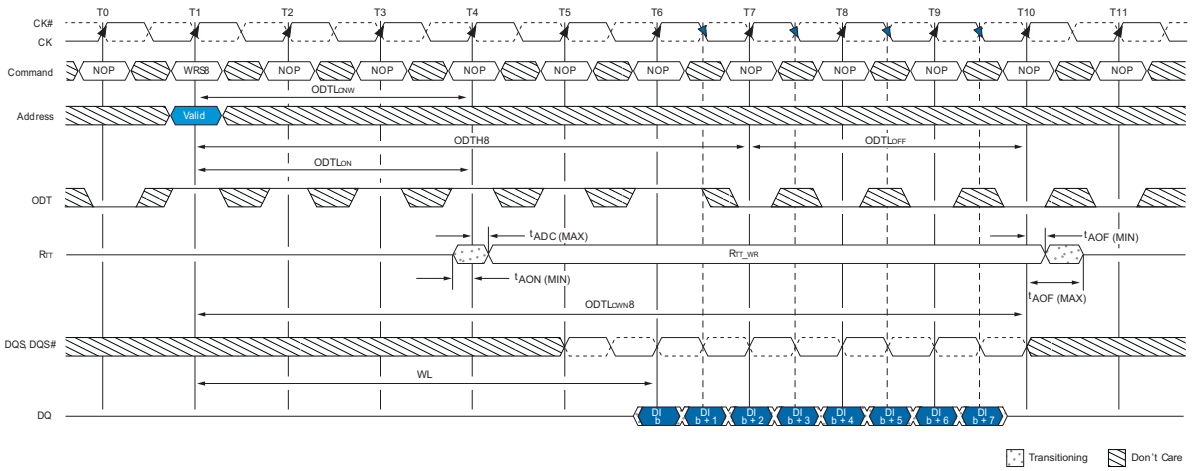

Notes:
1. Via MRS or OTF. AL = 0, CWL = 5. RTT_NOM and RTT_WR are enabled.
2. ODTH4 applies to first registering ODT HIGH and then to the registration of the WRITE command. In this example, ODTH4 is satisfied if ODT goes LOW at T8 (four clocks after the WRITE command).

## Figure 102 - Dynamic ODT: Without WRITE Command



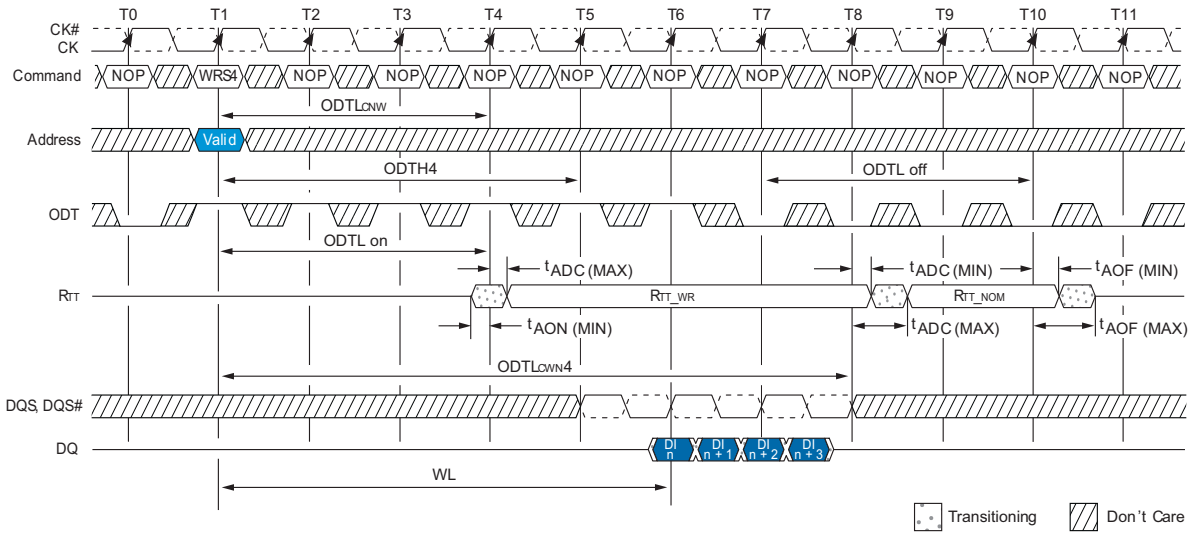

Notes:
1. AL = 0, CWL = 5. RTT_NOM is enabled and RTT_WR is either enabled or disabled.
2. ODTH4 is defined from ODT registered HIGH to ODT registered LOW; in this example, ODTH4 is satisfied. ODT registered LOW at T5 is also legal.

## Figure 103 - Dynamic ODT: ODT Pin Asserted Together with WRITE Command for 6 Clock Cycles, BL8



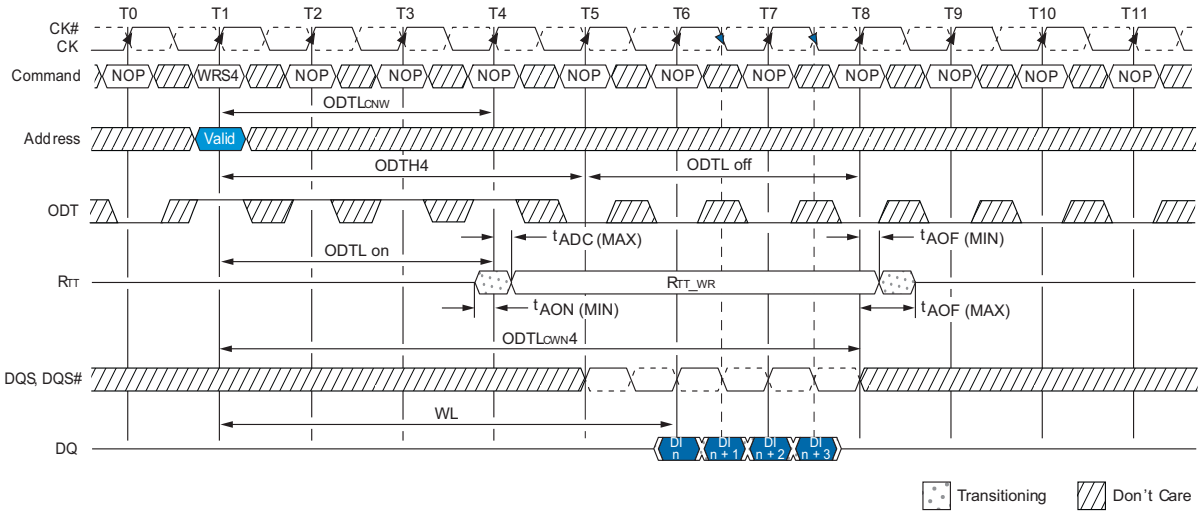

Notes: 1. Via MRS or OTF; AL = 0, CWL = 5. If RTT_NOM can be either enabled or disabled, ODT can be HIGH. RTT_WR is enabled.
2. In this example, ODTH8 = 6 is satisfied exactly.

## Figure 104 - Dynamic ODT: ODT Pin Asserted with WRITE Command for 6 Clock Cycles, BC4




Notes: 1. Via MRS or OTF. AL = 0, CWL = 5. RTT_NOM and RTT_WR are enabled.
2. ODTH4 is defined from ODT registered HIGH to ODT registered LOW, so in this example, ODTH4 is satisfied. ODT registered LOW at T5 is also legal.

## FIGURE 105 - DYNAMIC ODT: ODT PIN ASSERTED WITH WRITE COMMAND FOR 4 CLOCK CYCLES, BC4




Notes:
1. Via MRS or OTF. AL = 0, CWL = 5. RTT_NOM can be either enabled or disabled. If disabled, ODT can remain HIGH. RTT_WR is enabled.
2. In this example ODTH4 = 4 is satisfied exactly.

## SYNCHRONOUS ODT MODE

Synchronous ODT is selected whenever the DLL is turned on and locked while RTT_NOM or RTT_WR is enabled. Based on the POWER-DOWN definition, these modes are:

- Any bank ACTIVE with CKE HIGH
- REFRESH mode with CKE HIGH
- DLE mode with CKE HIGH
- ACTIVE POWER-DOWN mode (regardless of MR0[12])
- PRECHARGE POWER-DOWN mode if DLL is enabled during PRECHARGE POWER-DOWN by MR0[12]

## ODT LATENCY AND POSTED ODT

In synchronous ODT mode, RTT turns on ODTL on clock cycles after ODT is sampled HIGH by a rising clock edge and turns off ODTL off clock cycles after ODT is registered LOW by a rising clock edge. The actual on/off times varies by tAON and tAOF around each clock edge (see Table 78). The ODT LATENCY is tied to the WRITE LATENCY (WL) by ODTL on =WL-2 and ODTL off = WL- 2.

Since WRITE LATENCY is made up of CAS WRITE LATENCY (CWL) and ADDITIVE LATENCY (AL), the AL value programmed into the mode register MR1[4,3], also applies to the ODT signal. The SDRAM's internal ODT signal is delayed a number of clock cycles defined by the AL relative to the external ODT signal. Thus, ODTL on = CWL + AL – 2 and ODTL off = CWL + AL – 2.

## SYNCHRONOUS ODT TIMING PARAMETERS

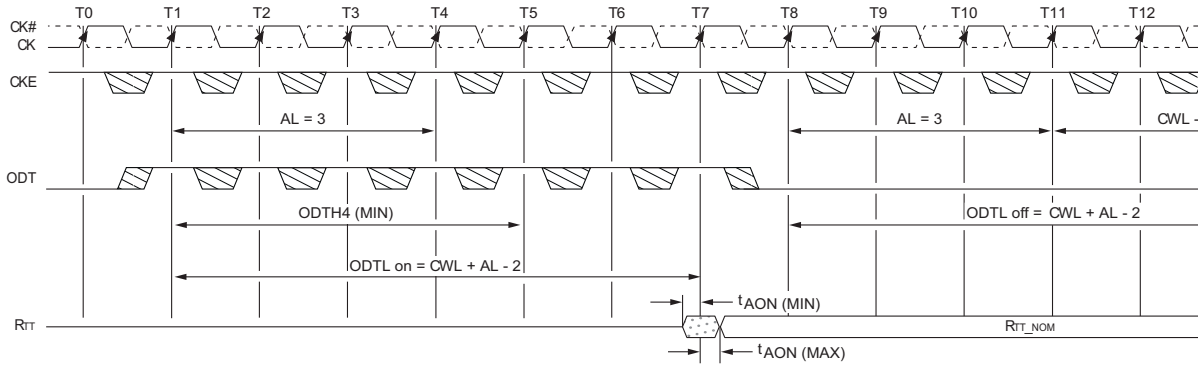
Synchronous ODT mode uses the following timing parameters: ODTL on, ODTL off, ODTH4, ODTH8, $^{t}$AON and $^{t}$AOF (see Table 78 and Figure 106). The minimum RTT turn-on time ($^{t}$AON [MIN]) is the point at which the device leaves HIGH-A and ODT resistance begins to turn on. Maximum RTT turn-on time ($^{t}$AON [MAX]) is the point at which ODT resistance is fully on. Both are measured relative to ODTL on. The minimum RTT turn-off time ($^{t}$AOF [min]) is the point at which the device starts to turn-off ODT resistance. Maximum RTT turn-off time ($^{t}$AOF [MAX]) is the point at which ODT has reached HIGH-Z. Both are measured from ODTL off.

When ODT is asserted, it must remain HIGH until ODTH4 is satisfied. If a WRITE command is registered by the SDRAM with ODT HIGH, then ODT must remain HIGH until ODTH4 (BC4) or ODTH8 (BL8) after the WRITE command (see Figure 107). ODTH4 and ODTH8 are measured from ODT registered HIGH to ODT registered LOW or from the registration of a WRITE command until ODT is registered LOW.

### TABLE 78: SYNCHRONOUS ODT PARAMETERS

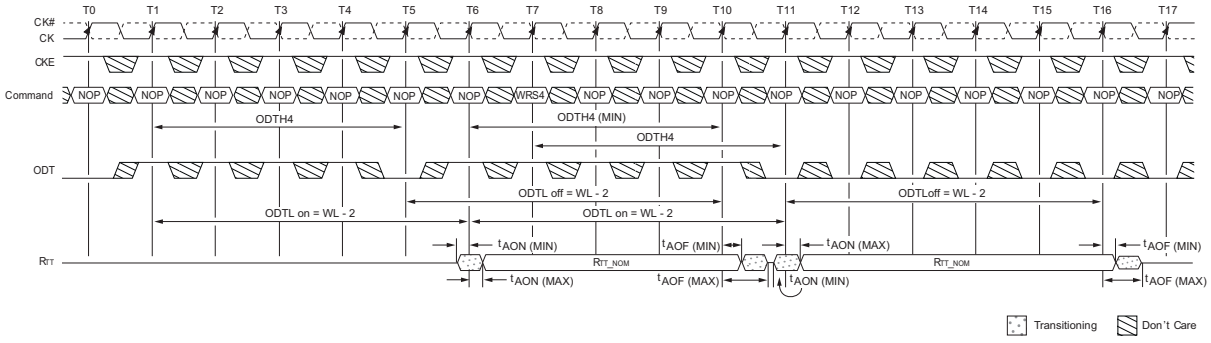
| Symbol | Description | Begins at | Defined to | Definition for All DDR3 bins | Units |
|---|---|---|---|---|---|
| ODTL ON | ODT synchronous TURN-ON delay | ODT registered HIGH | RTT_ON ± $^{t}$AON | CWL + AL - 2 | $^{t}$CK |
| ODTL OFF | ODT synchronous TURN-OFF delay | ODT registered HIGH | RTT_OFF ± $^{t}$AOF | CWL + AL - 2 | $^{t}$CK |
| ODTH4 | ODT Minimum HIGH time after ODT assertion or WRITE (BC4) | ODT registered HIGH, or WRITE registration with ODT HIGH | ODT registered LOW | 4$^{t}$cK | $^{t}$CK |
| ODTH8 | ODT Minimum HIGH time after WRITE (BL8) | WRITE registration with ODT HIGH | ODT registered LOW | 6$^{t}$cK | $^{t}$CK |
| $^{t}$AON | ODT TURN-ON relative to ODTL on completion | Completion of ODTL on | RTT_ON | See Table 50 | ps |
| $^{t}$AOF | ODT TURN-OFF relative to ODTL off completion | Completion of ODTL off | RTT_OFF | 0.5$^{t}$cK ± 0.2$^{t}$cK | $^{t}$CK |

### FIGURE 106 - SYNCHRONOUS ODT




Notes: 1. AL = 3; CWL = 5; ODTL on = WL = 6.0; ODTL off = WL - 2 = 6. RTT_NOM is enabled.

## FIGURE 107 - SYNCHRONOUS ODT (BC4)

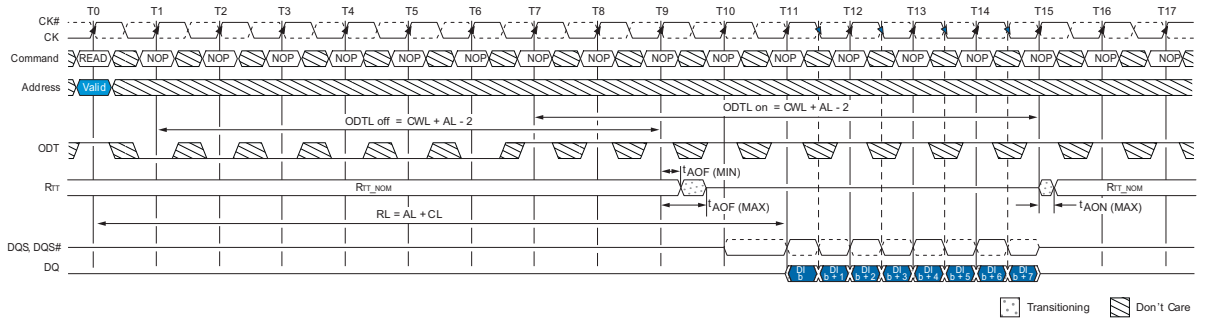



Notes:
1. WL = 7. RTT_NOM is enabled. RTT_WR is disabled.
2. ODT must be held HIGH for at least ODTH4 after assertion (T1).
3. ODT must be kept HIGH ODTH4 (BC4) or ODTH8 (BL8) after the WRITE command (T7).
4. ODTH is measured from ODT first registered HIGH to ODT first registered LOW or from the registration of the WRITE command with ODT HIGH to ODT registered LOW.
5. Although ODTH4 is satisfied from ODT registered HIGH at T6, ODT must not go LOW before T11 as ODTH4 must also be satisfied from the registration of the WRITE command at T7.

## ODT OFF DURING READS

As the DDR3 SDRAM cannot terminate and drive at the same time, RTT must be disabled at least one-half clock cycle before the READ preamble by driving the ODT ball LOW. RTT may not be enabled until the end of the postamble as shown in Figure 108.

## FIGURE 108 - ODT DURING READS




Notes:
1. ODT must be disabled externally during READs by driving ODT LOW. For example, CL = 6; AL = CL - 1 = 5; RL = AL + CL = 11; CWL = 5; ODTL on = CWL + AL - 2 = 8; ODTL off = CWL + AL - 2 = 8. RTT_NOM is enabled. RTT_WR is a "Don't Care."

## ASYNCHRONOUS ODT MODE

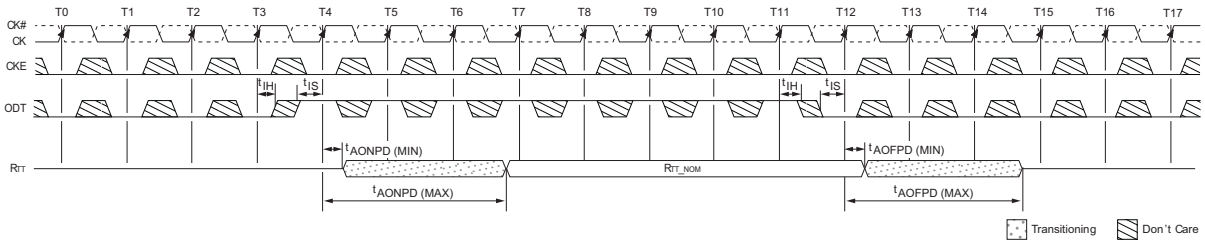
Asynchronous ODT mode is available when the SDRAM runs in DLL ON mode and when either RTT_NOM or RTT_WR is enabled; however, the DLL is temporarily turned off in PRECHARGED POWER-DOWN standby via MR0[12]. Additionally, ODT operates asynchronously when the DLL is synchronizing after being RESET. See "POWER-DOWN MODE" for definition and guidance over POWER-DOWN details.

In asynchronous ODT timing mode, the internal ODT command is not delayed by AL relative to the external ODT command. In asynchronous ODT mode, ODT controls RTT by analog time. The timing parameters $^{t}$AONPD and $^{t}$AOFPD (see Table 79) replace ODTL on/$^{t}$AON and ODTL off/$^{t}$AOF respectively, when ODT operates asynchronously (see Figure 109).

The minimum RTT turn-on time ($^{t}$AONPD [MIN]) is the point at which the device termination circuit leaves HIGH-Z and ODT resistance begins to turn-on. Maximum RTT turn-on time ($^{t}$AONPD [MAX]) is the point at which ODT resistance is fully on. $^{t}$AONPD (MIN) and $^{t}$AONPD (MAX) are measured from ODT being sampled HIGH.

The minimum RTT turn-off time ($^{t}$AOFPD [MIN]) is the point at which the device termination circuit starts to turn off ODT resistance. Maximum RTT turn-off time ($^{t}$AOFPD [MAX]) is the point at which ODT has reached HIGH-Z. $^{t}$AOFPD (MIN) and $^{t}$AOFPD (MAX) are measured from ODT being sampled LOW.

### FIGURE 109 - ASYNCHRONOUS ODT TIMING WITH FAST ODT TRANSITION




Notes: 1. AL is ignored.

### TABLE 79: ASYNCHRONOUS ODT TIMING PARAMETERS FOR ALL SPEED BINS

| Symbol | Description | MIN | MAX | Units |
|---|---|---|---|---|
| $^{t}AON_{PD}$ | Asynchronous RTT TURN-ON delay (POWER-DOWN with DLL off) | 2 | 8.5 | ns |
| $^{t}AOF_{PD}$ | Asynchronous RTT TURN-OFF delay (POWER-DOWN with DLL off) | 2 | 8.5 | ns |

## SYNCHRONOUS TO ASYNCHRONOUS ODT MODE TRANSITION (POWER-DOWN ENTRY)

There is a transition period around POWER-DOWN ENTRY (PDE) where the SDRAM's ODT may exhibit either synchronous or asynchronous behavior. This transition period occurs if the DLL is selected to be off when in PRECHARGE POWER-DOWN mode by the setting of MR0[12] = 0. POWER-DOWN entry begins $^{t}$ANPD prior to CKE first being registered LOW and it ends when CLE is first registered LOW. $^{t}$ANPD is equal to the greater of ODTL off + 1$^{t}$CK or ODTL on + 1$^{t}$CK. If a REFRESH command has been issued, and it is in progress when CKE goes LOW, POWER-DOWN entry will end $^{t}$RFC after the REFRESH command rather than when CKE is first registered LOW. POWER-DOWN ENTRY will then become the greater of $^{t}$ANPD and $^{t}$RFC – REFRESH command to CKE registered LOW.

ODT assertion during POWER-DOWN ENTRY results in an RTT change as early as the lesser of $^{t}$AONPD (MIN) and ODTL on x $^{t}$CK + $^{t}$AON (MIN) or as late as the greater of $^{t}$AONPD (MAX) and ODTL on x $^{t}$CK + $^{t}$AON (MAX). ODT de-assertion during POWER-DOWN ENTRY may result in an RTT change as early as the lesser of $^{t}$AOFPD (MIN) and ODTL off x $^{t}$CK + $^{t}$AOF (MIN) or as late as the greater of $^{t}$AOFPD (MAX) and ODTL off x $^{t}$CK + $^{t}$AOF (MAX). Table 80 summarizes these parameters.

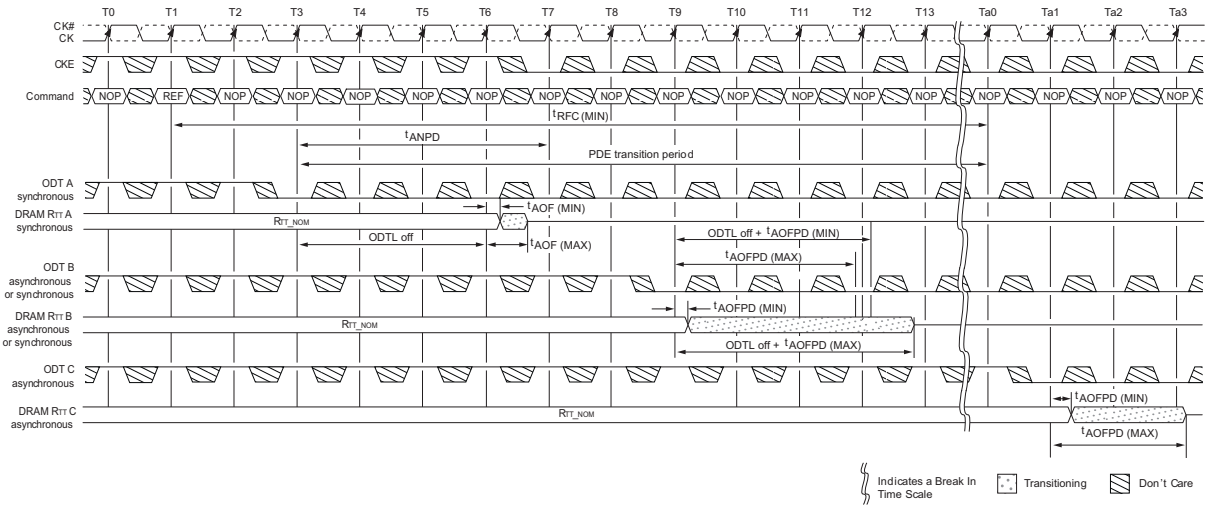
If the AL has a large value, the uncertainty of the state of RTT becomes quite large. This is because ODTL on and ODTL off are derived from the WL and WL is equal to CWL + AL. Figure 110 shows three different cases;

- ODT_A: Synchronous behavior before $^{t}$ANPD
- ODT_B: ODT state changes during the transition period with $^{t}$AONPD (MIN) less than ODTL on x $^{t}$CK + $^{t}$AON (MIN) and $^{t}$AONPD (MAX) greater than ODTL on x $^{t}$CK + $^{t}$AON (MAX)
- ODT_C: ODT state changes after the transition period with asynchronous behavior

### TABLE 80: ODT PARAMETERS FOR POWER-DOWN (DLL OFF) ENTRY AND EXIT TRANSITION PERIOD

| Description | MIN | MAX |
|---|---|---|
| POWER-DOWN entry transition period (POWER-DOWN entry) | Greater of: $^{t}AN_{PD}$ or $^{t}$RFC - REFRESH to CKE LOW | |
| POWER-DOWN entry transition (POWER-DOWN exit) | $^{t}AN_{PD}$ + $^{t}$XPDLL | |
| ODT to RTT TURN-ON delay (ODTL on = WL - 2) | Lesser of: $^{t}AN_{PD}$ (MIN) [1ns] or ODL on x $^{t}$CK + $^{t}$AON (MIN) | Lesser of: $^{t}AN_{PD}$ (MIN) [1ns] or ODL on x $^{t}$CK + $^{t}$AON (MIN) |
| ODT to RTT TURN-OFF delay (ODTL off = WL - 2) | Lesser of: $^{t}AOF_{PD}$ (MIN) [1ns] or ODL off x $^{t}$CK + $^{t}$AOF (MIN) | Lesser of: $^{t}AOF_{PD}$ (MIN) [1ns] or ODL off x $^{t}$CK + $^{t}$AOF (MIN) |
| $^{t}AN_{PD}$ | WL - 1 (Greater of ODTL off + 1 or ODTL on + 1) | |

## FIGURE 110 - SYNCHRONOUS TO ASYNCHRONOUS TRANSITION DURING PRECHARGE POWER-DOWN (DLL OFF) ENTRY




Notes: 1. AL = 0; CWL = 5; ODTL off = WL - 2 = 3.

## ASYNCHRONOUS TO SYNCHRONOUS ODT MODE TRANSITION (POWER-DOWN EXIT)

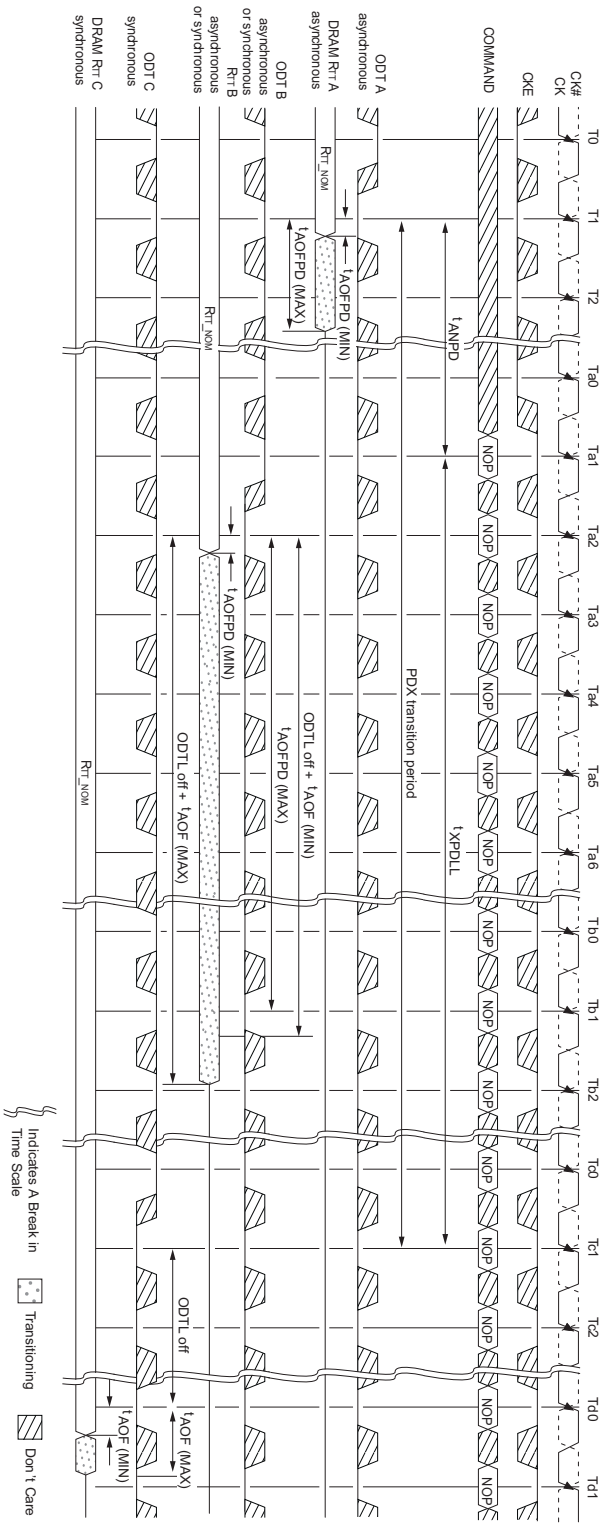
The SDRAM's ODT may exhibit either asynchronous or synchronous behavior during POWER-DOWN EXIT (PDX). This transition period occurs if the DLL is selected to be off when in PRECHARGE POWER-DOWN mode by setting MR0[12] to "0". POWER-DOWN exit begins $^{t}$ANPD prior to CKE first being registered HIGH and it ends $^{t}$XPDLL after CKE is first registered HIGH. $^{t}$ANPD is equal to the greater of ODTL off + 1$^{t}$CK or ODTL on + 1$^{t}$CK. The transition period is $^{t}$ANPD plus $^{t}$XPDLL.

ODT assertion during POWER-DOWN exit results in an RTT change as early as the lesser of $^{t}$AONPD (MIN) and ODTL on x $^{t}$CK + $^{t}$AON (MIN) or as late as the greater of $^{t}$AONPD (MAX) and ODTL on x $^{t}$CK + $^{t}$AON (MAX). ODT de-assertion during POWER-DOWN EXIT may result in an RTT change as early as the lesser of tAOFPD (MIN) and OFTL off x $^{t}$CK + tAOF (MIN) or as late as the greater of tAOFPD (MAX) and ODTL off x $^{t}$CK + tAOF (MAX). Table 80 summarizes these parameters.

If the AL has a large value, the uncertainty of the RTT state becomes quite large. This is because ODTL on and ODTL off are derived from the WL, and the WL is equal to CWL + AL. Figure 111 shows three different cases.

- ODT C: Asynchronous behavior before $^{t}$ANPD
- ODT B: ODT state changes during the transition period with $^{t}$AOFPD (MIN) less than ODTL off x $^{t}$CK + $^{t}$AOF (MIN) and ODTL off x $^{t}$CK + $^{t}$AOF (MAX) greater than $^{t}$AOFPD (MAX)
- ODT A: ODT state changes after the transition period with synchronous response

## FIGURE 111 - ASYNCHRONOUS TO SYNCHRONOUS TRANSITION DURING PRECHARGE POWER-DOWN (DLL OFF) EXIT



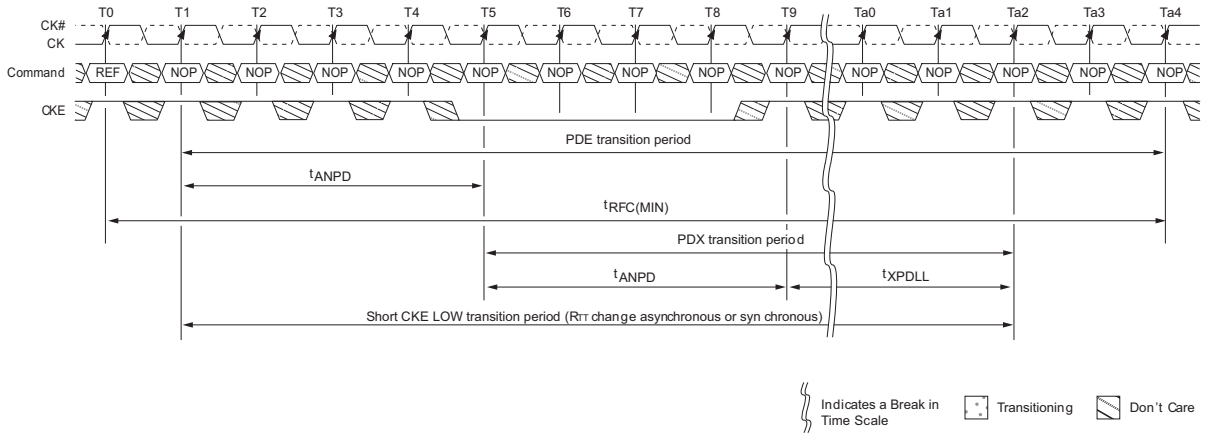

Notes: 1. CL = 6; AL = CL - 1; CWL = 5; ODTL off = WL - 2 = 8.

## ASYNCHRONOUS TO SYNCHRONOUS ODT MODE TRANSITION (SHORT CKE PULSE)

If the time in the PRECHARGE POWER DOWN or IDLE states is very short (short CKE LOW pules), the POWER-DOWN ENTRY and POWER-DOWN EXIT transition periods will overlap. When overlap occurs, the response of the SDRAM's RTT to a change in the ODT state may be synchronous or asynchronous from the start of the POWER-DOWN ENTRY transition period to the end of the POWER-DOWN EXIT transition period even if the ENTRY period ends later than the EXIT period. (see Figure 112).

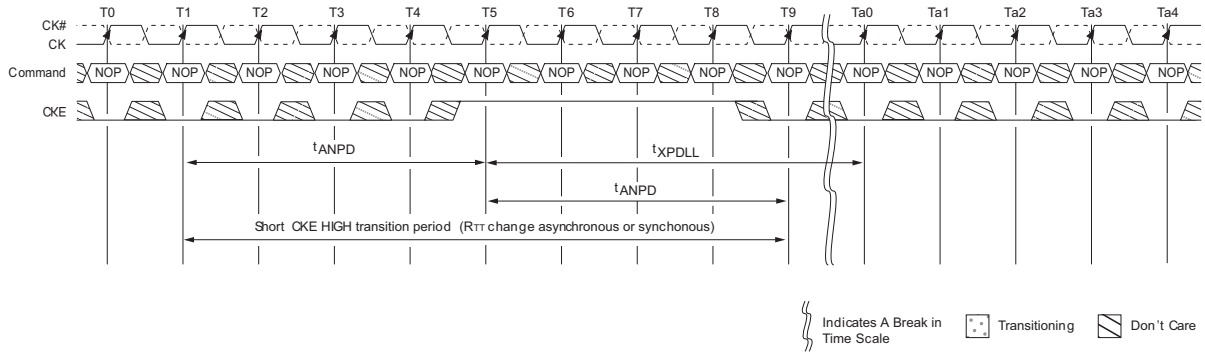
If the time in the idle state is very short (short CKE HIGH pulse), the POWER-DOWN EXIT and POWER-DOWN ENTRY transition periods overlap. When this overlap occurs, the response of the SDRAM's RTT to a change in the ODT state may be synchronous or asynchronous from the start of the POWER-DOWN EXIT transition period to the end of the POWER-DOWN ENTRY transition period (see Figure 113).

### FIGURE 112 - TRANSITION PERIOD FOR SHORT CKE LOW CYCLES WITH ENTRY AND EXIT PERIOD OVERLAPPING




Notes: 1. AL = 0, WL = 5, $^{t}$ANPD = 4.

### FIGURE 113 - TRANSITION PERIOD FOR SHORT CKE HIGH CYCLES WITH ENTRY AND EXIT PERIOD OVERLAPPING




Notes: 1. AL = 0, WL = 5, $^{t}$ANPD = 4.

## Revision History

| Revision | Engineer | Issue Date | Description Of Change |
|---|---|---|---|
| A | DH/JM | 07.06..2009 | INITIATE |
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